# Wire Bondable Vertical Silicon Capacitor WBSC / WLSC 0202 1nF BV150

Rev.3.02

## General description

WBSC / WLSC Capacitors targets power supplies decoupling and filtering of active devices. They are based on PICS Integrated Passive technology.

This product is a single 1nF capacitor array in a 0202 [0.5 x 0.5 mm] package size. Other capacitance values and other package size are available as a single die or capacitor array; please feel free to contact us.

WBSC / WLSC capacitors are directly mounted on the PCB application using die bonding or wire bonding processes. Standard FR4 PCB can be used. The bottom electrode is in TiNiAu and the top electrode is in TiWAu. Other top finishings such as Aluminium are available on request.

## Key features

- Compatible with MLCC footprint
- Ultra-high stability of capacitance value:
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  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.02%/Volt
  - Negligible capacitance loss through ageing
- Low profile 250µm or 100µm
- Small size 0.5 x 0.5 mm (0202 format)
- Break down voltage : 150V
- Low leakage current
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0202 footprint
- Applicable for standard wire bonding assembly (ball and wedge)

## Key applications

- Any demanding applications, such as medical, aerospace, automotive industrial…
- Supply decoupling / filtering of active device
- High reliability applications
- High temperature applications
- High volumetric efficiency *(i.e. capacitance per unit volume)*

## Functional diagram

The next figure provides implementation set-up diagram.

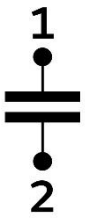


*Figure 1 Block Diagram*

## Electrical performances

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| C | Capacitance value | @+25°C | - | 1 | - | nF |
| $\Delta C_P$ | Capacitance tolerance (1) | @+25°C | -15 | - | +15 | % |
| $T_{OP}$ | Operating temperature | | -55 | 20 | 150 | °C |
| $T_{STG}$ | Storage temperature (2) | | -70 | - | 165 | °C |
| $\Delta C_T$ | Capacitance temperature variation | -55°C to +150°C | | 70 | | ppm/K |
| $RV_{DC}$ | Rated voltage (3) | | - | | 68 (4)<br>61 (5) | $V_{DC}$ |
| BV | Breakdown voltage | @+25°C | 150 | - | - | $V_{DC}$ |
| $\Delta C_{RVDC}$ | DC Capacitance voltage variation | From 0V to $RV_{DC}$, @+25°C | - | - | -0.02 | $\%/V_{DC}$ |
| IR | Insulation resistance | @ $RV_{DC}$, +25°C, 120s | - | 10 | - | GΩ |
| ESR | Equivalent Series Resistance | @+25°C, shunt mode | - | 10 | - | mΩ |
| ESL | Equivalent Series Inductance | @+25°C, SRF shunt mode | - | 8 | - | pH |
| ESD | HBM stress (6) | JS-001-2017 | 2 | - | - | kV |

*Table 1 - Electrical performances*

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

For extended frequency range (up to 26GHz), see Ultra large band Wire bondable vertical Silicon Capacitor (UWSC).

## Pinning definition

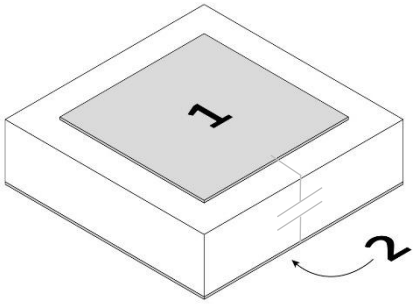


*Figure 2 Pinning definition*

| pin # | Symbol | Coordinates X / Y |
|---|---|---|
| 1 | Signal | 0.0 / 0.0 |
| 2 | GND | Backside |

*Table 2 - Pining description. Reference (0,0) located at the centre of the die.*

## Ordering Information

Regardless of packaging, Murata Integrated Passive Devices delivers products with AQL level II (0.65).

| Type number | Package | | |
|---|---|---|---|
| | Packaging | Finishing | Description |
| 935142521410-F1T | 6” FFC(1) | Au(2) | WBSC 1nF/0202 – 1 bondpad – 0.50 x 0.50mm x 0.25mm(3) |
| 935142521410-F2T | 8” FFC(1) | Au(2) | |
| 935142521410-E1T | 6” expander grip ring(1) | Au(2) | |
| 935142521410-T3T | T&R 1Kunits(4) | Au(2) | |
| 935142521410-W0T | Waffle pack 400units | Au(2) | |
| 935146521410-F1T | 6” FFC(1) | Au(2) | WLSC 1nF/0202 1 bondpad – 0.50 x 0.50mm x 0.10mm(3) |
| 935146521410-F2T | 8” FFC(1) | Au(2) | |
| 935146521410-E1T | 6” expander grip ring(1) | Au(2) | |
| 935146521410-T3T | T&R 1Kunits(4) | Au(2) | |
| 935146521410-W0T | Waffle pack 400units | Au(2) | |

(1) Other film frame carrier are possible on request
(2) Au = TiWAu(0.3µm) / Au (3µm)
(3) Refer to Figure 7
(4) missing capacitors can reach 0.5%

*Table 3 - Packaging and ordering information*

| Product Name | Die Name | Description |
|---|---|---|
| WBSC521.410 | WO0202410 | WBSC 1nF/0202/BV150– 1 bondpad – 0.50 x 0.50mm x 0.25mm |
| WLSC521.410 | WO0202410 | WLSC 1nF/0202/BV150– 1 bondpad – 0.50 x 0.50mm x 0.10mm |

*Table 4 - Die information*

## Pad Metallization

This wire bondable capacitor is delivered as standard with the bottom electrode in TiNiAu (Ti (0.1 µm)/Ni (0.3µm)/Au (0.2µm)) and top electrode in TiWAu (TiWAu (0.3µm) / Au (3µm)).
Other Metallization, such as thick Gold or Aluminum top pads are possible on request.
Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

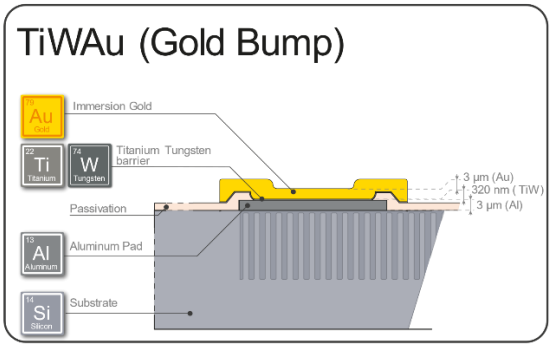


*Figure 3 - Top electrode description*

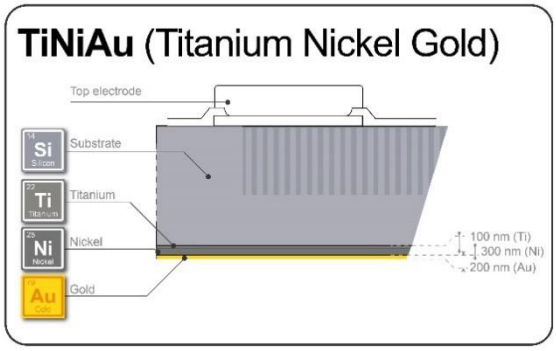


*Figure 4 - Bottom electrode description*

## Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

## Package outline

The product is delivered as a bare silicon die.

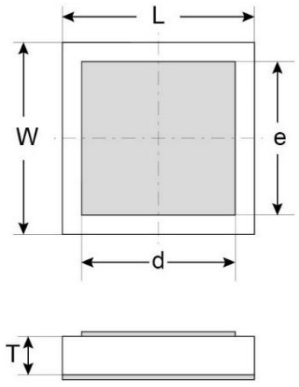


*Figure 5 - Package outline drawing*

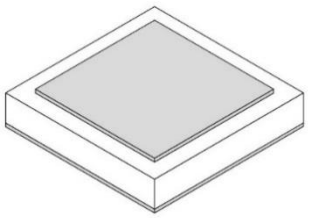

*Figure 6 - Package isometric view*

| L (mm) | W (mm) | T (mm) | d (mm) | e (mm) |
|---|---|---|---|---|
| 0.50 ±0.03 | 0.50 ±0.03 | 0.25 or 0.10 ±0.015 | 0.4 | 0.4 |

*Table 5 - Dimensions and tolerances*

## Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

*Figure 7 Scan this QR Code to access the Murata Silicon Capacitor web page*

## Packaging format

Please refer to application note ‘Products Storage Conditions and Shelf Life’.

**Tape and Reel:**

Die orientation (No flip) within the case related to T&R orientation)

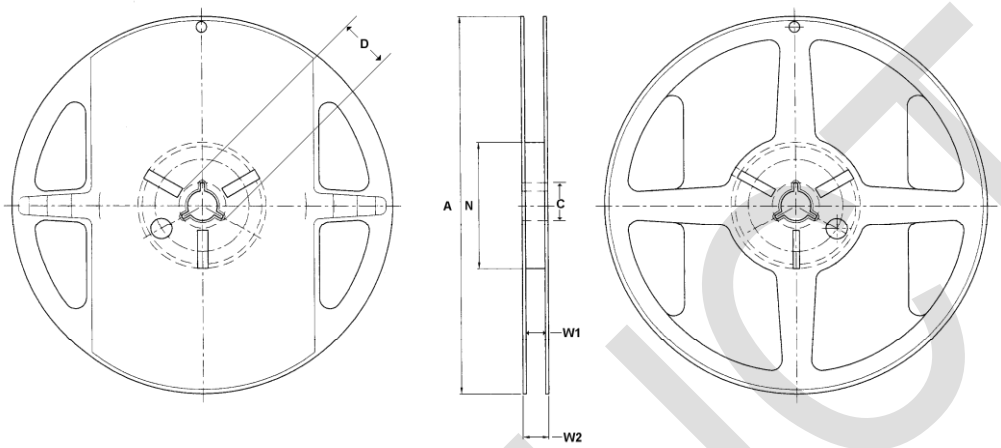


*Figure 8 - Reel drawing*

| Tape Width | Diameter A | C | D | Hub N | W1 | W2 |
|---|---|---|---|---|---|---|
| 8 | 178 (7 inches) | 13.5 | 20.2 | 60 | 9.3 | 11.5 |

*Table 6 – Reel dimensions (mm)*

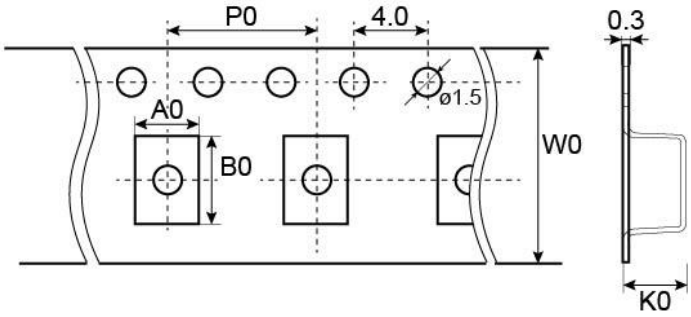


*Figure 9 - Tape drawing*

| Cavity dimensions | | | Carrier tape width W0 | Carrier tape pitch P0 | Reel Capacity |
|---|---|---|---|---|---|
| Ao | Bo | Ko | | | |
| 0.56 | 0.56 | 0.31 | 8 mm | 4mm | 1000 |

*Table 7 - Tape dimensions (mm)*

**Waffle pack:**

Please refer to application note 'Waffle Pack Chip Carrier Handling & Opening Procedure'. Dies are not flipped in the waffle pack cavity (wire bond pad up).

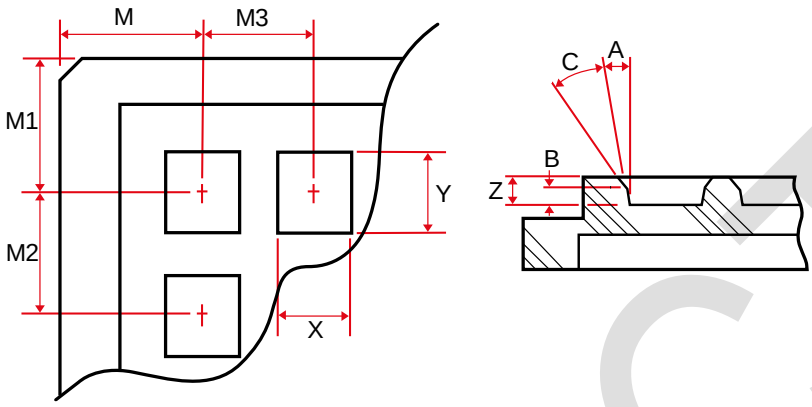


*Table 8 - Waffle pack drawing*

| External dimensions | Max. capacity | Pocket length X | Pocket width Y | Pocket depth Z |
|---|---|---|---|---|
| 2 inches | 20 x 20 | 0.64 ±0.05 | 0.64 ±0.05 | 0.36 ±0.05 |

*Table 9 - Waffle pack dimensions (mm) for 250µm thick product*

| M | M1 | M2 | M3 | A |
|---|---|---|---|---|
| 4.65 ±0.08 | 4.65 ±0.08 | 2.18 ±0.05 | 2.18 ±0.05 | 15° ±1/2° |

*Table 10 - Waffle pack dimensions (mm) for 250µm thick product*

| External dimensions | Max. capacity | Pocket length X | Pocket width Y | Pocket depth Z |
|---|---|---|---|---|
| 2 inches | 20 x 20 | 0.58 ±0.05 | 0.58 ±0.05 | 0.28 ±0.05 |

*Table 11 : Waffle pack dimensions (mm) for 100µm thick product*

| M | M1 | M2 | M3 | A |
|---|---|---|---|---|
| 4.89 ±0.08 | 4.89 ±0.08 | 2.16 ±0.05 | 2.16 ±0.05 | 18° ±1/2° |

*Table 12 : Waffle pack dimensions (mm) for 100µm thick product*

**Film Frame Carrier:**

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

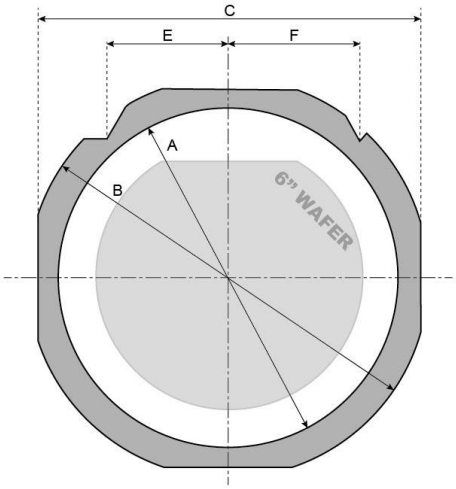


*Figure 10 FF070 Frame with a 6" wafer*

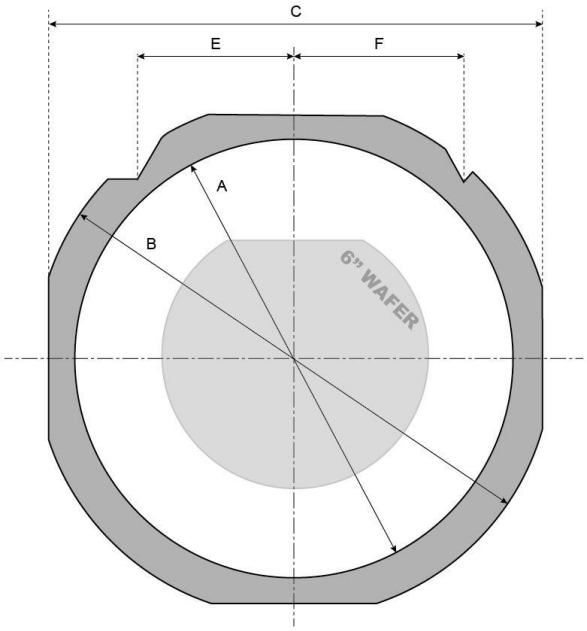


*Figure 11 FF108 Frame with a 6" wafer*

| Frame Reference | Frame Style | Inside diameter A | Outside diameter B | Width C | Thickness | Pin location E | Pin location F |
|---|---|---|---|---|---|---|---|
| FF070 (1) | DTF-2-6-1 | 7.638” | 8.976” | 8.346” | 0.048’’ | 2.370” | 2.5’’ |
| FF108 (1) | DTF-2-8-1 | 9.842” | 11.653” | 10.866” | 0.048” | 2.381” | 2.5’’ |

*Table 13 - Frame dimensions (inches)*

(1) or equivalent

**Expander grip ring 6” diameter:**

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

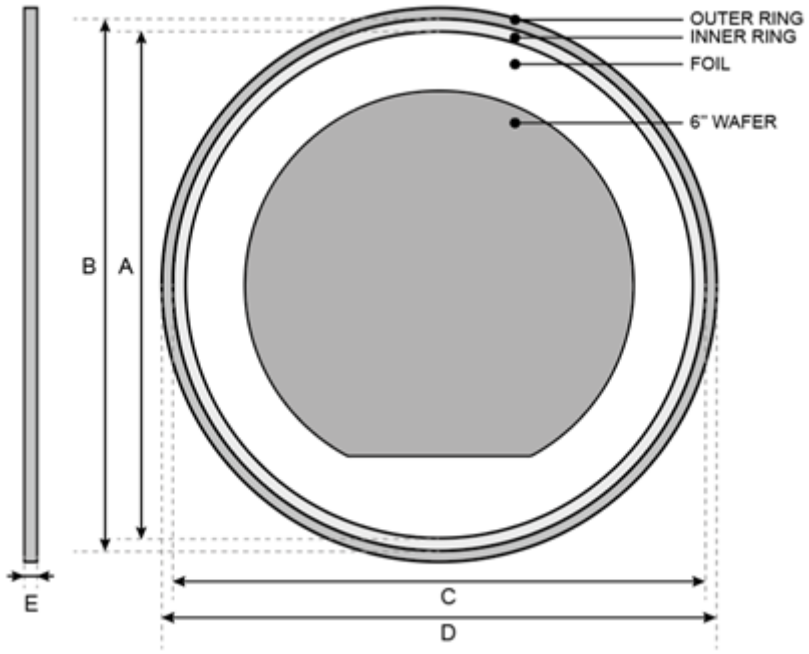


*Figure 12 – Grip Ring drawing*

| Grip Ring Style | A | B | C | D | E | Locator Notch |
|---|---|---|---|---|---|---|
| GRP-2620-6 (1) | 7.670” | 7.973” | 7.975” | 8.280” | 0.236” | None |

*Table 14 - Frame dimensions (inches)*

(1) or equivalent

## Definitions

Data sheet status

**Objective specification:** This data sheet contains target or goal specifications for product development.

**Preliminary specification:** This data sheet contains preliminary data; supplementary data may be published later.

**Product specification:** This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

## Revision history

| Revision | Date | Description | Author |
|---|---|---|---|
| Rev 1.00 | 2014 May 12th | Creation | OGA |
| Rev 2.01 | 2021 Feb 23rd | Preliminary revision | CGU / LLE / OGA |
| Rev 3.00 | 2021 March 30rd | Product revision | CGU / LLE / OGA |
| Rev 3.01 | 2022 July 12th | GR updated | CGU / LLE / OGA |
| Rev 3.02 | 2023 Nov. 28th | Adding of Top & Bottom electrode description | DYE |

## Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.



www.murata.com

mis@murata.com