Ultra-large band Wire bondable Vertical SiCap
UWSC 0101 100pF BV150

Rev. 3.10

General description

UWSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The UWSC is suitable for DC blocking, RF bypassing, matching networks and filtering applications in all broadband optoelectronics and High speed data system.
The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with high rejection up to 60 GHz.
These Ultra large band Wire Bondable MOS vertical Silicon Capacitors (UWSC) have been developed in a semiconductor process, in order to combine *ultra-deep trench MOS capacitors for high capacitance value of 100 pF in a 0101 package size*. Other capacitance values and other package size are available as a single capacitor or capacitor array; please feel free to contact us.
The UWSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.
UWSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).

Assembly: UWSC capacitors are directly mounted on the PCB application using die bonding and wire bonding. UWSC capacitors have the bottom electrode in Ti (0.1 µm)/Ni (0.3µm)/Au (0.2µm) and top electrode in gold, other top finishing are available on request such as Aluminum.

Key features

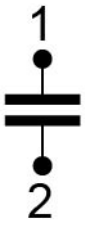
- Ultra large band performance to 67 GHz
- Resonance free
- Phase stability
- High rejection at 60 GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage < -0.02%/Volts
  - Negligible capacitance loss through ageing
- Low profile: 0.10mm (standard).
- Break down voltage: 150V
- Low leakage current < 70pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0101 footprint
- Applicable for standard wire bonding assembly (ball and wedge)

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimeter system
- Volume limited applications
- Broadband test equipment

Functional diagram

The next figure provides implementation set-up diagram.



Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	100	-	pF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	+150	°C
T_{STG}	Storage temperature (2)		-70	-	+165	°C
ΔC_T	Capacitance temperature variation	-55°C to +150°C		70		ppm/K
RV_{DC}	Rated voltage (3)		-	50	68 (4) 61 (5)	V_{DC}
BV	Breakdown voltage	@+25°C	150	-	-	V_{DC}
ΔC_{RVDC}	DC Capacitance voltage variation	From 0V to RV_{DC}, @25°C	-	-	-0.02	$\%/V_{DC}$
IR	Insulation resistance	@ RV_{DC}, +25°C, 120s	-	100	-	GΩ
ESL	Equivalent Series Inductance	@+25°C, SRF shunt mode	-	17	-	pH
ESD	HBM stress (6)	JS-001-2017	500	-	-	V

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

Impedance characteristic of 100pF UWSC in Shunt mode

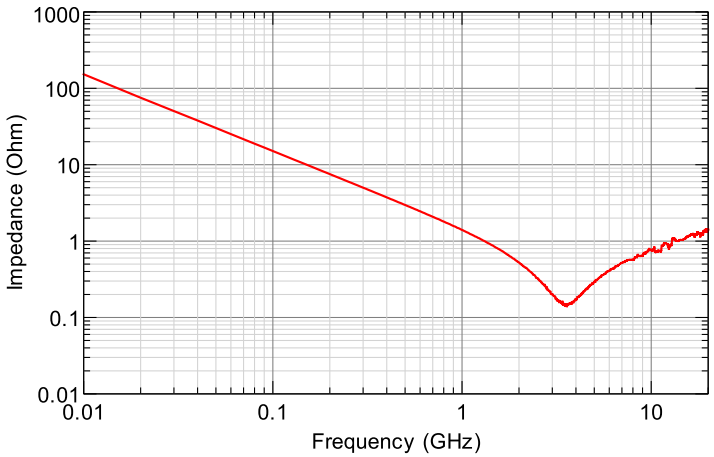


Figure 2 – 100pF UWSC measurement results (Impedance characteristic versus Frequency in shunt mode)

Schematic of 100pF UWSC in transmission mode

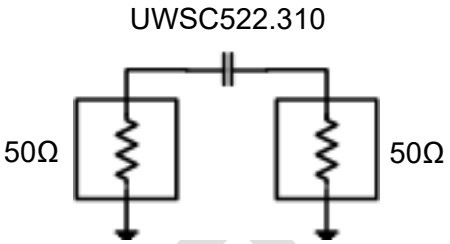


Figure 3 - 100pF UWSC measurement schematic

Test bench

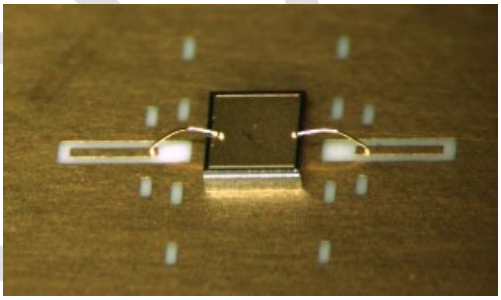


Figure 4 - test bench picture used for 100pF UWSC characterization

Pinning definition

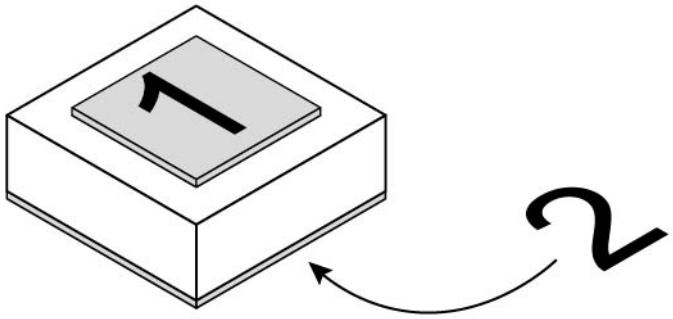


Figure 5 Pinning definition

pin #	Symbol	Coordinates X / Y
1	Signal	0.0/0.0
2	GND	Backside

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information

Part number	Package		
	Packaging	Finishing	Description
935154522310-F1T	6” FFC(1)	Au(2)	100pF/0101 – 1 bondpad – 0.25 x 0.25mm x 0.10mm
935154522310-F2T	8” FFC(1)	Au(2)	100pF/0101 – 1 bondpad – 0.25 x 0.25mm x 0.10mm
935154522310-E1T	6” GR(1)	Au(2)	100pF/0101 – 1 bondpad – 0.25 x 0.25mm x 0.10mm
935154522310-W0T	Waffle pack 400units	Au(2)	100pF/0101 – 1 bondpad – 0.25 x 0.25mm x 0.10mm

Table 3 - Packaging and ordering information

(1) Other film frame carrier are possible on request
(2) Au = TiW (0.3µm) / Au (3µm)

Product Name	Die Name	Description
UWSC522.310	WO0101310	UWSC 100pF/0101/BV150 – 1 bondpad – 0.25 x 0.25mm x 0.10mm

Table 4 - Die information

Pad Metallization

The UWSC Capacitor is delivered as standard with the bottom electrode in TiNiAu and top electrode in TiWAu.

Other Metallization, such as thick Gold or Aluminum top pads are possible on request.

UWSC capacitors are directly mounted on the PCB application using die bonding and wire bonding.

It is applicable for standard wire bonding assembly (ball and wedge).
Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’.

For further information, please see our mounting application note.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

Figure 6 - Micro photography of a 100pF Capacitor

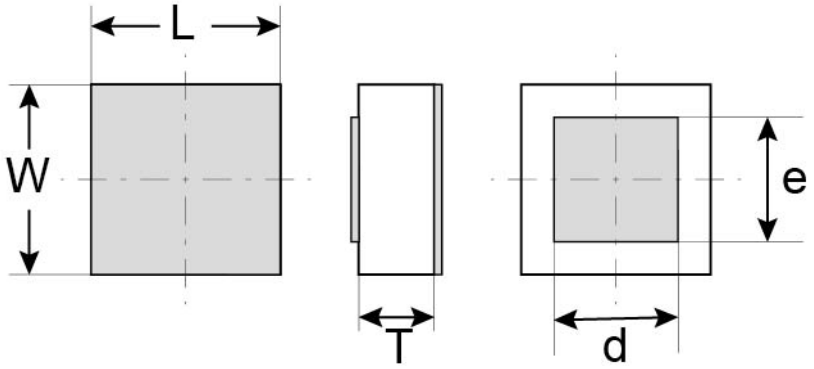


Figure 7 - Package outline drawing

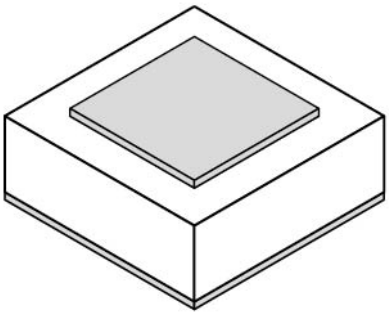


Figure 8 - Package isometric view

L (mm)	W (mm)	T (mm)	d (mm)	e (mm)
0.25 ±0.03	0.25 ±0.03	0.10 ±0.01	0.164	0.164

Table 5 - Dimensions and tolerances

Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 9 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Film Frame Carrier:

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

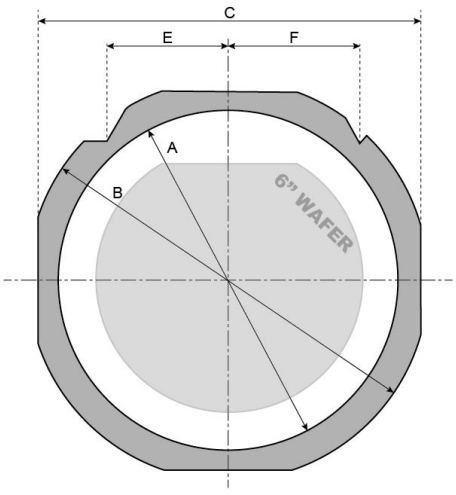


Figure 10 FF070 Frame with a 6" wafer

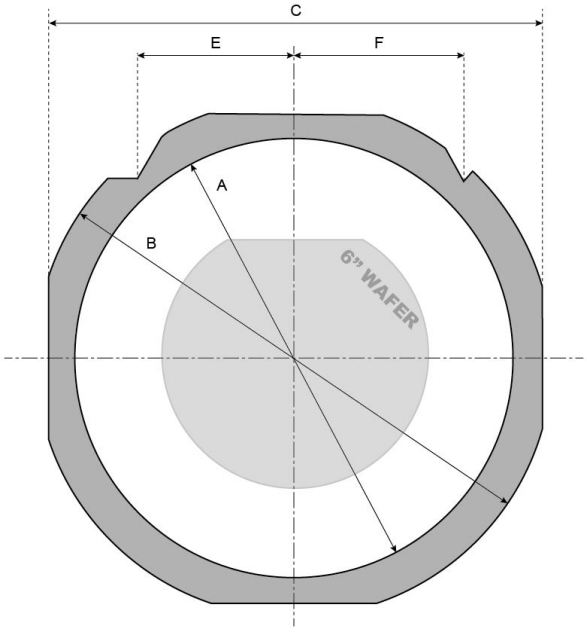


Figure 11 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 (1)	DTF-2-6-1	7.638”	8.976”	8.346”	0.048’’	2.370”	2.5’’
FF108 (1)	DTF-2-8-1	9.842”	11.653”	10.866”	0.048”	2.381”	2.5’’

Table 6 - Frame dimensions (inches)

(1) or equivalent

Waffle pack:

Please refer to application note ‘Waffle Pack Chip Carrier Handling & Opening Procedure’. Dies are not flipped in the waffle pack cavity (wire bond pad up).

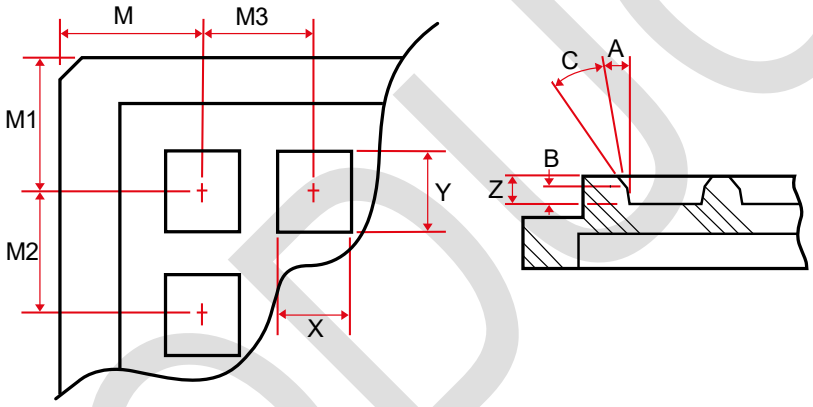


Table 7 - Waffle pack drawing

External dimensions	Max. capacity	Pocket length X	Pocket width Y	Pocket depth Z
2 inches	20 x 20	0.36 ±0.05	0.36 ±0.05	0.13 ±0.05

Table 8 - Waffle pack dimensions (mm)

M	M1	M2	M3	A
4.55 ±0.08	4.55 ±0.08	2.18 ±0.05	2.18 ±0.05	7° ±1/2°

Table 9 - Waffle pack dimensions (mm)

Expander grip ring 6” diameter:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

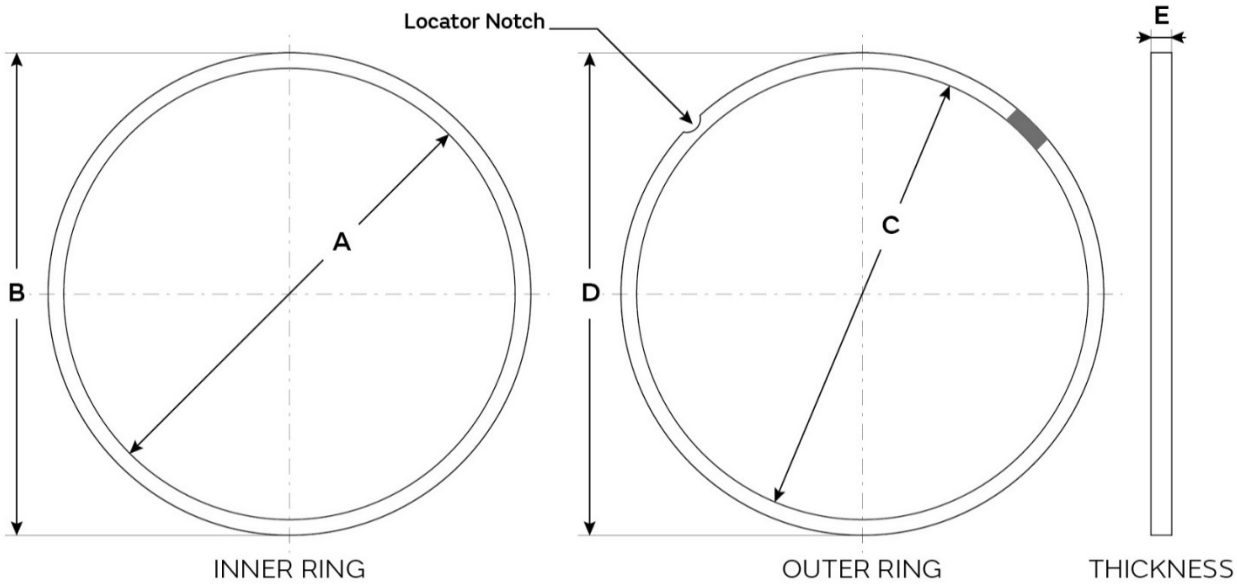


Figure 12 – Grip Ring drawing

Grip Ring Style	A	B	C	D	E	Locator Notch
GRP-2620-6 (1)	7.670”	7.973”	7.975”	8.280”	0.236”	None

Table 10 - Frame dimensions (inches)

(1) or equivalent

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 1.00	2014 April 1st	Creation	OGA
Release 3.00	2021 Feb. 19th	Update	OGA, SCA
Release 3.10	2022 Feb. 8th	ESD performance change	SCA

Disclaimer / Life support applications

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