# Ultra large band Wire Bondable Vertical SiCap UWSC 015015 150pF BV150

Rev. 3.00

## General description

UWSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The UWSC is suitable for DC blocking, RF bypassing, matching networks and filtering applications in all broadband optoelectronics and High speed data system.
The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with high rejection up to 60 GHz.
These Ultra large band Wire Bondable MOS vertical Silicon Capacitors (UWSC) have been developed in a semiconductor process, in order to combine *ultra-deep trench MOS capacitors for high capacitance value of 150 pF in a 015015 package size*. Other capacitance values and other package size are available as a single capacitor or capacitor array; please feel free to contact us.
The UWSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.
UWSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).

UWSC capacitors are directly mounted on the PCB application using die bonding and wire bonding processes. Standard FR4 PCB can be used. The bottom electrode is in TiNiAu and the top electrode is in TiWAu. Other top finishings such as Aluminum are available on request.

## Key features

- Ultra large band performance to 26 GHz
- Resonance free
- Phase stability
- High rejection at 20 GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +30 °C)
  - Voltage <-0.02%/Volt
  - Negligible capacitance loss through ageing
- Low profile 0.1mm
- Small size 0.381 x 0.381 mm (015015 format)
- Break down voltage : 150V
- Low leakage current < 70pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 015015 footprint
- Applicable for standard wire bonding assembly (ball and wedge)

## Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency (i.e. capacitance per unit volume
- Broadband test equipment

## Functional diagram

The next figure provides implementation set-up diagram.

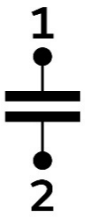


*Figure 1 Block Diagram*

## Electrical performances

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| C | Capacitance value | @+25°C | - | 150 | - | pF |
| $\Delta C_P$ | Capacitance tolerance (1) | @+25°C | -15 | - | +15 | % |
| $T_{OP}$ | Operating temperature | | -55 | 20 | 150 | °C |
| $T_{STG}$ | Storage temperature (2) | | -70 | - | 165 | °C |
| $\Delta C_T$ | Capacitance temperature variation | -55 °C to 150 °C | - | 70 | - | ppm/K |
| $RV_{DC}$ | Rated voltage (3) | | - | - | 68(4)<br>61(5) | $V_{DC}$ |
| BV | Break down voltage | @+25°C | 150 | - | - | V |
| $\Delta C_{RVDC}$ | Capacitance voltage variation | From 0 V to $RV_{DC}$, @+25°C | - | - | -0.02 | %/$V_{DC}$ |
| IR | Insulation resistor | @$RV_{DC}$, +25°C, 120s | - | 10 | - | GΩ |
| ESR | Equivalent Serial Resistance | @+25°C, SRF shunt mode | - | 50 | - | mΩ |
| ESL | Equivalent Serial Inductance | @+25°C, SRF shunt mode | - | 10 | - | pH |
| ESD | HBM stress (6) | JS-001-2017 | 0.7 | - | - | kV |

*Table 1 - Electrical performances*

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic lifetime prediction at 100°C continuous operation
(5): 10 years of intrinsic lifetime prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

**Impedance characteristic of 150pF UWSC in Shunt mode**

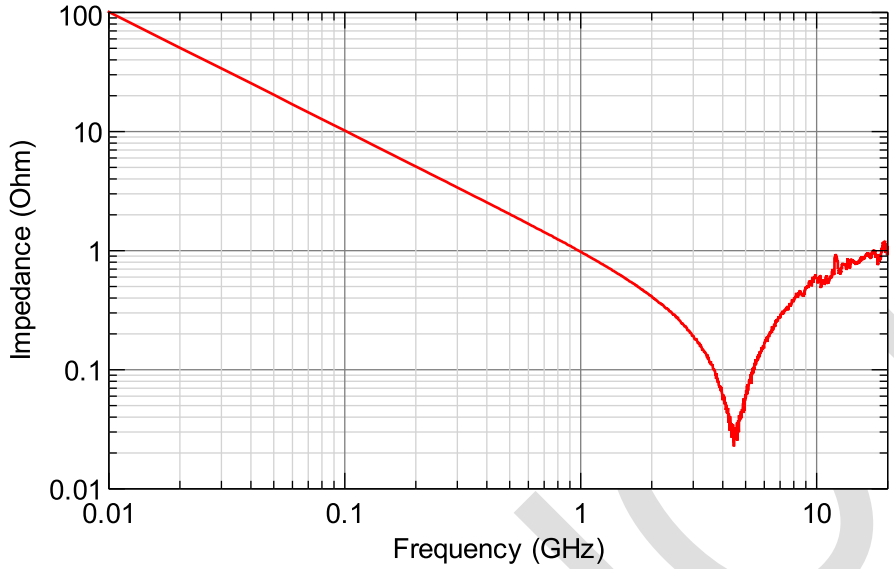


*Figure 4 - 150pF UWSC measurement results (Impedance characteristic versus Frequency in shunt mode)*

**Schematic of 150pF UWSC in Shunt mode**

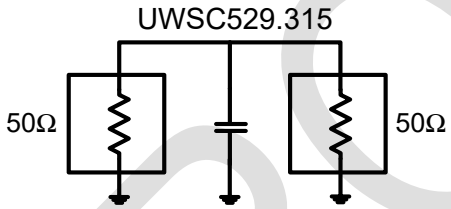


*Figure 2 - 150pF UWSC measurement schematic*

**Example of mounted 015015**

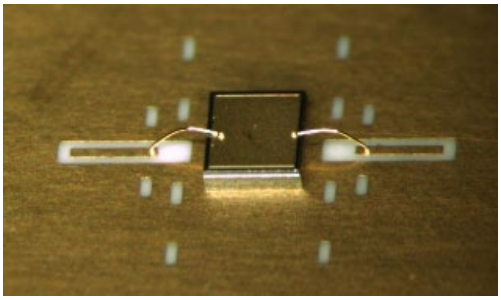

*Figure 3 – micro picture of mounted 015015 UWSC*

## Pinning definition

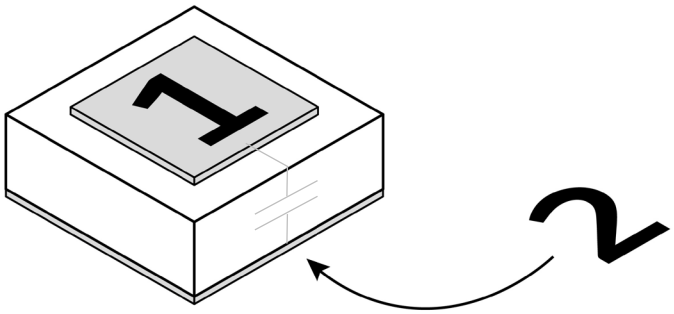


*Figure 5 Pinning definition*

| pin # | Symbol | Coordinates X / Y |
|---|---|---|
| 1 | Signal | 0.0 / 0.0 |
| 2 | GND | Backside |

*Table 2 - Pining description. Reference (0,0) located at the centre of the die.*

## Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65). Tighter quality levels are available upon request.

| Part number | Package | | |
|---|---|---|---|
| | Packaging | Finishing | Description |
| 935154529315-F1T | 6” FFC (1) | Au(2) | 150pF/015015 – 1 bondpad – 0.381 x 0.381mm x 0.10mm (3) |
| 935154529315-F2T | 8” FFC(1) | Au(2) | 150pF/015015 – 1 bondpad – 0.381 x 0.381mm x 0.10mm (3) |
| 935154529315-E1T | 6” grip ring(1) | Au(2) | 150pF/015015 – 1 bondpad – 0.381 x 0.381mm x 0.10mm (3) |
| 935154529315-W0T | Waffle pack 400units | Au(2) | 150pF/015015 – 1 bondpad – 0.381 x 0.381mm x 0.10mm (3) |

*Table 3 - Packaging and ordering information*

(1) Other film frame carrier are possible on request
(2) Au = TiWAu (0.3µm) / Au (3µm)
(3) Refer to Figure 7

| Product Name | Die Name | Description |
|---|---|---|
| UWSC529.315 | WO015015315 | UWSC 150pF/015015/BV150 – 1 bondpad – 0.381 x 0.381mm x 0.10mm |

*Table 4 - Die information*

## Pad Metallization

The wire bondable capacitor like UWSC is delivered as standard with the bottom electrode in TiNiAu (Ti=0.1µm; Ni=0.3µm; Au=0.2µm) and top electrode in TiWAu (0.3µm) / Au (3µm).

Other Metallization, such as Thick Gold or Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

## Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

## Package outline

The product is delivered as a bare silicon die.

*Figure 6 - Micro photography*

| Al (mm) | Aw (mm) | B (mm) | d (mm) | e (mm) |
|---|---|---|---|---|
| 0.381 ±0.02 | 0.381 ±0.02 | 0.10 ±0.015 | 0.295 | 0.295 |

*Table 5 - Dimensions and tolerances*

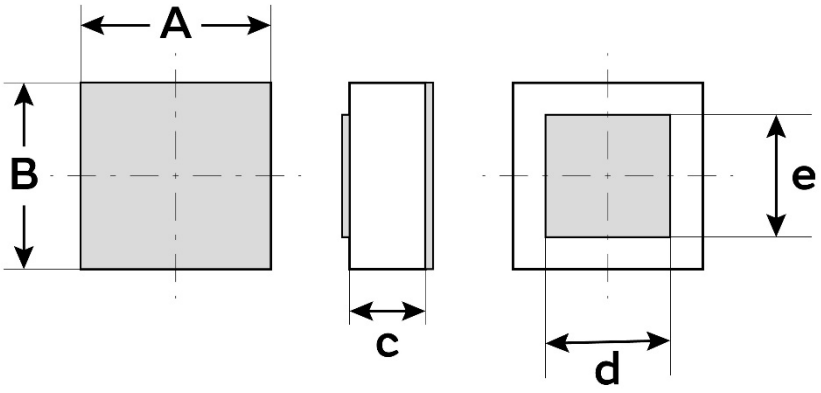


*Figure 7 - Package outline drawing*

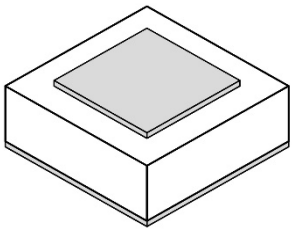

*Figure 8 - Package isometric view*

## Assembly

UWSC capacitors are directly mounted on the PCB application using die bonding and wire bonding.

It is applicable for standard wire bonding assembly (ball and wedge).

For further information, please see our mounting application note.

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

*Figure 9 Scan this QR Code to access the Murata Silicon Capacitor web page*

## Packaging format

Please refer to application note ‘Products Storage Conditions and Shelf Life’.

**Film Frame Carrier:**

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

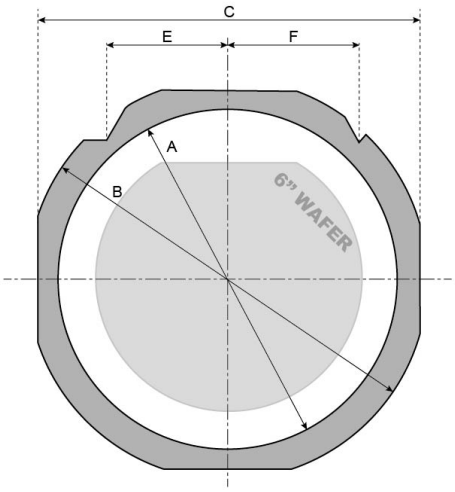


*Figure 10 FF070 Frame with a 6" wafer*

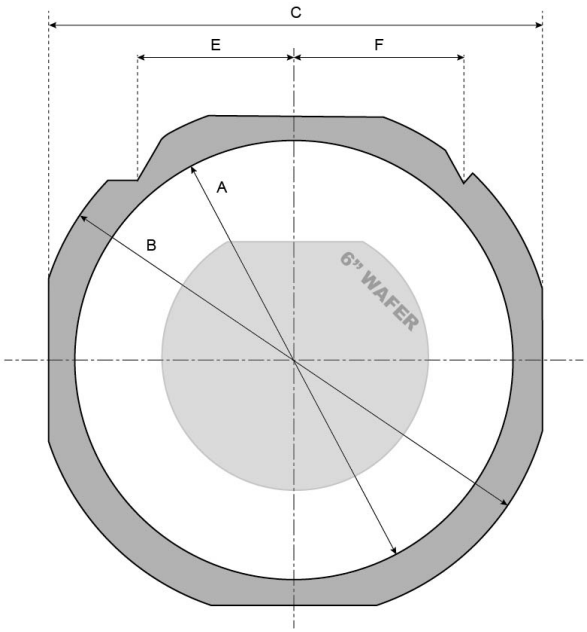


*Figure 11 FF108 Frame with a 6" wafer*

| Frame Reference | Frame Style | Inside diameter A | Outside diameter B | Width C | Thickness | Pin location E | Pin location F |
|---|---|---|---|---|---|---|---|
| FF070 (1) | DTF-2-6-1 | 7.638” | 8.976” | 8.346” | 0.048’’ | 2.370” | 2.5’’ |
| FF108 (1) | DTF-2-8-1 | 9.842” | 11.653” | 10.866” | 0.048” | 2.381” | 2.5’’ |

*Table 6 - Frame dimensions (inches)*

(1) or equivalent

**Expander grip ring 6” diameter:**

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

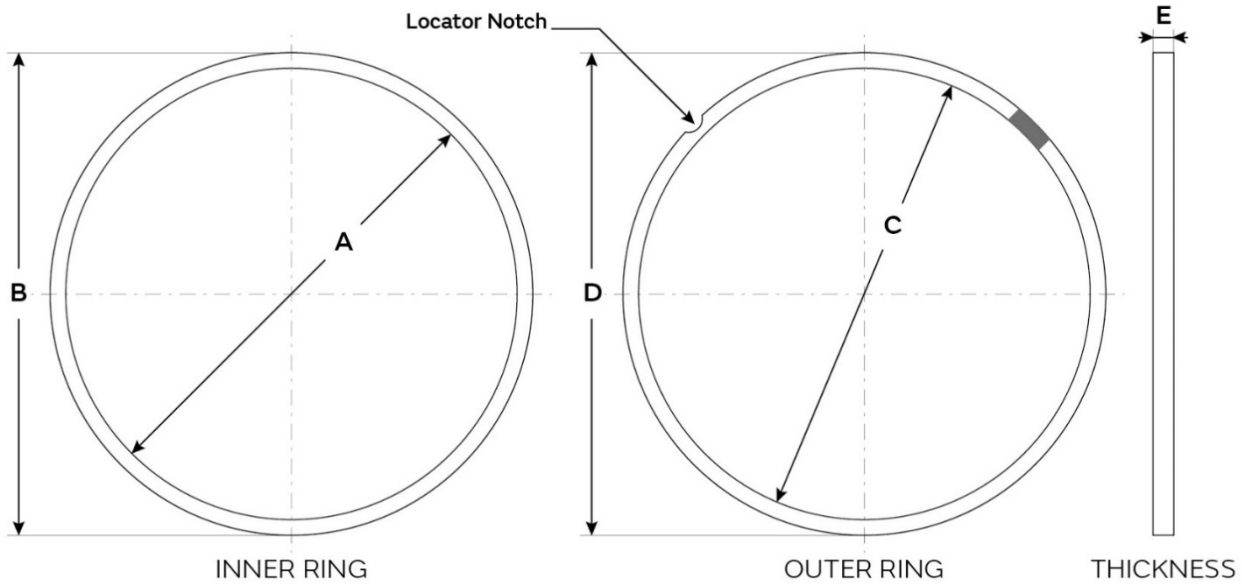


*Figure 12 – Grip Ring drawing*

| Grip Ring Style | A | B | C | D | E | Locator Notch |
|---|---|---|---|---|---|---|
| GRP-2620-6 (1) | 7.670” | 7.973” | 7.975” | 8.280” | 0.236” | None |

*Table 7 - Frame dimensions (inches)*

(1) or equivalent

**Waffle pack:**

Please refer to application note 'Waffle Pack Chip Carrier Handling & Opening Procedure'. Dies are not flipped in the waffle pack cavity (wire bond pad up).

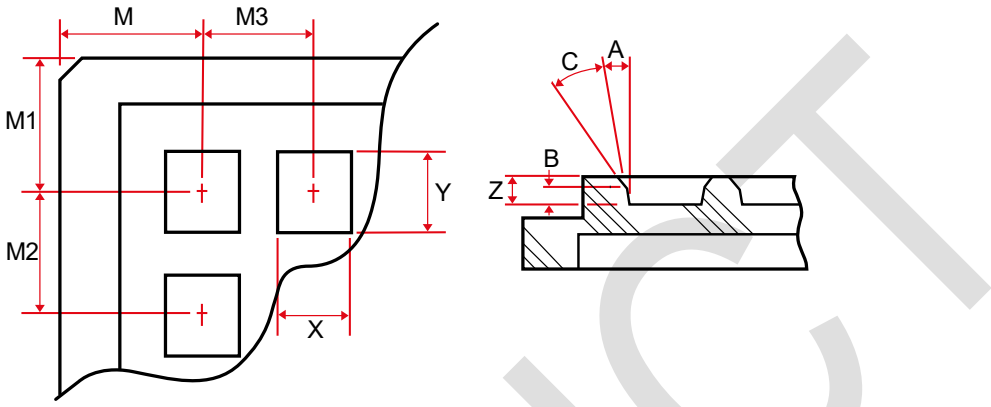


*Table 8 - Waffle pack drawing*

| External dimensions | Max. capacity | Pocket length X | Pocket width Y | Pocket depth Z |
|---|---|---|---|---|
| 2 inches | 20 x 20 | $0.48_{\pm 0.05}$ | $0.48_{\pm 0.05}$ | $0.28_{\pm 0.05}$ |

*Table 9 - Waffle pack dimensions (mm)*

| M | M1 | M2 | M3 | A |
|---|---|---|---|---|
| $4.60_{\pm 0.08}$ | $4.60_{\pm 0.08}$ | $2.18_{\pm 0.05}$ | $2.18_{\pm 0.05}$ | $7^{\circ}$ $_{\pm 1/2^{\circ}}$ |

*Table 10 - Waffle pack dimensions (mm)*

## Definitions

Data sheet status

**Objective specification:** This data sheet contains target or goal specifications for product development.

**Preliminary specification:** This data sheet contains preliminary data; supplementary data may be published later.

**Product specification:** This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

## Revision history

| Revision | Date | Description | Author |
|---|---|---|---|
| Release 1.00 | 2019 July 11th | Creation | OGA, SCA |
| Release 2.00 | 2020 Oct 20th | Preliminary release | OGA, SCA |
| Release 3.00 | 2021 June 18th | Product release | OGA, SCA, LLR, CGU, SYO, DYO |

## Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.





www.murata.com
mis@murata.com