

# Ultra-Broadband wire bondable / Embedding Silicon Capacitor UBEC 0201M 10nF BV11



Rev. 3.00

## General description

UBEC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.

The UBEC is suitable for DC decoupling, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.

These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 10 nF in a SMT 0201M. The UBEC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.

UBEC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (70ppm/K).

**Assembly:** Suitable for Wire bonded or embedded applications through existing laminated packages (LGA, BGA) or rigid PCB, FR4 (laminated) or flex platforms.

**Pads finishing:** Min 3µm Aluminium for wire bonding, other finishing available on request such as thin copper for embedding.

## Key features

- Broadband performance up to 67 GHz
- Resonance free
- Phase stability
- Insertion loss < 0.4dB Typ. up to 60 GHz.
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 100 µm
- Break down voltage: 11V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0201 footprint

## Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency (*i.e.* capacitance per unit volume)
- Broadband test equipment



## Functional diagram

The next figure provides implementation set-up diagram.

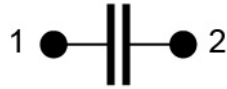


Figure 1 Block Diagram

## Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	10	-	nF
$\Delta C_P$	Capacitance tolerance <sup>(1)</sup>	@+25°C	-15	-	+15	%
T <sub>OP</sub>	Operating temperature		-55	20	150	°C
T <sub>STG</sub>	Storage temperature <sup>(2)</sup>		-70	-	165	°C
$\Delta C_T$	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
R <sub>VDC</sub>	Rated voltage <sup>(3)</sup>		-	-	3.8 <sup>(4)</sup> 3.4 <sup>(5)</sup>	V <sub>DC</sub>
BV	Break down voltage	@+25°C	11	-	-	V
$\Delta C_{RVDC}$	Capacitance voltage variation	From 0 V to R <sub>VDC</sub> , @+25°C	-	-	0.1	%/V <sub>DC</sub>
IR	Insulation resistor	@R <sub>VDC</sub> , +25°C, 120s	-	10	-	GΩ
ESL	Equivalent Serial Inductance <sup>(6)</sup>	@+25°C, SRF shunt mode	-	100	-	pH
ESR	Equivalent Serial Resistance <sup>(6)</sup>	@+25°C, shunt mode	-	300	-	mOhm
F <sub>C-3dB</sub>	Cut-off frequency at 3dB <sup>(6)</sup>	@+25°C	-	160	187	kHz
IL	Insertion loss <sup>(6)</sup>	@ 20 GHz, +25°C	-	0.2	-	dB
		@ 40 GHz, +25°C	-	0.3	-	dB
		@ 60 GHz, +25°C	-	0.4	-	dB
RL	Return loss <sup>(6)</sup>	Up to 60 GHz, +25°C	24	-	-	dB
ESD	HBM stress <sup>(7)</sup>	JS-001-2017	8	-	-	kV

Table 1 - Electrical performances

<sup>(1)</sup>: other tolerance available upon request.

<sup>(2)</sup>: without packaging.

<sup>(3)</sup>: Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'.

<sup>(4)</sup>: 10 years of intrinsic life time prediction at 100°C continuous operation.

<sup>(5)</sup>: 10 years of intrinsic life time prediction at 150°C continuous operation.

<sup>(6)</sup>: with wire bonding de-embedded

<sup>(7)</sup>: please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'.

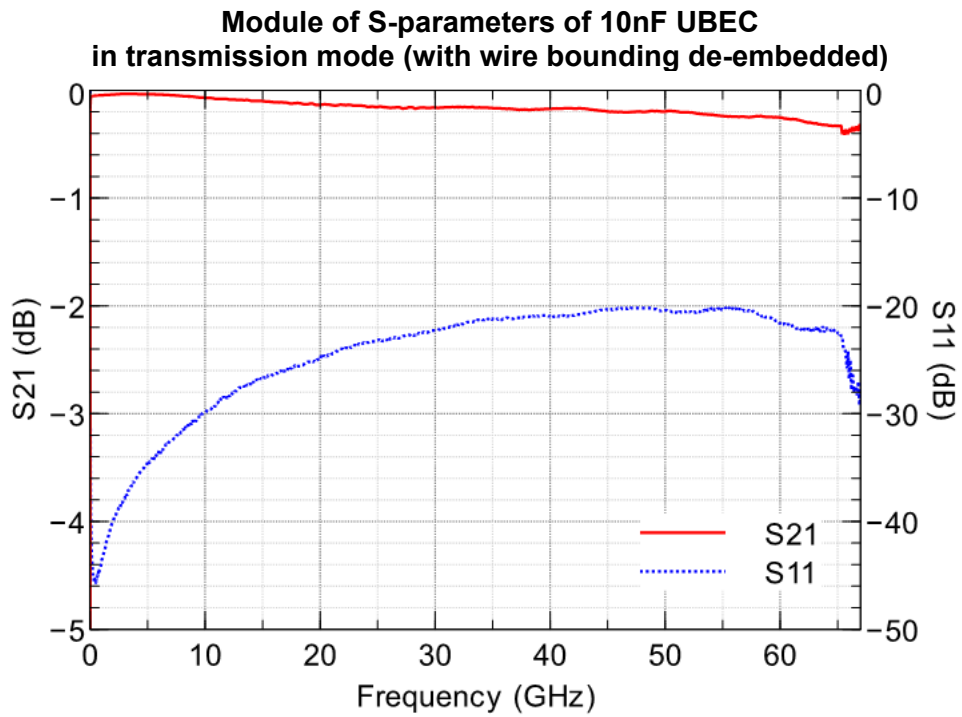


Figure 2 - 10nF UBEC measurement results (module of S-parameters)

**Schematic of 10nF UBEC in transmission mode**

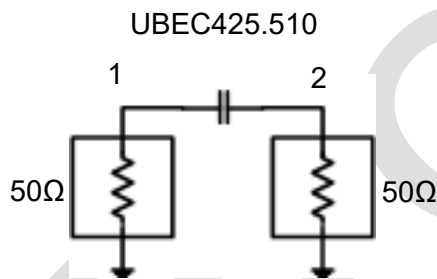


Figure 3 - 10nF UBEC measurement schematic

**Example of 0201M wire bonded**

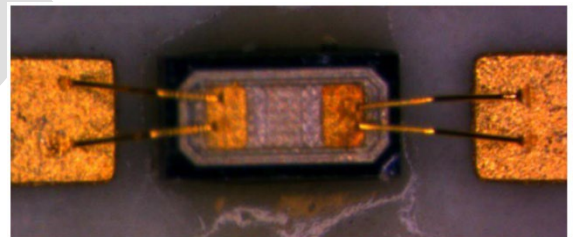


Figure 4 – micro picture of UBEC mounted on board in coplanar mode



## Pinning definition

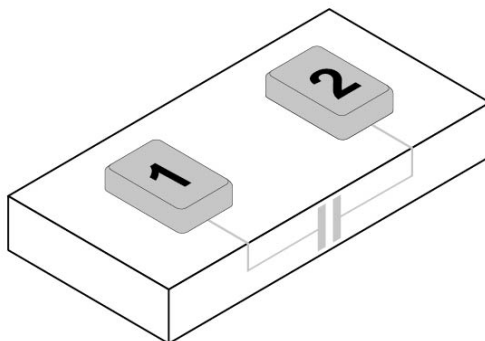


Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-150.0 / 0.0
2	Signal	150.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

## Ordering Information

Regardless of packaging, Murata Integrated Passive Devices delivers products with AQL level II (0.65).

Type number	Package		
	Packaging	Finishing	Description
935157425510-W0A	2" X 2" WP	Al <sup>(2)</sup>	UBEC 0201M - 10nF – 2 pads – 0.6 x 0.3 mm x 0.10mm <sup>(3)</sup>
935157425510-F1A	6" film frame carrier <sup>(1)</sup>	Al <sup>(2)</sup>	UBEC 0201M - 10nF – 2 pads – 0.6 x 0.3 mm x 0.10mm <sup>(3)</sup>

- (1) Other Film Frame Carrier are possible on request
- (2) Al = Min 3µm Aluminium
- (3) Refer to Figure 7

Table 3 - Packaging and ordering information

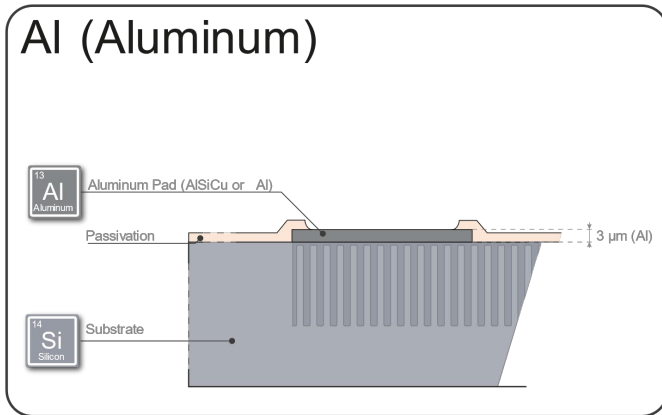
Product Name	Die Name	Description
UBEC425.510	XEM0201510	UBEC 10nF/0201M/BV11 – 2 pads – 0.6 x 0.3 x 0.10 mm

Table 4 - Die information

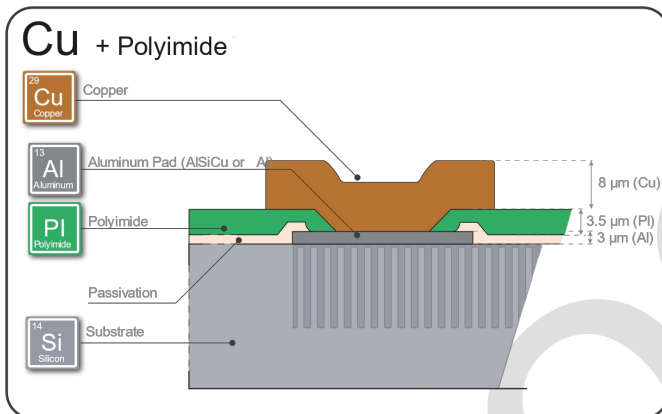


## Pad Metallization

This wire bonding / embedding Silicon Capacitor is delivered as standard with Aluminium pads.



Other Metallization, such as Copper or thick Gold pads are possible on request.



Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

## Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

## Package outline

The product is delivered as a bare silicon die.

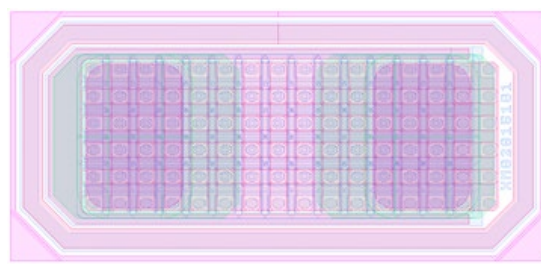


Figure 6 – Layout view



L (mm)	W (mm)	T (mm)	c (mm)	p (mm)	e (mm)	t (mm)
0.60 ±0.02	0.30 ±0.02	0.10 ±0.01	0.10	0.20	0.15	0.003 <sup>(1)</sup> 0.008 <sup>(2)</sup>

(1) Standard Al with wire bonding application.  
 (2) Standard Cu with *embedding* application

Table 5 - Dimensions and tolerances

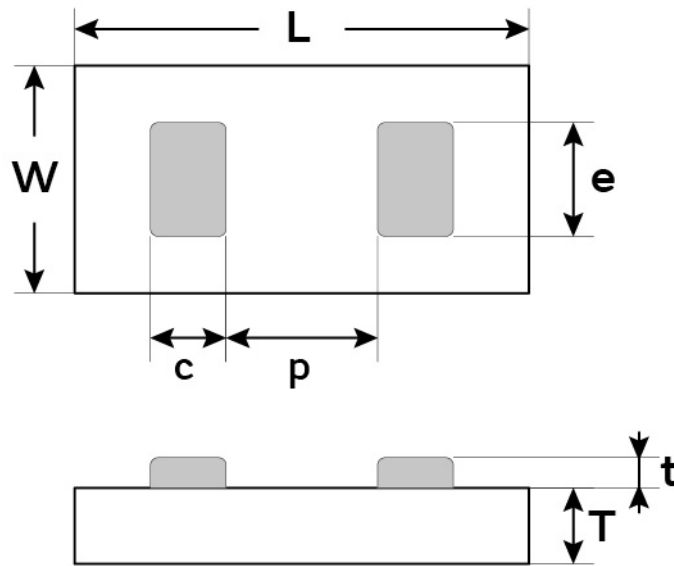


Figure 7 - Package outline drawing

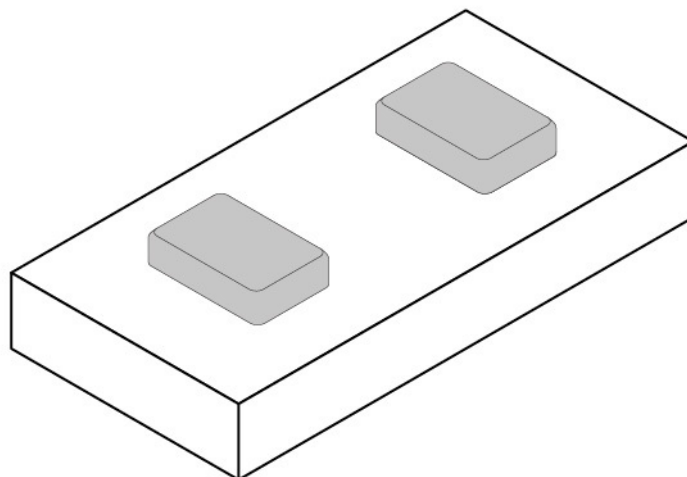
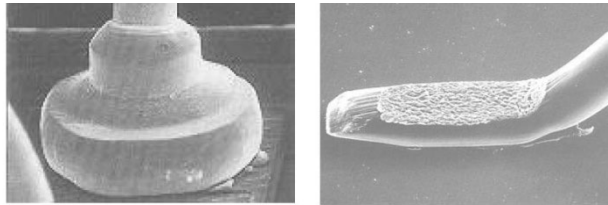


Figure 8 Isometric top view



## Assembly

UBEC series is compatible with standard wire bonding assembly (ball and wedge) technology. It can be directly mounted on the PCB using standard.



Ball bond

Wedge bond

For further information, please see our mounting application note

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



Figure 9 Scan this QR Code to access the Murata Silicon Capacitor web page



## Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

### Film frame carrier:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

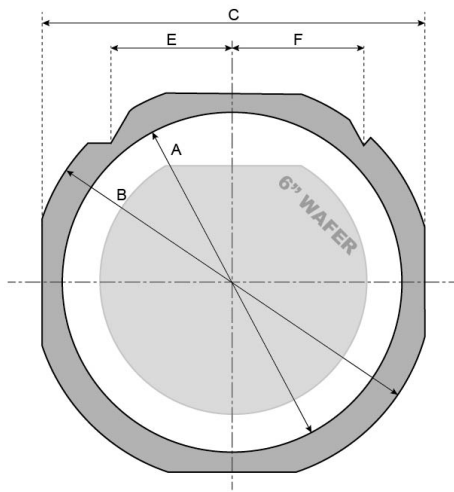


Figure 10 FF070 Frame with a 6" wafer

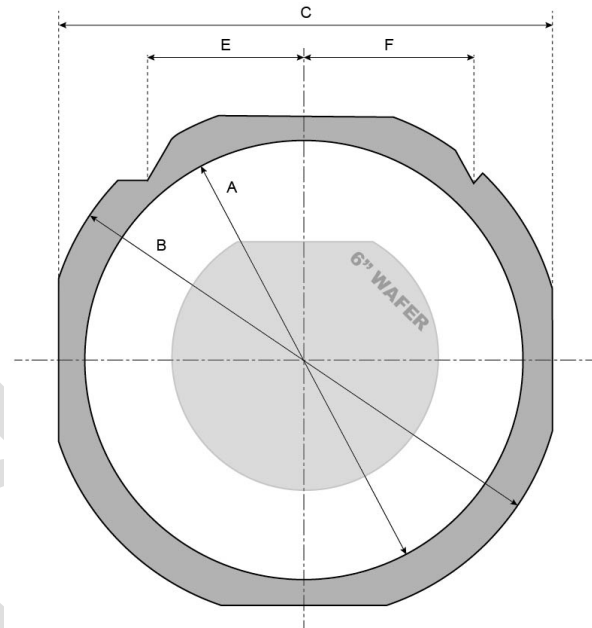


Figure 11 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 <sup>(1)</sup>	DTF-2-6-1	7.638"	8.976"	8.346"	0.048"	2.370"	2.5"
FF108 <sup>(1)</sup>	DTF-2-8-1	9.842"	11.653"	10.866"	0.048"	2.381"	2.5"

Table 6 - Frame dimensions (inches)

(1) or equivalent





**Definitions**

Data sheet status

**Objective specification:** This data sheet contains target or goal specifications for product development.

**Preliminary specification:** This data sheet contains preliminary data; supplementary data may be published later.

**Product specification:** This data sheet contains final product specifications.

Limiting values: Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information: Where application information is given, it is advisory and does not form part of the specification.

**Revision history**

Revision	Date	Description	Author.
Release 1.00	2016 April 04th	Objective specification	OGA
Release 1.07	2021 March 10 <sup>th</sup>	Update and new template	SCA; CGU; LLE; SJA, OGA
Release 1.08	2021 Feb. 09 <sup>th</sup>	Packaging update	CGU
Release 2.00	2022 Oct. 29th	Preliminary specification	OGA
Release 3.00	2023 April 07th	Product specification	OGA

**Disclaimer / Life support applications**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.

Murata Integrated Passive Solutions S.A. makes no representation that the use of its products in the circuits described herein, or the use of other technical information contained herein, will not infringe upon existing or future patent rights. The descriptions contained herein do not imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith. Specifications are subject to change without notice.



[www.murata.com](http://www.murata.com)

[mis@murata.com](mailto:mis@murata.com)