



Rev. 2.01

## General description

The aim of this document is to give a description of Murata Integrated Passive Solutions' Wire Bonding Silicon vertical Capacitor (WBSC) characteristics for Chip On Board (COB) assembly solutions.

The WBSC/WLSC Capacitor targets power supplies decoupling and filtering of active devices. This version is a single 2.7nF capacitor in 0.5 x 1.25mm package size. Other capacitance values and other package size are available as a single die or capacitor array; please feel free to contact us.

The WBSC/WLSC Capacitor is based on PICS Integrated Passive technology.

Standard PCB FR4 can be used.

WBSC/WLSC capacitors are directly mounted on the PCB application using die bonding and wire bonding processes. Standard FR4 PCB can be used. The bottom electrode is in TiNiAu and the top electrode is in TiWAu. Other top finishings such as Aluminum are available on request.

## Key features

- Full compatible Monolithic ceramic capacitors for replacement
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.02%/Volts
  - Negligible capacitance loss through ageing
- Low profile 0.25mm $\pm$ 0.010mm (standard), but lower thickness is possible (i.e 0.10mm) on request.
- Small size 0205 [0.5 x 1.25 mm  $\pm$ 0.02mm ]
- Break down voltage: 150V
- Low leakage current
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Applicable for standard wire bonding assembly (ball and wedge)

## Key applications

- Any demanding applications, such as medical, aerospace, automotive industrial...
- Supply decoupling / filtering of active device
- High reliability applications
- Devices with battery operations
- High temperature applications
- High volumetric efficiency (i.e. capacitance per unit volume)



## Functional diagram

The next figure provides implementation set-up diagram.

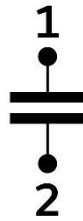


Figure 1 Block Diagram

## Electrical performances

| Symbol            | Parameter                                   | Conditions                               | Min. | Typ. | Max.                                   | Unit              |
|-------------------|---|--|------|------|--|-------------------|
| C                 | Capacitance value                           | @+25°C                                   | -    | 2.7  | -                                      | nF                |
| $\Delta C_P$      | Capacitance tolerance <sup>(1)</sup>        | @+25°C                                   | -15  | -    | +15                                    | %                 |
| T <sub>OP</sub>   | Operating temperature                       |  | -55  | 20   | 150                                    | °C                |
| T <sub>STG</sub>  | Storage temperature <sup>(2)</sup>          |  | -70  | -    | 165                                    | °C                |
| $\Delta C_T$      | Capacitance temperature variation           | -55 °C to 150 °C                         | -    | 60   | -                                      | ppm/K             |
| RV <sub>DC</sub>  | Rated voltage <sup>(3)</sup>                |  | -    | -    | 61 <sup>(4)</sup><br>68 <sup>(5)</sup> | V <sub>DC</sub>   |
| BV                | Break down voltage                          | @+25°C                                   | 150  | -    | -                                      | V                 |
| $\Delta C_{RVDC}$ | Capacitance voltage variation               | From 0 V to RV <sub>DC</sub> ,<br>@+25°C | -    | -    | -0.02                                  | %/V <sub>DC</sub> |
| IR                | Insulation resistor                         | @RV <sub>DC</sub> , +25°C, 120s          | -    | 1    | -                                      | GΩ                |
| ESL               | Equivalent Serial Inductance <sup>(6)</sup> | @+25°C, SRF shunt mode                   | -    | 20   | -                                      | pH                |
| ESR               | Equivalent Serial Resistance <sup>(6)</sup> | @+25°C, shunt mode                       | -    | 30   | -                                      | mOhm              |

Table 1 - Electrical performances

(1): other tolerance available upon request

(2): without packaging

(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'

(4): 10 years of intrinsic life time prediction at 100°C continuous operation

(5): 10 years of intrinsic life time prediction at 150°C continuous operation

(6): estimate, theoretical two terminal equivalent (applicable to multi term capacitors)

(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

For extended frequency range (up to 26GHz), see Ultra large band Wire bonding vertical Silicon Capacitor (UWSC).



**Pinning definition**

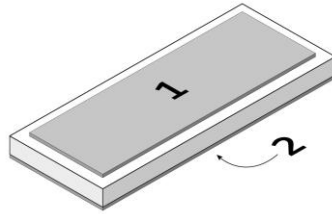


Figure 2 Pinning definition

| pin # |  |
|-------|--|
| 1     | Top side 7<br>top electrode in Au                                  |
| 2     | Back side<br>bottom electrode in Ti (0.1 μm)/Ni (0.3μm)/Au (0.2μm) |

Table 2 - Pinning description.

**Ordering Information**

Murata Integrated Passive Devices delivers products with AQL level II (0.65).

| Part number      | Die Name  | Package                    |                   |   |
|------------------|-----------|----------------------------|-------------------|---|
|                  |           | Packaging                  | Finishing         | Description   |
| 935242520427-F1T | WO0205427 | 6" FFC <sup>(1)</sup>      | Au <sup>(2)</sup> | WBSC 2.7nF BV150 – 1 bondpad – 0.5 x 1.25mm x 0.25mm <sup>(3)</sup> |
| 935242520427-T3T | WO0205427 | T&R 1Kunits <sup>(4)</sup> | Au <sup>(2)</sup> | WBSC 2.7nF BV150 – 1 bondpad – 0.5 x 1.25mm x 0.25mm <sup>(3)</sup> |
| 935246520427-F1T | WO0205427 | 6" FFC <sup>(1)</sup>      | Au <sup>(2)</sup> | WLSC 2.7nF BV150 – 1 bondpad – 0.5 x 1.25mm x 0.10mm <sup>(3)</sup> |
| 935246520427-T3T | WO0205427 | T&R 1Kunits <sup>(4)</sup> | Au <sup>(2)</sup> | WLSC 2.7nF BV150 – 1 bondpad – 0.5 x 1.25mm x 0.10mm <sup>(3)</sup> |

Table 3 - Packaging and ordering information

- (1) Other film frame carrier are possible on request
- (2) Au = TiWAu(0.3μm) / Au (3μm)
- (3) Refer to Figure 3
- (4) Missing capacitors can reach 0.5%



**Pad Metallization**

The wire bondable capacitor like WBSC / WLSC is delivered as standard with the bottom electrode in TiNiAu (Ti=0.1µm; Ni=0.3µm; Au=0.2µm) and top electrode in TiWAu (0.3µm) / Au (3µm). Other Metallization, such as Thick Gold or Aluminum pads are possible on request. Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

**Material regulation**

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative

**Package outline**

The product is delivered as a naked silicon die, with passivation opening for contacts.

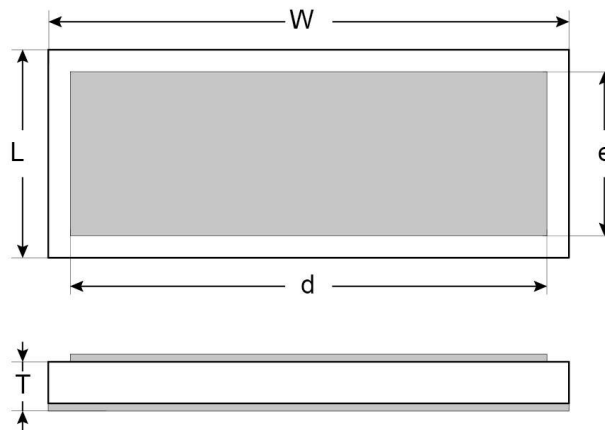


Figure 3 - Package outline drawing

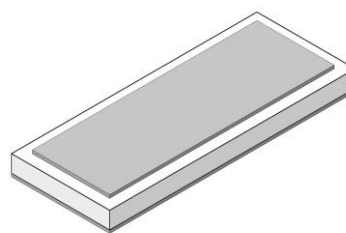


Figure 4 - Package isometric view

| L (mm)     | W (mm)     | T (mm)                | d (mm) | e (mm) |
|------------|------------|-----------------------|--------|--------|
| 0.50 ±0.02 | 1.25 ±0.02 | 0.25 or 0.10<br>±0.01 | 1.414  | 0.394  |

Table 4 - Dimensions and tolerances



## Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



Figure 5 Scan this QR Code to access the Murata Silicon Capacitor web page

## Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

### Tape and Reel:

Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

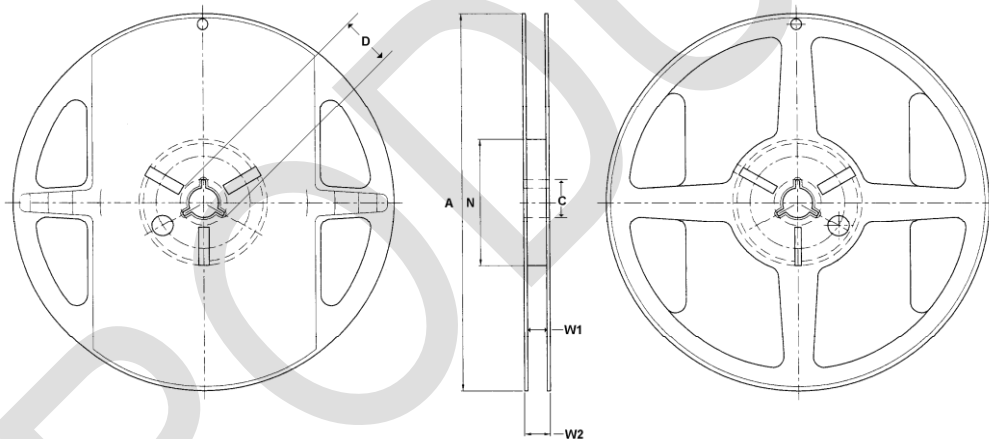


Figure 6 - Reel drawing

| Tape Width | Diameter A        | C    | D    | Hub N | W1 | W2   |
|------------|-------------------|------|------|-------|----|------|
| 8          | 178<br>(7 inches) | 13.5 | 20.2 | 60    | 9  | 11.5 |

Table 5 – Reel dimensions (mm)

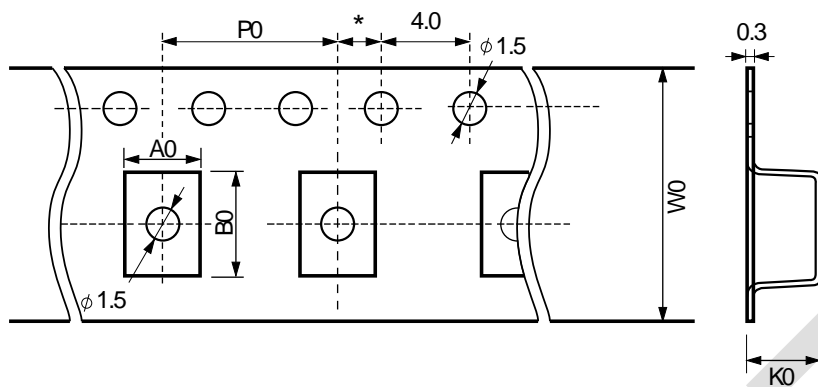


Figure 7 - Tape drawing

| Cavity dimensions |      |   | Carrier tape width W0 | Carrier tape pitch P0 |
|-------------------|------|---|-----------------------|-----------------------|
| Ao                | Bo   | Ko  |                       |                       |
| 0.6               | 1.35 | 0.2 (for 0.10mm thick.)<br>0.33 (for 0.10mm thick.) | 8 mm                  | 2 mm                  |

Table 6 - Tape dimensions (mm)

**Film frame carrier:**

With UV curable dicing tape (UV performed). Good dies are identified using the appropriate e-mapping format. No ink is added on wafer to label other dies.

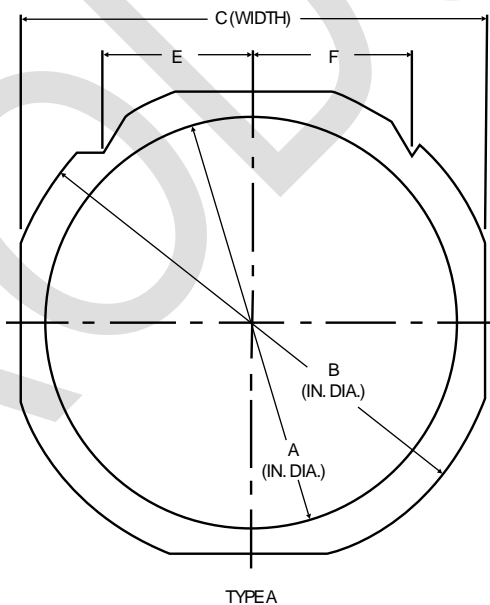


Figure 8 - Film frame drawing

| Wafer diameter r | Inside diameter r A | Outside diameter B | Width C | Thickness | Pin location E | Pin location F | Frame style |
|------------------|---------------------|--------------------|---------|-----------|----------------|----------------|-------------|
| 6"               | 7.639"              | 8.976"             | 8.346"  | 0.048"    | 2.370"         | 2.5"           | DTF-2-6-1   |

Table 7 - Frame dimensions (inches)



## Definitions

### Data sheet status

**Objective specification:** This data sheet contains target or goal specifications for product development.

**Preliminary specification:** This data sheet contains preliminary data; supplementary data may be published later.

**Product specification:** This data sheet contains final product specifications.

### Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

### Application information

Where application information is given, it is advisory and does not form part of the specification.

## Revision history

| Revision     | Date                | Description             | Author    |
|--------------|---------------------|-------------------------|-----------|
| Release 1.0  | 2019 January 09th   | Objective specification | LLE       |
| Release 1.1  | 2019 may 24th       | Objective specification | LLE       |
| Release 1.4  | 2019 september 12th | Objective specification | LLE       |
| Release 1.5  | 2020 April 15th     | Objective specification | LLE + SCA |
| Release 2.01 | 2020 July 29th      | Product Release         | LLE + SCA |

## Disclaimer / Life support applications

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