MAX32675C

Ultra-Low-Power Arm Cortex-M4F with Precision Analog Front-End and HART for Industrial and Medical Sensors

General Description

The MAX32675C is a highly integrated, mixed-signal, ultra-low-power microcontroller for industrial applications and is especially suitable for 4-20mA loop-powered sensors and transmitters. It is based on an ultra-low-power Arm® Cortex®- M4 with floating point unit (FPU) and includes 384KB (376KB user) flash and 160KB of SRAM. Error correction coding (ECC), capable of single-error correction, double-error detection (SEC-DED), is implemented over the entire flash, SRAM, and cache to ensure ultra-reliable code execution for demanding applications.

An analog front-end (AFE) with an integrated, low-power HART modem enables the bidirectional transfer of digital data over a current loop with industrial sensors for configuration and diagnostics. The AFE also provides two 12-channel delta-sigma (Δ-Σ) ADCs with features and specifications optimized for precision sensor measurement. Each Δ-Σ ADC can digitize external analog signals as well as system temperature. A PGA with gains of 1x to 128x precedes each ADC. ADC outputs can be optionally converted on the fly from integer to single-precision floating-point format. A 12-bit DAC is also included.

The device also provides robust security features, including an AES engine and persistent key storage.

Applications

- 4-20mA Industrial Sensors and Transmitters
- Industrial Pressure, Temperature, Flow, and Level Sensors/Transmitters
- Medical Pressure, Temperature, and Flow Sensors

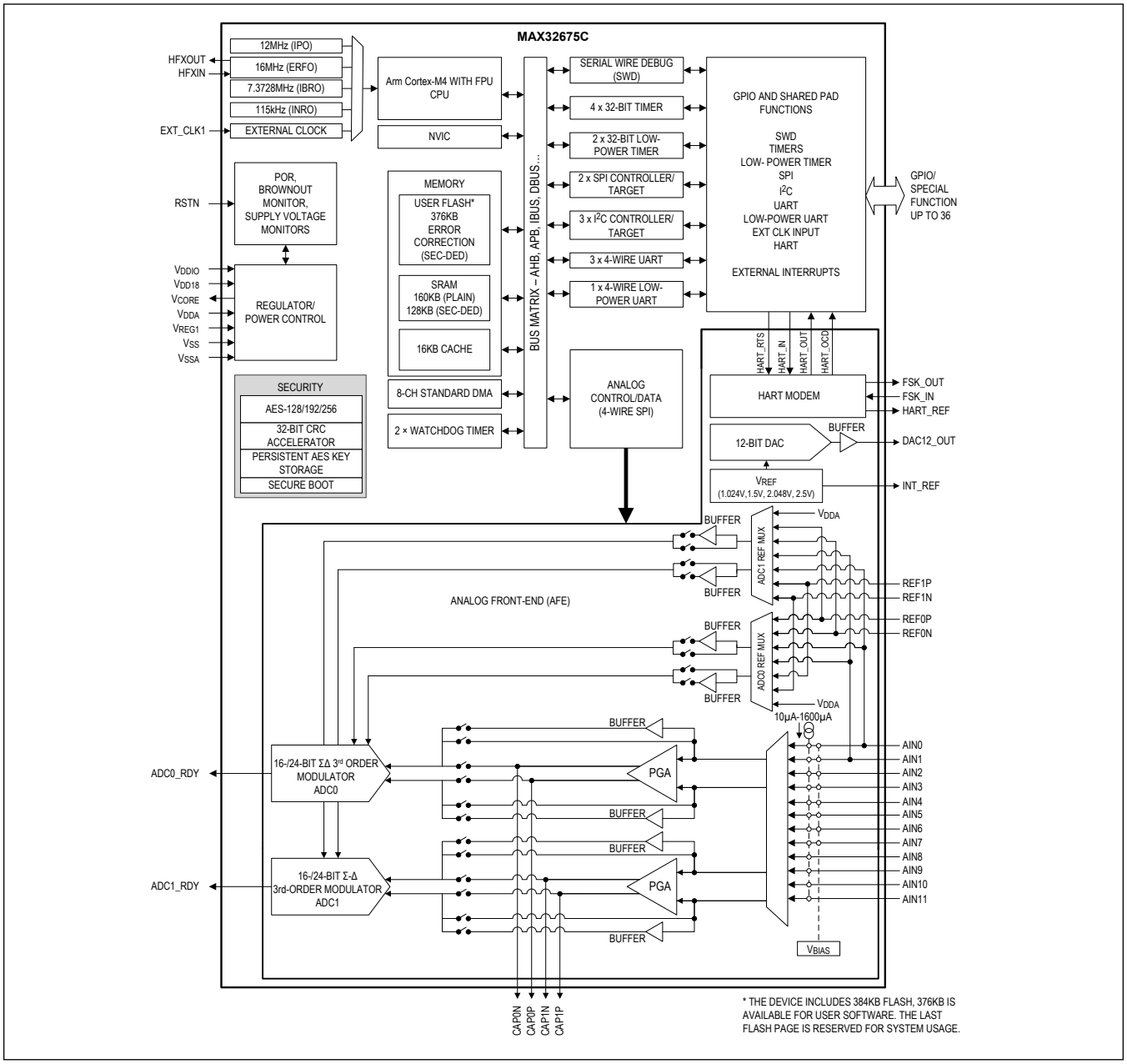
Benefits and Features

- Low-Power, High-Performance for Industrial Applications
  - 12MHz Arm Cortex-M4 with FPU
  - 384KB (376KB User) Flash Memory
  - 160KB SRAM (128KB with ECC Enabled)
    - Optionally Retained in Low-Power Modes
  - ACTIVE Current (I_{DD_ACTS}) ≤ 2.1mA at T_A = +85°C
    - Ideal for 4-20mA Current Sense Loops
  - Startup Current Typical (I_{DD_STRT}) of 1.02mA
  - 375µA Full Memory Retention Current in BACKUP (I_{DD_FBKUS})
- Smart Integration Reduces BOM, Cost, and PCB Size
  - Integrated HART Modem
  - Two Δ-Σ ADCs
    - 12 Channels, Assignable to Either ADC
    - Flexible Resolution and Sample Rates
      - 24-Bits at up to 0.4ksps
  - 12-Bit DAC
  - Internal Reference
  - Digital Peripherals
    - Up to Two SPI
    - Up to Three I^2C
    - Up to Three 4-Wire UART
    - Up to One 4-Wire Low-Power UART (LPUART)
  - 8-Channel Standard DMA Controller
  - Up to 36 GPIOs
  - Timers
    - Four 32-Bit Timers
    - Two 32-Bit Low-Power Timers (LPTMR)
    - Two Windowed Watchdog Timers
  - Robust Security and Reliability
    - UART ROM Bootloader
    - AES 128/192/256 Hardware Acceleration Engine
    - Persistent Key Storage
    - 32-Bit CRC Acceleration Engine
    - Wide, -40°C to +105°C Operating Temperature Range

Ordering Information *appears at end of data sheet.*

19-101896; Rev 0; 6/24

Simplified Block Diagram



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Absolute Maximum Ratings

HFXIN ..... -0.3V to 0.95V
AIN[0-11][1] ..... -0.3V to V_{DDA} + 0.3V
V_{DDIO}, V_{DDA} ..... -0.3V to +3.63V
RSTN, GPIO, ADC0_RDY, ADC1_RDY ... -0.3V to V_{DDIO} + 0.3V
FSK_OUT, FSK_IN, HART_REF ..... -0.3V to 1.98V
CAP1N, CAP1P, CAP0N, CAP0P, DAC12_OUT[1] -0.3V to V_{DDA} + 0.3V
REF1P, REF1N, REF0P, REF0N[1] ..... -0.3V to V_{DDA} + 0.3V
Total Current, All GPIO Combined (sink) 100mA
Total Current, All GPIO Combined (source) ..... -100mA
V_{SS}, V_{SSA} 100mA
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA
Continuous Package Power Dissipation 72L LGA (multilayer board) T_A = 70°C) (derate 29.77mW/°C above +70°C) 2381.66mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +125°C
Soldering Temperature (reflow) ..... +260°C

Note 1: No device pin can exceed 3.63V.

Note 2: All voltages with respect to V_{SS}, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

72L LGA

Package Code	L7288M+1
Outline Number	21-100599
Land Pattern Number	90-100210
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	33.59°C/W
Junction to Case (θ_{JC})	12.37°C/W

For the latest package outline information and land patterns (footprints), go to analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.

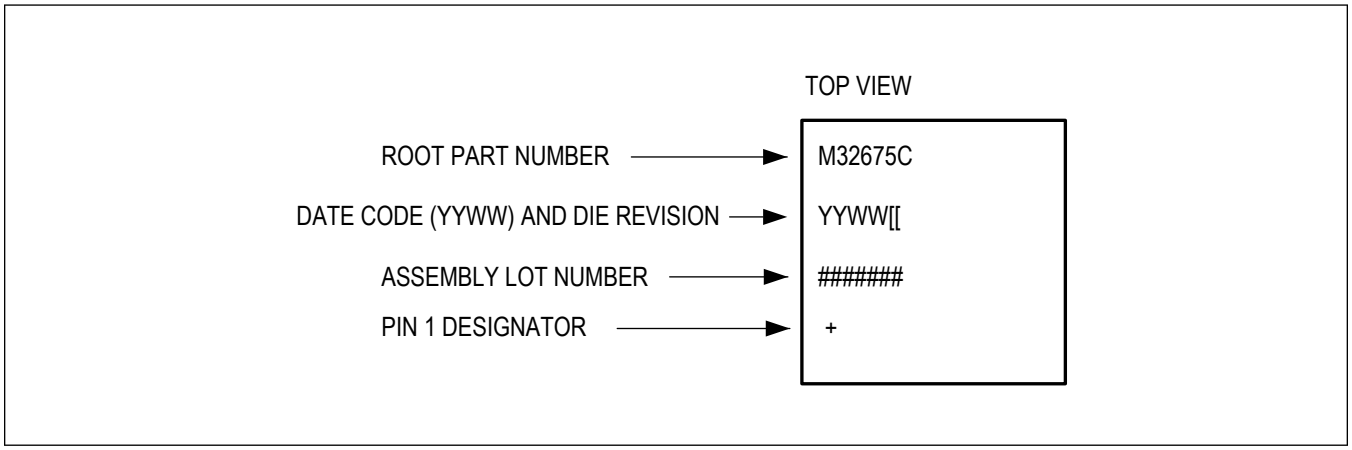


Figure 1. Example 72L LGA Top Marking

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER							
Supply Voltage, Digital	V_{DDIO}	The V_{DDIO} device pin must be connected to the V_{DDA} device pin.		2.7	3.0	3.63	V
Supply Voltage, Analog	V_{DDA}	The V_{DDIO} device pin must be connected to the V_{DDA} device pin.		2.7	3.0	3.63	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DDIO}		1.55		2.4	V
Power-On-Reset (POR) Voltage	V_{POR}	Monitors V_{DDIO}			1.4		V
Total V_{DDIO} and V_{DDA} Current ACTIVE Mode	I_{DD_ACTS}	Total current into V_{DDIO} and V_{DDA} pins. T_A = +85°C (*Note 3*) V_{DDIO} = V_{DDA} = 3.0V OVR[00] (*Note 4*). ERFO enabled and clocked externally at 16MHz, does not include oscillator current. IPO and IBRO disabled. ECC disabled. HART modem active in receive mode. All external pins biased.	CPU in ACTIVE mode at 2MHz with cache enabled.		1.4		mA
			CPU in ACTIVE mode at 4MHz with cache enabled.		1.5	2.1	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DDIO} and V_{DDA} Current ACTIVE Mode	I_{DD_DACTS}	Dynamic current. CPU in ACTIVE mode executing Coremark. OVR = [00] (*Note 4*). Total current into V_{DDIO} and V_{DDA} pins. V_{DDIO} = V_{DDA} = 3.0V. ECC disabled. AFE disabled. HART unbiased. Inputs tied to V_{SS} or V_{DDIO}. Outputs source/sink 0mA.		53		µA/MHz
		Dynamic current. CPU in ACTIVE mode executing while(1). OVR = [00] (*Note 4*). Total current into V_{DDIO} and V_{DDA} pins. V_{DDIO} = V_{DDA} = 3.0V. ECC disabled. AFE disabled. HART unbiased. Inputs tied to V_{SS} or V_{DDIO}. Outputs source/sink 0mA.		40		
	I_{DD_FACTS}	Fixed current. CPU in ACTIVE mode, 0MHz execution. OVR = [00] (*Note 4*). Total current into V_{DDIO} and V_{DDA} pins. V_{DDIO} = V_{DDA} = 3.0V. ECC disabled. AFE disabled. HART unbiased. Inputs tied to V_{SS} or V_{DDIO}. Outputs source/sink 0mA.		875		µA
Total V_{DDIO} and V_{DDA} Current SLEEP Mode	I_{DD_SLPS}	Total current into V_{DDIO} and V_{DDA} pins. CPU in SLEEP mode. V_{DDIO} = V_{DDA} = 3.0V OVR[00] (*Note 4*). ERFO enabled and clocked externally at 16MHz, does not include oscillator current. IPO and IBRO disabled. ECC disabled. AFE disabled. HART modem biased. All external pins biased.		840		µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total V_{DDIO} and V_{DDA} Fixed Current, DEEPSLEEP Mode	I_{DD_FDSLS}	Total current into V_{DDIO} and V_{DDA} pins. CPU in DEEPSLEEP mode. V_{DDIO} = V_{DDA} = 3.0V. OVR[00] (*Note 4*). ERFO enabled and clocked externally at 16MHz, does not include oscillator current. IPO and IBRO disabled. AFE disabled. HART modem biased. All external pins biased.			425		µA
Total V_{DDIO} and V_{DDA} Fixed Current BACKUP Mode	I_{DD_FBKUS}	Total current into V_{DDIO} and V_{DDA} pins. CPU in BACKUP mode. V_{DDIO} = V_{DDA} = 3.0V INRO enabled, all other clocks disabled. AFE held in reset. All pins biased.	0KB SRAM retained (retention regulator enabled). HART modem unbiased.		300		µA
			0KB SRAM retained (retention regulator enabled). HART modem biased.		375		
			160KB SRAM retained (retention regulator enabled). HART modem biased.		375		
Total V_{DDIO} and V_{DDA} Fixed Current STORAGE Mode	I_{DD_FSTOS}	Total current into V_{DDIO} and V_{DDA} pins. CPU in STORAGE mode. V_{DDIO} = V_{DDA} = 3.0V INRO enabled, all other clocks disabled. AFE held in reset. All pins biased. HART modem biased.			375		µA
Total V_{DDIO} and V_{DDA} Reset Current	I_{DD_RST}	Total current into V_{DDIO} and V_{DDA} pins. V_{DDIO} = V_{DDA} = 3.0V IBRO enabled. All pins biased. HART modem biased. Device in reset (external reset active).			590		µA
Total V_{DDIO} and V_{DDA} Startup Current	I_{DD_STRT}	Total current into V_{DDIO} and V_{DDA} pins. V_{DDIO} = V_{DDA} = 3.0V IBRO enabled. All pins biased. HART modem biased. After release of external reset until while(1) code execution.			1020		µA
SLEEP Mode Resume Time	t_{SLP_ONS}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code.			21.2		µs

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DEEPSLEEP Mode Resume Time	t_{DSL_ONS}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code.	fast_wk_en = 1		206		µs
			fast_wk_en = 0		351		
BACKUP Mode Resume Time	t_{BKU_ONS}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code, includes system initialization and ROM execution time.			16.3		ms
STORAGE Mode Resume Time	t_{STO_ONS}	f_{SYS_OSC} = IBRO, time from power mode exit to execution of application code, includes system initialization and ROM execution time.			16.7		ms
GENERAL-PURPOSE I/O							
Input Low Voltage for All GPIO, RSTN	V_{IL_GPIO}	Pin configured as GPIO				0.3 × V_{DDIO}	V
Input High Voltage for All GPIO, RSTN	V_{IH_GPIO}	Pin configured as GPIO		0.7 × V_{DDIO}			V
Output Low Voltage for ADC0_RDY	$V_{OL\_ADC0RDY}$	P0.26 must be set to output mode disabled (GPIO0_OUTEN[26] = 0)	V_{DDIO} = V_{DDA} = 2.7V, I_{OL} = 1mA			0.1 × V_{DDA}	V
Output Low Voltage for ADC1_RDY	$V_{OL\_ADC1RDY}$	P0.21 must be set to output mode disabled (GPIO0_OUTEN[21] = 0)	V_{DDIO} = V_{DDA} = 2.7V, I_{OL} = 1mA			0.1 × V_{DDA}	V
Output High Voltage for ADC0_RDY	$V_{OH\_ADC0RDY}$	P0.26 must be set to output mode disabled (GPIO0_OUTEN[26] = 0)	V_{DDIO} = V_{DDA} = 2.7V, I_{OH} = 1mA	0.9 × V_{DDA}			V
Output High Voltage for ADC1_RDY	$V_{OH\_ADC1RDY}$	P0.21 must be set to output mode disabled (GPIO0_OUTEN[21] = 0)	V_{DDIO} = V_{DDA} = 2.7V, I_{OH} = 1mA	0.9 × V_{DDA}			V
Output Low Voltage for All GPIO Except P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OL_GPIO}	V_{DDIO} = 2.7V, I_{OL} = 1mA, DS[1:0] = 00			0.2	0.4	V
		V_{DDIO} = 2.7V, I_{OL} = 2mA, DS[1:0] = 10			0.2	0.4	
		V_{DDIO} = 2.7V, I_{OL} = 4mA, DS[1:0] = 01			0.2	0.4	
		V_{DDIO} = 2.7V, I_{OL} = 6mA, DS[1:0] = 11			0.2	0.4	
Output Low Voltage for GPIO P0.6, P0.7, P0.12, P0.13, P0.18, P0.19	V_{OL_I2C}	V_{DDIO} = 2.7V, I_{OL} = 2mA, DS = 0			0.2	0.4	V
		V_{DDIO} = 2.7V, I_{OL} = 10mA, DS = 1			0.2	0.4	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage for All GPIO Except P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OH_GPIO}	V_{DDIO} = 2.7V, I_{OH} = -1mA, DS[1:0] = 00	V_{DDIO} - 0.4			V
		V_{DDIO} = 2.7V, I_{OH} = -2mA, DS[1:0] = 10	V_{DDIO} - 0.4			
		V_{DDIO} = 2.7V, I_{OH} = -4mA, DS[1:0] = 01	V_{DDIO} - 0.4			
		V_{DDIO} = 2.7V, I_{OH} = -6mA, DS[1:0] = 11	V_{DDIO} - 0.4			
Output High Voltage for GPIO P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OH_I2C}	V_{DDIO} = 2.7V, I_{OH} = -2mA, DS = 0	V_{DDIO} - 0.4			V
		V_{DDIO} = 2.7V, I_{OH} = -10mA, DS = 1	V_{DDIO} - 0.4			
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				100	mA
Combined I_{OH}, All GPIO	I_{OH_TOTAL}		-100			mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input/Output Pin Capacitance for All Pins	C_{IO}			4		pF
Input Leakage Current Low	I_{IL}	T_A = +85°C V_{IN} = 0V, internal pull-up disabled	-500		+500	nA
Input Leakage Current High	I_{IH}	T_A = +85°C V_{IN} = 3.63V, internal pull-down disabled	-500		+500	nA
Input Pull-up Resistor to RSTN	R_{PU_VDD}	Pull up to V_{DDIO} = V_{RST}, RSTN at V_{IH}		18.7		kΩ
		Pull up to V_{DDIO} = 3.63V, RSTN at V_{IH}		10.0		
Input Pull-up Resistor for All GPIO	R_{PU}	Device pin configured as GPIO, pull up to V_{DDIO} = V_{RST}, device pin at V_{IH}		18.7		kΩ
		Device pin configured as GPIO, pull up to V_{DDIO} = 3.63V, device pin at V_{IH}		10.0		
Input Pull-down Resistor for All GPIO	R_{PD}	Device pin configured as GPIO, pull down to V_{SS}, V_{DDIO} = V_{RST}, device pin at V_{IL}		17.6		kΩ
		Device pin configured as GPIO, pull down to V_{SS}, V_{DDIO} = 3.63V, device pin at V_{IL}		8.8		
RSTN Assertion Time	t_{RSTN}	Device in *ACTIVE* mode, RSTN device pin assertion duration to entry into device reset state.		6 x t_{SYS_CLK}		µs
CLOCKS						
System Clock Frequency	f_{SYS_CLK}				12	MHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS\_CLK}$		µs

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External RF Oscillator (ERFO)	f_{ERFO}	The oscillator supports a crystal of 16MHz. Required crystal characteristics: f_{XTAL} = 16MHz, C_{L_XTAL} = 12pF, ESR ≤ 50Ω, C_0 ≤ 7pF, crystal power dissipation ≥ 100µW. Refer to the device user guide for calculating the load capacitors. The accuracy is determined by the crystal and PCB layout.	16		16	MHz
Internal Baud Rate Oscillator (IBRO)	f_{IBRO}			7.3728		MHz
Internal Nanoring Oscillator (INRO)	f_{INRO}	V_{DDIO} = 3.0V		115		kHz
External System Clock Input Frequency	f_{EXT_CLK1}	EXT_CLK1 selected as system oscillator (P0.12 AF4)			8	MHz
External Clock Input Frequency for Low-Power Peripherals	f_{EXT_CLK2}	EXT_CLK2 enabled (P0.12 AF2)			1	MHz
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		20		ms
	t_{P_ERASE}	Page erase		20		
Flash Programming Time per Word	t_{PROG}	32-bit programming mode, f_{FLC_CLK} = 1MHz		16		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +125°C	10			years
Current Consumption During Flash Programming	I_{PROG}	Current required for flash write/erase, V_{DDIO}		6.5		mA

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Full-Scale Input Voltage	FS			±V_{REF}/ gain		
Absolute Input Voltage		Buffers disabled	V_{SSA} - 30mV		V_{DDA} + 30mV	V
Input Voltage Range		Unipolar	0		V_{REF}	V
		Bipolar	-V_{REF}		V_{REF}	

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Voltage Range	V_{CM}	AIN buffers/PGA disabled	V_{SSA}		V_{DDA}	V
		Buffers enabled	V_{SSA} + 0.1		V_{DDA} - 0.1	
		PGA gain = 1 to 16	V_{SSA} + 0.1 + (V_{IN})(gain)/2		V_{DDA} - 0.1 - (V_{IN})(gain)/2	
		PGA gain = 32 to 128	V_{SSA} + 0.2 + (V_{IN})(gain)/2		V_{DDA} - 0.2 - (V_{IN})(gain)/2	
Differential Input Current		Buffer disabled		±1		µA/V
		Buffer enabled		0 to 50		nA
		PGA enabled		±1		
Absolute Input Current		Buffer disabled		±1		µA/V
		Buffer enabled		20 to 80		nA
		PGA enabled, -40°C to +105°C		±2		
Input Capacitance		Bypass mode		10		pF
SYSTEM PERFORMANCE						
Resolution				24		bits

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate		50Hz/60Hz FIR filter, single-cycle conversions		1, 2, 4, 8, 16		sps
		50Hz FIR filter, single-cycle conversions		1.3, 2.5, 5, 10, 20, 35.6		
		60Hz FIR filter, single-cycle conversions		1.3, 2.5, 5, 10, 20, 36.5		
		SINC4 filter, single-cycle conversions		1, 2.5, 5, 10, 15, 30, 60, 120, 240, 480		
		SINC4 filter, continuous conversions		4, 10, 20, 40, 60, 120, 240, 480, 960, 1920		
		SINC4 filter, duty cycle conversions		0.25, 0.0625, 1.25, 2.5, 3.75, 7.7, 15, 30, 60, 120		
Data Rate Tolerance		Determined by internal clock accuracy	-6		6	%
Integral Nonlinearity (*Note 7*)	INL	Differential input, reference buffer enabled, PGA = 1, tested at 16sps, measured at +25°C, V_{DDA} = 3.0V	-12	+2	+12	ppmFS
		Differential input, PGA = 2 - 16		6		
		Differential input, PGA = 32 - 64		11		
		Differential input, PGA = 128		15		
Offset Error		Referred to modulator input. After self and system calibration; V_{REFP} - V_{REFN} = 2.5V, tested at 16sps, V_{DDA} = 3.0V	-25	±0.5	+25	µV
Offset Error Drift				50		nV/°C
PGA Gain Settings				1, 2, 4, 8, 16, 32, 64, 128		
Digital Gain Settings				2, 4		
PGA Gain Error (*Note 6*)		No calibration		±0.3		%
		Gain = 1, after calibration	-0.012		+0.012	

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGA Gain Drift				32		ppmFS/°C
Input Noise	V_n	FIR50Hz/60Hz, 16.8sps, PGA = 128		208		nV_{RMS}
Noise-Free Resolution	NFR	FIR50Hz/60Hz, 16.8sps, PGA = 1		17.3		bits
Normal-Mode Rejection (Internal Clock)	NMR	50Hz/60Hz FIR filter, 50Hz ±1%, 16sps conversion, GBD		88		dB
		50Hz/60Hz FIR filter, 60Hz ±1%, 16sps single-cycle conversion, GBD		88		
		50Hz FIR filter, 50Hz ±1%, 35.6sps single-cycle conversion, GBD		49		
		60Hz FIR filter, 60Hz ±1%, 35.6sps single-cycle conversion, GBD		55.6		
		SINC4 filter, 50Hz ±1%, 10sps single-cycle conversion, GBD		88		
		SINC4 filter 60Hz ±1%, 10sps single-cycle conversion, GBD		91		
Normal-Mode Rejection (External Clock)	NMR	50Hz/60Hz FIR filter, 50Hz or 60Hz ±1%, 16sps single-cycle conversion		91		dB
		50Hz FIR filter, 50Hz ±1%, 35.6sps single-cycle conversion		49.4		
		60Hz FIR filter, 60Hz ±1%, 35.6sps single-cycle conversion		55.6		
		SINC4 filter, 50Hz ±1%, 10sps single-cycle conversion		92.4		
		SINC4 filter, 60Hz ±1%, 10sps single-cycle conversion		92.6		
Common-Mode Rejection	CMR	DC rejection, any PGA gain		100		dB
	CMR60	50Hz/60Hz rejection, PGA enabled		104		
Power Supply Rejection	PSRRA			94		dB
REFERENCE INPUTS						
Reference Voltage Range		Reference buffer(s) disabled	V_{SSA} - 30m		V_{DDA} + 30m	V
		Reference buffer(s) enabled	V_{SSA} + 0.1		V_{DDA} - 0.1	
Reference Voltage Input		V_{REF} = V_{REFP} - V_{REFN}	0.75	2.5	V_{DDA}	V
Reference Input Current		Reference buffer disabled		2.1		µA/V
		Reference buffer enabled	-200	61	+200	nA
Reference Input Capacitance		Reference buffers disabled		15		pF

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MATCHED CURRENT SOURCES						
Matched Current Source Outputs				10, 50, 75, 100, 125, 150, 175, 200, 225, 250, 300, 400, 600, 800, 1200, 1600		µA
Current Source Output Voltage Compliance		IDAC ≤ 250µA	0		V_{DDA} - 0.7	V
		IDAC = 1.6mA	0		V_{DDA} - 1.2	
Tolerance		T_A = +25°C	-10	±1	+10	%
Current Matching		Between IDACs		±0.5		%
Temperature Drift Matching		Between IDACs		10		ppm/C
Current Source Output Noise	I_N	Output current = 250µA; SINC4 filter, 60sps continuous; noise is referred to input		0.47		pA rms
V_{BIAS} OUTPUTS						
V_{BIAS} Voltage				V_{DDA}/2		V
V_{BIAS} Voltage Output Impedance				125k (active), 20k (passive), 125k (passive)		Ω
SYSTEM TIMING						
Power-On Wake-Up Time		From V_{DDA} > V_{POR}		240		µs
PGA Power-Up Time		C_{FILTER} = 0		0.25		ms
		C_{FILTER} = 20nF		2		
		C_{FILTER} = 100nF		10		
PGA Settling Time		After changing gain settings to gain = 1, C_{FILTER} = 0		0.25		ms
		After changing gain settings to gain = 1, C_{FILTER} = 100nF		10		
		After changing gain settings to gain = 128, C_{FILTER} = 0		2		

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Multiplexer Power-up Time		Settled to 21 bits with 10pF load		2		µs
Input Multiplexer Channel-to-Channel Settling Time		Settled to 21 bits with 2kΩ external source resistor		2		µs
V_{BIAS} Power-Up Time		Active generator; settled within 1% of final value; C_{LOAD} = 1µF		10		ms
		125K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		575		
		20K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		90		
V_{BIAS} Settling Time		Active generator; settled within 1% of final value; C_{LOAD} = 1µF		10		ms
		125K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		605		
		20K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		100		
Matched Current Source Startup Time				110		µs
Matched Current Source Settling Time				12.5		µs

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SPECIFICATIONS							
V_{DDA} Current		ADC0 only	Standby mode, V_{DDA} = V_{REF} = V_{IN} = 3.0V		70		µA
			Bypass mode, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 60sps		160		
			Buffered mode, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 60sps		185		
			PGA enabled, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 60sps		275		
		ADC1. ADC0 must be in Standby mode	Bypass mode, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 60sps		160		
			Buffered mode, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 60sps		185		

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			PGA enabled, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 60sps		275		

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DDA} Duty Cycle Power Mode		ADC0 only	Bypass mode, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 15sps		75		µA
			Buffered mode, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 15sps		95		
			PGA enabled, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 15sps		190		
		ADC1. ADC0 must be enabled in Standby mode	Bypass mode, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 15sps		75		
			Buffered mode, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 15sps		95		
			PGA enabled, IDAC, V_{BIAS} sources off, V_{DDA} = V_{REF} = V_{IN} = 3.0V, SINC4 filter, continuous conversions at 15sps		190		
LDO							
V_{DD18} Output Capacitance					100		nF

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(V_{DDIO} = V_{DDA} = +3.0V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD18} Output Voltage		V_{DD18} configured as an output	1.71	1.8	1.98	V

Electrical Characteristics—HART Modem

(V_{DDIO} = V_{DDA} = 3.0V; T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE							
Internal Voltage Reference	HART_REF	HART modem enabled			1.23		V
FSK INPUT							
Input Voltage Range at FSK_IN				0		HART_REF	V
FSK OUTPUT							
Output Voltage Range at FSK_OUT		AC-coupled max 250Ω load		400	500	600	mV_{P-P}
Frequency of FSK_OUT		Accuracy is guaranteed based on the external crystal or clock provided.	For a mark	-1%	1200	+1%	Hz
			For a space	-1%	2200	+1%	

Electrical Characteristics—12-Bit DAC

(V_{DDIO} = V_{DDA} = 3.0V, R_L = 10kΩ and C_L = 100pF, V_{REF} = 1.5V, T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	DAC_R		12			bits
Differential Nonlinearity	DNL	Power mode = 2 or 3, noise filter enabled, GBD		±1		LSB
Integral Nonlinearity	INL	Power mode = 2 or 3, noise filter enabled, GBD		±1		LSB
Offset Error	E_O	Measure at V_{DDA} = 3.3V		4		mV
Output Voltage Range	V_O	DAC12_OUT device pin; min code to max code, GBD	V_{SSA} + E_O		V_{DDA} - 0.5	V
Output Impedance		Power mode = 3		6.1		kΩ
		Power mode = 2		8.9		
		Power mode = 1		16.3		
		Power mode = 0		97.7		
Voltage Output Settling Time	t_{SFS}	Noise filter enabled, code 400h to C00h, rising or falling, to ±0.5 LSB		4		ms
		Noise filter disabled, code 400h to C00h, rising or falling, to ±0.5 LSB		0.03		
Glitch Energy		Power mode = 0, 1, or 2		12		V x ns
		Power mode = 3, code 000h to A50h		12		

Electrical Characteristics—12-Bit DAC (continued)

(V_{DDIO} = V_{DDA} = 3.0V, R_L = 10kΩ and C_L = 100pF, V_{REF} = 1.5V, T_A = +25°C for typical specifications, unless otherwise noted. Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Current	I_{DAC12}	Static, V_{REF} = 2.5V	Power mode = 3		680		µA
			Power mode = 2		570		
			Power mode = 1		458		
			Power mode = 0		347		
		Static, V_{REF} = 2.0V	Power mode = 3		601		
			Power mode = 2		509		
			Power mode = 1		418		
			Power mode = 0		327		
		Static, V_{REF} = 1.5V	Power mode = 3		497		
			Power mode = 2		431		
			Power mode = 1		364		
			Power mode = 0		297		
		Static, V_{REF} = 1.0V	Power mode = 3		407		
			Power mode = 2		361		
			Power mode = 1		304		
			Power mode = 0		284		
Power-on Time		Excluding reference			10		µs

Electrical Characteristics—Internal Voltage Reference

(Internal reference mode, 4.7µF at INT_REF; V_{REF} = 1.5V. T_A = +25°C for typical specifications, unless otherwise noted. Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage at INT_REF	V_{INT_REF}	T_A = +25°C	INT_REF 1.024V		1.024		V
			INT_REF 1.50V		1.500		
			INT_REF 2.048V		2.048		
			INT_REF 2.50V		2.500		
Internal Reference Temperature Coefficient	T_{CREF}				±50		ppm/°C
Turn-On Time	t_{ON}				0.1 + (INT_VREF x 1.8)	10	ms
Leakage Current with INT_REF Output Disabled	I_{INT_REF}				15		nA
INT_REF Line Regulation					±50		µV/V
INT_REF Load Regulation	INT_Load	I_{SOURCE} = 0 to 500µA, T_A = +25°C			10		µV/µA
Reference Supply Current		Buffer enabled			270		µA

Electrical Characteristics—SPI

(V_{DDIO} = V_{DDA} = +3.0V, T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROLLER MODE						
SPI Controller Operating Frequency	f_{MCK}				$f_{SYS\_CLK}/4$	MHz
SPI Controller SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
TARGET MODE						
SPI Target Operating Frequency	f_{SCK}				$f_{SYS\_CLK}/4$	MHz
SPI Target SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I²C

(V_{DDIO} = V_{DDA} = +3.0V, T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD-MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST-MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns

Electrical Characteristics—I²C (continued)

(V_{DDIO} = V_{DDA} = +3.0V, T_A = +25°C for typical specifications, unless otherwise noted. *Note 5*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST-MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Note 3: Tested and guaranteed at T_A = +85°C.

Note 4: OVR[00] sets the internal regulator output voltage (V_{CORE}) to 0.85V. *Do not modify this field from the default value.*

Note 5: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 6: Gain error does not include zero-scale errors. It is calculated as (full-scale error – offset error).

Note 7: ppmFS is parts per million of full scale.

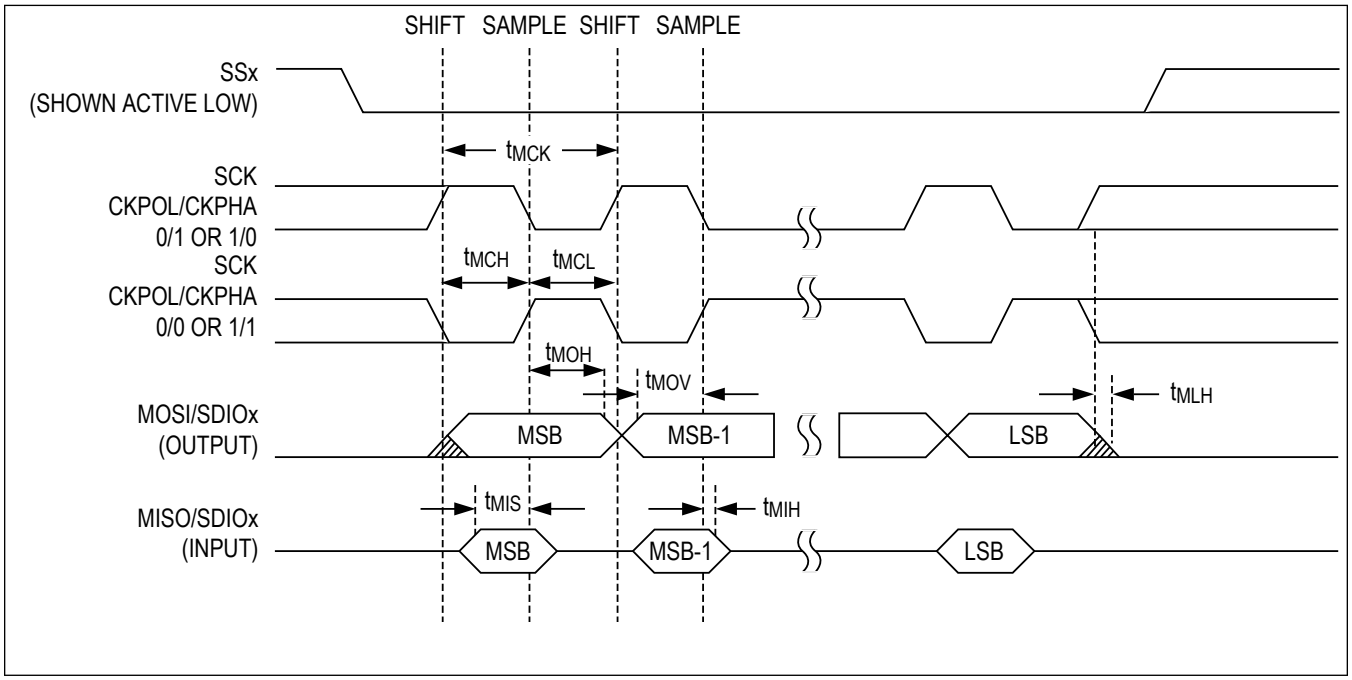


Figure 2. SPI Controller Mode Timing Diagram

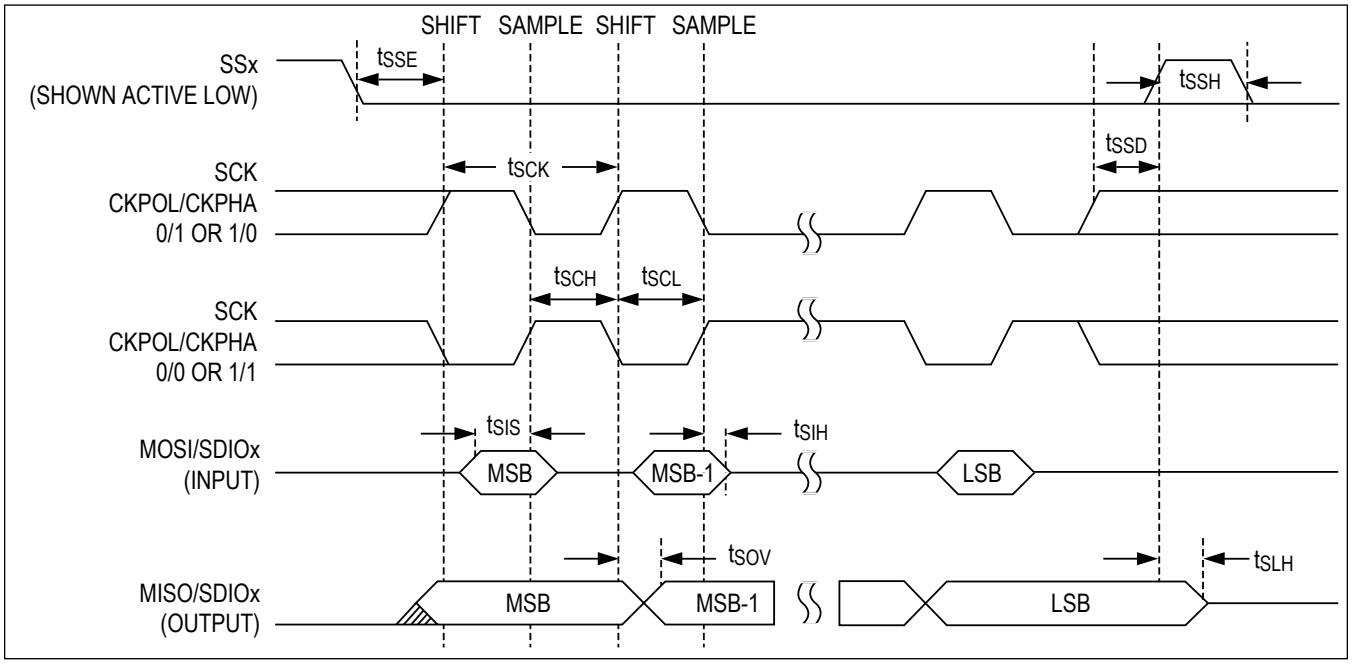


Figure 3. SPI Target Mode Timing Diagram

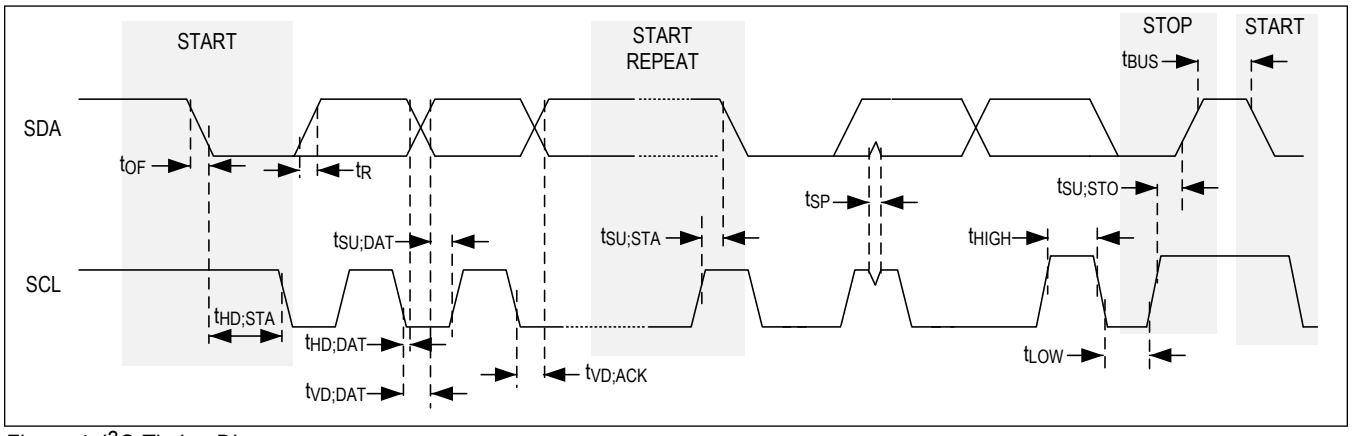
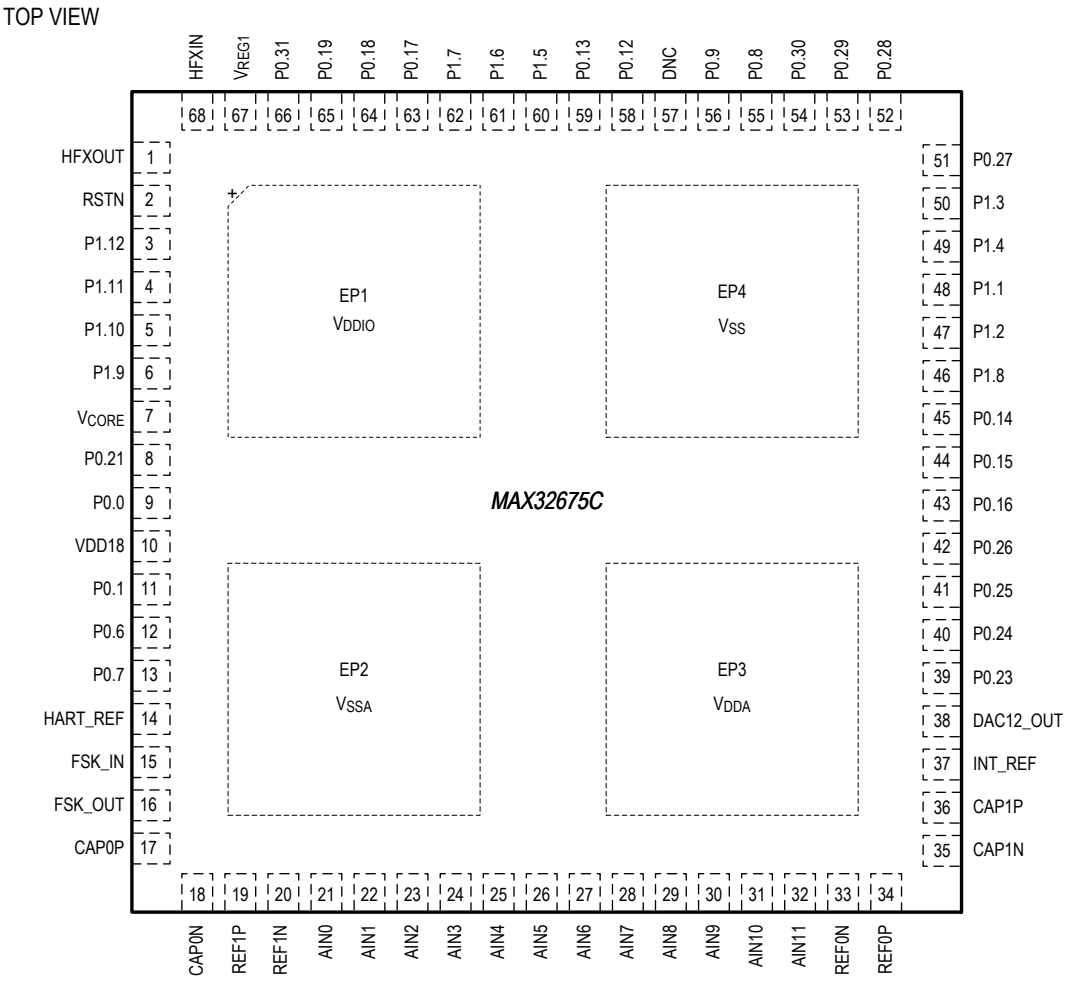


Figure 4. I²C Timing Diagram

Pin Configuration

72L LGA



72L LGA
8mm x 8mm x 0.91mm

Pin Description

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
POWER (See *Bypass Capacitor Recommendations*)							
7	V_{CORE}	—	—	—	—	—	Bypass with 100nF and 1µF (≥0.95V 10mΩ to 150mΩ ESR) to V_{SS}.
10	V_{DD18}	—	—	—	—	—	Bypass with 100nF to V_{SS}. Do not connect this device pin to any other external circuitry.

72L LGA

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
EP1	V_{DDIO}	—	—	—	—	—	Power Supply Input. Exposed Pad. Connect this pad to the V_{DDA} exposed pad at the PCB level. Bypass this exposed pad with 100nF to V_{SSA} and 1µF (10mΩ to 150mΩ ESR) to V_{SS}. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.
EP3	V_{DDA}	—	—	—	—	—	Analog Supply Voltage Input. Exposed Pad. This pad must always be connected to the V_{DDIO} exposed pad. Bypass this exposed pad to V_{SSA} with 1.0µF and 0.01µF capacitors to V_{SSA}. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.
67	V_{REG1}	—	—	—	—	—	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
EP4	V_{SS}	—	—	—	—	—	Digital Ground. Exposed Pad. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.
EP2	V_{SSA}	—	—	—	—	—	Analog Ground. Exposed Pad. This pad must be connected to V_{SS}. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.
RESET AND CONTROL							
2	RSTN	—	—	—	—	—	External System Reset Input (Active-Low). The device remains in reset while this pin is low. When the pin transitions high, the device performs a system reset and begins execution. This pin has an internal pull-up to the V_{DDIO} supply.

72L LGA

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
CLOCK							
68	HFXIN	—	—	—	—	—	16MHz Crystal Oscillator Input. Connect a crystal between HFXIN and HFXOUT. See f_{ERFO} in the *Electrical Characteristics* table for the crystal requirements. Refer to the device user guide for calculating the load capacitors. Optionally, this pin can be configured as the input for an external CMOS-level clock source. Alternately, if this pin is unused, connect it to V_{SS} through a 10kΩ resistor.
1	HFXOUT	—	—	—	—	—	16MHz Crystal Oscillator Output. Connect the crystal between HFXIN and HFXOUT. If a crystal is not used or if HFXIN is unused, do not connect.
HART MODEM							
15	FSK_IN	—	—	—	—	—	FSK In, Analog Input. Input for the FSK-modulated HART receive signal from the 4–20mA current loop interface circuit.
16	FSK_OUT	—	—	—	—	—	FSK Out, Analog Output. Output of the modulator. Provides a phase-continuous, FSK-modulated output signal (1200Hz and 2200Hz output frequencies) to the 4–20mA current loop interface circuit.
14	HART_REF	—	—	—	—	—	HART Reference, Analog Output. The internal voltage reference is provided as an output when the HART modem is biased. Bypass with a 0.1µF capacitor to V_{SS}. External filter and biasing required.
24-16 BIT DELTA SIGMA ADC WITH PGA							
34	REF0P	—	—	—	—	—	Positive Differential Reference 0 Input. REF0P must be more positive than REF0N.
33	REF0N	—	—	—	—	—	Negative Differential Reference 0 Input. REF0P must be more positive than REF0N.
19	REF1P	—	—	—	—	—	Positive Differential Reference 1 Input. REF1P must be more positive than REF1N.
20	REF1N	—	—	—	—	—	Negative Differential Reference 1 Input. REF1P must be more positive than REF1N.

72L LGA

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
17	CAP0P	—	—	—	—	—	ADC0 PGA Positive Output. Connect a 1nF capacitor between CAP0P and CAP0N.
18	CAP0N	—	—	—	—	—	ADC0 PGA Negative Output. Connect a 1nF capacitor between CAP0P and CAP0N.
36	CAP1P	—	—	—	—	—	ADC1 PGA Positive Output. Connect a 1nF capacitor between CAP1P and CAP1N.
35	CAP1N	—	—	—	—	—	ADC1 PGA Negative Output. Connect a 1nF capacitor between CAP1P and CAP1N.
21	AIN0	—	—	—	—	—	Channel 0 Analog Input/Positive Differential Reference Input. When used as an analog input, may serve as either the positive or negative differential input. May also serve as a current source output. When used as a reference input paired with AIN1, AIN0 must be more positive than AIN1.
22	AIN1	—	—	—	—	—	Channel 1 Analog Input/Negative Differential Reference Input. When used as an analog input, may serve as either the positive or negative differential input. May also serve as a current source output. When used as a reference input paired with AIN0, AIN0 must be more positive than AIN1.
23	AIN2	—	—	—	—	—	Channel 2 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
24	AIN3	—	—	—	—	—	Channel 3 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
25	AIN4	—	—	—	—	—	Channel 4 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.

72L LGA

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
26	AIN5	—	—	—	—	—	Channel 5 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
27	AIN6	—	—	—	—	—	Channel 6 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
28	AIN7	—	—	—	—	—	Channel 7 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
29	AIN8	—	—	—	—	—	Channel 8 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
30	AIN9	—	—	—	—	—	Channel 9 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
31	AIN10	—	—	—	—	—	Channel 10 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
32	AIN11	—	—	—	—	—	Channel 11 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as a current source output.
12-BIT DAC							
38	DAC12_ OUT	—	—	—	—	—	12-Bit DAC Analog Voltage Output
INTERNAL REFERENCE							
37	INT_REF	—	—	—	—	—	Internal Reference Output. Bypass with a 4.7µF capacitor to V_{SSA}.

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
GPIO AND ALTERNATE FUNCTION							
9	P0.0	SWDIO	—	—	TMR0C_IA	—	Single-Wire Debug I/0; TMR0 Port Map C Input 32 Bits or Lower 16 Bits
11	P0.1	SWDCLK	—	—	TMR0C_OA	—	Single-Wire Debug Clock; TMR0 Port Map C Output 32 Bits or Lower 16 Bits
12	P0.6	P0.6	I2C0A_SCL	LPTMR0B_IA	TMR3C_IA	—	I2C0 Port Map A Serial Clock; LPTMR0 Port Map B Input 32 Bits or Lower 16 Bits; TMR3 Port Map C Input 32 Bits or Lower 16 Bits
13	P0.7	P0.7	I2C0A_SDA	LPTMR0B_OA	TMR3C_OA	—	I2C0 Port Map A Serial Data; LPTMR0 Port Map B Output 32 Bits or Lower 16 Bits; TMR3 Port Map C Output 32 Bits or Lower 16 Bits
55	P0.8	P0.8	UART0A_RX	—	TMR0C_IA	—	UART0 Port Map A Receive; TMR00 Port Map C Input 32 Bits or Lower 16 Bits
56	P0.9	P0.9	UART0A_TX	—	TMR0C_OA	—	UART0 Port Map A Receive; TMR0 Port Map C Output 32 Bits or Lower 16 Bits
58	P0.12	P0.12	I2C1A_SCL	EXT_CLK2	TMR2C_IA	EXT_CLK1	I2C1 Port Map A Serial Clock; Low-Power External Clock Input; TMR2 Port Map C Input 32 Bits or Lower 16 Bits; External Clock Input
59	P0.13	P0.13	I2C1A_SDA	—	TMR2C_OA	SPI1D_SS0	I2C1 Port Map A Serial Data; TMR2 Port Map C Output 32 Bits or Lower 16 Bits; SPI1 Port Map D Target Select 0
45	P0.14	P0.14	SPI1A_MISO	UART2B_RX	TMR3C_IA	HART_OUT	SPI1 Port Map A Controller In Target Out; UART2 Port Map B Receive; Timer 3 Port Map C Input 32 Bits or Lower 16 Bits; HART Digital Data Out. ***Note:*** *HART_OUT is not an alternate function, refer to the device user guide for configuration details.* ***Note****: This pin is internally connected between P0.14 and HART_OUT.*
44	P0.15	P0.15	SPI1A_MOSI	UART2B_TX	TMR3C_OA	HART_IN	SPI1 Port Map A Controller Out Target In; UART2 Port Map B Transmit; TMR3 Port Map B Output 32 Bits or Lower 16 Bits; HART Digital Data In; ***Note:*** *HART_IN is not an alternate function, refer to the device user guide for configuration details.* ***Note:*** *This pin is internally connected between P0.15 and HART_IN.*

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
43	P0.16	P0.16	SPI1A_SCK	UART2B_CTS	TMR0C_IA	HART_OCD	SPI1 Port Map A Serial Clock; UART2 Port Map B Clear to Send; TMR0 Port Map C Input 32 Bits or Lower 16 Bits; HART Carrier Detect Output; ***Note:*** *HART_OCD is not an alternate function, refer to the device user guide for configuration details.* ***Note:*** *This pin is internally connected between P0.16 and HART_OCD.*
63	P0.17	P0.17	SPI1A_SS0	UART2B_RTS	TMR0C_OA	—	SPI1 Port Map A Target Select 0; UART2 Port Map B Request to Send; TMR0 Port Map C Output 32 Bits or Lower 16 Bits
64	P0.18	P0.18	I2C2A_SCL	—	TMR1C_IA	—	I2C2 Port Map A Serial Clock; TMR1 Port Map C Input 32 Bits or Lower 16 Bits
65	P0.19	P0.19	I2C2A_SDA	—	TMR1C_OA	—	I2C2 Port Map A Serial Data; TMR1 Port Map C Output 32 Bits or Lower 16 Bits
8	P0.21	P0.21 (Bootloader Activation Pin)	CM4_TX	—	TMR2C_OA	ADC1_RDY	CM4 Transmit Event Output; TMR2 Port Map C Output 32 Bits or Lower 16 Bits; ADC Ready 1 ***Note:*** *ADC1_RDY is not an alternate function, refer to the device user guide for configuration details.* ***Note:*** *This pin is internally connected between P0.21 and ADC1_RDY.*
39	P0.23	P0.23	LPTMR1A_OA	—	TMR3C_OA	—	LPTMR1 Port Map A Output 32 Bits or Lower 16 Bits; TMR3 Port Map C Output 32 Bits or Lower 16 Bits
40	P0.24	P0.24	LPUART0A_CTS	UART0B_RX	TMR0C_IA	—	LPUART0 Port Map A Clear to Send; UART0 Port Map B Receive; TMR0 Port Map C Input 32 Bits or Lower 16 Bits
41	P0.25	P0.25	LPUART0A_RTS	UART0B_TX	TMR0C_OA	—	LPUART0 Port Map A Request to Send; UART0 Port Map B Transmit; TMR0 Port Map B Output 32 Bits or Lower 16 Bits
42	P0.26	P0.26	LPUART0A_RX	UART0B_CTS	TMR1C_IA	ADC0_RDY	LPUART0 Port Map A Receive; UART0 Port Map B Clear to Send; TMR1 Port Map C Input 32 Bits or Lower 16 Bits; ADC 0 Ready ***Note:*** *ADC0_RDY is not an alternate function, refer to the device user guide for configuration details.* ***Note:*** *This pin is internally connected between P0.26 and ADC0_RDY.*

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
51	P0.27	P0.27	LPUART0A_TX	UART0B_RTS	TMR1C_OA	—	LPUART0 Port Map A Transmit; UART0 Port Map B Request to Send; TMR1 Port Map C Output 32 Bits or Lower 16 Bits
52	P0.28	P0.28	UART1A_RX	—	TMR2C_IA	—	UART1 Port Map A Receive; TMR2 Port Map C Input 32 Bits or Lower 16 Bits
53	P0.29	P0.29	UART1A_TX	—	TMR2C_OA	—	UART1 Port Map A Transmit; TMR2 Port Map C Output 32 Bits or Lower 16 Bits
54	P0.30	P0.30	UART1A_CTS	—	TMR3C_IA	—	UART1 Port Map A Clear to Send; TMR3 Port Map C Input 32 Bits or Lower 16 Bits
66	P0.31	P0.31	UART1A_RTS	—	TMR3C_OA	—	UART1 Port Map A Request to Send; TMR3 Port Map C Output 32 Bits or Lower 16 Bits
48	P1.1	P1.1	SPI2A_MISO	UART1B_RX	—	—	SPI2 Port Map A Controller In Target Out; UART1 Port Map B Receive
47	P1.2	P1.2	SPI2A_MOSI	UART1B_TX	—	HART_CLK_OUT	SPI2 Port Map A Controller Out Target In; UART1 Port Map A Transmit; HART Clock Output
50	P1.3	P1.3	SPI2A_SCK	UART1B_CTS	—	—	SPI2 Port Map A Serial Clock; UART1 Port Map B Clear to Send
49	P1.4	P1.4	SPI2A_SS0	UART1B_RTS	—	—	SPI2 Port Map A Target Select 0. UART1 Port Map B Request to Send
60	P1.5	P1.5	—	—	—	—	
61	P1.6	P1.6	—	—	—	—	
62	P1.7	P1.7	—	—	—	—	
46	P1.8	P1.8	UART2A_RX	UART2B_RTS	—	HART_RTS	UART2 Port Map A Receive; UART2 Port Map B Request to Send; HART Request to Send; ***Note:*** *HART_RTS is not an alternate function, refer to the device user guide for configuration details.* ***Note:*** *UART2 Port Map A cannot be used if the HART modem is in use. HART is internally connected to UART2 Port Map B,* ***Note:*** *Internally connected between P1.8 and HART_RTS.*
6	P1.9	P1.9	UART2A_TX	—	—	—	UART2 Port Map A Transmit ***Note:*** *UART2 Port Map A cannot be used if the HART modem is in use. HART is internally connected to UART2 Port Map B.*

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
5	P1.10	P1.10	UART2A_CTS	—	—	—	UART 2 Port Map A Clear to Send ***Note:*** *UART2 Port Map A cannot be used if the HART modem is in use. HART is internally connected to UART2 Port Map B.*
4	P1.11	P1.11	UART2A_RTS	—	—	—	UART2 Port Map A Request to Send ***Note:*** *UART2 Port Map A cannot be used if the HART modem is in use. HART is internally connected to UART2 Port Map B.*
3	P1.12	P1.12	—	—	—	—	
NO CONNECT							
57	DNC	DNC	—	—	—	—	Do Not Connect. Internally connected. Do not make any electrical connection to this pin, including power supply grounds.

Detailed Description

The MAX32675C is a highly integrated, mixed-signal, ultra-low-power microcontroller for industrial applications and is especially suitable for 4-20mA loop-powered sensors and transmitters. It is based on an ultra-low-power Arm Cortex-M4 with FPU and includes 376KB of user flash and 160KB of SRAM. ECC, capable of SEC-DED, is implemented over the entire flash, SRAM, and cache to ensure ultra-reliable code execution for demanding applications.

An AFE with an integrated, low-power HART modem enables the bidirectional transfer of digital data over a current loop to/from industrial sensors for configuration and diagnostics. The AFE also provides two 12-channel Δ-Σ ADCs with features and specifications that are optimized for precision sensor measurement. Each Δ-Σ ADC can digitize external analog signals as well as system temperature and supplies. A PGA with gains of 1x to 128x precedes each ADC. ADC outputs can be optionally converted on the fly from integer to single-precision floating-point format. A 12-bit DAC is also included.

The device also provides robust security features including an AES engine and persistent key storage.

Arm Cortex-M4 Processor with FPU Engine

The Arm Cortex-M4 processor with FPU combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 processor with FPU supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed or unsigned data with or without saturation

Memory

Internal Flash Memory

The device provides 384KB of flash memory for nonvolatile program and data storage. 376KB is available for application usage; the last page (8KB) is reserved for system use and must not be modified.

Internal SRAM

The internal 160KB SRAM provides low-power retention of application information in all power modes except STORAGE. For enhanced system reliability, the SRAM can be configured as 128KB with ECC single error correction, double error detection (SEC-DED). The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

Clocking Scheme

Multiple system clock sources are available to maximize performance and minimize power consumption.

- 7.3728MHz internal baud-rate oscillator (IBRO)
- 12MHz internal primary oscillator (IPO)
- 115kHz internal nanoring oscillator (INRO)
- 16MHz external oscillator (ERFO) (external crystal required)*
- External square-wave clock (EXT_CLK1) up to 8MHz

The AFE is configured by the internal SPI0. The ADCs can be clocked by the ERFO divided by 4 or by 8 or by the Δ-Σ clock generation. For HART operation, the AFE must be clocked at 4MHz (ERFO divided by 4). The AOD_CLK or the INRO can clock the LPUART0 and LPTMR0/LPTMR1 in the AOD. Addtionally, EXT_CLK2 can clock the LPUART0 and LPTMR0/LPTMR1. The default oscillator selected after POR is the IBRO, enabling lower power start-up current.

**Note: If the ERFO is selected as the system oscillator (SYS_OSC), it must be divided by 2 or greater to use as the*

system clock (SYS_CLK).

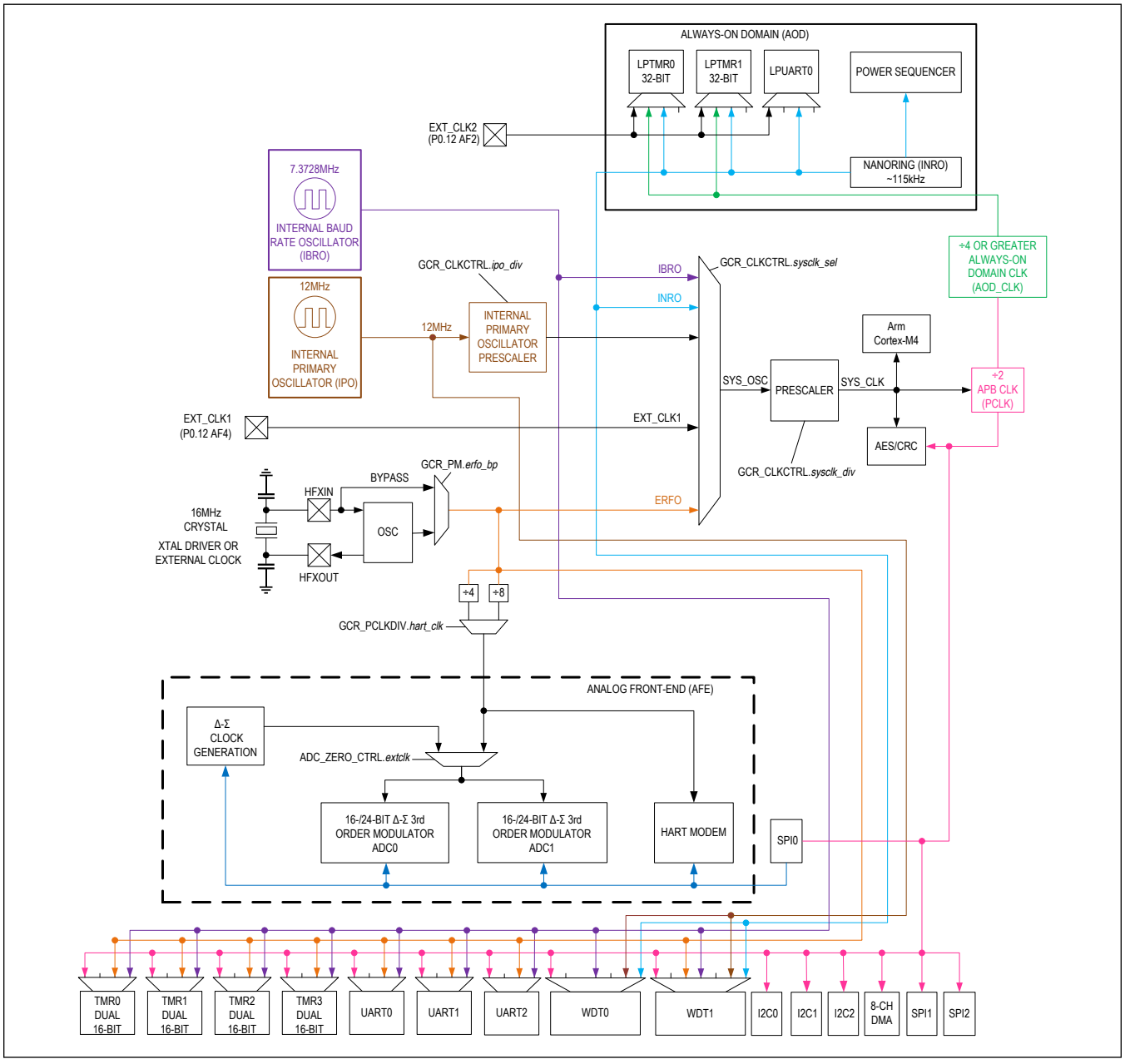

Figure 5. Clocking Scheme Diagram

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a software-controlled I/O function and one or more special function signals associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a software-controlled I/O. Though this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, each pin of a port has an interrupt function that can be independently enabled and configured as a level- or edge-sensitive interrupt. All GPIOs share the same interrupt vector.

When configured as GPIOs, the following features are provided. These features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high-impedance
- Optional internal pull-up resistor or internal pull-down resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable drive-strength modes

The MAX32675C provides up to 36 GPIOs.

Standard DMA Controller

The standard direct memory access (DMA) controller provides a means to offload the CPU for memory/peripheral data transfer, leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following features are supported:

- 8-channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Power Management

Power Management Unit (PMU)

The PMU provides the optimal mix of high-performance and low-power consumption. It exercises intelligent, precise control of power distribution to the CPU and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of the oscillator based on power mode
- Multiple clock domains
- Fast wakeup of powered-down peripherals when activity detected

ACTIVE

In this mode, the CPU is executing application code and all digital and analog peripherals are available on demand. Dynamic clocking disables local clocks in peripherals not in use. This mode corresponds to the Arm Cortex-M4 processor with FPU Active mode. The power mode of the AFE is software-controlled.

SLEEP

This mode allows for lower power consumption operation than ACTIVE. The CPU is asleep, peripherals are on, and the standard DMA block is available. The GPIO or any active peripheral can be configured to interrupt and cause transition to ACTIVE. This mode corresponds to the Arm Cortex-M4 processor with FPU sleep mode. The power mode of the AFE is software-controlled.

DEEPSLEEP

In this mode, the CPU and critical peripheral configuration settings and all volatile memory are preserved.

The device status is a follows:

- CPU is powered down. The system state and all SRAM is retained.
- The GPIO pins retain their state.

- The transition from DEEPSLEEP to ACTIVE is faster than the transition from BACKUP because system initialization is not required.
- All oscillators except INRO are all disabled to provide additional power savings over SLEEP.
- LPUART0 and LPTMR0/LPTMR1 can be active and are optional wake-up sources

This mode corresponds to the Arm Cortex-M4 with FPU DeepSleep mode. The power mode of the AFE is software-controlled.

BACKUP

This mode places the CPU in a static, low-power state. BACKUP supports the same wake-up sources as the DEEPSLEEP.

The device status is as follows:

- CPU is powered down
- SRAM retention as per Table 1. Each of the RAM blocks can be retained
- LPUART0 and LPTMR0/LPTMR1 can be active and are optional wake-up sources

The AFE should be held in reset (GCR_RST1.*afe* = 1).

Table 1. BACKUP RAM Retention

RAM BLOCK	RAM SIZE WITHOUT ECC (KB)	RAM SIZE WITH ECC (KB)	RETAINED RAM (KB)
sysram0	20	16	0
sysram1	20	16	20
sysram2	40	32	40
sysram3	80	64	80

Note: The ROM bootloader erases *sysram0* during a system reset, watchdog timer reset, an external reset, and an exit from BACKUP. The ROM bootloader uses this RAM to perform system checks.

STORAGE

The device status is as follows:

- The CPU is powered off.
- All peripherals are powered off.
- Wake-up from GPIO interrupt.
- No SRAM retention.

The AFE should be held in reset (GCR_RST1.*afe* = 1).

Windowed Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the watchdog timer, which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software using a special timed sequence. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution.

The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific window of time.

The instances of the peripheral and the clock source options are shown in Table 2. The MAX32675C provides two instances of the watchdog timer.

Table 2. Watchdog Timer Instances

INSTANCE	WINDOW SUPPORT	OPERATING MODES	CLK0	CLK1	CLK2	CLK3	CLK4	CLK5	CLK6	CLK7
WDT0	YES	ACTIVE SLEEP	PCLK	IPO	IBRO	INRO	—	EXT_CLK1	ERFO	—
WDT1	YES	ACTIVE SLEEP	PCLK	IPO	IBRO	INRO	—	EXT_CLK1	ERFO	—

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generate pulse-width modulated (PWM) signals with minimal software interaction. The timers provide the following features:

- 32-bit up/down auto-reload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, output, clock gating, or capture
- TMR0–TMR3 can be configured as 2 × 16-bit general-purpose timers
- Timer interrupt

The MAX32675C provides timer instances as shown in Table 3. I/O functionality is supported for all of the timers.

Table 3. Timer Configuration Options

INSTANCE	SINGLE 32-BIT	DUAL 16-BIT	OPERATING MODES	CLOCK OPTIONS			
				CLK0	CLK1	CLK2	CLK3
TMR0	Yes	Yes	ACTIVE SLEEP	PCLK	EXT_CLK1	IBRO	ERFO
TMR1							
TMR2							
TMR3							
LPTMR0	Yes	No	ACTIVE SLEEP	AOD_CLK	EXT_CLK2	N/A	INRO
			DEEPSLEEP BACKUP	N/A			
LPTMR1	Yes	No	ACTIVE SLEEP	AOD_CLK	EXT_CLK2	N/A	INRO
			DEEPSLEEP BACKUP	N/A			

Serial Peripherals

I^2C Interface (I2C)

The I^2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. These engines support Standard-mode, Fast-mode, and Fast-mode Plus I^2C speeds. It provides the following features:

- Controller or target mode operation
  - Supports up to four different target addresses in target mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Transmit FIFO preloading

- Support for clock stretching to allow slower target devices to operate on higher speed busses
- Multiple transfer rates
  - Standard-mode: 100kbps
  - Fast-mode: 400kbps
  - Fast-mode Plus: 1000kbps
- Internal filter to reject noise spikes
- Receive FIFO depth of 8 bytes
- Transmit FIFO depth of 8 bytes

The MAX32675C provides three instances of the I^2C peripheral (I2C0, I2C1, and I2C2).

Serial Peripheral Interface (SPI)

The SPI is a highly configurable, flexible, and efficient synchronous interface among multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals and one or more target select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either target or controller mode and provide the following features:

- SPI modes 0, 1, 2, 3 for single-bit communication
- 3- or 4-wire mode for single-bit target device communication
- Full-duplex operation in single-bit, 4-wire mode
- Multicontroller mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Target select assertion and deassertion timing with respect to leading/trailing SCK edge

The MAX32675C provides two instances of the SPI peripheral (SPI1 and SPI2). See Table 4 for configuration options.

Table 4. SPI Configuration Options

INSTANCE	DATA	TARGET SELECT LINES	MAXIMUM FREQUENCY CONTROLLER MODE (MHz)	MAXIMUM FREQUENCY TARGET MODE (MHz)
SPI1*	3 wire, 4 wire	1	3	3
SPI2	3 wire, 4 wire	1	3	3

*SPI1 cannot be used if HART is in use.

UART (UART, LPUART)

The universal asynchronous receiver-transmitter (UART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) flow control signaling. Each instance is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for multiple events reduce overhead:
  - Frame error
  - Parity error
  - CTS
  - Receive FIFO overrun
  - FIFO full
  - FIFO partially full
  - FIFO half-empty
  - FIFO one byte remaining

- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The instances of the peripheral, operating modes, and clock source options are shown in Table 5.

Table 5. UART Clock Options

INSTANCE	POWER MODE	CLOCK OPTIONS			
		CLK0	CLK1	CLK2	CLK3
UART0	ACTIVE SLEEP	PCLK	EXT_CLK1	IBRO	ERFO
UART1					
UART2*					
LPUART0	ACTIVE SLEEP	AOD_CLK	EXT_CLK2	N/A	INRO**
	DEEPSLEEP BACKUP	N/A			

*UART2 cannot be used if HART is in use.

**INRO accuracy varies up to ±50% across temperature and voltage. Baud rate accuracy must be taken into account when using INRO as the clock source.

16-/24-Bit Δ-Σ Analog-to-Digital Converter with Programmable Gain Amplifier

A low-power, multichannel, 24-bit Δ-Σ ADC has features and specifications optimized for the precision measurement of sensors and other analog signal sources. The architecture includes a low-noise programmable gain amplifier (PGA), low-power input buffers, programmable matched current sources, differential/single-ended input multiplexer, and integrated on-chip oscillator.

- PGA with available gains 1x to 128x
  - Very high input impedance
  - Optimizes overall dynamic range
- Low-power input buffers
  - Provide input isolation
- Selectable reference
  - Internal differential (V_{REF})
  - External differential
- Programmable current sources
  - Bias for resistive sensors
  - 16 current levels available
  - Detection of broken sensor wires
- 12 analog inputs
  - 6 differential or 12 single ended
- FIR digital filters
  - Provides single-cycle settling in 16ms
  - 90dB of noise rejection at 50Hz and 60Hz
- On-chip clock source
  - No external components required
- External clock capable

- Sample ready interrupts
  - ADC0_RDY and ADC1_RDY

The MAX32675C provides two instances of this ADC (ADC_ZERO, ADC_ONE) that share the 12 multiplexed analog inputs (AIN0–AIN11).

12-Bit Digital-to-Analog Converter (DAC)

The 12-bit DAC outputs a single-ended voltage. It can be set independently to generate either a static output voltage or to generate a series of preloaded sample outputs at a specified sample rate.

The 12-bit DAC peripheral supports the following features:

- Configurable clock rate and output sample rate.
- Selectable output voltage reference.
- Can be set to output a static voltage level, a preset number of samples at a configurable sample rate, or samples continuously at a configurable sample rate.
- Interpolation filter allows for linearly interpolated output samples to be generated between each pair of output samples (2 to 1, 4 to 1, or 8 to 1).
- DAC output samples are pulled from a FIFO allow continuous sample output generation.

HART Modem

The Highway Addressable Remote Transducer (HART) modem is ideal for low-power process control transmitters. The device integrates the HART FSK Physical Layer, integrating modulation and demodulation of the 1200Hz/2200Hz FSK signal, has very low power consumption, and needs only a few external components due to the integrated digital signal processing. The input signal is sampled by an ADC, followed by a digital filter/demodulator. This architecture ensures reliable signal detection in noisy environments. The device is ideal for low-power process control transmitters.

Security

ROM Bootloader

The bootloader allows the loading and verification of program memory through a serial interface. Features include:

- ROM-based
- Bootloader interface through UART
- Program loading of Motorola® SREC format files
- Permanent lock state prevents altering or erasing program memory through the ROM bootloader
- Access to the USN for device or customer application identification
- Disable SWD interface to block debug access port functionality

The contents of SRAM are not guaranteed following the activation of the bootloader. See *ROM Bootloader Activation* for additional details.

Secure Boot

On devices that support the secure boot feature, the device ensures software integrity by automatically comparing program memory against a stored HMAC SHA-256 hash value after every reset. A program that fails the integrity check indicates corrupted or modified program memory and is prevented from executing any instructions.

Devices with the secure boot feature also provide an optional challenge/response that authenticates before executing bootloader commands. Not all devices provide the secure boot feature; see the *Ordering Information* table for availability.

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

AES keys can be stored in a dedicated persistent memory.

Cyclic Redundancy Check (CRC) Module

A CRC hardware module provides fast calculations and data integrity checks by application software. The CRC polynomial is programmable to support custom CRC algorithms as well as the common algorithms shown in Table 6.

Table 6. Common CRC Polynomials

ALGORITHM	POLYNOMIAL EXPRESSION
CRC-32-ETHERNET	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + x^0$
CRC-CCITT	$x^{16} + x^{12} + x^5 + x^0$
CRC-16	$x^{16} + x^{12} + x^2 + x^0$
USB DATA	$x^{16} + x^{12} + x^2 + x^0$
PARITY	$x^1 + x^0$

Serial Wire Debug (SWD) and Development Interface

The device provides an Arm Debug Access Port (DAP) that supports debugging during application development. The DAP enables an external debugger to access the device. The DAP is a standard Arm CoreSight™ SWD port and uses a two-pin serial interface (SWDCLK and SWDIO) to communicate.

Applications Information

Bypass Capacitor Recommendations

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The *Pin Descriptions* table indicates which pins should be connected to bypass capacitors, and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the *Pin Descriptions* table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Place capacitors as close as possible to their corresponding device pins. Pins that recommend more than one value of capacitor per pin should place them in parallel with the lowest value capacitor first, closest to the pin.

ROM Bootloader Activation

The bootloader samples the bootloader stimulus pins during any of the bootloader events shown in Table 7. If any of the stimulus pin is not in its active state during a bootloader activation event, the bootloader is bypassed and the device begins executing the application code.

If all stimulus pins are in their active state during a bootloader activation event, the application software does not execute and instead the ROM bootloader assumes control of the device. The device outputs a status prompt and begins a bootloader session with the host system controlling the programming. While the ROM bootloader is in control, the state of the stimulus pins are ignored and can be driven to any value or used for communication if applicable.

The bootloader session is terminated at any time by performing a POR or asserting RSTN while the stimulus pin is in its inactive state.

Table 7. ROM Bootloader Interface

PART NUMBER	INTERFACE PINS	STIMULUS PINS	BOOTLOADER ACTIVATION EVENTS
All part numbers	UART0A_RX (P0.8) UART0A_TX (P0.9) P0.21 RSTN	P0.21 (active high)	POR System reset (including RSTN and WDT resets) Exit from BACKUP Exit from STORAGE

Ordering Information

PART	BOOTLOADER	SECURE BOOT	TMR	LPTMR	WDT	UART	LPUART	AES/ CRC	HART MODEM	24-/16-BIT Δ-Σ ADC	PIN-PACKAGE
MAX32675CALZ+	Y	N	4	2	2	2	1	1	Y	2	72L LGA 8mm x 8mm x 0.91mm, 0.4mm pitch
MAX32675CALZ+T	Y	N	4	2	2	2	1	1	Y	2	72L LGA 8mm x 8mm x 0.91mm, 0.4mm pitch

All devices have 376KB user flash, 160KB SRAM, 36 GPIO, SWD, two SPI, and three I²C.

UART = Universal Asynchronous Receiver-Transmitter; SPI = Serial peripheral interface;

TMR = Timer; I²C = Inter-IC; ADC = Analog-to-digital converter; LPUART = Low-power UART;

GPIO = General-purpose input/output; CRC = Cyclic redundancy check;

HART = Highway Addressable Remote Transducer;

+ Denotes a lead(Pb)-free /RoHS-compliant package.

T = Tape and reel. Full reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/24	Initial release	—