High Power, 100 W Peak, Silicon SPDT, Reflective Switch, 0.4 GHz to 8 GHz

FEATURES

- Frequency range: 0.4 GHz to 8 GHz
- Low insertion loss: 0.6 dB typical to 4 GHz
- High Isolation: 45 dB typical to 4 GHz
- High input linearity
  - 0.1 dB power compression (P0.1dB): 50 dBm
  - Third order intercept (IP3): >76 dBm
- High power handling at T_{CASE} = 85°C:
  - Insertion loss path
    - Average: 45.5 dBm
    - Pulsed (>100 ns pulse width, 15% duty cycle): 48.5 dBm
    - Peak (≤100 ns peak duration, 5% duty cycle): 50 dBm
  - Hot-switching at RFC: 43 dBm
- 0.1 dB RF settling time with P_{IN} ≤ 43 dBm: 1.2 µs
- No low frequency spurious
- Positive control interface: CMOS/LVTTL-compatible
- 24-lead, 4.0 mm × 4.0 mm LFCSP package

APPLICATIONS

- Military radios, radars, and electronic counter measures
- Cellular infrastructure
- Test and instrumentation
- GaN and PIN diode replacement

FUNCTIONAL BLOCK DIAGRAM

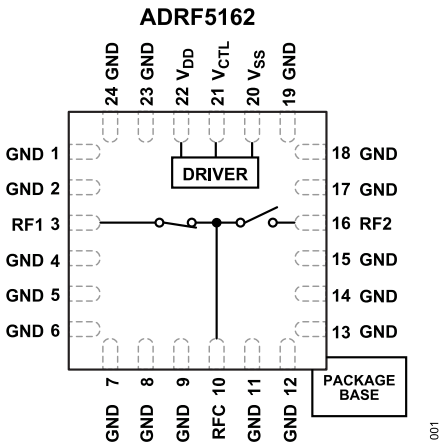

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5162 is a reflective, single pole double-throw (SPDT) switch manufactured in the silicon process.

The ADRF5162 operates from 0.4 GHz to 8 GHz with typical insertion loss of 0.6 dB and typical isolation of 45 dB. The device has a radio frequency (RF) input power handling capability of 45.5 dBm average power and 50 dBm peak power for the insertion loss path.

The ADRF5162 draws a low current of 130 µA on the positive supply of +3.3 V and 500 µA on negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low-voltage transistor to transistor logic (LVTTL)-compatible controls. The ADRF5162 requires no additional driver circuitry, which makes it an ideal alternative to GaN and PIN diode-based switches.

The ADRF5162 comes in a 24-lead, 4.0 mm × 4.0 mm, RoHS-compliant, lead frame chip scale package (LFCSP) package and can operate from −40°C to +105°C.

TABLE OF CONTENTS

REVISION HISTORY

7/2024—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = -3.3 V, V_{CTRL} = 0 V or V_{DD} V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		400		8,000	MHz
INSERTION LOSS						
Between RFC and RF1/RF2 (ON)		400 MHz to 4 GHz		0.6		dB
		4 GHz to 6 GHz		0.7		dB
		6 GHz to 8 GHz		0.8		dB
RETURN LOSS						
RFC and RF1/RF2 (ON)		400 MHz to 4 GHz		25		dB
		4 GHz to 6 GHz		20		dB
		6 GHz to 8 GHz		20		dB
ISOLATION						
Between RFC and RF1/RF2 (OFF)		400 MHz to 4 GHz		45		dB
		4 GHz to 6 GHz		35		dB
		6 GHz to 8 GHz		30		dB
Between RF1 and RF2		400 MHz to 4 GHz		40		dB
		4 GHz to 6 GHz		35		dB
		6 GHz to 8 GHz		30		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		200		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		800		ns
RF Settling Time						
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF output, P_{IN} ≤ 43 dBm		1.2		µs
INPUT LINEARITY		f = 1 GHz to 5 GHz				
0.1 dB Power Compression	P0.1dB			50		dBm
Input Third-Order Intercept	IIP3	Two tone input power = 30 dBm each tone, Δf = 1 MHz		>76		dBm
SUPPLY CURRENT		V_{DD}, V_{SS} pins				
Positive Supply Current	I_{DD}			130		µA
Negative Supply Current	I_{SS}			500		µA
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<0.1		µA
RECOMMENDED OPERATING CONDITONS						
Positive Supply Voltage	V_{DD}		3.15		3.45	V
Negative Supply Voltage	V_{SS}		−3.45		−3.15	V
Digital Control Input Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power Wait Time[1]	t_{Wait}	P_{IN} ≤ 43 dBm	0			µs
		43 dBm < P_{IN} ≤ 45 dBm	1.0			µs
		45 dBm < P_{IN} ≤ 46 dBm	1.5			µs
		46 dBm < P_{IN} ≤ 47 dBm	2.0			µs
		47 dBm < P_{IN} ≤ 48 dBm	3.0			µs
		48 dBm < P_{IN} ≤ 48.5 dBm	4.0			µs
RF Input Power[2]	P_{IN}	f = 1 GHz to 5 GHz, T_{CASE} = 85°C[3]				

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Insertion Loss Path		RF signal applied to the RFC or through connected RF1/RF2				
Average					45.5	dBm
Pulsed[4]		>100 ns pulse width, 15% duty cycle			48.5	dBm
Peak		≤100 ns peak duration, 5% duty cycle			50	dBm
Hot Switching		RF signal applied to the RFC			43	dBm
LTE Signal		T_{CASE} = 105°C				
Average		8.5 dB PAR, long-term (>10 years)			41.5	dBm
Average		8.5 dB PAR, single event (<10sec)			42.5	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For more details, see the Theory of Operation section.

[2] For power derating over frequency, see Figure 2 and Figure 3.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

[4] For different pulsed conditions, contact Applications Support.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Positive	−0.3 V to +3.6 V
Negative	−3.6 V to +0.3 V
Digital Control Input Voltage	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power[1] (f = 1 GHz to 5 GHz, T_{CASE} = 85°C)	
Insertion Loss Path	
Average	46.0 dBm
Pulsed	49.0 dBm
Peak	50.5 dBm
Hot Switching	43.5 dBm
RF Power Under Unbiased Condition (V_{DD}, V_{SS} = 0 V)	
Input at RFC	33 dBm
Input at RFx	27 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C

[1] For power derating over frequency, see Figure 2 and Figure 3.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at a time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to the case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CP-24-22	8.6	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

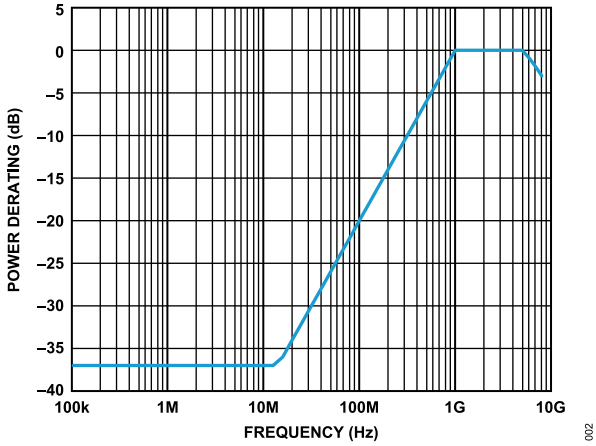

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

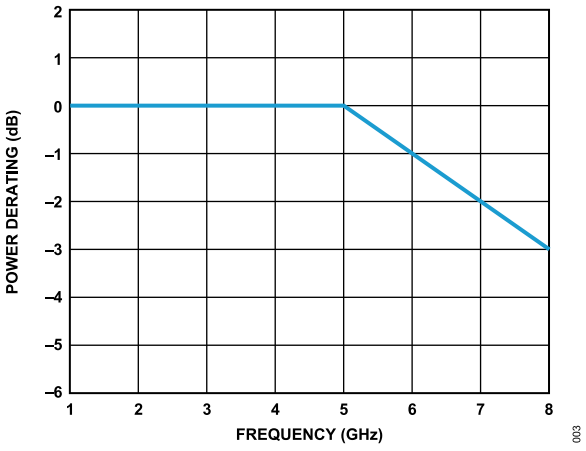

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5162

Table 4. ADRF5162, 24-Terminal LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±2000 for all pins	2
CDM	±500 for all pins	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

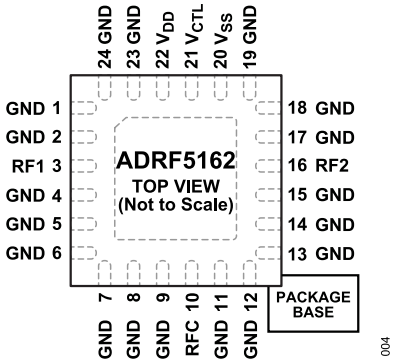

Figure 4. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 9, 11 to 15, 17 to 19, 23, 24	GND	Ground. These pins must be connected to the RF/DC ground of the PCB.
3	RF1	RF Throw Port 1. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
10	RFC	RF Common Port. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
16	RF2	RF Throw Port 2. This pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC.
20	VSS	Negative Supply Voltage.
21	CTRL	Control Input. For the truth table, see Table 6.
22	VDD	Positive Supply Voltage.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/DC ground of the PCB.

INTERFACE SCHEMATICS

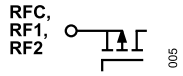

Figure 5. RF Pins (RFC, RF1, and RF2)

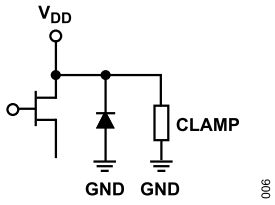

Figure 6. V_{DD} Pin

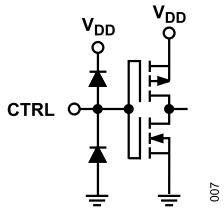

Figure 7. Digital Pin (CTRL)

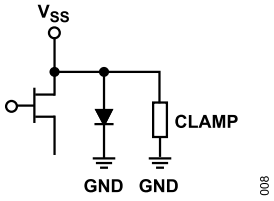

Figure 8. V_{SS} Pin

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = -3.3 V or 0 V, V_{CTRL} = 0 V or V_{DD} V, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted. Measured on the ADRF5162-EVALZ.

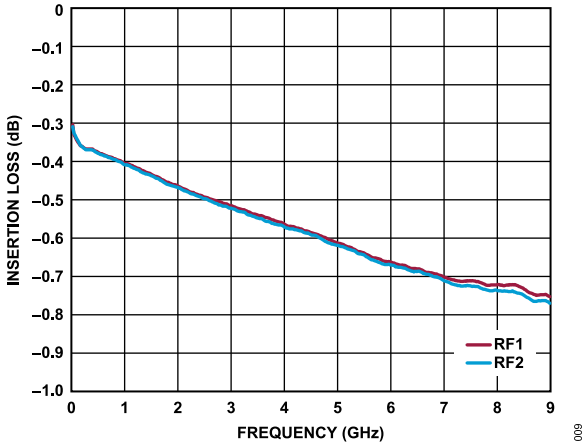

Figure 9. Insertion Loss vs. Frequency at Room Temperature for RF1 and RF2

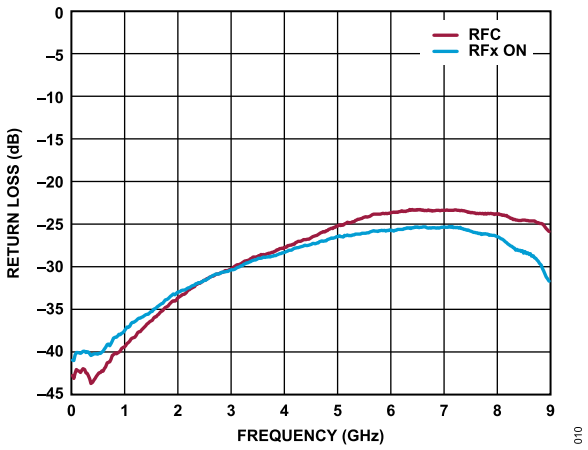

Figure 10. Return Loss vs. Frequency

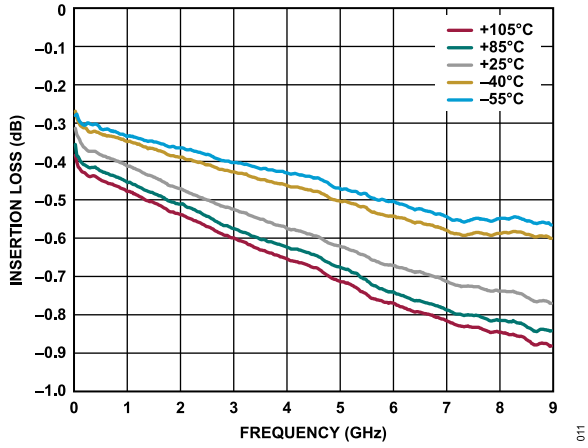

Figure 11. Insertion Loss vs. Frequency over Temperature

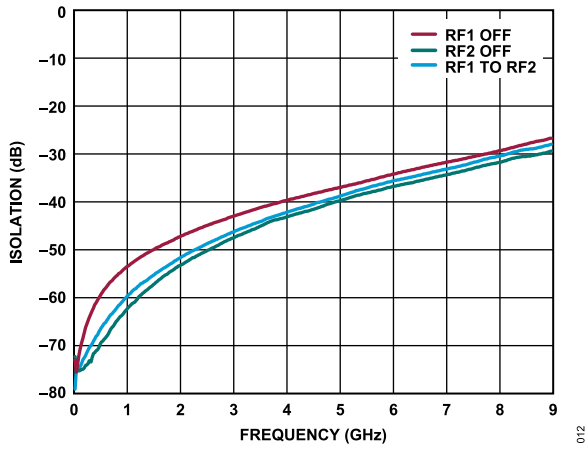

Figure 12. Isolation vs. Frequency

THEORY OF OPERATION

The ADRF5162 integrates a driver to perform logic function internally and to provide the advantage of a simplified control interface. The driver features a single control input pin, CTRL, that controls the state of RF paths, determining which RF port is in insertion loss state and which RF port is in isolation state (see Table 6).

POWER SUPPLY

The ADRF5162 requires a positive supply voltage applied to the V_{DD} pin and a negative supply voltage applied to the V_{SS} pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect the ground.
2. Power up V_{DD} and V_{SS}. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp-up.
3. Power up the digital control inputs. Power the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high-impedance state after V_{DD} is powered up, and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.
5. The ideal power-down sequence is the reverse order of the power-up sequence.

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port. The unselected RF port of the ADRF5162 is reflective.

The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

Table 6. Control Voltage Truth Table

	RF Paths	
Digital Control Input, V_{CTRL}	RF1 to RFC	RF2 to RFC
Low	Insertion loss (on)	Isolation (off)
High	Isolation (off)	Insertion loss (on)

TIMING SPECIFICATIONS

When RF input power is greater than the maximum recommended hot-switching power level, a wait time of t_{WAIT} must be respected after switching between RF throw ports (see Figure 13).

There is no wait time required if applying RF power levels lower than or equal to the maximum recommended hot-switching power level (see Table 1).

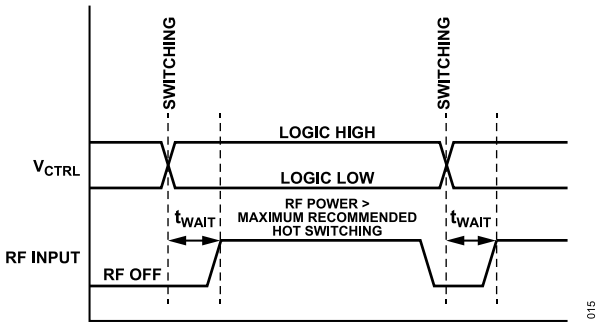

Figure 13. RF Input Power Wait Time

APPLICATIONS INFORMATION

The ADRF5162 has two power supply pins (V_{DD} and V_{SS}) and one control pin (CTRL). Figure 14 shows the external components and connections for supply and control pins.

The V_{DD} and V_{SS} pins are decoupled with 100 pF and 0.1 µF multilayer ceramic capacitors, respectively, while the control pin is decoupled with a 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. For more details, see the Pin Configuration and Function Descriptions section.

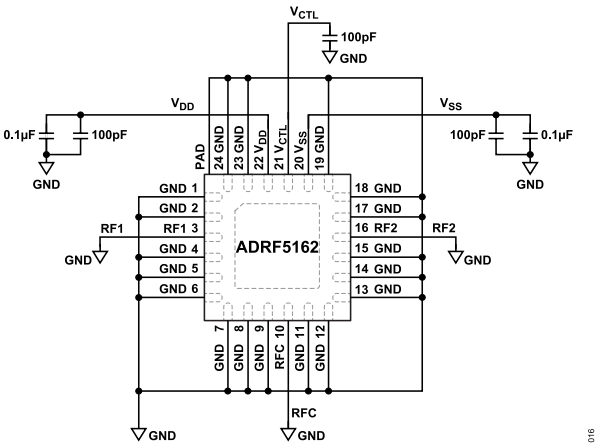

Figure 14. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 15 shows the referenced CPWG RF trace design for an RF substrate with 10 mil thick Rogers RO4350 dielectric material. RF trace with 18 mil width and 13 mil clearance is recommended for 2.8 mil finished copper thickness.

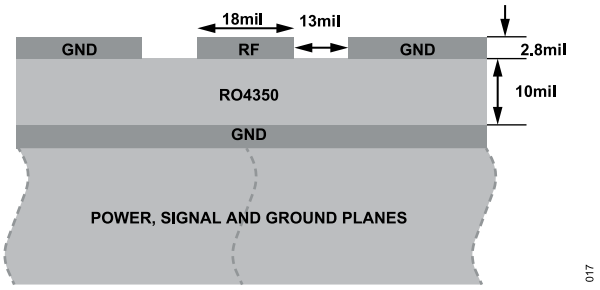

Figure 15. Example PCB Stack-Up

Figure 16 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled, through vias as allowed for optimal RF, and thermal performance. The primary thermal path for the device is the bottom side. Therefore, a heatsink is required underneath the PCB to ensure maximum heat dissipation and to reduce thermal rise on the PCB during high-power applications.

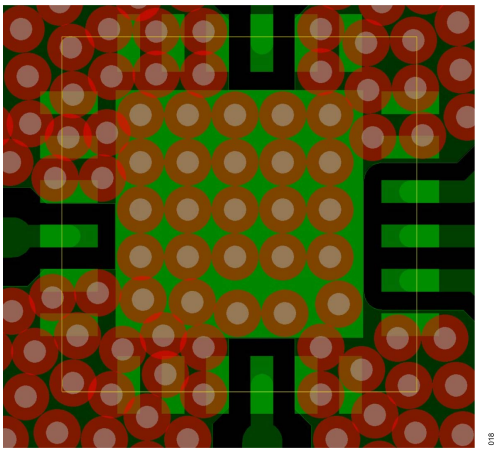

Figure 16. PCB Routings

Figure 17 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn soldermask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width and tapered to RF trace. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

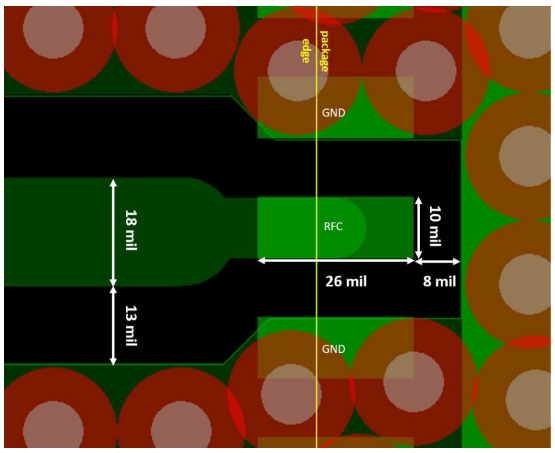

Figure 17. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, and for further recommendations, contact Analog Devices Technical Support.

OUTLINE DIMENSIONS

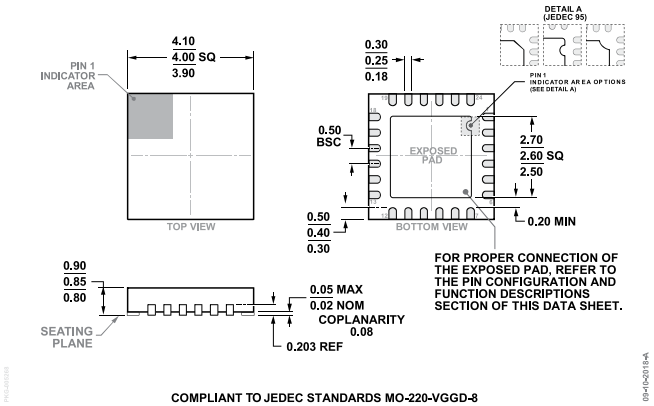

Figure 18. 24-Terminal Lead Frame Chip Scale Package [LFCSP]
4.0 mm × 4.0 mm Body and 0.85 mm Package Height
(CP-24-22)
Dimensions Shown in Millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Quantity	Package Option
ADRF5162BCPZN	−40°C to +105°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	Reel, 500	CP-24-22
ADRF5162BCPZN-R7	−40°C to +105°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	Reel, 500	CP-24-22

[1] Z = RoHS-Compliant Part.

EVALUATION BOARD

Table 7. Evaluation Board

Model[1]	Description
ADRF5162-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.