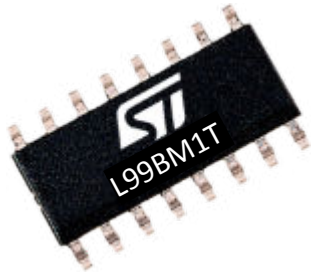
L99BM1T

Datasheet

General purpose SPI to isolated SPI transceiver



SO-16 narrow

Features

- Compatible with both 3.3 V and 5 V logics
- Supports both XFMR and Capacitive isolation
- 10 MHz SPI peripheral for SPI Slave operation. Configurable SPI frequency (250 kHz to 8 MHz) for SPI Master operation
- 333 kbps and 2.66 Mbps Vertical InterFace (VIF) for isolated SPI communication
- Low standby current

Application

- High voltage battery packs
- Backup energy storage systems and UPS
- Industrial communication networks
- Portable and semi-portable equipment
- Remote sensors

Description

L99BM1T is a general purpose SPI to isolated SPI transceiver intended to create a communication bridge between devices located into different voltage domains.

L99BM1T is able to transfer communication data incoming from a classical 4-wire based SPI interface to a 2-wire isolated interface (and viceversa).

The transceiver supports both transformer and capacitive isolation.

The device can be configured either as Slave or as Master of the SPI bus and supports any protocol made of SPI frames 8 to 64 bit long.

SPI peripheral can work up to 10 MHz when configured as Slave. SPI clock frequency can be programmed among (250 kHz; 1 MHz; 4 MHz; 8 MHz) when configured as Master.

Isolated SPI peripheral features two different operating modes: slow @333 kbps and fast @2.66 Mbps.

The asynchronicity between the two sides is internally managed, allowing all possible configuration frequencies on both peripherals to be used in application.

The device is natively compatible with L99BM114 isolated SPI, allowing its usage in the BMS applications.

L99BM1T is compatible with both 3.3 V and 5 V logics.

Product status link
L99BM1T

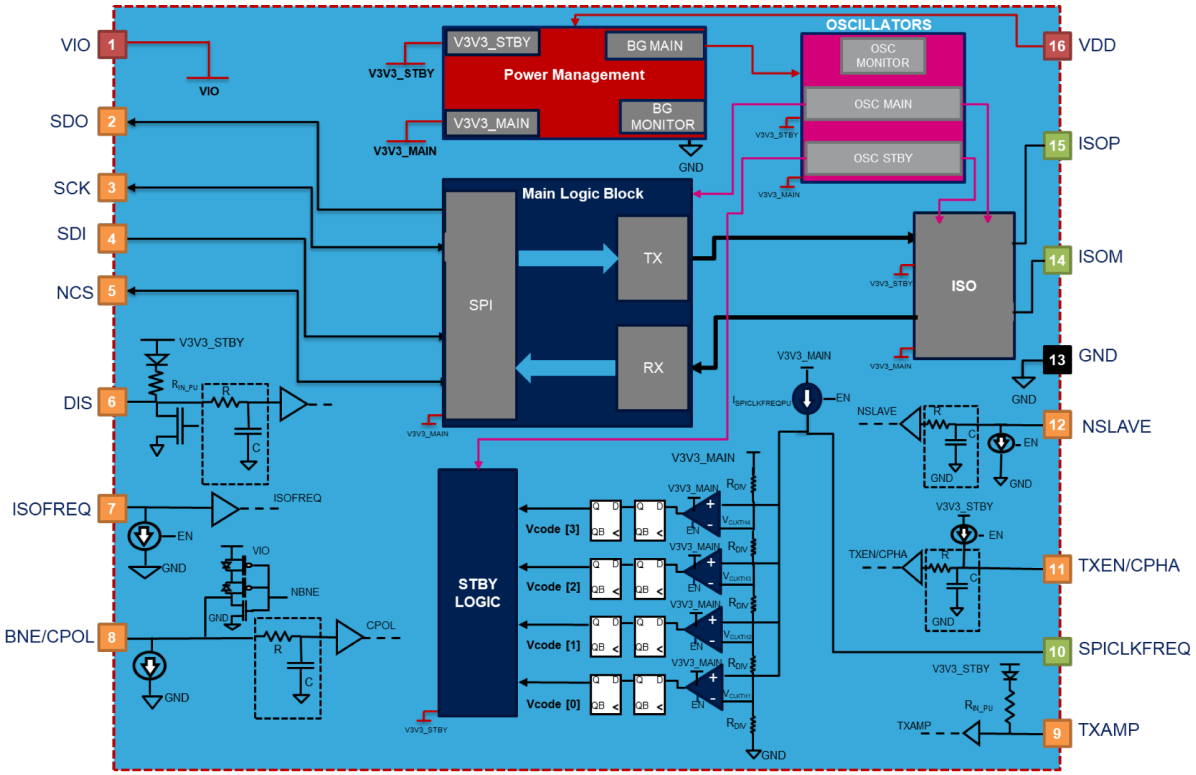
Product summary		
Order code	Package	Packing
L99BM1T-TR	SO16N	Tape and reel

Product label
SUSTAINABLE TECHNOLOGY

1 Block diagram and pin description

1.1 Block diagram

Figure 1. **Block diagram**



1.2 Pin description

Figure 2. **Pin connection diagram (top view)**

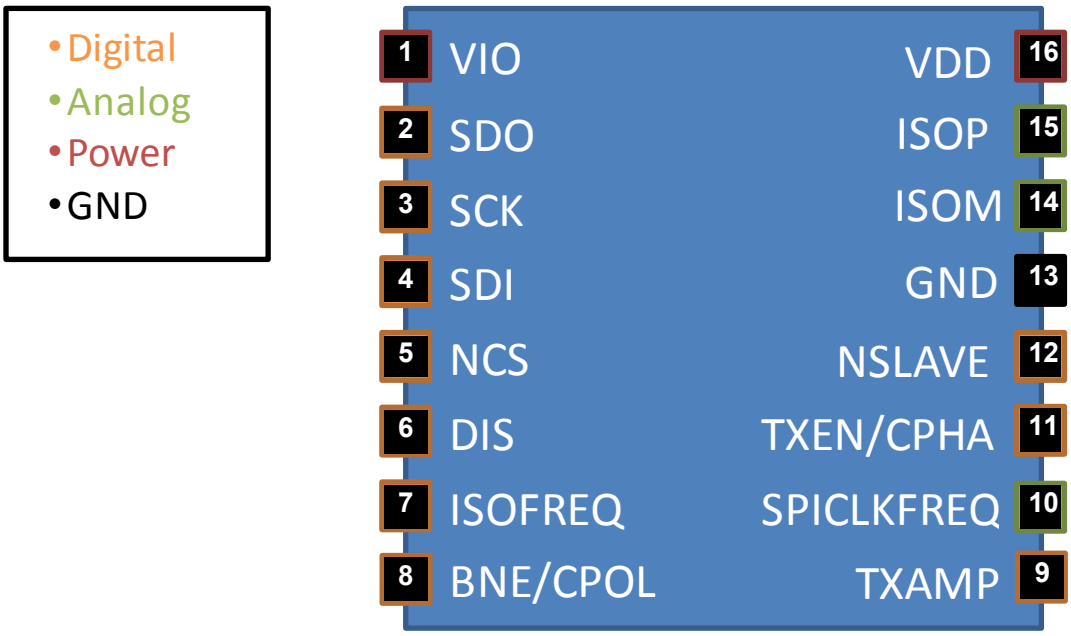


Table 1. **Pin list description**

Pin #	Type		Local/ Global	Active	Description
POWER					
VDD	Power		Local	-	5V supply input for internal logic and isolated SPI
VIO	Power		Local	-	Digital Output Buffer Supply. Connect either to 5 V or to 3.3 V supply.
GND	Ground		Local	-	Device Ground
SPI					
SDO	Digital Output (Push-Pull)		Local	-	SPI Serial Data Output. Needs external pull up/pull down resistor to define inactive level.
SCK	Digital Input/ Output (Push-Pull)	NSLAVE = 0 → Digital Input NSLAVE = 1 → Digital Output	Local	-	SPI Serial Clock. Internally pulled down with 100 kΩ
SDI	Digital Input		Local	-	SPI Serial Data Input. Internally pulled down with a 100 kΩ resistor for safety purposes.
NCS	Digital Input/ Output (Push-Pull)	NSLAVE = 0 → Digital Input NSLAVE = 1 → Digital Output	Local	-	SPI Chip Select. Internally pulled up with a 100 kΩ resistor for safety purposes.
BNE/CPOL	NSLAVE = 0 → BNE Digital Output (Push-Pull)		Local	High	SDO Buffer Not Empty flag. It is set high when at least one frame is in the RX buffer. It is set low when RX buffer is empty. When L99BM1T is configured as Slave, connect this pin to MCU GPIO for interrupt/polling based communication.

Pin #	Type	Local/ Global	Active	Description
BNE/CPOL	NSLAVE = 1 → CPOL Digital Input	Local	-	SPI Clock Polarity selection input. Latched during Trimming & Config Latch. Connect either to VDD (CPOL = 1) or to GND (CPOL = 0). Internally pulled down (active). Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
NSLAVE	Digital Input	Local	-	SPI Slave/Master selection. Latched during Trimming & Config Latch Connect to GND to select Slave operation. Connect to VDD to select Master operation. Internally pulled down (active). Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
TXEN/CPHA	NSLAVE = 0 → TXEN Digital Input	Local	High	Transmitter enable signal. Set high to enable the TX activity. Pull down to disable TX. Any data received on the SDI line while TXEN is low will be discarded and not stored into TX buffer. Internally pulled up (active). Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
	NSLAVE = 1 → CPHA Digital Input	Local	-	SPI Clock Phase selection input. Latched during Trimming & Config Latch. Connect either to VDD (CPHA = 1) or to GND (CPHA = 0). Internally pulled up (active). Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
SPICLKFREQ	Analog Input	Local	-	SPI Master Clock selection. Latched during Trimming & Config Latch. Leave open to set minimum frequency. Connect a pull down resistor to set a higher frequency. Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.
ISOLATED SPI				
ISOP	Analog Input/Output	Global	-	Isolated SPI Positive terminal
ISOM	Analog Input/Output	Global	-	Isolated SPI Negative terminal
TXAMP	Digital Input	Local	-	Isolated SPI TX amplitude selection. Set low to select low amplitude/low threshold. Set high to select high amplitude/high threshold. Internally pulled up with a 100 kΩ resistor.
ISOFREQ	Digital Input	Local	-	Isolated SPI operating frequency selection. Pull high to set high frequency. Pull down to set low frequency. Internally pulled down (active).

Pin #	Type	Local/ Global	Active	Description
DISABLE				
DIS	Digital Input/Output (Open Drain)	Local	High	Transceiver Disable Input. Pull it up with external resistor connected to VIO. When DIS is high, L99BM1T enters in low power mode. When DIS is low, L99BM1T is enabled and working in Normal mode. It can be either pulled-down by the MCU to enable the unit, or pulled down internally when a wakeup condition occurs, in order to interrupt the MCU. Pin is internally pulled up with 100 kΩ resistor. Input filtered with RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.

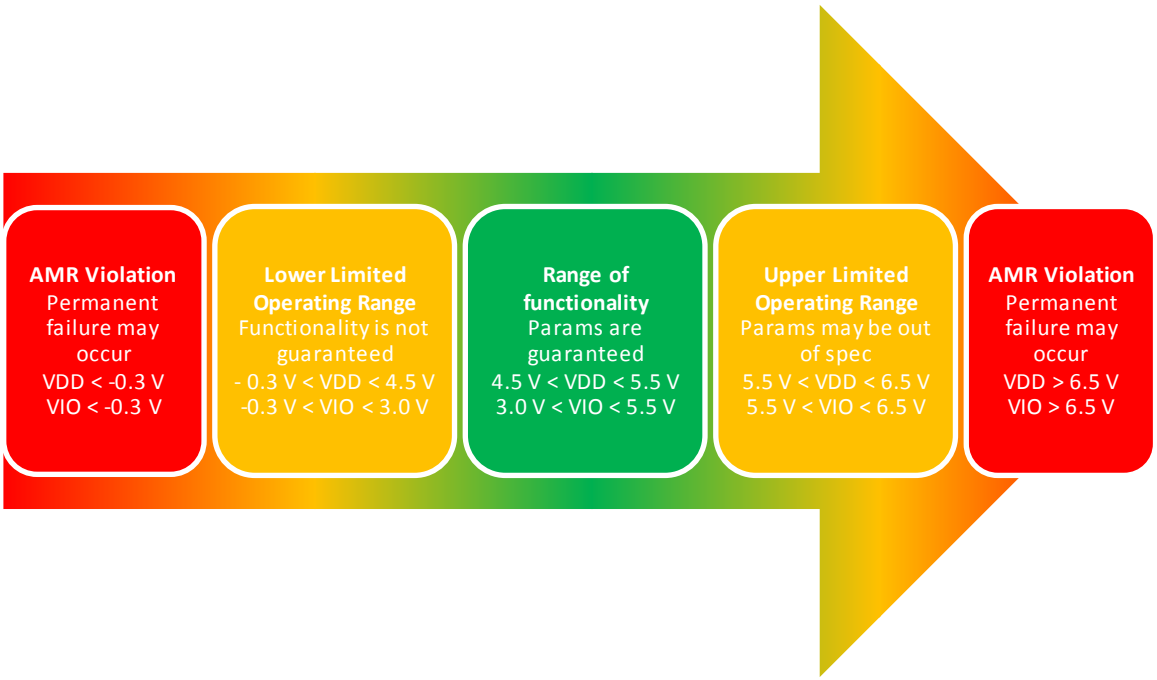
2 Product electrical and thermal ratings

2.1 Supply ranges

Figure 3 lists the product power supply ranges:

- Within the range of functionality the part operates as specified and without parameter deviations. All the functionalities and the electrical parameters are guaranteed.
- If either the upper or the lower limited operating range is reached, the device may not operate properly. Only a limited set of functionalities and electrical parameters are guaranteed. However, neither damage nor parameter deviation occurs, and the device will operate properly once returned to the range of functionality.
- If AMR are violated, permanent damage or parametric deviation may occur.

Figure 3. Supply ranges



Note: all voltages are related to the potential at substrate ground GND.

2.2 Operating range

Table 2. Pin operating range

Pin	Condition	Min	Typ	Max	Unit
VDD	Supply pin	4.5	-	5.5	V
VIO	Digital Output Buffers supply pin	3.0	-	5.5	V
DIS, ISOFREQ, BNE/CPOL, TXAMP, TXEN/CPHA, NSLAVE	Digital I/Os	0	-	VIO	V
|ISOP + ISOM| / 2	Isolated SPI Common Mode Voltage	1	1.2	1.4	V
|ISOP – ISOM|	Isolated SPI Differential Voltage	0	-	2.5	V
SDO, SCK, SDI, NCS	SPI pins	0	-	VIO	V
SPICLKFREQ	Analog Input	0	-	VDD	V

Note: all voltages are related to the potential at substrate ground GND.

2.3 Absolute maximum rating

Table 3. Absolute maximum rating

Symbol	Parameter	Min	typ	Max	Unit
VIO, VDD	Supply Input Voltage	-0.3	-	6.5	V
BNE/CPOL, NSLAVE, DIS, TXEN/CPHA, ISOFREQ, TXAMP	Digital I/Os	-0.3	-	6.5	V
ISOP, ISOM	Analog I/Oson isolated SPI side	-0.3	-	6.5	V
SDO, SCK, SDI, NCS	Serial Peripheral Interface Communicati on Ports	-0.3	-	VIO + 0.3	V
SPICLKFRQ	Analog Input for SPI clock frequency selection	-0.3	-	6.5	V

Note: all voltages are related to the potential at substrate ground GND.

2.4 ESD protection

Table 4. ESD protection

Item	Condition	Min	Typ	Max	Unit
All pins Except Isolated Communication Terminals and Global pins(1)	HBM(2)	-2	-	2	KV
Isolated Communication Terminals(1)(2) and Global pins versus all GND connected		-4	-	4	KV
All pins except Corner Pins	CDM(3)	-500	-	500	V
Corner Pins		-750	-	750	V
All pins	Latch up(4)	-100	-	100	mA

1. *Tested per AEC-Q100-002.*
2. *Isolated Communication Terminals: ISOP, ISOM.*
3. *Tested per AEC-Q100-011.*
4. *Tested per AEC-Q100-004, Class-2, Level-A.*

Note: pins are all GND connected together.

2.5 Temperature ranges and thermal data

Table 5. Temperature ranges and thermal data

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating and testing temperature (ECU environment)	-40	-	105	°C
T_j	Junction temperature for all parameters	-40	-	125	°C
T_{stg}	Storage temperature	-65	-	125	°C
$R_{THj\text{-}amb}$	Thermal resistance junction-to-ambient	-	-	90	°C/W

2.6 Power mangement

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: -40 °C < Tj < 125 °C

Table 6. Power management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply VDD						
V_{VDD}	Supply Voltage	FullyOperational	4.5	-	5.5	V
$I_{VDD(NORMAL\_COMM)}$	Supply Current	NormalMode, DIS = 0 and continuos communication	-	9	14	mA
$I_{VDD(NORMAL)}$	Supply Current	NormalMode, DIS = 0	5	6.5	8	mA
$I_{VDD(SLEEP)}$	Supply Current	Sleep Mode, DIS = 1	-	-	64	µA
Power Supply VIO						
V_{VIO}	Supply Voltage		3.0	-	5.5	V
$I_{VIO(NORMAL\_COMM)}$	VIO Supply Current	NormalMode, DIS = 0 and continuous communication Design info	-	-	12	mA
$I_{VIO(NORMAL)}$	VIO Supply Current	NormalMode, DIS = 0	1.5	2.5	3.5	mA
$I_{VIO(SLEEP)}$	VIO Supply Current	Sleep Mode, DIS = 1	-	-	1	µA

To optimize power consumption, the device selectively disables unnecessary peripherals according to FSM state and **NSLAVE** pin value latched at first power up.

Table 7. Device configuration according to NSLAVE pin

FSM STATE	TRIMMING AND CONFIG	STAND-BY	NORMAL	
Resource	**NSLAVE not latched**	**NSLAVE latched but don't care**	**NSLAVE = 0 (SPI Slave)**	**NSLAVE = 1 (SPI Master)**
Main Oscillator Monitor	Disabled	Disabled	Enabled	
V3V3_MAIN Monitor	Disabled	Disabled	Enabled	
V3V3_STBY Monitor	Disabled	Disabled	Enabled	
BG STBY	Enabled	Enabled	Enabled	
BG Main (STBY Monitor)	Disabled	Disabled	Enabled	
SDO Output Buffer	Disabled	Disabled	Enabled only when NCS is active	
SCK Output Buffer	Disabled	Disabled	Disabled	Enabled
SCK Input Buffer	Disabled	Disabled	Enabled	
SDI Input Buffer	Disabled	Disabled	Enabled	
NCS Output Buffer	Disabled	Disabled	Disabled	Enabled
NCS Input Buffer	Disabled	Disabled	Enabled	
BNE/CPOL Output Buffer	Disabled	Disabled	Enabled	Disabled
BNE/CPOL Input Buffer	Enabled	Disabled	Enabled	Enabled
NSLAVE Input Buffer	Enabled	Disabled	Disabled	
TXEN/CPHA Input Buffer	Enabled	Disabled	Enabled	Disabled
SPICLKFREQ Input Comparators	Enabled	Disabled	Disabled	
ISOP TX	Disabled	Disabled	Enabled	
ISOM RX	Disabled	Disabled	Enabled	

FSM STATE	TRIMMING AND CONFIG	STAND-BY	NORMAL	
Resource	NSLAVE not latched	NSLAVE latched but don't care	NSLAVE = 0 (SPI Slave)	NSLAVE = 1 (SPI Master)
ISOM RX Wake up	Disabled	Enabled	Disabled	
TXAMP Input Buffer	Disabled	Disabled	Enabled	
ISOFREQ Input Buffer	Disabled	Disabled	Enabled	
DIS Input Buffer	Disabled	Enabled	Enabled	
DIS Open Drain Driver	Disabled	Disabled	Enabled only if wakeup from VIF detected, and pulled down for TDIS_PULLDOWN	
NSLAVE Pull down	Enabled	Disabled	Disabled	
BNE/CPOL Pull down	Enabled	Disabled	Enabled	
TXEN/CPHA Pull up	Enabled	Disabled	Enabled	
SPICLKFREQ Pull up & Divider	Enabled	Disabled	Disabled	

3 Functional description

In the following paragraphs, the functionalities of the device are listed and described in detail.

3.1 Internal oscillators

L99BM1T features two internal oscillators for both main and stand-by functionalities.

Table 8. Device oscillators

Symbol	PARAMETER	MIN	TYP	MAX	UNIT
f_{MAIN_OSC}	Internal MAIN Oscillator frequency	15	16	17	MHz
f_{STBY_OSC}	Internal STBY Oscillator frequency	24	32	50	kHz

3.2 Pin configuration

All device pins are hereby described.

3.2.1 Digital I/Os

In the following paragraph, the functionality of the Digital I/Os is explained.

BNE/CPOL, TXEN/CHPA are used as standard digital input (Schmitt trigger) or digital output (Output buffer) configuration, depending on the configuration defined by digital NSLAVE pin.

DIS is used as standard digital input (Schmitt trigger) or digital output (Open Drain) configuration, depending on the state the device is in. When it's in STAND-BY state and a wake up comes from ISO line the DIS pin is driven low by L99BM1T.

NSLAVE, ISOFREQ, TXAMP are used as standard digital input (Schmitt trigger) for the configuration of device.

3.2.1.1 SPI pin

SDO, SCK, SDI, NCS pins implement the SPI peripheral, whose configuration depends on the **NSLAVE** value latched at first power up:

- SDI is always configured as digital input. It is internally pulled down with RIN_PD in order to generate a 0x0 frame in case of pin loss (purpose is to lead to CRC violation in safety applications). Its buffer is enabled only in **Normal state**.
- SDO is always configured as digital output. Its buffer is enabled only if **NCS** is asserted. An external pull up/pull down resistor defines the inactive level of the line.
- SCK, NCS can be either configured as digital input (NSLAVE = 0, SPI Slave) or as digital output (NSLAVE = 1, SPI Master):
  - SCK pin is internally pulled down with RIN_PD in order to stabilize clock signal to logic '0' in case of pin loss.
  - NCS pin is internally pulled up with RIN_PU in order to disable SPI peripheral in case of pin loss.
  - When SCK and NCS are configured as digital input (NSLAVE = 0), the output buffers are permanently disabled after **Trimming & Config Latch** is left.
  - When SCK and NCS are configured as digital output (NSLAVE = 1), the NCS inactive level is high, and it is actively forced by the output buffer while no SPI communication is ongoing. The SCK inactive level depends on the CPOL value latched in **Trimming & Config Latch** state, and it is actively forced by the output buffer while no SPI communication is ongoing.

The selective enable/disable of the buffers helps reducing the power consumption of the device when SPI works at high frequencies.

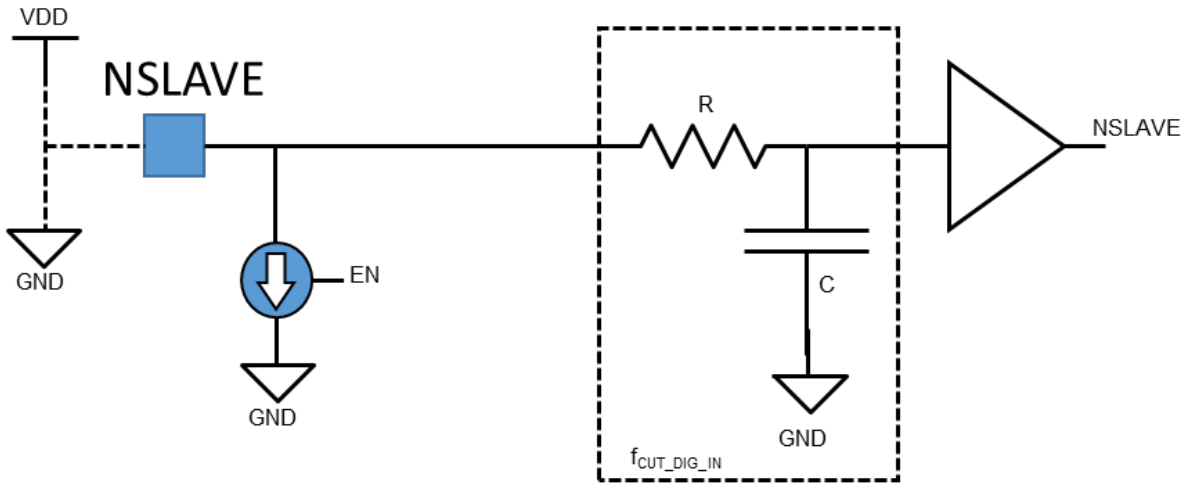
3.2.1.2 NSLAVE

NSLAVE pin is latched by the standby logic in the **Trimming & Config Latch** state, $\mathbf{3T_{OSC\_STBY}}$ after POR_MAIN release. It must be either shorted to VDD or to GND. The internal pull-down is enabled only while in **Trimming & Config Latch** state. This allows reducing power consumption. Once **Trimming & Config Latch** state is left, the **NSLAVE** input buffer is permanently disabled, since it is no longer needed.

NSLAVE selects SPI Master (**NSLAVE = 1**) or Slave (**NSLAVE = 0**) operation and determines the Digital I/Os configuration as described in Table 7.

To increase immunity to BCI and guarantee a correct latch of the **NSLAVE** pin during each power-up, the input is filtered with an integrated RC filter having $f_{CUT\_DIG\_IN}$ cut frequency.

Figure 4. NSLAVE pin structure



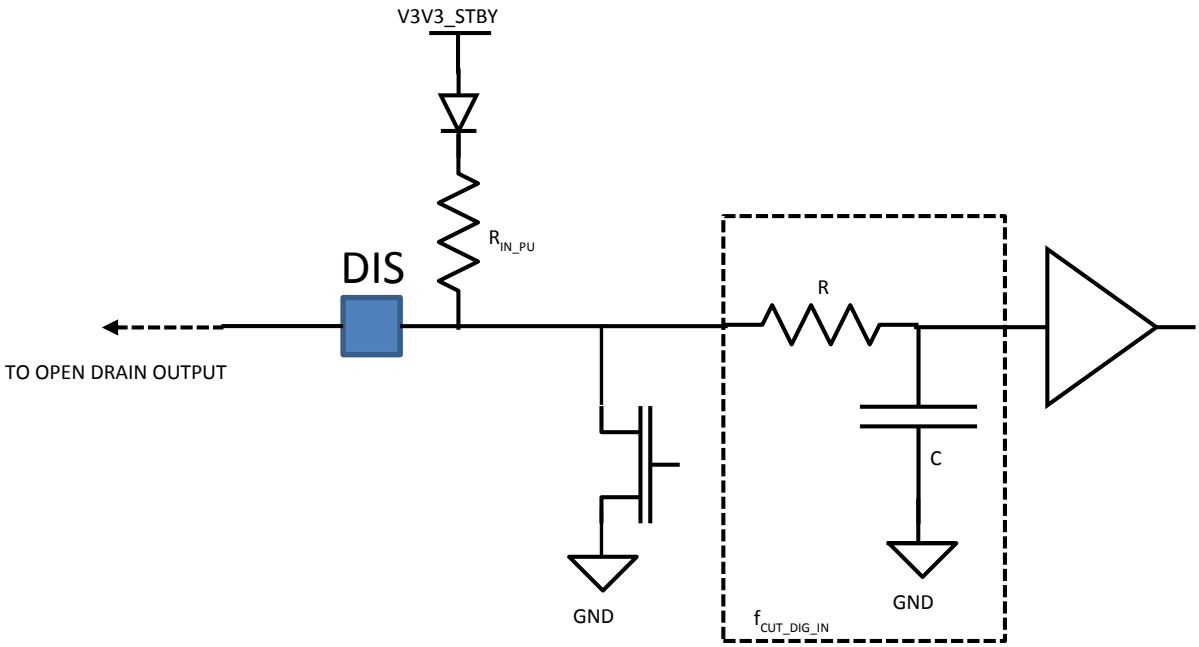
3.2.1.3 *DIS*

DIS is a Digital Input-Output pin featuring an internal pull-up resistor towards V3V3_STBY. Its purpose is to be driven by open-drain outputs. Its functionality is summarized as follows:

- **Input:** it is an active high Disable input driven by the MCU:
  - When DIS is released by the MCU longer than T_{RC_DELAY} +$T_{DIS\_DEGLITCH}$ the device starts the Go To Sleep sequence that will bring L99BM1T to **Stand-by state** (refer to **L99BM1T FSM**).
  - When DIS is pulled down by the MCU longer than T_{RC_DELAY} + (1/ f_{STBY_OSC}) the device moves from **Stand-by state** to **Regulators enabling state** and then to **Normal state**.
- **Output:** when L99BM1T is in **Stand-by state**, and a wakeup event by isolated SPI occurs, it moves to **Regulators enabling state** and then to **Normal state**. Once the latter is reached, **DIS** is internally pulled-down by logic for $T_{DIS\_PULLDOWN}$ in order to trigger an interrupt in the MCU or a wake up event on a PMIC. After $T_{DIS\_PULLDOWN}$ expires, **DIS** is released, and if not kept low by an external source, L99BM1T moves back to **Stand-by state**.

To protect **DIS** internal open drain driver in case of external short to VDD, a current limitation circuitry limits the current to I_{DIS_LIM}.

Figure 5. **DIS pin structure**



3.2.1.4 *ISOFREQ*

ISOFREQ pin is a digital input used to switch ISOline bit rate:

- **ISOFREQ = 1** selects fast operation: bit time is **TBIT_LENGTH_FAST**
- **ISOFREQ = 0** selects slow operation: bit time is **TBIT_LENGTH_SLOW**

ISOFREQ sampling depends on device state and configuration:

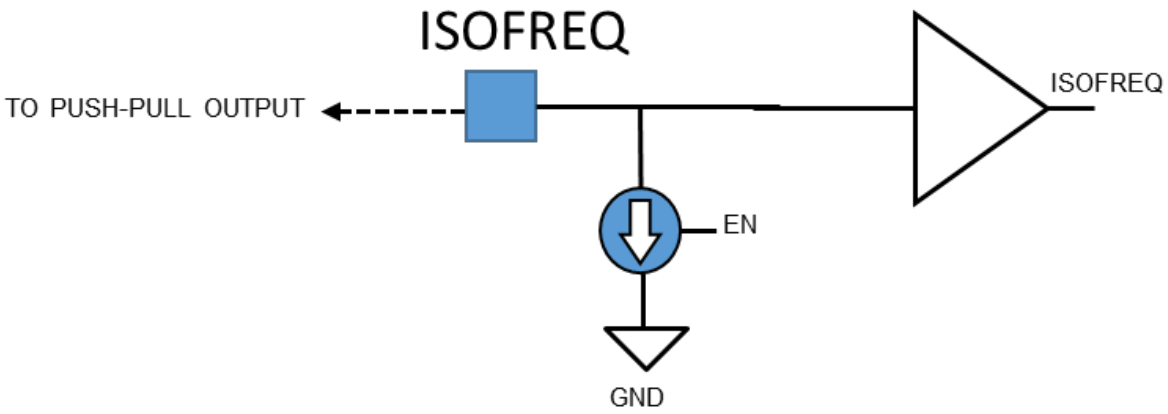
Table 9. **ISOFREQ sampling strategy**

L99BM1T state	L99BM1T configuration	ISOFREQ sampling	Note
Normal state	Slave (NSLAVE = 0)	The **ISOFREQ** pin is latched upon **NCS** assertion. Therefore, it must be stable at least $T_{ISOFREQ\_DEGLITCH}$ + $T_{ISOFREQ\_SETUP}$ before NCS assertion. Moreover, ISOFREQ must be kept stable $T_{ISOFREQ\_HOLD}$ after NCS assertion in order to fulfil hold time constraints. The new bit rate setting is immediately applied to the RX interface, while it is applied to the TX interface after the SPI frame has been completely transmitted over the isolated SPI interface. This allows **Managing ISOFREQ And TXAMP Pins For Communicating With L99BM114**	In case several SPI frames are being pushed into the TX queue, the setting applied once the TX interface is in idle depends on the last one latched (no pipelining supported).
	Master (NSLAVE = 1)	The ISOFREQ setting is simply resynchronized ($T_{ISOFREQ\_SETUP}$ and $T_{ISOFREQ\_HOLD}$ requirements still apply) and deglitched ($T_{ISOFREQ\_DEGLITCH}$ filter still present), but it is not latched upon NCS assertion.	
Stand-by state	Slave/Master (NSLAVE = X)	The new ISOFREQ setting is latched during the wake up sequence. Hence, the ISOFREQ pin shall be stable $T_{ISOFREQ\_SETUP}$ before the DIS high → low transition is applied and shall not change during T_{WAKEUP}.	-
Reset state	Slave/Master (NSLAVE = X)	The initial ISOFREQ setting is latched during the first power up sequence. Hence, the ISOFREQ pin shall be stable before VDD is applied and shall not change during $T_{FIRST\_POWERUP}$.	-

The new bit rate of L99BM1T must be compatible with the one of all other units communicating on the same bus.

The internal pull-down guarantees a limp home operation in low frequency in case of pin-loss.

Figure 6. ISOFREQ pin structure



3.2.1.5 *BNE/CPOL*

BNE/CPOL is a digital input/output pin whose configuration depends on the value of NSLAVE latched during **Trimming & Config Latch**:

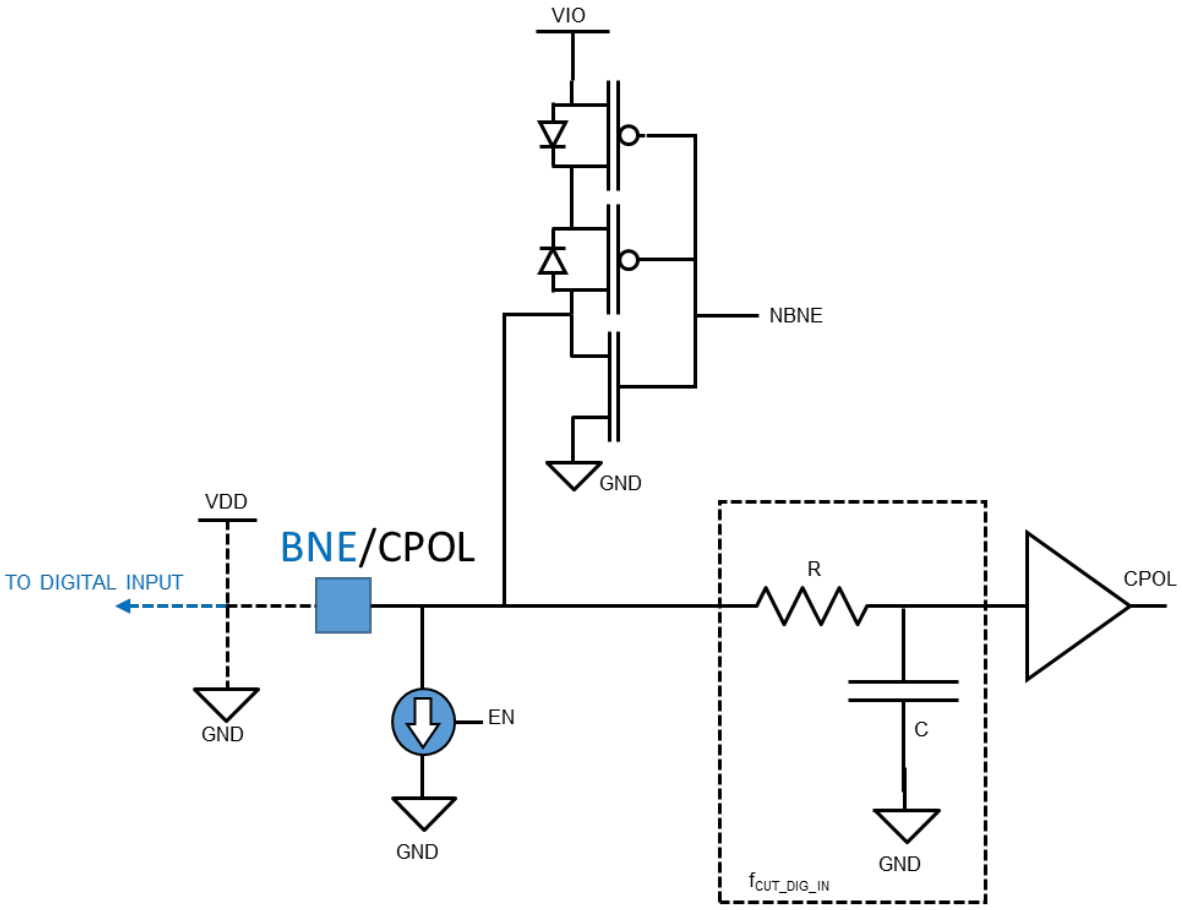
- When **NSLAVE = 0** (Slave configuration), this pin acts as **BNE** (Buffer Not Empty) digital output and its purpose is to implement interrupt based communication with the MCU. When asserted high, it means that the RX queue stores at least one frame.
- When **NSLAVE = 1** (Master configuration), this pin acts as digital input for the selection of **CPOL** (Clock POLarity):
  - CPOL = 0 (shorted to GND) implies that the clock inactive level (when NCS is high) is low.
  - CPOL = 1 (shorted to VDD) implies that the clock inactive level (when NCS is high) is high.

The internal pull-down is always enabled during **Trimming & Config Latch** and in **Normal state**.

The **BNE** output buffer is disabled if NSLAVE = 1 has been latched during **Trimming & Config Latch.** The **CPOL** input buffer is permanently enabled.

In case NSLAVE = 0 has been latched during **Trimming & Config Latch**, **BNE** output buffer is kept enabled while in **Normal state**. A short to GND/VDD detection is implemented to protect the **BNE** output buffer. If the value forced on the BNE output buffer differs from the one sampled by the CPOL input buffer for more than $T_{BNE\_SHORT\_DET}$, the BNE output buffer is put into HiZ. Automatic re-engagement of the BNE output buffer occurs upon next wakeup sequence (MCU needs to toggle DIS pin).

Figure 7. **BNE/CPOL pin structure**



3.2.1.6 *TXEN/CPHA*

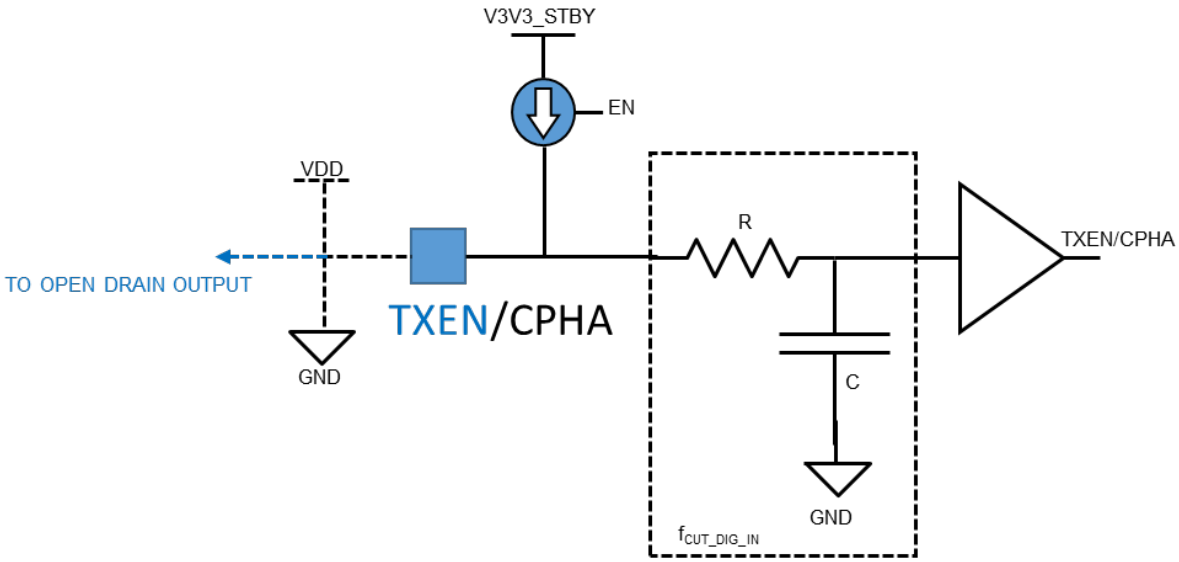
TXEN_CPHA is a digital input pin whose configuration depends on the value of NSLAVE latched during **Trimming & Config Latch**:

- When NSLAVE = 0 (Slave Configuration) the pin works as transmitter enable input **TXEN**:
  - MCU should release TXEN (or pull it up actively) prior to **NCS** assertion in order to enable the transmission of the data from **SDI** input buffer to the TX queue (and then to the isolated SPI interface).
    - In case the communication protocol does not feature any burst read capability, each command sent by the master unit will generate a single answer from the addressed slave unit. Hence TXEN pin can be connected to VDD in order to keep the transmitter permanently enabled.
  - In case of burst read operations, where user SW has to empty the RX queue without transmitting any frame on the isolated SPI, the TXEN input must be pulled down before beginning the burst read.
    - Even if data on the SDI line is discarded while TXEN = 0, it is highly recommended that MCU sends dummy frames (or intentionally corrupted frames) on the SDI line during the burst read. In the event of TXEN stuck high, such frames will generate errors according to the implemented communication protocol.
  - To avoid chopping frames currently being transmitted, the **TXEN** pin is latched upon **NCS** assertion. Therefore, it must be stable at least $T_{TXEN\_DEGLITCH}$ + T_{TXEN_SETUP} before NCS assertion. Moreover, TXEN must be kept stable T_{TXEN_HOLD} after NCS assertion in order to fulfil hold time constraints.

- When NSLAVE = 1 (Master configuration), this pin acts as digital input for the selection of **CPHA** (Clock PHAse). It is latched during **Trimming & Config Latch** and should be therefore either shorted to GND or to VDD:
  - CPHA = 0 (shorted to GND) implies that the SDI signal will be sampled upon the first SCK edge after NCS assertion.
  - CPHA = 1 (shorted to VDD) implies that the SDI signal will be sampled upon the second SCK edge after NCS assertion.

The internal pull-up is enabled when L99BM1T is in **Trimming & Config Latch** and is kept enabled in **Normal state** in order to allow a correct driving of the pin by the open-drain output of the MCU. Moreover, in case of pin loss, the pull-up guarantees a limp home operation where the transmitter is always enabled. To guarantee standby consumption requirements, the pull-up is disabled while in **Stand-by state**.

Figure 8. TXEN/CPHA pin structure



3.2.1.7 *TXAMP*

TXAMP pin can be used to switch between the two possible ISOline TX amplitude configurations:

- TXAMP = 0 selects low TX amplitude (RDIFF_ISO_OUTL)
- TXAMP = 1 selects high TX amplitude (RDIFF_ISO_OUTH)

TXAMP sampling depends on the device state and configuration:

Table 10. TXAMP sampling strategy

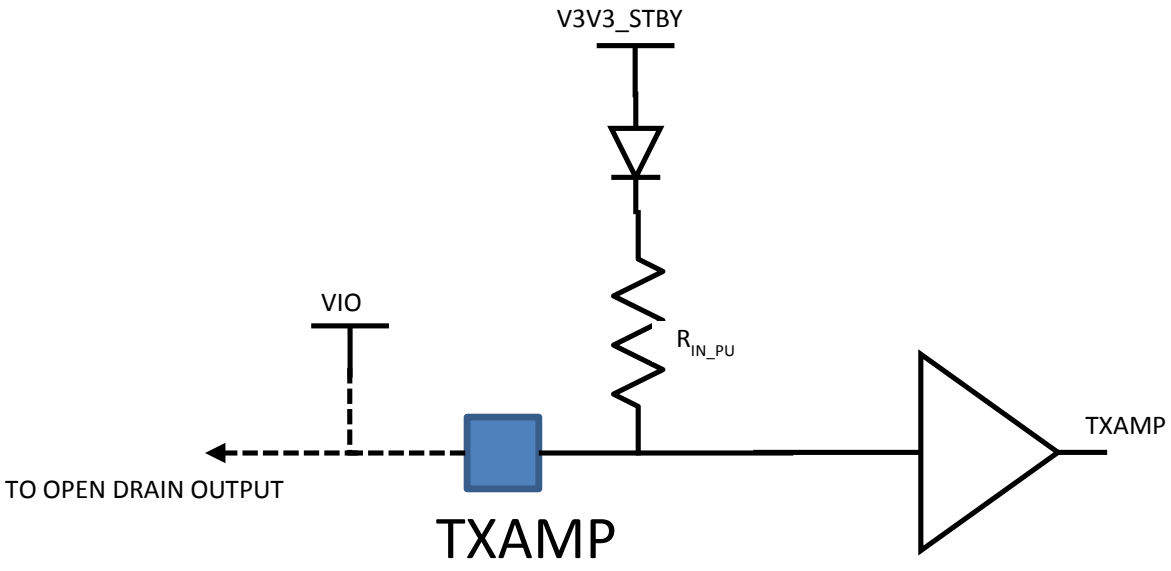
L99BM1T state	L99BM1T configuration	TXAMP sampling	Note
Normal state	Slave (NSLAVE = 0)	The **TXAMP** pin is latched upon **NCS** assertion. Therefore, it must be stable at least $T_{TXAMP\_DEGLITCH}$ + T_{TXAMP_SETUP} before NCS assertion. Moreover, TXAMP must be kept stable T_{TXAMP_HOLD} after NCS assertion in order to fulfil hold time constraints. The new amplitude setting is applied to the TX interface after the SPI frame has been completely transmitted over the isolated SPI interface. This allows **Managing ISOFREQ And TXAMP Pins For Communicating With L99BM114**.	In case several SPI frames are being pushed into the TX queue, the setting applied depends on the last one latched (no pipelining supported).
	Master (NSLAVE = 1)	The TXAMP setting is simply resynchronized (T_{TXAMP_SETUP} and T_{TXAMP_HOLD} requirements still apply) and deglitched ($T_{TXAMP\_DEGLITCH}$ filter still present), but it is not latched upon NCS assertion. The new amplitude setting is applied to the TX interface as soon as the transmission of the SPI frame over the isolated SPI interface begins.	

L99BM1T state	L99BM1T configuration	TXAMP sampling	Note
Stand-by state	Slave/Master (NSLAVE = X)	The new TXAMP setting is latched during the wakeup sequence. Hence, the TXAMP pin shall be stable T_{TXAMP_SETUP} before the DIS high → low transition is applied and shall not change during T_{WAKEUP}.	-
Reset state	Slave/Master (NSLAVE = X)	The initial TXAMP setting is latched during the first power up sequence. Hence, the TXAMP pin shall be stable before VDD is applied and shall not change during $T_{FIRST\_POWERUP}$.	-

It is recommended to apply the same TXAMP setting to all the devices communicating on the bus, in order to keep a constant SNR in every communication phase.

In order to meet standby consumption requirements, MCU must release the open drain output connected to **TXAMP** while L99BM1T is in **Stand-by state**.

Figure 9. TXAMP pin structure



3.2.1.8 *Electrical parameters - Digital I/O*

3.2.1.8.1 Digital input

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: 4.5 V ≤ V_{VDD} ≤ 5.5 V ; -40 °C < Tj < 125 °C

Table 11. Digital input electrical characteristics

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
V_{IN_L}	Logic input low voltage.	-	-	-	0.8	V
V_{IN_H}	Logic input high voltage.	-	1.8	-	-	V
V_{IN_HYS}	Input hysteresis.	Calculation $V_{IN\_H-VIN\_L}$	0.15	-	0.4	V
$f_{CUT\_DIG\_IN}$	Input Buffer RC filter. Applies to BNE_CPOL, NSLAVE, TXEN_CPHA, SPICLKFREQ, DIS.	Design info, not tested in ATE	0.7	-	1	MHz
T_{RC_DELAY}	Analog delay introduced by the $f_{CUT\_DIG\_IN}$ RC filter.	VIO = 3.3 V	-	-	700	ns
R_{IN_PD}	Input pull down resistor. Applies to SCK, SDI.	-	70	100	130	kΩ

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
R_{IN_PU}	Input pull up resistor. Applies to NCS, TXAMP, DIS.	-	70	100	130	kΩ
$T_{TXEN\_DEGLITCH}$	Up/Reset counter to avoid glitches on TXEN input. The counter counts up if TXEN is stable. The counter is reset upon a TXEN glitch (whatever slope). TXEN must be stable at least $T_{TXEN\_DEGLITCH}$ before the NCS assertion.	Guaranteed by SCAN	562.5	625	687.5	ns
T_{TXEN_HOLD}	TXEN hold time after the NCS assertion.		-	-	300	ns
$T_{TXAMP\_DEGLITCH}$	Up/Reset counter to avoid glitches on TXAMP input. The counter counts up if TXAMP is stable. The counter is reset upon a TXAMP glitch (whatever slope). TXAMP must be stable at least $T_{TXAMP\_DEGLITCH}$ + T_{TXAMP_SETUP} before the NCS assertion.		562.5	625	687.5	ns
T_{TXAMP_HOLD}	TXAMP hold time after the NCS assertion.		-	-	300	ns
$T_{ISOFREQ\_DEGLITCH}$	Up/Reset counter to avoid glitches on ISOFREQ input. The counter counts up if ISOFREQ is stable. The counter is reset upon a ISOFREQ glitch (whatever slope). ISOFREQ must be stable at least $T_{ISOFREQ\_DEGLITCH+TISOFREQ\_SETUP}$ before the NCS assertion.		562.5	625	687.5	ns
$T_{ISOFREQ\_HOLD}$	ISOFREQ hold time after the NCS assertion.		-	-	300	ns
I_{IN_PD}	Input pull down current. Applies to NSLAVE, ISOFREQ, BNE/CPOL.	V_{PIN} = 5 V	35	50	65	µA
I_{IN_PU}	Input pull up current. Applies to TXEN/CPHA.	V_{PIN} = 0 V	35	50	65	µA

3.2.1.8.2 Digital output

3.2.1.8.2.1 Output buffer

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: 4.5 V ≤ V_{VDD} ≤ 5.5 V ; -40 °C < Tj < 125 °C

Table 12. Output buffer electrical characteristics

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
V_{OUT_L}	Low output level.	I = 2 mA	0	-	0.4	V
V_{OUT_H}	High output level.	I = -2 mA	VIO-0.4	-	VIO	V
T_{OUT_trans}	Digital output Rise and Fall time. Not valid for SDO.	Cload = 12 0pF 20-80% on rising edge of DIG_OUT 80-20% on falling edge of DIG_OUT	5	-	400	ns
$T_{BNE\_SHORT\_DET}$	BNE output short detection filter time.	Guaranteed by SCAN	-	5	-	µs

3.2.1.8.2.2 Open drain (DIS)

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: 4.5 V ≤ V_{VDD} ≤ 5.5 V ; -40 °C < Tj < 125 °C

Table 13. Open drain electrical characteristics

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
VDISL	-	DIS output level when the pull down stage is ON I_{DIS} = 5 mA	-	-	0.4	V
I_{DIS_LIM}	-	DIS output current limitation for V_{DIS} = 5 V	8	-	18	mA
$T_{DIS\_PULLDOWN}$	Time interval after POR_MAIN when DIS pin is internally pulled-down, upon a wake up by VIF. Purpose is to trigger interrupt in the MCU or wake up on a PMIC.	Guaranteed by SCAN	-	800	-	ms
$T_{DIS\_DEGLITCH}$	Up/Reset counter to avoid positive glitches on DIS input when the L99BM1T is in Normal state. The counter counts up if DIS = 1, while it is reset if DIS = 0.	Guaranteed by SCAN	1	2	3	µs

3.2.2 Analog input

3.2.2.1 *SPICLKFREQ*

SPICLKFREQ pin is an analog input, compared to four thresholds by a set of analog comparators.

An external resistor R_{CLKPD} must be connected between SPICLKFREQ and GND, in order to generate a voltage $V_{SPICLKFREQ} = R_{CLKPD} * I_{SPICLKFREQPU}$.

The code obtained from these 4 comparators outputs (as indicated in the following table) is latched in the **Trimming & Config Latch** to determine the SPI Clock frequency when L99BM1T works in Master mode (**NSLAVE = 1**).

Figure 10. SPICLKFREQ thresholds

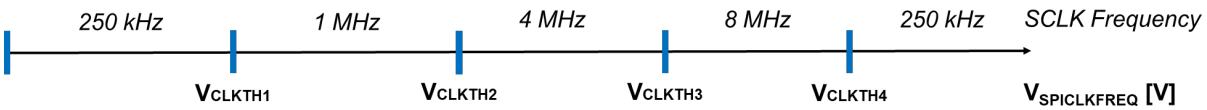


Table 14. SPICLKFREQ thresholds

$V_{SPICLKFREQ}$ [V] (typ.)	Vcode [3:0]	SCLK Frequency
$V_{SPICLKFREQ} \geq V_{CLKTH4}$	1111	250 kHz
Circuit malfunction	1110	250 kHz
	1101	250 kHz
	1100	250 kHz
	1011	250 kHz
	1010	250 kHz
	1001	250 kHz
	1000	250 kHz
$V_{CLKTH3} \leq V_{SPICLKFREQ} < V_{CLKTH4}$	0111	8 MHz
Circuit malfunction	0110	250 kHz
	0101	250 kHz

$V_{SPICLKFREQ}$ [V] (typ.)	Vcode [3:0]	SCLK Frequency
Circuit malfunction	0100	250 kHz
$V_{CLKTH2} \leq V_{SPICLKFREQ} < V_{CLKTH3}$	0011	4 MHz
Circuit malfunction	0010	250 kHz
$V_{CLKTH1} \leq V_{SPICLKFREQ} < V_{CLKTH2}$	0001	1 MHz
$V_{SPICLKFREQ} < V_{CLKTH1}$	0000	250 kHz

Refer to Table 15 for the recommended selection of the external pull down resistor.

Table 15. Recommended components for SPI clock frequency selection in master mode

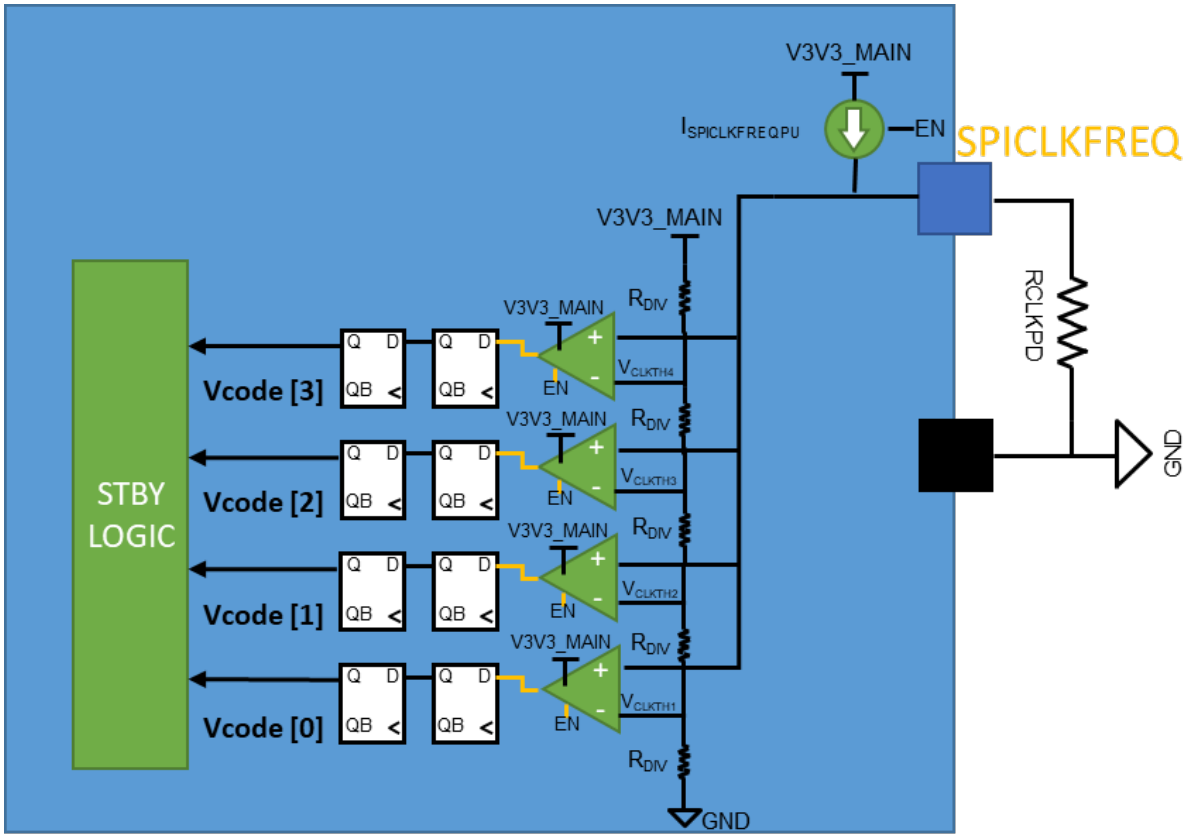
SCLK Frequency	Recommended $R_{SPICLKFREQ}$ [kΩ]	$R_{SPICLKFREQ}$ Tolerance [%]
250 kHz	Short to GND	-
1 MHz	9.31	10
4 MHz	16.2	5
8 MHz	22.9	1

The 4 analog comparators are BISTed during **Trimming & Config Latch** and, in case the BIST fails, the slowest SCLK configuration is chosen (250 kHz).

MCU is supposed to implement a communication timeout mechanism able to detect slower than normal communication bit rate.

The biasing current ISPICLKFREQPU, the comparators and voltage divider are disabled once **Trimming & Config Latch** is left, in order to avoid unnecessary power consumption.

Figure 11. **SPICLKFREQ pin structure**



3.2.2.2 *Electrical parameters - Analog input*

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: 4.5 V ≤ V_{VDD} ≤ 5.5 V ; -40 °C < Tj < 125 °C

Table 16. Analog input electrical characteristics

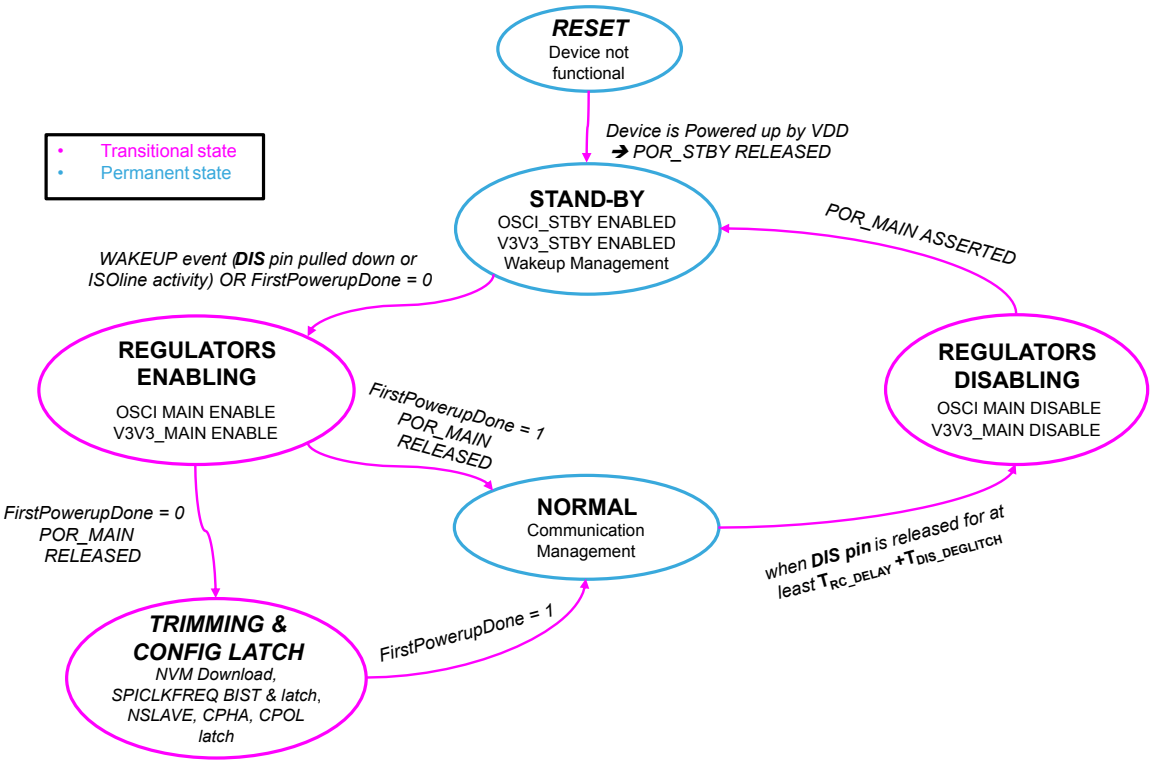
Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
V_{CLKTH4}	Input Voltage Thresold	Ramp on SPICLKFREQ	-2.5%	2.64	+2.5%	V
V_{CLKTH3}	Input Voltage Thresold	Ramp on SPICLKFREQ	-2.5%	1.98	+2.5%	V
V_{CLKTH2}	Input Voltage Thresold	Ramp on SPICLKFREQ	-3%	1.32	+3%	V
V_{CLKTH1}	Input Voltage Thresold	Ramp on SPICLKFREQ	-7%	0.66	+7%	V
$I_{SPICLKFREQPU}$	Bias current on SPICLKFREQ, active only in **Trimming & Config Latch**	0.75 V < $V_{SPICLKFREQ}$ < 2.5 V	-11%	100	+11%	µA

3.3 Device functional states

3.3.1 L99BM1T FSM

The following picture shows all L99BM1T possible states.

Figure 12. L99BM1T FSM



Different state transition sequences occur according to the following different scenarios:

1. ***First power up:*** **Reset state → Stand-by state → Regulators enabling state → Trimming & Config Latch → Normal state** (see Figure 13). The first power up sequence lasts $T_{FIRST\_POWERUP}$.
2. ***Wake up:*** **Stand-by state → Regulators enabling state → Normal state**. See Figure 14 for an example of the wake up sequence triggered by a frame received on the vertical interface. In case of wake up triggered by DIS release, the state transition is the same. The wake up sequence lasts T_{WAKEUP}.
3. ***Go To Sleep:*** **Normal state → Regulators disabling state → Stand-by state**. The go to sleep sequence lasts T_{GO2SLP}.

Figure 13. **First power up sequence**

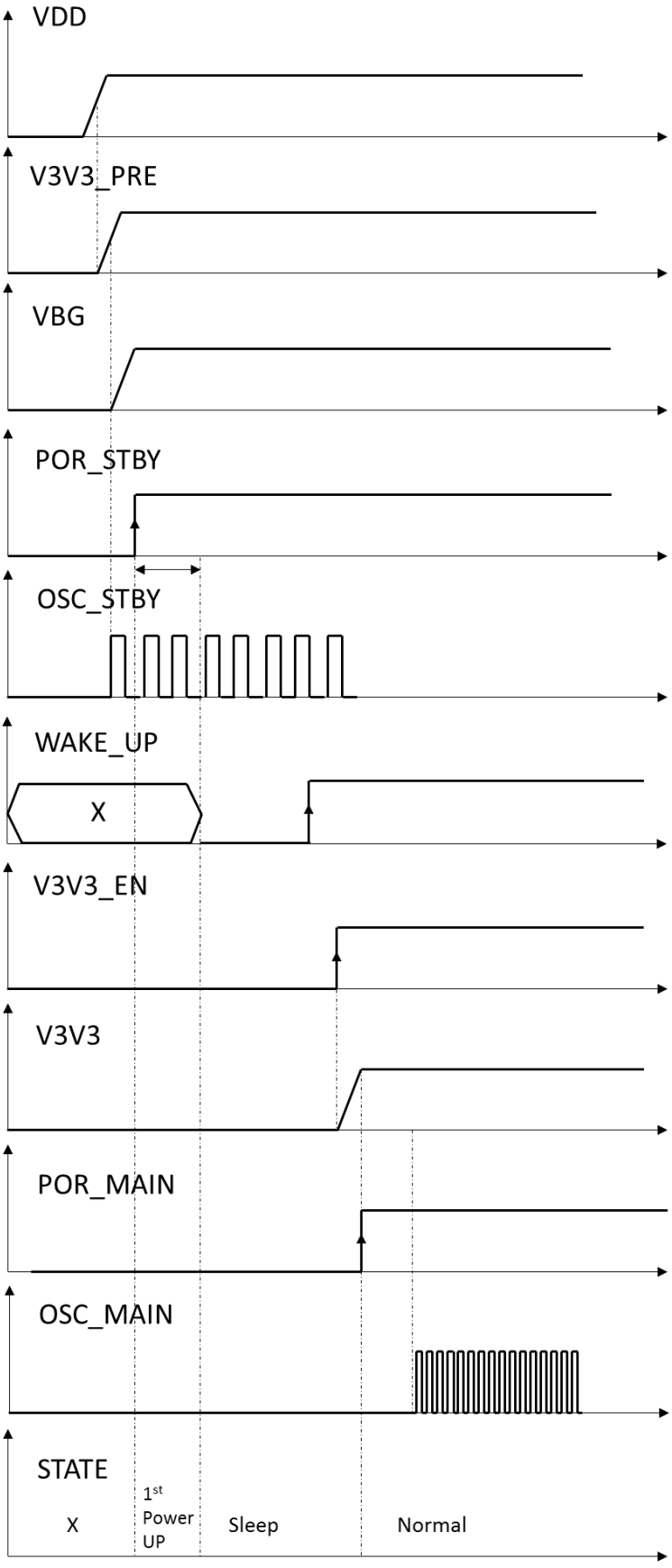
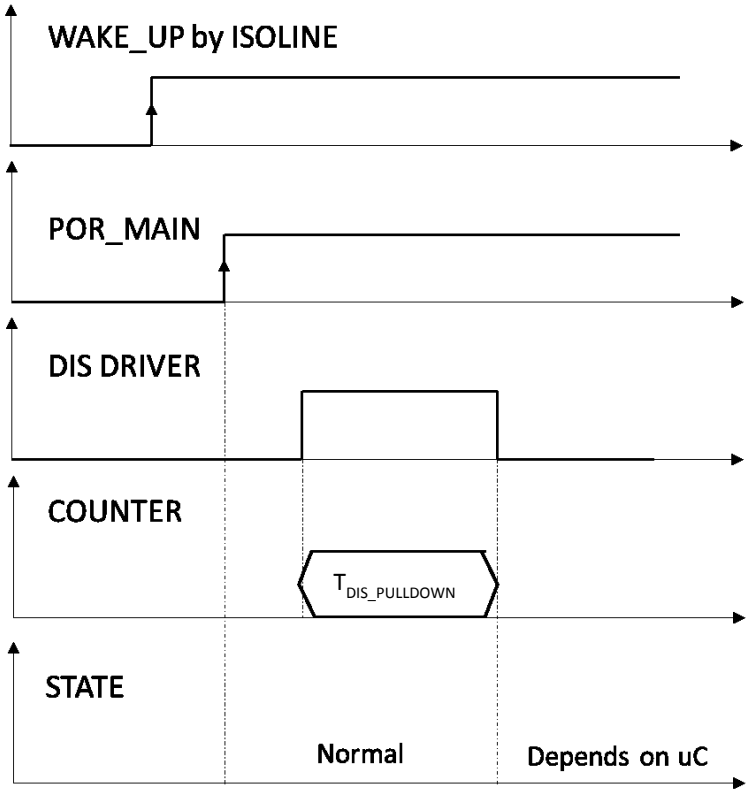


Figure 14. **Wake up sequence**



3.3.2 Reset state

When VDD is below the value triggering the power up, the device is not functional. No operation is possible while under reset.

3.3.3 Stand-by state

This state is entered either from **Reset state** or from **Regulators disabling state**:

- Transition from **Regulators disabling state** only occurs upon DIS low → high transition while L99BM1T is in **Normal state.** DIS input signal is filtered in both analog (T_{RC_DELAY}) and digital ($T_{DIS\_DEGLITCH}$) domains.
- Transition from **Reset state** only occurs upon first power up, after POR_STBY release.

While in standby, the logic checks the **FirstPowerupDone** latch, whose reset value is '0' upon first power up:

- In case **FirstPowerupDone = 0**, the first power up has never been accomplished. Hence, the device moves to **Regulators enabling state**, regardless of any wake up source state.
- In case **FirstPowerupDone = 1**, the first power up has already been accomplished. Hence, the device is kept in **Stand-by state** and eventual transitions are determined by the wake up sources.

When a wake up source is asserted, it triggers the wake up sequence that will move L99BM114 to **Regulators enabling state**. The possible wakeup sources are:

- The deassertion of **DIS** pin, pulled down by an external open drain source (T_{RC_DELAY} + (1/ f_{STBY_OSC}) filter applies).
- The detection of at least $N_{MIN\_ISO\_WUP\_EDGES}$ pulses within $T_{WAKEUP\_TIMEOUT\_ISO}$ on the ISOline.

3.3.4 Regulators enabling state

This is a transitional state reached from **Stand-by state**.

While L99BM1T is in this state, it enables the V3V3 regulator and the OSCI_MAIN.

During this process lasting T_{WAKEUP} the device must not be sensitive to **DIS** pin, SPI interface and ISOline sources.Once a wake up sequence is started, it cannot be interrupted.

The **Regulators enabling state** is left upon POR_MAIN release. Next state depends on **FirstPowerupDone** latch:

- In case **FirstPowerupDone = 0**, the first power up has never been accomplished. Hence, the device moves to**Trimming & Config Latch**.
- In case **FirstPowerupDone = 1**, the first power up has already been accomplished. Hence, the device moves to **Normal state**.

3.3.5 Trimming and config latch

This state is entered from the **Regulators enabling state** the first time the device is powered up (FirstPowerupDone = 0).

While in this state, the device must:

- Download the OTP data.
- Latch the configuration inputs (**NSLAVE**, **CPHA**, **CPOL**, **SPICLKFREQ**)storing them into the STBY logic registers according to Table 7.

SPICLKFREQ comes from a set of comparators that must be checked by an internal BIST before latching the comparator output. In case the BIST fails, a default 0 value (corresponding to the slowest SPI configuration) must be stored into the related stand-by internal register.

Stand-by registers hold their value as long as the POR_STBY stays deasserted.

While in this state, L99BM1T is not sensitive to SPI/VIF activity and wake up conditions (DIS/VIF).

This phase must safely go to an end and may last a maximum time interval of T_{SETUP_LATCH}.

After this phase has come to an end, the FirstPowerupDone latch is set to **"1"** in the standby logic and the device moves to **Normal state**.

3.3.6 Normal state

While in this state, all references and main logic are powered. Both communication interfaces are ready for data TX/RX activity.

This state is reached either from **Trimming & Config Latch** (first power up) or from **Regulators enabling state** (following a normal wake up sequence):

- When woken up by an activity on the ISOline, once **Normal state** is reached, the device must neglect the DIS pin value (even if it is high) and, on the contrary, it must drive the DIS pin low for $\mathbf{T_{DIS\_PULLDOWN}}$ (please note that DIS is an input/output pin). Such a strategy allows to generate an interrupt into the MCU, or to trigger a wake up into a PMIC device. Once $\mathbf{T_{DIS\_PULLDOWN}}$ expires, L99BM1T releases the DIS pull down and unmasks the DIS deglitched input. If the MCU or the PMIC have been correctly woken up, they will confirm their activity by pulling down the DIS pin externally, so that L99BM1T will be kept in **Normal state**. Otherwise, DIS will be found asserted (high) and the IC will move back to **Regulators disabling state**.
- When woken up by the DIS pin itself the device must start listening to the deglitched DIS pin as soon as it enters the **Normal state**.

To detect a "Go to Sleep" condition, the DIS pin status must be constantly monitored through a synchronous-deglitch filter ($\mathbf{T_{DIS\_DEGLITCH}}$, implemented in the main logic through the main oscillator).

Its effect is cascaded to the passive RC filter placed on the input comparator ($\mathbf{T_{RC\_DELAY}}$).

When DIS is sensed "high", the main logic raises a signal that triggers the “Go To Sleep” sequence in the IC FSM. L99BM1T moves to **Regulators disabling state** and finally to **Stand-by state**.

3.3.7 Regulators disabling state

This is a transitional state reached from **Normal state** during a "Go To Sleep" sequence.

While in this state, the V3V3_MAIN regulator and main oscillator enable signals are deasserted, leading to POR_MAIN assertion and reset of the main logic.

POR_MAIN assertion marks the transition to **Stand-by state**.

Even if the main logic is still alive while the device is in **Regulators disabling state**, it must not be sensitive to external pins (wake up sources, COM interfaces, etc.). Once started, a "Go To Sleep" sequence cannot be interrupted.

3.3.8 Electrical parameters - FSM

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: 4.5 V ≤ V_{VDD} ≤ 5.5 V ; -40 °C < Tj < 125 °C

Table 17. FSM electrical parameters

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
$T_{FIRST\_POWERUP}$	Time needed to perform first power up sequence (refer to L99BM1T FSM)	-	-	-	1.25	ms
T_{WAKEUP}	Time from wake up detection to ISOL-ISOP ready to transmit	-	-	-	1.06	ms
T_{GO2SLP}	Time needed to perform a power down sequence (refer to L99BM1T FSM)	-	-	-	400	µs
$N_{MIN\_ISO\_WUP\_EDGES}$	-	Guaranteed by SCAN	-	-	8	-
$T_{WAKEUP\_TIMEOUT\_ISO}$	Timeout of the pulse counter for wake up detection (isolated SPI)	Tested by SCAN	150	-	630	µs

3.4 Serial communication interface

L99BM1T integrates two communication interfaces:

- **SPI interface** can be used for the local data exchange with a master MCU (**NSLAVE = 0**) or with a generic slave IC (**NSLAVE = 1**). SPI electrical parameters are listed in Table 21.
- **Isolated SPI interface** can be used for global/local isolated communication with another L99BM1T or with an ISOLine compatible device (such as the L99BM114). ISOLine electrical parameters are listed in Section 3.4.4.1.1.1: Electrical parameters - ISO receiver and Section 3.4.4.1.2.1: Electrical parameters - ISO transmitter.

The throughputs on the 2 communication interfaces are different and not related. The two interfaces can work at the same time.

3.4.1 Frame input/output management

L99BM1T manages the asynchronicity and the different throughputs between SPI and ISOline (ISOline usually slower than SPI). It does it by buffering the incoming frames into queues then propagating them outside when possible.

Queues are managed according to their status (empty, not empty, full) and according to device I/Os.

L99BM1T mechanisms are frame-based but the device totally neglects frame's contents, thus not performing any protocol check.

The allowed frame length in terms of bits is not fixed, it can vary in the **$N_{BIT\_PER\_FRAME\_RANGE}$** range, on a frame by frame basis.

3.4.1.1 Input from ISOline interface

The device detects the end of an incoming frame if no valid bit has been received for at least **ISO_RX_EOF**. When the end of frame is detected, the frame is transferred into the RX queue as a single frame.

Being **ISO_TX_IF** greater than **ISO_RX_EOF**, a correct frame handling is guaranteed by design.

After the end of frame event, any new valid ISOLine bit must be considered as the first one of a new frame.

Any frame whose bit length is in the allowed **$N_{BIT\_PER\_FRAME\_RANGE}$** is stored into the RX queue.

The RX queue size is **MAX_RX_QUEUE_FRAME_NUMBER** frame. In case of FIFO full, any incoming frame replaces the last received one.

3.4.1.2 Input from SPI interface

When the device is configured as SPI Slave (**NSLAVE = 0**), it detects the start of frame sensing the assertion of NCS (chip select) and the end of frame sensing NCS deassertion.

In case the device is configured as SPI Master (**NSLAVE = 1**), L99BM1T directly manages the start/end of frame by driving NCS and SCK according to the SPI parameters in Table 21.

Between the start and end of frame events, the incoming synchronous bit on **SDI** pin are accepted and, if their number is in the allowed **NBIT_PER_FRAME_RANGE** range, the frame is stored into TX queue, provided that the **TXEN** pin is high. In case of FIFO full and TXEN pin high the incoming frame replaces the last received frame. In case the **TXEN** pin is latched low at the start of frame, the data incoming on SDI pin is discarded and not stored into the TX queue. This typically happens when the MCU is performing a burst read on the RX queue (e.g. after having issued a burst command to an L99BM114 device). The TX queue can contain up to **MAX_TX_QUEUE_FRAME_NUMBER** frames. Such frames can have different length (within the $N_{BIT\_PER\_FRAME\_RANGE}$). Frames with different length can be stored at the same time in the TX queue.

3.4.1.3 *Output to ISOline interface*

When the TX queue is not empty, the device transfers the frames not read yet towards the ISOline, following a FIFO approach.

The propagation of the queued frames is done as soon as the ISOline is sensed IDLE, meaning that the peripheral has finished transmitting previous frames from TX queue itself and it is not busy receiving frames from outside.

Frames transmitted towards the ISOline are separated with an inter-frame delay **ISO_TX_IF** depending on the frequency configuration:

- $8_{TBIT\_LENGTH\_FAST}$ (ISOFREQISOFREQ = 1)
- $4_{TBIT\_LENGTH\_SLOW}$ (ISOFREQ = 0)

Such an inter-frame delay is needed in order to guarantee a correct split between the different frames by the ISOline receiver on the other communication side.

3.4.1.4 *Output to SPI interface*

3.4.1.4.1 Output to SPI interface in case of Master transceiver (NSLAVE = 1)

When the RX queue is not empty L99BM1T asserts the NCS pin towards the external Slave device and starts sending out the RX queue content following a FIFO approach.

SCLK frequency has been latched while in **Trimming & Config Latch** and will not vary during device operation.

3.4.1.4.2 Output to SPI interface in case of Slave transceiver (NSLAVE = 0)

Whenever the RX queue is not empty (it contains at least a not-yet-read frame), the **BNE** pin must be set high in order to perform interrupt based communication with the Master MCU.

As soon as the MCU asserts the NCS, L99BM1T starts sending out the RX queue content following a FIFO approach. Each bit is sent synchronously with SCK provided by the MCU itself. The timings of SDO with respect to SCK and NCS must follow the electrical characteristics listed in Table 21. In case RX queue is empty (**BNE = 0**) and MCU still performs a read access, the SDO buffer is left in HiZ.

Values read by the MCU on its SDI pin depend on the external pull up/pull down resistor.

3.4.2 Communication parameters

Table 18. Communication parameters

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
$N_{BIT\_PER\_FRAME\_RANGE}$	Frame width	Design info	8	-	64	bit
MAX_TX_QUEUE_FRAME_NUMBER	TX queue size	Design info	-	-	3	frame
MAX_RX_QUEUE_FRAME_NUMBER	RX queue size	Design info	-	-	20	frame
ISO_IDLE	Minimum ISOline inactivity time, measured in respect to the last valid received bit. Marks the recognition of the IDLE state. Must be always greater than **ISO_TX_IF** to avoid TX conflicts.	ISOFREQ = 0 (Slow ISO)	11	13.75	16.5	µs
		ISOFREQ = 1 (Fast ISO)	3.4	4.25	5.1	

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
ISO_TX_IF	Interframe delay applied by L99BM1T to the transimission of two consecutive frames stored in the TXFIFO. Must be always greater than **ISO_RX_EOF** to allow correct EOF recognition by the L99BM1T receiver on the other side.	ISOFREQ = 0 (Slow ISO)	7.3	9.1	10.9	us
		ISOFREQ = 1 (Fast ISO)	2.25	2.8	3.36	
ISO_RX_EOF	Minimum inter-frame delay between two consecutive received frames. Marks the recognition of the EOF (End Of Frame).	ISOFREQ = 0 (Slow ISO)	4.8	6	7.2	us
		ISOFREQ = 1 (Fast ISO)	1.44	1.8	2.16	
$N_{MIN\_ISO\_WAKEUP\_EDGES}$	Minimum number of isolated SPI pulses that triggers a wake up.	Tested by SCAN	-	8	-	-

3.4.3 Serial Peripheral Interface (SPI)

The SPI pinout is listed in the following tables:

Table 19. L99BM1T Pin used as SPI

L99BM1T pin	SPI function	Configuration
SDI	Serial Data Input (SDI)	Digital Input
NCS	Chip Select (CS)	Digital Input. Active Low.
SCK	Serial Clock (SCK)	Digital Input.
SDO	Serial Data Out (SDO)	Digital Output

Table 20. SPI interface quick look

Parameter	Description
Single Frame Length	$N_{BIT\_PER\_FRAME\_RANGE}$
Max. Frequency	10 MHz (NSLAVE = 0), 8 MHz (NSLAVE = 1)
CPOL	'0' (NSLAVE = 0); CPOL (NSLAVE = 1)
CPHA	'1' (NSLAVE = 0); CPHA (NSLAVE = 1)
Master or Slave configuration	Slave (NSLAVE = 0); Master (NSLAVE = 1)

3.4.3.1 *Electrical parameters - SPI*

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: 4.5 V ≤ V_{VDD} ≤ 5.5 V ; -40 °C < Tj < 105 °C

Table 21. SPI electrical parameters

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit	Note
Parameters for L99BM1T SPI Slave (NSLAVE =0)							
F_{CLK_SPI}	CLK frequency (50% duty cycle)	Application info	-	-	10	MHz	-
T_{cll}	Minimum time CLK = LOW	Application info	42.5	-	-	ns	Allocating a 15% clock uncertainty to the SPI Master
T_{clh}	Minimum time CLK = HIGH	Application info	42.5	-	-	ns	Allocating a 15% clock uncertainty to the SPI Master
T_{pcld}	Propagation delay (time passed after propagating SCK edge @ at SDO active)	Cload = 60 pF Valid for SDO	-	-	30	ns	60% of ½ Tclk @ 10 MHz

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit	Note
T_{lead}	time passed after NCS H/L edge @ first SCK edge	Application info	100	-	-	ns	-
T_{scld}	SDI input setup time (time passed after SDI data valid @ sampling SCK edge)	Application info	10	-	-	ns	20% of ½ Tclk @ 10 MHz
T_{hcld}	SDI input hold time (time passed after propagating SCK edge @ SDI data “not valid anymore”)	Application info	10	-	-	ns	20% of ½ Tclk @ 10 MHz
T_{sclch}	Time passed after CLK -> CPOL @ NCS H/L edge	F_{CLK_SPI} = 10 MHz	75	-	-	ns	-
T_{lag}	Time passed after CLK -> CPOL @ NCS L/H edge	F_{CLK_SPI} = 10 MHz	100	-	-	ns	-
T_{hclch}	CLK high after NCS high	F_{CLK_SPI} = 10 MHz	100	-	-	ns	-
T_{onncs}	NCS min high time	F_{CLK_SPI} = 10 MHz	300	-	-	ns	> 4 T_{MAIN_OSC} max value (considering f_{MAIN_OSC} = 15 MHz)
T_{pchdz}	NCS L/H to SDO @ high impedance	F_{CLK_SPI} = 10 MHz Cload = 60 pF	-	-	75	ns	<<T_{onncs}
T_{csdv}	NCS H/L to SDO active	F_{CLK_SPI} = 10 MHz Cload = 60 pF	-	-	75	ns	-
Parameters for L99BM1T SPI Master (NSLAVE = 1)							
F_{CLK_SPI}	CLK frequency (50% duty cycle)	Design info	0.25	-	8	MHz	Selectable among 250 kHz, 1 MHz, 4 MHz, 8 MHz
T_{cll}	Minimum time CLK = LOW	F_{CLK_SPI} = 8 MHz	58.6	62.5	-	ns	Considering 6.25% internal clock uncertainty
		F_{CLK_SPI} = 4 MHz	117.2	125	-	ns	
		F_{CLK_SPI} = 1 MHz	468.8	500	-	ns	
		F_{CLK_SPI} = 250 kHz	1.88	2	-	µs	
T_{clh}	Minimum time CLK = HIGH	F_{CLK_SPI} = 8 MHz	58.6	62.5	-	ns	Considering 6.25% internal clock uncertainty
		F_{CLK_SPI} = 4 MHz	117.2	125	-	ns	
		F_{CLK_SPI} = 1 MHz	468.8	500	-	ns	
		F_{CLK_SPI} = 250 kHz	1.88	2	-	µs	
T_{pcld}	Propagation delay (time passed after propagating SCK edge @ at SDO active)	F_{CLK_SPI} = 10 MHz Cload = 60 pF	-	-	25	ns	50% of ½ Tclk @ 10MHz (Constrained by Slave spec)
TI_{lead}	CLK toggle after NCS = low	F_{CLK_SPI} = 8 MHz	1	-	1.51	µs	Less important when CPHA = 1 because the first SPI data bit is propagated by the first SCK edge after the NCS low
		F_{CLK_SPI} = 4 MHz	1	-	1.51	µs	
		F_{CLK_SPI} = 1 MHz	4	-	7.72	µs	
		F_{CLK_SPI} = 250 kHz	4	-	7.72	µs	
T_{scld}	SDI input setup time (time passed after SDI data valid @ sampling SCK edge)	F_{CLK_SPI} = 10 MHz	10	-	-	ns	20% of ½ Tclk @ 10 MHz (Constrained by Slave spec)
T_{hcld}	SDI input hold time (time passed after propagating SCK edge @ SDI data “not valid anymore”)	F_{CLK_SPI} = 10 MHz	10	-	-	ns	20% of ½ Tclk @ 10 MHz (Constrained by Slave spec)
T_{lag}	CLK toggle before NCS = high	F_{CLK_SPI} = 8 MHz	1	-	1.51	µs	-

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit	Note
T_{lag}	CLK toggle before NCS = high	F_{CLK_SPI} = 4 MHz	1	-	1.51	µs	-
		F_{CLK_SPI} = 1 MHz	4	-	7.72	µs	
		F_{CLK_SPI} = 250 kHz	4	-	7.72	µs	
T_{onncs}	CLK toggle before NCS = high	F_{CLK_SPI} = 8 MHz	1	-	1.44	µs	-
		F_{CLK_SPI} = 4 MHz	1	-	1.44	µs	
		F_{CLK_SPI} = 1 MHz	4	-	5.72	µs	
		F_{CLK_SPI} = 250 kHz	4	-	5.72	µs	
T_{pchdz}	NCS L/H to SDO high impedance	Cload = 30 pF Valid for SDO	-	-	75	ns	<< T_{onncs}
T_{csdv}	NCS H/L to SDO active	Cload = 30 pF Valid for SDO	-	-	75	ns	75% of T_{lead} important when CPHA=0

3.4.4 Isolated Serial Peripheral Interface

The Isolated SPI interface allows units with different ground levels and/or on different boards to communicate with each other. Physically the interface is based on twisted-pair wire.

The isolated SPI pinout is listed in the following tables:

Table 22. L99BM1T pins used as isolated SPI

L99BM1T Pin	SPI function	Configuration
ISOP	positive differential input/output	Analog Input/Output
ISOM	negative differential input/output	Analog Input/Output

Table 23. Isolated SPI quick look

Parameter	Description
Protocol	Half-Duplex / Out of frame
Max. Bit-rate	2.66 Mbps (high speed configuration, ISOFREQ = 1)
	333 kbps (low speed configuration, ISOFREQ = 0, default if pin is left floating)

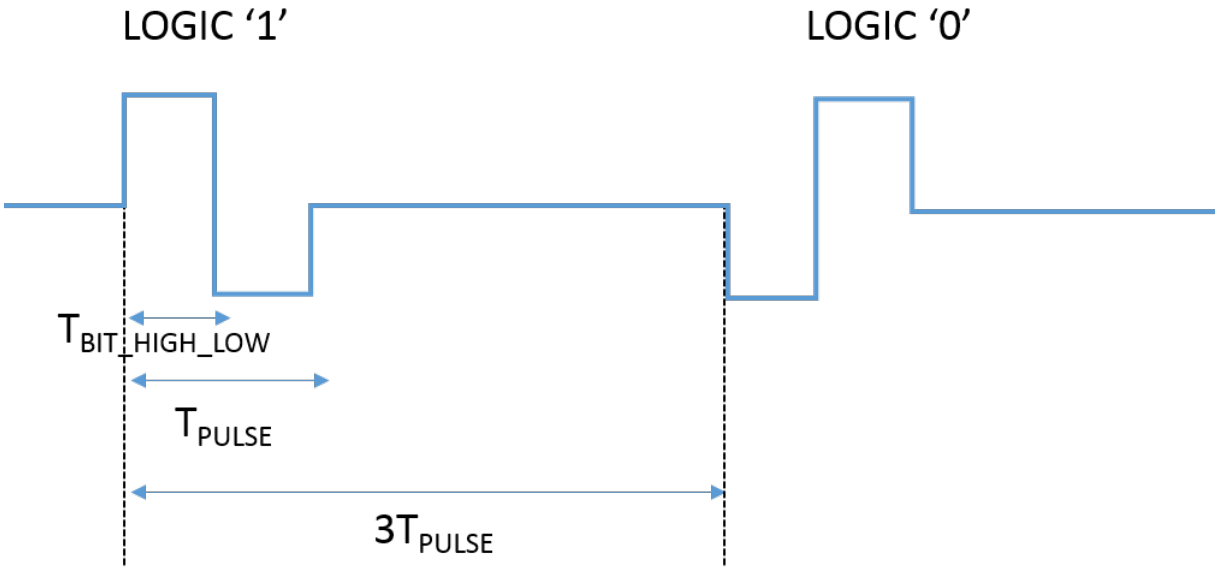
The transmission line on the isolated SPI exploits a single twisted pair. Communication data is transmitted/ received over a pulse-shaped signal, in a half-duplex protocol.

Line bit rate can be selected by programming the **ISOFREQ** device pin.

A single bit is made of a pulse time (T_{PULSE}) followed by two pause slices ($2T_{PULSE}$):

- $T_{PULSE} = 2T_{BIT\_HIGH\_LOW\_FAST}$ for the high speed configuration (ISOFREQ = 1)
- $T_{PULSE} = 2T_{BIT\_HIGH\_LOW\_SLOW}$ for the low speed configuration (ISOFREQ = 0)

Figure 15. **Isolated SPI pulse shape and logical meaning**



3.4.4.1 *ISO communicator receiver and transmitter*

An isolated receiver and transmitter are connected to the couple of pins and ISOP/M. Depending on the communication phase, they can be enabled or disabled.

3.4.4.1.1 ISO communicator receiver

The receiver is able to convert a differential input signal into a single ended signal that is provided to the logic:

- While in **Normal state**, in order to guarantee a correct communication, the input common mode must stand within VCM_ISO_IN limits.
- When in **Stand-by state**, the ISOP and ISOM pins are not biased with a common mode. If the device receives a series of differential pulses longer than **NMIN_ISO_WAKEUP_EDGES**, a wake up condition is triggered. Pulse amplitude must be higher than **Wakeup_thr** in order to be counted.

3.4.4.1.1.1 Electrical parameters - ISO receiver

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: 4.5 V ≤ V_{VDD} ≤ 5.5 V ; -40 °C < Tambient < 105 °C

Table 24. **Isolated receiver electrical parameters**

Symbol	Parameters	Test condition	Min	Typ	Max	Unit
$V_{DIFF\_ISO\_IN}$	Differential input voltage threshold	|V(ISOP) – V(ISOM)| $V_{CM\_ISO\_IN}$ = 0 V , $V_{CM\_ISO\_IN}$ = 1.4 V	180	250	320	mV
$V_{CM\_ISO\_IN}$	Input voltage common mode range	|V(ISOP) + V(ISOM)| /2 Design info	-	1.2	-	V
R_{ISO_DIFF}	Differential input resistance	VIF enabled, no communication Resistance measured between ISOP and ISOM pins	5	-	15	kΩ
R_{ISO_EXT}	External termination resistance connected between ISOxP and ISOxM pins	Application info	-	120	-	Ω
I_{ISO_LEAK}	ISO input leakage current	0V < ISOP/M, ISOP/M < VDD	-	-	5	µA
$T_{DET\_MIN\_WU}$	Minimum pulse duration to be detected	Design info	50	-	-	ns
Wakeup_thr	Wake up comparator threshold	|V(ISOP) – V(ISOM)| $V_{CM\_ISO\_IN}$ = 0 V , $V_{CM\_ISO\_IN}$ = 1.4 V	80	150	230	mV

3.4.4.1.2 ISO communicator transmitter

The transmitter is able to translate a single ended logic signal into a differential one output on the ISOP-ISOM pins. Bit symbols are shown in Figure 15.

Transmitter output impedance can be programmed via **TXAMP** pin among $R_{DIFF\_ISO\_OUTL}$ and $R_{DIFF\_ISO\_OUTH}$ values. It affects transmitted pulse amplitude, as described in **TXAMP**dedicated paragraph.

In order to work properly, the transmitter needs to be terminated with an **RISO_EXT** resistor connected between ISOP and ISOM pins. This allows generating differential signals with an amplitude suitable to be interpreted by the **ISO Communicator Receiver**.

3.4.4.1.2.1 Electrical parameters - ISO transmitter

All parameters are tested and guaranteed in the following conditions, unless otherwise specified: 4.5 V ≤ V_{VDD} ≤ 5.5 V ; -40 °C < Tambient < 105 °C

Table 25. Isolated transmitter electrical parameters

Symbol	Parameters	Test condition	Min	Typ	Max	Unit
$R_{DIFF\_ISO\_OUTL}$	Total output resistance: sum of pull up and pull down resistance contribution	Rpullup measured with $V_{CM\_ISO\_IN}$ = 1.5 V Rpulldown measured with $V_{CM\_ISO\_IN}$ = 0.9 V T_{XAMP} = 0	310	440	570	Ω
$R_{DIFF\_ISO\_OUTH}$		Rpullup measured with $V_{CM\_ISO\_IN}$ = 1.5 V Rpulldown measured with $V_{CM\_ISO\_IN}$ = 0.9 V T_{XAMP} = 0	170	244	310	Ω
$V_{CM\_ISO\_OUT}$	Output voltage common mode	|V(ISOP) + V(ISOM)|/2	1	-	1.4	V
$T_{BIT\_HIGH\_LOW\_FAST}$	High/low level bit duration into a whole period in case of high frequency configuration	Guarantee by SCAN	-	62.5	-	ns
$T_{BIT\_HIGH\_LOW\_SLOW}$	High/low level bit duration into a whole period in case of low frequency configuration	Guarantee by SCAN	-	500	-	ns
$T_{BIT\_LENGTH\_FAST}$	Bit duration with high frequency configured	Guarantee by SCAN	-	375	-	ns
$T_{BIT\_LENGTH\_SLOW}$	Bit duration with low frequency configured	Guarantee by SCAN	-	3	-	µs
F_{ISO_FAST}	Isolated Communication Rate	I_{SOFREQ} = 1 Application info	-	2.66	-	Mbps
F_{ISO_SLOW}	Isolated Communication Rate	I_{SOFREQ} = 0 Application info	-	333.3	-	Kbps

3.5 Diagnostic features

This paragraph lists all the diagnostics mechanisms implemented in the L99BM1T.

3.5.1 Bandgap monitor

Two BG references are used, to guarantee independency between monitor functions. In case a BG shifts in respect to the other, the device is kept under POR.

3.5.2 Main oscillator monitor

The oscillator used for the main logic functionalities and digital timings is monitored with a redundant oscillator that is electrically independent from the main one. Redundant oscillator is used just for safety purpose, in order to check a possible drift condition.

In case a failure is detected, communication is inhibited in both directions since ISOline and SPI blocks are kept disabled. If fault disappears, the device becomes fully functional again and any **BNE Short Detection** is reset, thus re-engaging the BNE output.

Table 26. **Main oscillator electrical parameters**

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
FAUX_OSC	Internal redundant Oscillator frequency		15	16	17	MHz
Freq_diff	Oscillator drift detection threshold	Guaranteed by design	+/-12	-	+/-22	%

3.5.3 BNE short detection

A short to GND/VDD detection is implemented to protect the **BNE** output buffer. If the value forced on the BNE output buffer differs from the one sampled by the CPOL input buffer for more than $T_{BNE\_SHORT\_DET}$, the BNE output buffer is put into HiZ.

Automatic re-engagement of the BNE output buffer occurs upon next **Stand-by state** to **Normal state** transition (MCU needs to toggle DIS pin).

3.5.4 SPICLKFREQ Comparator BIST

The analog comparators used for latching **SPICLKFREQ** value are BISTed during **Trimming & Config Latch**.

In case the BIST fails, the slowest SCLK configuration is chosen (250 kHz).

MCU is supposed to implement a communication timeout mechanism able to detect slower than normal communication bit rate.

4 Application information

4.1 ISO lines circuit - Transformer-Based insulation

The transformer-based insulation is recommended for global communication lines between different modules in a distributed BMS. It offers better insulation and higher immunity to BCI, being the transformer an intrinsic common mode filter.

Figure 16. Transformer-Based ISO lines circuit

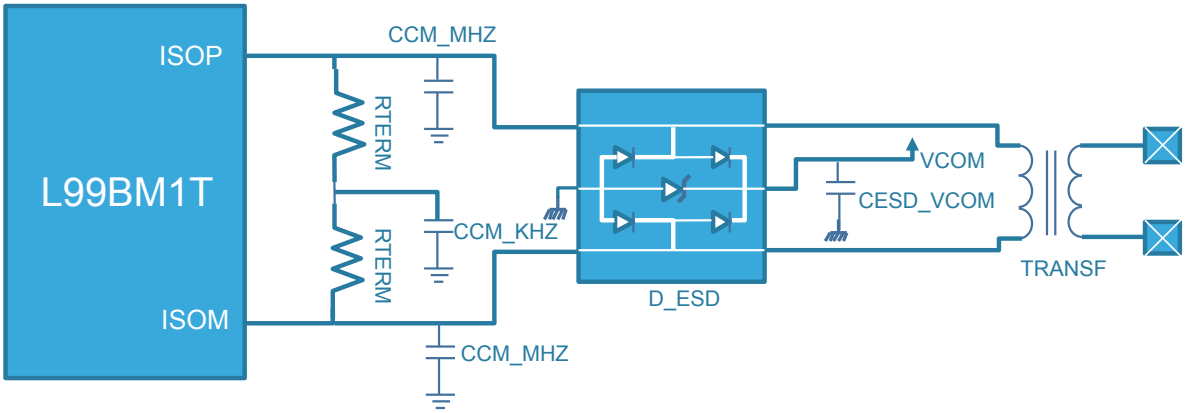


Table 27. Transformer-Based ISO lines BOM

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{TERM}	60	Ω	10%	1/16 W	Termination resistance. Differential output signal amplitude can be calculated with the following equation: $V_{ISO_{DIFF}} = V_{COM} \times \frac{R_{TERM}}{R_{DIFF\_ISO\_OUT}}$
C_{CM_KHZ}	6.8	nF	10%	10 V	Filter common mode noise in the kHz range (inverter and other power converters). Pole introduced is: $f_{cut\_khz} = \frac{1}{nC_{CM\_KHZ} \times \left(\frac{R_{ISODIFF}}{2} + R_{TERM} + 7.2k\Omega\right)}$ Do not exceed 10 nF, otherwise common mode settling time upon ISO port enable will last too long.
C_{CM_MHZ}	22	pF	10%	16 V	Filter common mode noise in the MHz range for improved BCI immunity. Pole introduced is: $f_{cut\_khz} = \frac{1}{2\pi C_{CM\_MHZ} \times R_{TERM}}$ Do not exceed 47 pF, otherwise differential output signal in high frequency mode might be strongly distorted.
C_{ESD_VCOM}	1	µF	10%	16 V	Deviate energy clamped by DESD directly to GND, preventing any ESD strike from affecting other PCB components. Total capacity on the VCOM pin must be equal to 2.2 µF. Hence, in BMS configuration, the recommended capacity distribution is: 1 µF as CESD_VCOM on the ISOH clamp, 1 µF as CESD_VCOM on the ISOL clamp, 200 nF as CVCOM directly on the VCOM pin.

Components	Value	Unit	Max. tolerance	Rating	Comments
D_{ESD}	-	-	-	-	The USBLC6-2SC6Y is the recommended ESD clamp device. It also protects the circuitry from spikes caused by a sudden short to battery on the global ISO lines. Care must be taken while routing the component on the PCB in order to minimize inductive spikes upon ESD strikes.
TRANSF	-	-	-	3.75 kV	The ESMIT-4180/A is recommended for isolated communication interface

4.2 ISO lines circuit – capacitive-based insulation

The capacitive-based insulation is recommended for local communication lines between different L99BM1T in a centralized BMS. It helps reducing the bill of material, while still guaranteeing common mode filtering between stacked devices.

Figure 17. Capacitive-based ISO lines circuit

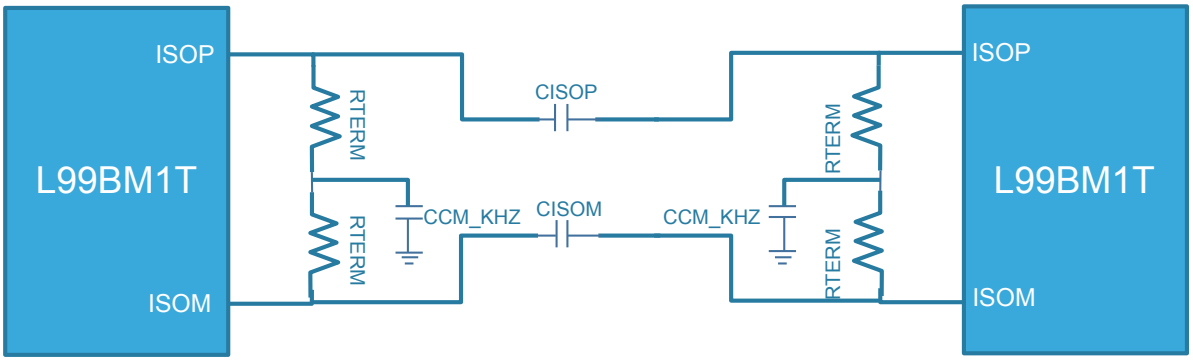


Table 28. Capacitive-based ISO lines BOM

Components	Value	Unit	Max. Tolerance	Rating	Comments
R_{TERM}	60	Ω	10%	1/16 W	Termination resistance. Differential output signal amplitude can be calculated with the following equation: $V_{ISO_{DIFF}} = V_{COM} \times \frac{R_{TERM}}{R_{DIFF\_ISO\_OUT}}$
C_{CM_KHZ}	6.8	nF	10%	10 V	Filter common mode noise in the kHz range (inverter and other power converters). Pole introduced is: $f_{cut\_khz} = \frac{1}{\pi C_{CM\_KHZ} \times \left(\frac{R_{ISO_{DIFF}}}{2} + T_{TERM} + 7.2\ k\Omega\right)}$ Do not exceed 10 nF, otherwise common mode settling time upon ISO port enable will last too long. Connect to AGND.
C_{ISOP}	47	nF	10%	100 V	Filters the common mode, while letting the differential mode pass. It acts as a high-pass filter with a cutoff frequency of: $f_{cut} = \frac{1}{2\pi\left[\left(\frac{R_{DIF\_ISO\_OUT}}{2} \parallel R_{TERMO}\right) + R_{TERM}\right] \times C_{ISOP}}$

Components	Value	Unit	Max. Tolerance	Rating	Comments
C_{ISOM}	47	nF	10%	100 V	Filters the common mode, while letting the differential mode pass. It acts as a high-pass filter with a cutoff frequency of: $f_{cut} = \frac{1}{2\pi\left[\left(\frac{R_{DIF\_ISO\_OUT}}{2} \parallel R_{TERMO}\right) + R_{TERM}\right] \times C_{ISOP}}$

4.3 Communication scenarios

The following section lists the different communication scenarios where L99BM1T can be exploited.

4.3.1 Dual access ring

The dual access ring topology allows for a higher communication integrity level, guaranteeing recovery upon single open failure on communication wires. It requires 2 SPI peripherals on the MCU, an additional transceiver unit and another transformer on the MASTER PCB.

Figure 18. Distributed BMS in dual access ring topology

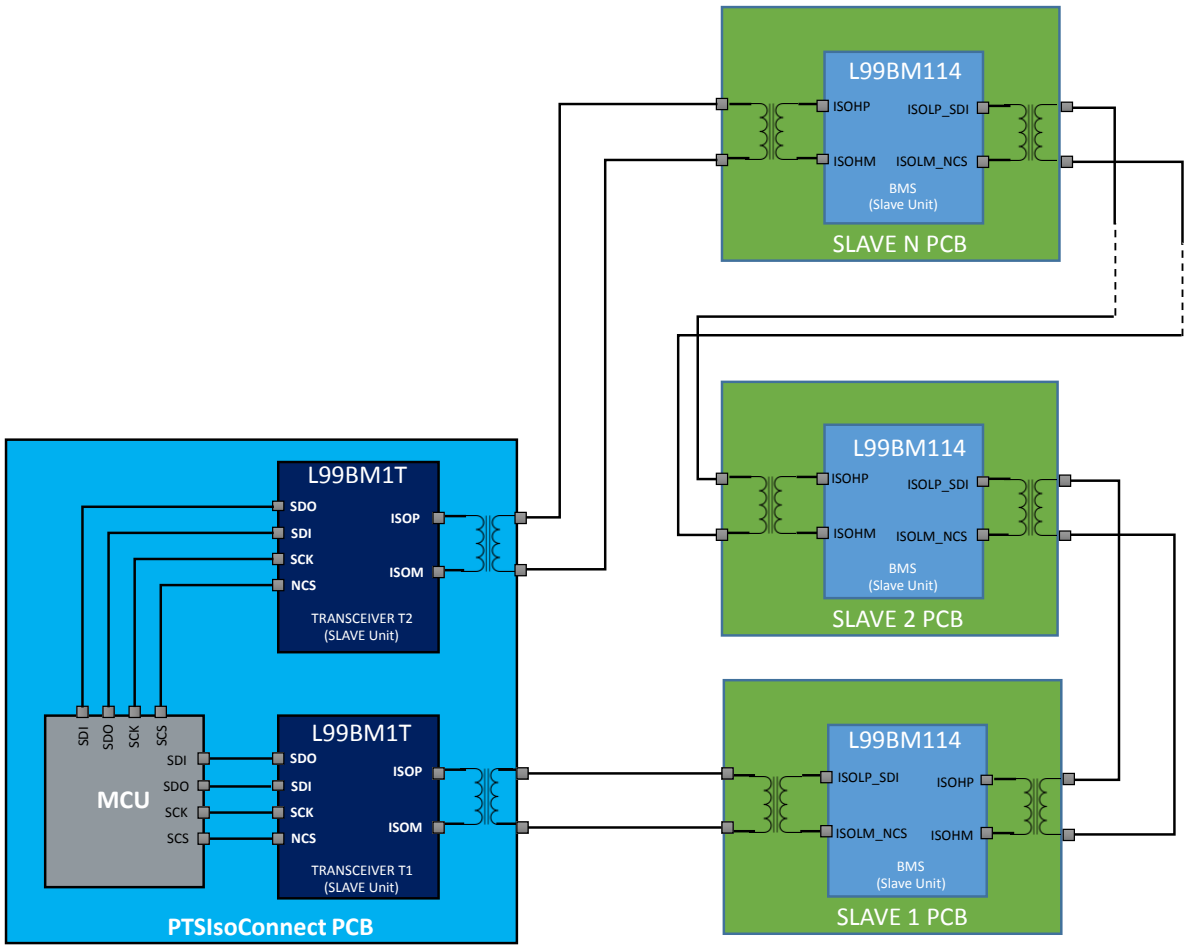
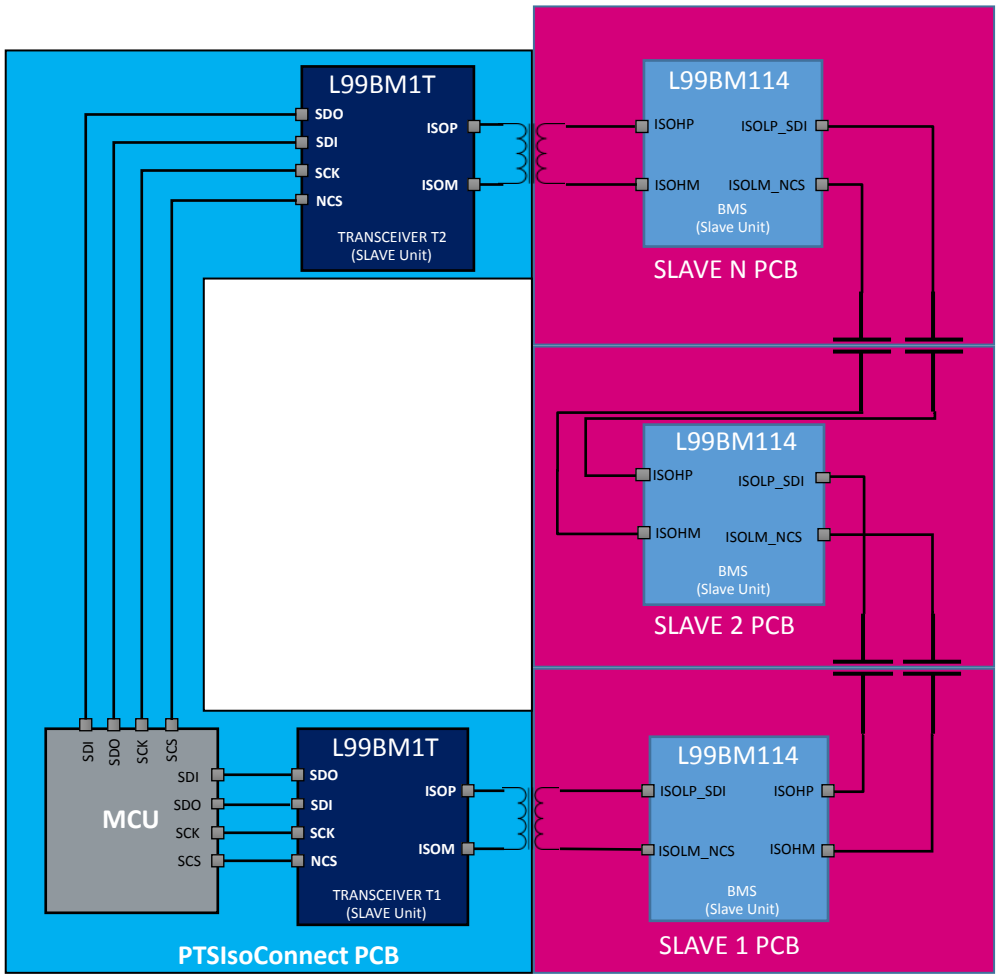


Figure 19. **Centralized BMS in dual access ring topology**

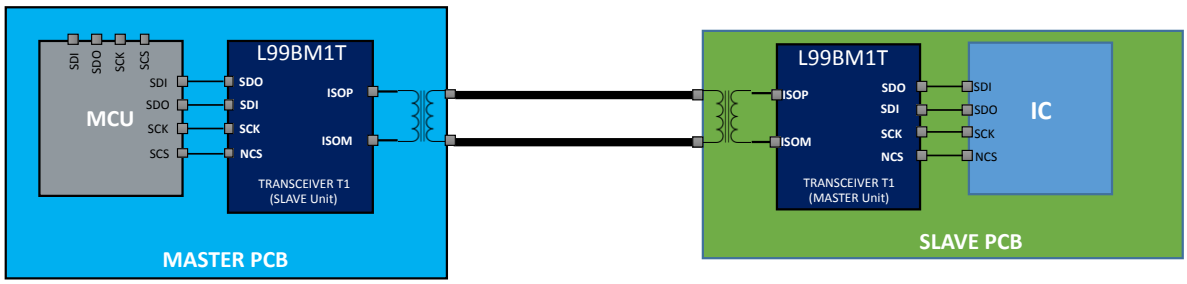


4.3.2 Generic application

Figure 20 represents a generic application scenario where a master MCU communicates with a generic slave IC located on a different PCB. Communication occurs via two L99BM1T:

- An L99BM1T configured as slave translates the SPI frames of the MCU to isolated SPI signals.
- The second L99BM1T on the right side is configured as SPI Master (NSLAVE = 1) pushing the frames to the slave IC, and sending the information backward.

Figure 20. **Generic application**



4.4 Managing ISOFREQ and TXAMP pin for communicating with L99BM1T

Both L99BM1T and L99BM114 feature the capability of communicating with different bit rate and amplitude settings. In order to avoid losing frames upon bit rate/amplitude switching, the following indications must be followed:

- To switch both devices from low to high frequency:
  1. Set ISOFREQ = 1
  2. Send the command programming L99BM114 **iso_freq_sel** bit to **0b11**. L99BM1T will send the frame in low frequency, but L99BM114 will answer back in high frequency. L99BM1T is already configured to receive answers in high frequency and no data will be lost.
- To switch both devices from high to low frequency:
  1. Set ISOFREQ = 0
  2. Send the command programming L99BM114 **iso_freq_sel** bit to **0b00**. L99BM1T will send the frame in high frequency, but L99BM114 will answer back in low frequency. L99BM1T is already configured to receive the answers in low frequency and no data will be lost.

Switching the amplitude alters the communication SNR. In principle, L99BM114 and L99BM1T could correctly communicate even if their amplitude settings are different. However, it is recommended to configure both devices with the same amplitude in order to reach a robust SNR.

- To switch both devices from low to high amplitude:
  1. Set TXAMP = 1
  2. Send the command programming L99BM114 **out_res_tx_iso** bit to **0b11**. L99BM1T will send the frame with low amplitude, but L99BM114 will answer back with high amplitude. L99BM1T is now configured to send frames with high amplitude.
- To switch both devices from high to low amplitude:
  1. Set TXAMP = 0
  2. Send the command programming L99BM114 **out_res_tx_iso** bit to **0b00**. L99BM1T will send the frame with high amplitude, but L99BM114 will answer back with low amplitude. L99BM1T is now configured to send frames with low amplitude.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SO16N (10x4x1.25 mm) package information

Figure 21. **SO16N (10x4x1.25 mm) package outline**

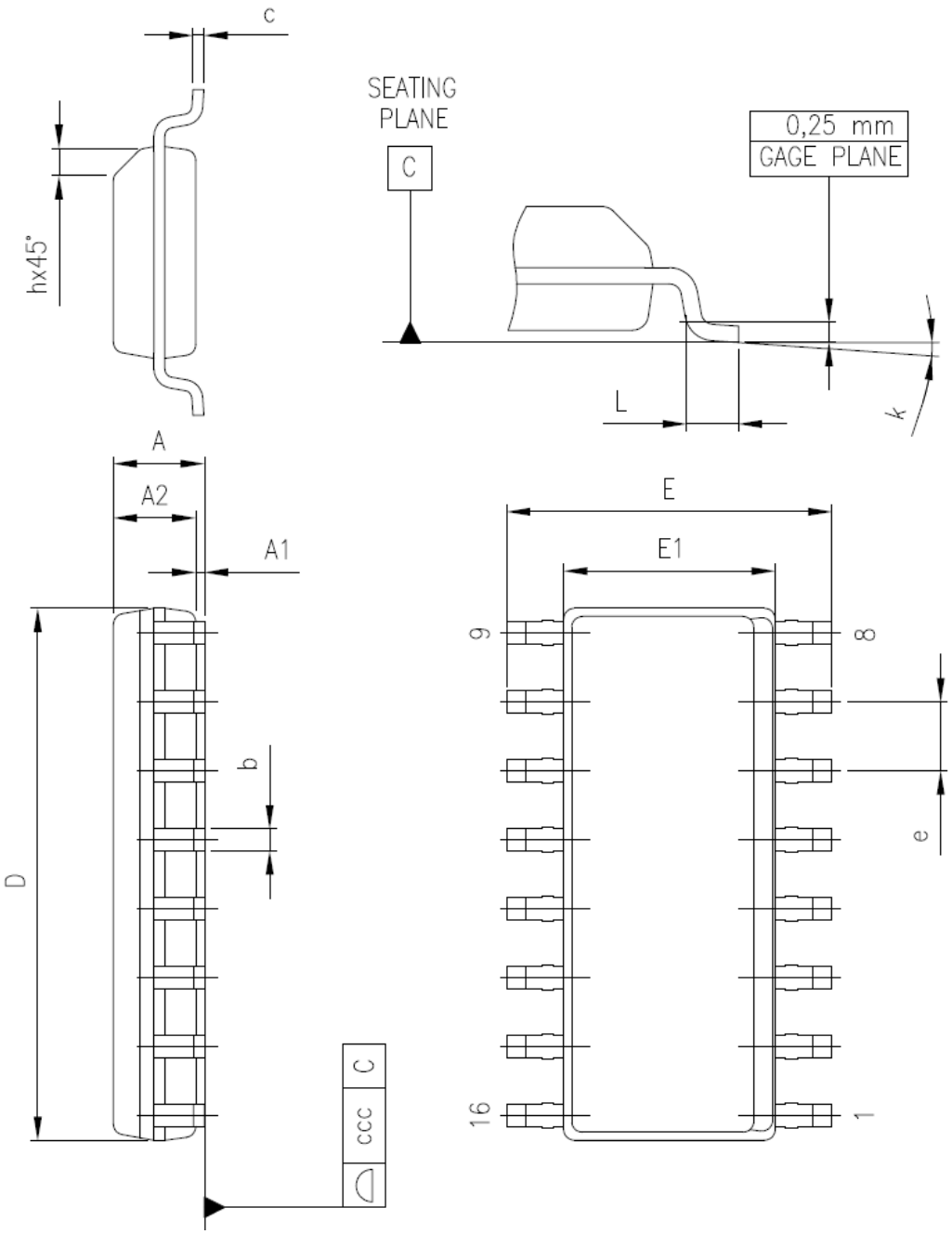
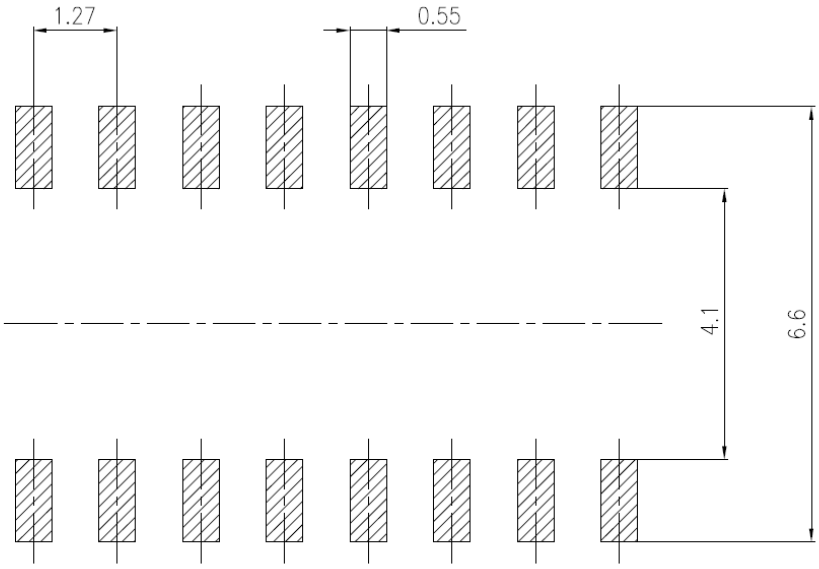


Table 29. **SO16N (10x4x1.25 mm) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D(1)(2)	9.80	9.90	10.00
E	5.80	6.00	6.20
E1(2)(3)	3.80	3.90	4.00
e	-	1.27	-
h	0.25	-	0.50
L	0.40	-	1.27
k	0	-	8
ccc	-	-	0.10

1. *Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).*
2. *Dimensions referred to the bottom side of the package.*
3. *Dimension "E1" does not include interlead flash or protrusions. Interlead flash, or protrusions or shall not exceed 0.25 mm per side.*

Figure 22. **Recommended footprint**



Parts marked as ES are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Revision history

Table 30. **Document revision history**

Date	Revision	Changes
01-Jul-2024	1	Initial release.

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