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MAX98380

Small, Boosted, Digital Input Class-D Amplifier

General Description

The MAX98380 is a small, mono Class-D audio amplifier featuring an integrated capacitive boost converter. The device implements a tripler charge pump-based boost converter that efficiently delivers up to 4.85W at 1% THD+N into an 8Ω load. The capacitive boost replaces the large and expensive inductor required for an inductive boost with smaller, lower-profile capacitors that reduce the total PCB solution.

Additionally, as the power-supply voltage varies due to declining battery life, an on-chip limiter (DHT) automatically optimizes the headroom available to the Class-D amplifier to maintain consistent distortion and listening levels.

Thermal-foldback protection ensures robust behavior when the thermal limits of the device are reached. When enabled, it automatically reduces the output power when the temperature exceeds a user-specified threshold. This allows for uninterrupted music playback even at high ambient temperatures. Traditional thermal protection is also available in addition to robust overcurrent protection.

The device provides a PCM interface for audio data and a standard I^2C interface for control data communication. The PCM interface supports audio playback using I^2S, left-justified, and TDM audio data formats. A unique clocking structure eliminates the need for an external master clock for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin count.

Active emissions-limiting and edge-rate limiting circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class-D devices and reduces the component count of the solution.

The IC is available in a 0.35mm pitch 24-bump wafer-level package (WLP). It is specified over the extended, -40°C to +85°C temperature range.

Applications

- Smartphones
- Smart Speakers
- IoT Devices
- Tablets

Benefits and Features

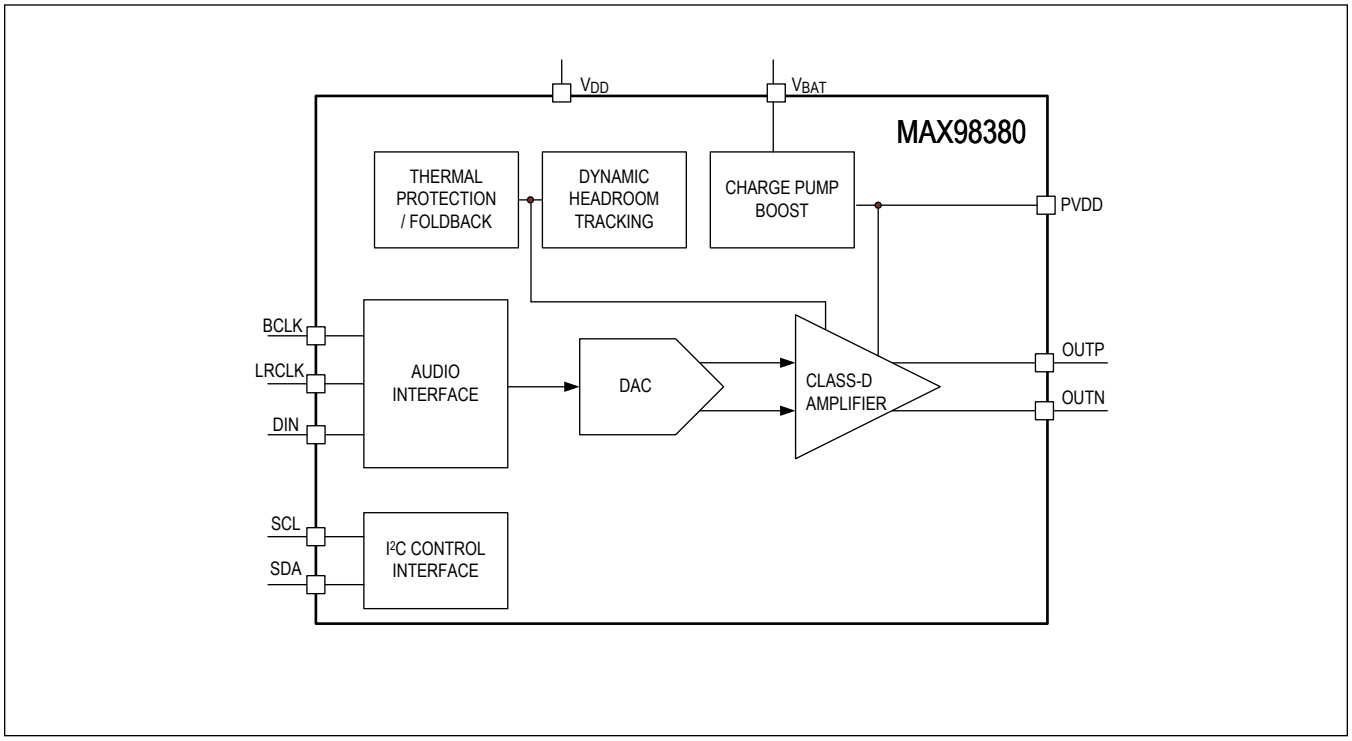
- Integrated Capacitive Boost Converter—No Bulky Inductors
- 3.6W Output Power into 6Ω at V_{BAT} = 3.7V
- 10mW Total Quiescent Power
- 3ms Turn-On Time
- 80% Efficiency (1.0W into R_L = 8Ω, V_{BAT} = 3.7V)
- 19.8μV_{RMS} Speaker Mode Output Noise
- 16.5μV_{RMS} Receiver Mode Output Noise
- Low 0.005% THD+N at 1kHz
- No MCLK Required
- Sample Rates of 8kHz to 192kHz
- Supports Left, Right, or (Left/2 + Right/2) Output in I^2S and Left-Justified Modes
- Sophisticated Edge Rate Control Enables Filterless Class-D Outputs
- Low RF Susceptibility Rejects TDMA Noise from GSM Radios
- Class-D Switching Frequency Trimmed to 10% for Better EMI Planning
- Extensive Click-and-Pop Reduction Circuitry
- Dynamic Headroom Tracking (DHT)
- Robust Short-Circuit and Thermal Protection
- Available in Space-Saving Package: 1.468mm x 2.138mm, 24-Bump WLP (0.35mm Pitch)

SMBus is a trademark of Intel Corp.

***Ordering Information** appears at end of data sheet.*

19-101484; Rev 0; 5/22

Simplified Block Diagram



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Absolute Maximum Ratings

V_{BAT} to PGND ..... -0.3V to +6V
V_{DD}, $\overline{RESET}$, ADDR, SCL, SDA, BCLK, LRCLK, and DIN to GND ..... -0.3V to +2.2V
PVDD to PGND ..... CPBYP - 0.3V to min(CPBYP + 6, 16)V
CPBYP to PGND ..... V_{BAT} - 0.3V to min(V_{BAT} + 6, 12)V
GND to PGND ..... -0.1V to +0.1V
Duration of OUTP or OUTN short circuit to PGND, PVDD, or V_{BAT} ..... Continuous
Duration of OUTP short to OUTN ..... Continuous
Continuous power dissipation (T_A = +70°C) WLP (derate 18.87mW/°C above +70°C) 1.51W
Junction temperature ..... +150°C
Operating temperature range ..... -40°C to +85°C
Storage temperature range ..... -65°C to +150°C
Soldering temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W241J2+1
Outline Number	21-100569
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	53°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM						
V_{BAT} Supply Voltage Operating Range	V_{BAT}	Guaranteed by PSRR test	3.0		5.5	V
V_{BAT} Supply Voltage	V_{BAT}	Device is functional but parametric performance is not guaranteed	2.5			V
V_{DD} Supply Voltage Range	V_{DD}	Guaranteed by PSRR test	1.71	1.8	1.89	V
V_{BAT} Undervoltage Lockout	V_{UVLO}	V_{BAT} rising	2.6		2.8	V
		V_{BAT} falling	2.3		2.5	
Quiescent Power	P_Q	T_A = +25°C, BST_BYPASS_MODE = 0		30		mW
		T_A = +25°C, BST_BYPASS_MODE = 1		10		

Electrical Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current	I_{Q_VBAT}	T_A = +25°C, V_{BAT}, BST_BYPASS_MODE = 0			7.2		mA
		T_A = +25°C, V_{BAT}, BST_BYPASS_MODE = 1			1.5		
	I_{Q_VDD}	T_A = +25°C, V_{DD}			2.8		
V_{BAT} Hardware Shutdown Current	$I_{VBAT\_HW\_SHDN}$	T_A = +25°C			0.3	1.0	µA
V_{DD} Hardware Shutdown Current	$I_{VDD\_HW\_SHDN}$	T_A = +25°C			0.1	1	µA
V_{BAT} Software Shutdown Current	$I_{VBAT\_SW\_SHDN}$	T_A = +25°C			0.3	1.0	µA
V_{DD} Software Shutdown Current	$I_{VDD\_SW\_SHDN}$	T_A = +25°C			1.4	2.5	µA
Turn-On Time	t_{ON}	Software Shutdown to full gain audio out, volume ramp disabled			2	3	ms
		Software Shutdown to full gain audio out, volume ramp enabled			5.5	6.5	
		From SPK_EN bit set to 1 to full operation, volume ramp disabled			0.75		
Turn-Off Time	t_{OFF}	From full operation to software shutdown ($\overline{RESET}$ = V_{DD}), volume ramp disabled			30	100	µs
		From full operation to software shutdown ($\overline{RESET}$ = V_{DD}), f_S ≤ 44.1kHz, volume ramp enabled			8.4	10.5	ms
		From full operation to software shutdown ($\overline{RESET}$ = V_{DD}), f_S > 44.1kHz, volume ramp enabled			6	6.5	
		From SPK_EN bit set to 0 to amplifier disabled, volume ramp disabled			0.025		ms
System Efficiency	η	f = 1kHz, Z_{SPK} = 6Ω + 33µH	P_{OUT} = 1.0W, BST_BYPASS_MODE = 0		80		%
			P_{OUT} = 1.0W, BST_BYPASS_MODE = 1		87		
		f = 1kHz, Z_{SPK} = 8Ω + 33µH	P_{OUT} = 1.0W, BST_BYPASS_MODE = 0		80		
			P_{OUT} = 0.8W, BST_BYPASS_MODE = 1		88		
CHARGE PUMP BOOST CONVERTER							
Maximum Soft-Start Time	t_{STR}	CP_SOFT_TIMER = 0x3, nominal caps (2x2.2µF/2x2.2µF)			1.725		ms

Electrical Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Startup Input Current Limit	$I_{STARTUP}$				0.5		A
Switching Frequency	f_{SW}			0.998	1.024	1.05	MHz
Output Voltage	V_{PVDD}	V_{BAT} = 3.0V to 4.5V, BST_BYPASS_MODE = 0			3 x V_{BAT}		V
		V_{BAT} > 4.5V, BST_BYPASS_MODE = 0			13.5		
		V_{BAT} = 3.0V to 5.5V, BST_BYPASS_MODE = 1			V_{BAT}		
Overvoltage Protection	OVP	Rising edge		15	15.5	16	V
		Falling edge		14.9	15.4	15.8	
CLASS-D AMPLIFIER							
Output Offset Voltage	V_{OS}	T_A = +25°C		-3.0	±0.3	+3.0	mV
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 6Ω + 33µH, into Standby or Shutdown			-66		dBV
		Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 6Ω + 33µH, out of Standby or Shutdown			-66		
V_{BAT} Supply Rejection DC	PSRR	T_A = +25°C, digital silence used for input signal, Z_{SPK} = ∞, DC, V_{VBAT} = 3.0V to 5.5V		63	80		dB
V_{BAT} Supply Rejection AC	PSRR	V_{RIPPLE} = 200mV_{PP}	f_{RIPPLE} = 217Hz, T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 6Ω + 33µH		75		dB
			f_{RIPPLE} = 1kHz, T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 6Ω + 33µH		75		
			f_{RIPPLE} = 10kHz, T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 6Ω + 33µH		75		
V_{DD} Supply Rejection DC	PSRR	T_A = +25°C, digital silence used for input signal, Z_{SPK} = ∞, DC, V_{DD} = 1.71V to 1.89V		60	83		dB

Electrical Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Supply Rejection AC	PSRR	V_{RIPPLE} = 200mV_{PP}	f_{RIPPLE} = 217Hz, T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 6Ω + 33µH		89		dB
			f_{RIPPLE} = 1kHz, T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 6Ω + 33µH		87		
			f_{RIPPLE} = 10kHz, T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 6Ω + 33µH		75		
Output Power	P_{OUT}	V_{BAT} = 3.7V, THD+N ≤ 10%, Z_{SPK} = 6Ω + 33µH	BST_BYPASS_MODE = 0		4.2		W
		V_{BAT} = 3.7V, THD+N ≤ 1%, Z_{SPK} = 6Ω + 33µH	BST_BYPASS_MODE = 0		3.6		
			BST_BYPASS_MODE = 1		0.88		
		V_{BAT} = 3.7V, THD+N ≤ 10%, Z_{SPK} = 6Ω + 33µH	BST_BYPASS_MODE = 1		1.1		
		V_{BAT} = 4.4V, THD+N ≤ 1%, Z_{SPK} = 8Ω + 33µH	BST_BYPASS_MODE = 0		4.85		
		V_{BAT} = 3.7V, THD+N ≤ 10%, Z_{SPK} = 8Ω + 33µH	BST_BYPASS_MODE = 0		4.1		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, T_A = +25°C	P_{OUT} = 1W, Z_{SPK} = 6Ω + 33µH, (Note 3)		-86		dB
			P_{OUT} = 1W, Z_{SPK} = 8Ω + 33µH		-85		
			P_{OUT} = 500mW, Z_{SPK} = 6Ω + 33µH, BST_BYPASS_MODE = 1		-85		
Intermodulation Distortion	IMD	ITU-R, 19kHz/20kHz, 1:1, V_{IN} = -3dBFS, Z_{SPK} = 8Ω + 33µH			-60		dB

Electrical Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	e_{Nd}	A-weighted, 24-bit or 32-bit data	BST_BYPASS_MODE = 0		19.8		μV_{RMS}
			BST_BYPASS_MODE = 1		16.5		
Dynamic Range	DR	A-weighted, -60dB 1kHz output signal, normalized to full scale (THD+N = 1%), 24- or 32-bit data T_A = +25°C	BST_BYPASS_MODE = 0		-108		dB
		A-weighted, -60dB 1kHz output signal, normalized to full scale (THD+N = 1%), 24- or 32-bit data, T_A = +25°C	BST_BYPASS_MODE = 1		-103		
Full-Scale Output Voltage	FS	BST_BYPASS_MODE = 0			13.4		dBV
		BST_BYPASS_MODE = 1			1.67		
Output Current Limit	I_{LIM}			2.7			A
Output Current Limit Auto-Restart Time					27		ms
Frequency Response				-0.2		+0.3	dB
Class-D Switching Frequency	f_{SW}			270	300	315	kHz
Spread-Spectrum Bandwidth	f_{SSM}				±14		kHz
Minimum Load Resistance	R_L				6		Ω
Maximum Device to Device Phase Error		Output phase shift between multiple devices from 20Hz to 20kHz across all sample rates and DAI operating modes			3		deg
DAC DIGITAL FILTER (LRCLK < 50kHz)							
Passband Cutoff	f_{PLP}	Ripple < δ_P		0.452 x f_S			Hz
		Droop < -3dB		0.457 x f_S			Hz
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}	Attenuation > δ_S				0.49 x f_S	Hz
Stopband Attenuation	δ_S	f > f_{SLP}		75			dB
Group Delay		f = 1kHz			5		samples

Electrical Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC DIGITAL FILTER (LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz	0.227 x f_S			Hz
		Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz	0.314 x f_S			Hz
	f_{PLP}	Ripple < δ_P, 176.4kHz ≤ f_S ≤ 192kHz	0.1135 x f_S			Hz
		Droop < -3dB cutoff, 176.4kHz ≤ f_S ≤ 192kHz	0.232 x f_S			Hz
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz	-0.25		+0.25	dB
Stopband Cutoff	f_{SLP}	Attenuation < δ_S			0.495 x f_S	Hz
Stopband Attenuation	δ_S	f > f_{SLP}	75			dB
Max Group Delay		f = 1kHz		5.5		samples
DAC DIGITAL FILTERS/DIGITAL DC BLOCKING FILTER						
DC Attenuation			80			dB
DC Blocking Filter -3dB Cutoff Frequency	f_C	For f_s = 8kHz, 16kHz, 32kHz, 48kHz, 96kHz, and 192kHz		1.872		Hz
		For f_s = 44.1kHz, 88.2kHz		1.72		
DIGITAL I/O / INPUT—DIN, BCLK, LRCLK						
Input Voltage High	V_{IH}		0.7 x V_{VDD}			V
Input Voltage Low	V_{IL}				0.3 x V_{VDD}	V
Input Leakage Current			-1		+1	µA
Input Hysteresis	V_{HYS}	Note 3	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
Internal Pulldown Resistance	R_{PD}	BCLK, LRCLK and DIN		3		MΩ
DIGITAL I/O / INPUT—$\overline{\text{RESET}}$						
Input Voltage High	V_{IH}		0.75 x V_{VDD}			V
Input Voltage Low	V_{IL}				0.25 x V_{VDD}	V
Input Leakage Current			-1		+1	µA
Input Hysteresis	V_{HYS}	Note 3	75			mV
Maximum Input Capacitance	C_{IN}			10		pF

Electrical Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O / INPUT—SCL, SDA, ADDR						
Input Voltage High	V_{IH}		0.7 x V_{VDD}			V
Input Voltage Low	V_{IL}				0.3 x V_{VDD}	V
Input Leakage Current		T_A = +25°C, input high	-1		+1	µA
Input Hysteresis	V_{HYS}	Note 3	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
DIGITAL I/O / OPEN DRAIN OUTPUT—SDA						
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Output High Leakage Current	I_{OH}	T_A = +25°C	-1		+1	µA
PCM AUDIO INTERFACE TIMING						
BCLK Frequency Range	f_{BCLK}	I²S/left-justified modes	0.256		12.288	MHz
		TDM mode	0.256		24.576	
BCLK Duty Cycle	DC		45		55	%
BCLK Period	t_{BCLK}	I²S/left-justified only	81.3			ns
		TDM mode	40			
Maximum BCLK Input Low-Frequency Jitter		Maximum allowable jitter before a -20dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter ≤ 40kHz		0.2		ns
Maximum BCLK Input High-Frequency Jitter		Maximum allowable jitter before a -60dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter > 40kHz		1		ns
PCM AUDIO INTERFACE TIMING / INTERFACE TIMING						
LRCLK to BCLK Active Edge Setup Time	$t_{SYNCSET}$		4			ns
LRCLK to BCLK Active Edge Hold Time	$t_{SYNCHOLD}$		4			ns
DIN to BCLK Active Edge Setup Time	t_{SETUP}		4			ns
DIN to BCLK Active Edge Hold Time	t_{HOLD}		4			ns
DIN Frame Delay After LRCLK Edge		Measured in number of BCLK cycles, set by selected TDM mode	0		2	cycles
I²C INTERFACE TIMING						
Serial Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5			µs

Electrical Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.26			µs
Data Hold Time	$t_{HD,DAT}$		0		450	ns
Data Setup Time	$t_{SU,DAT}$		50			ns
SDA and SCL Receiving Rise Time	t_R		20		120	ns
SDA and SCL Receiving Fall Time	t_F		20 x V_{DD}/5.5 V		120	ns
SDA Transmitting Fall Time	t_F		20 x V_{DD}/5.5 V		120	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.26			µs
Bus Capacitance	C_B				550	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
THERMAL PROTECTION						
Thermal Shutdown Trigger Point		THERMSHDN_THRESH = 0x64	140	150	160	°C
$\overline{\text{RESET}}$ TIMING						
$\overline{\text{RESET}}$ Low	t_{RESET_LOW}	Minimum low time for $\overline{\text{RESET}}$ to ensure device enters hardware shutdown		7.5		µs
Release from $\overline{\text{RESET}}$	$t_{I^2C\_READY}$	Time from $\overline{\text{RESET}}$ = 1 to I^2C communication available (software shutdown)			1.5	ms

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

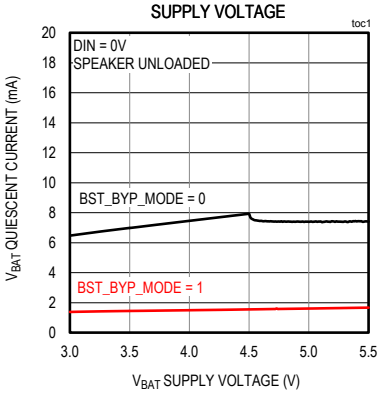
Note 2: See the *Digital Audio Interface Configuration* and *Valid Clock Frequencies* sections for more information.

Note 3: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

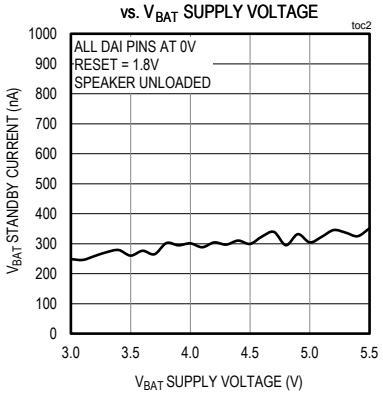
Typical Operating Characteristics

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

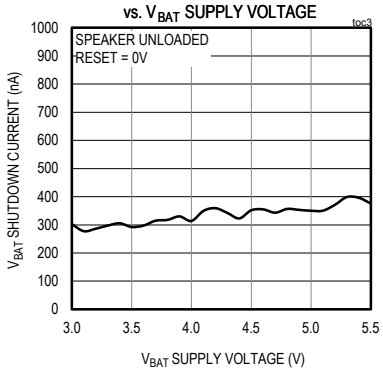
V_{BAT} QUIESCENT CURRENT vs. V_{BAT} SUPPLY VOLTAGE



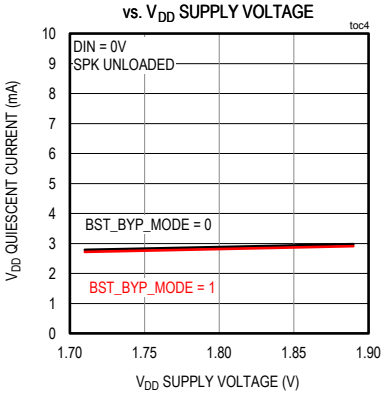
V_{BAT} STANDBY CURRENT vs. V_{BAT} SUPPLY VOLTAGE



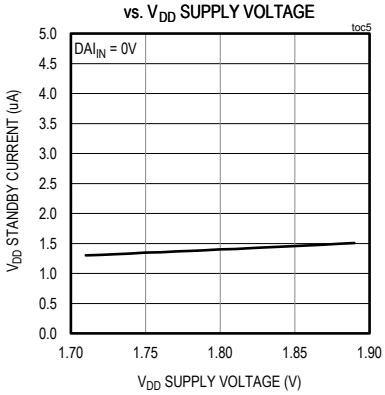
V_{BAT} SHUTDOWN CURRENT vs. V_{BAT} SUPPLY VOLTAGE



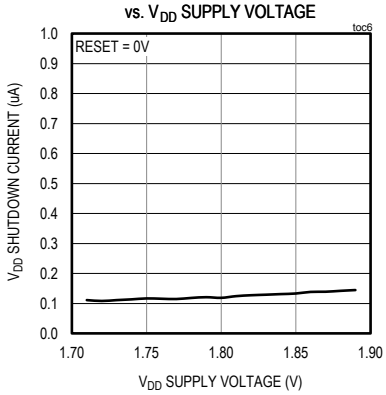
V_{DD} QUEISCENT CURRENT vs. V_{DD} SUPPLY VOLTAGE



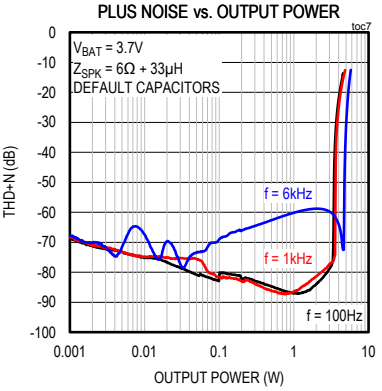
V_{DD} STANDBY CURRENT vs. V_{DD} SUPPLY VOLTAGE



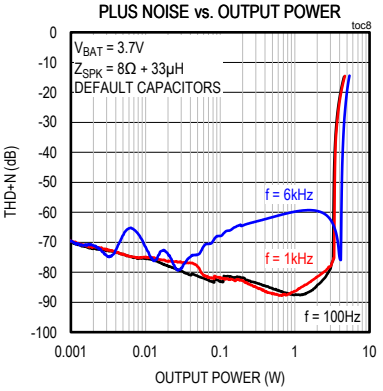
V_{DD} SHUTDOWN CURRENT vs. V_{DD} SUPPLY VOLTAGE



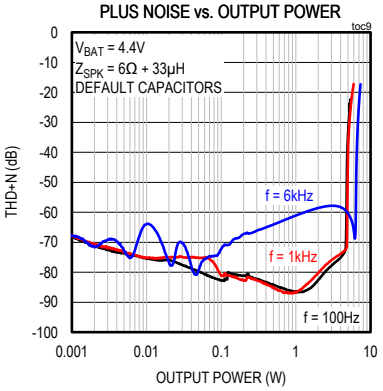
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



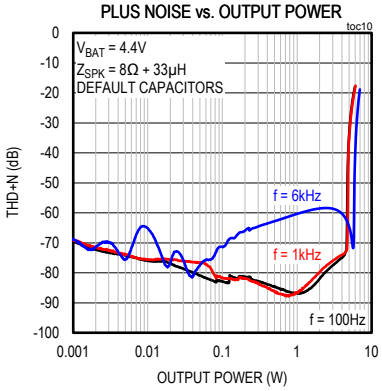
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



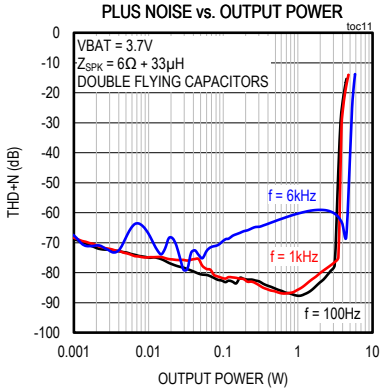
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

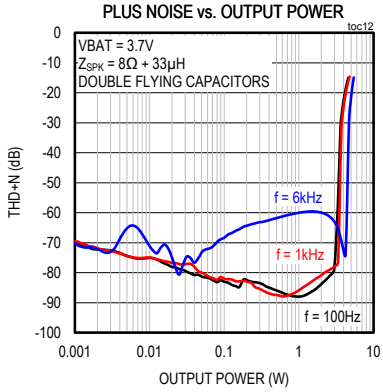
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



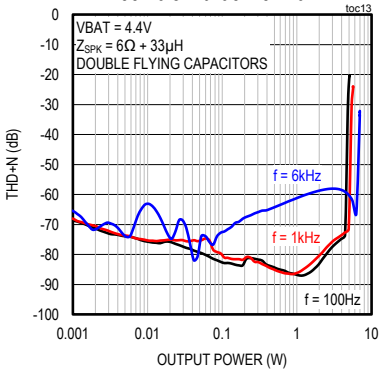
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



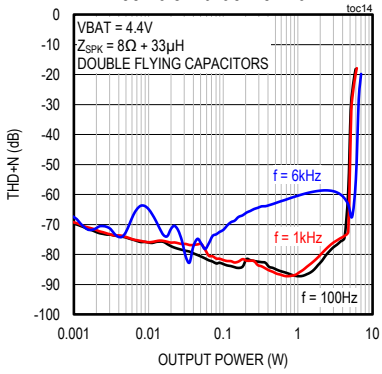
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



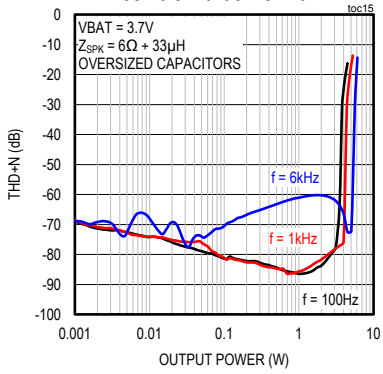
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



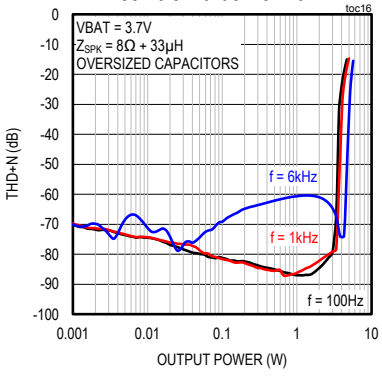
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



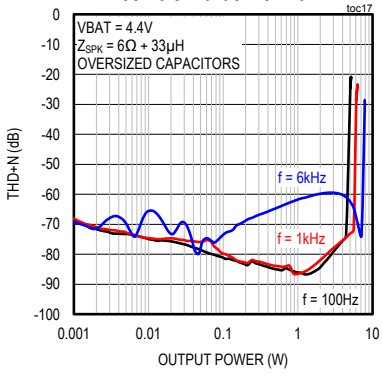
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



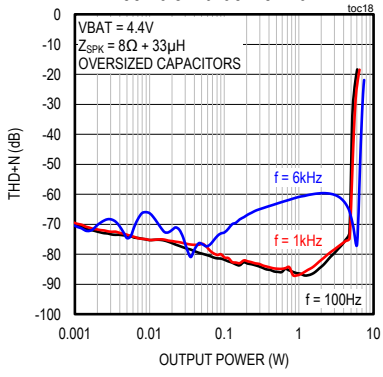
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



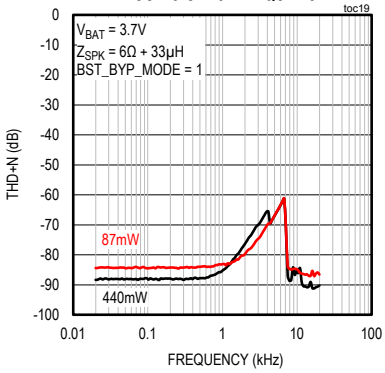
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



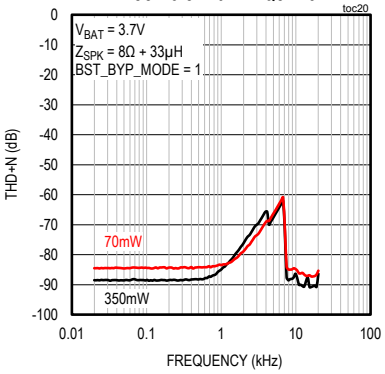
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

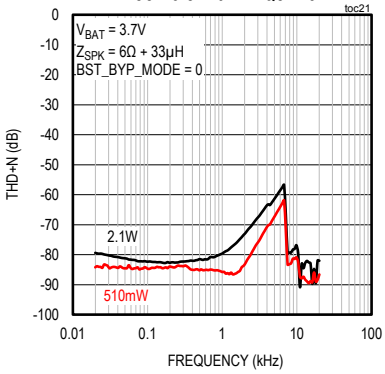
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



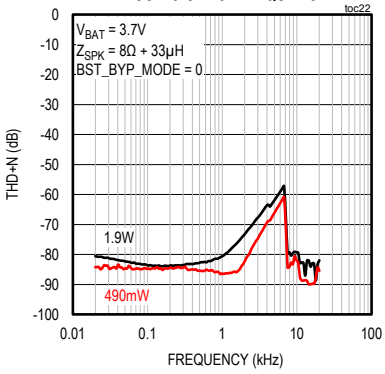
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



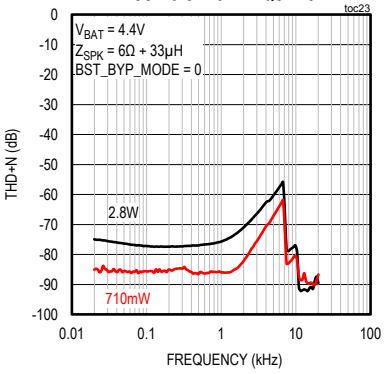
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



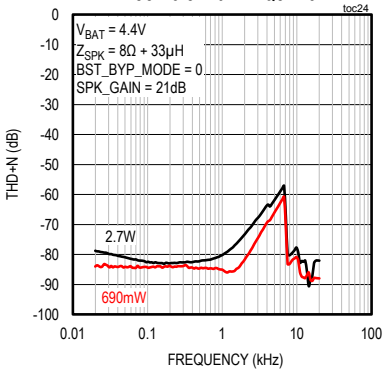
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



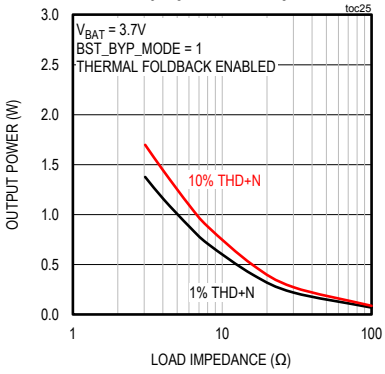
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



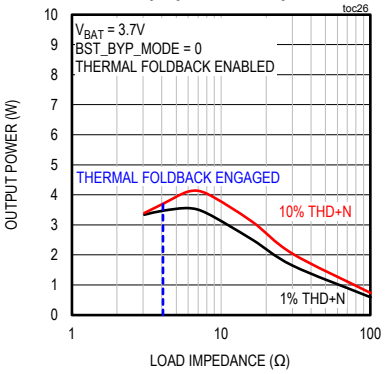
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



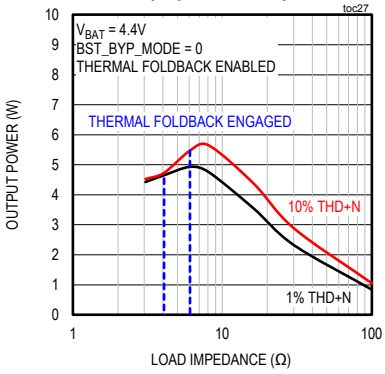
OUTPUT POWER vs. LOAD IMPEDANCE



OUTPUT POWER vs. LOAD IMPEDANCE



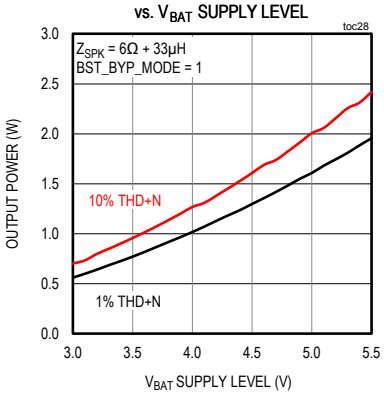
OUTPUT POWER vs. LOAD IMPEDANCE



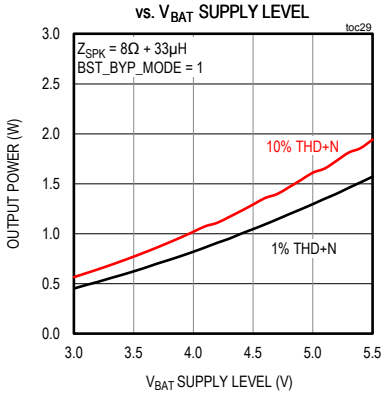
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

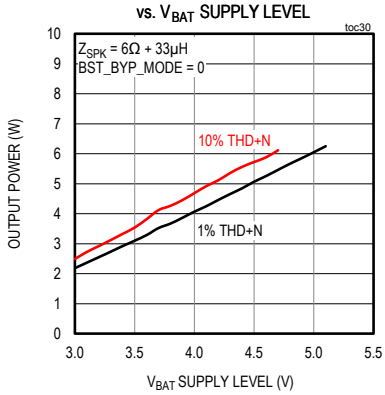
OUTPUT POWER vs. V_{BAT} SUPPLY LEVEL



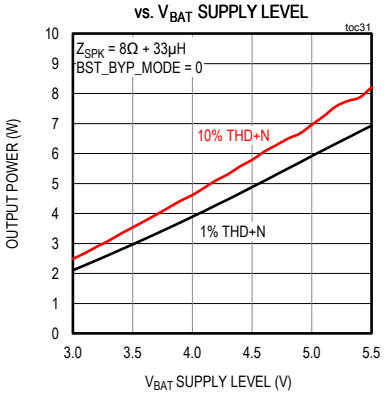
OUTPUT POWER vs. V_{BAT} SUPPLY LEVEL



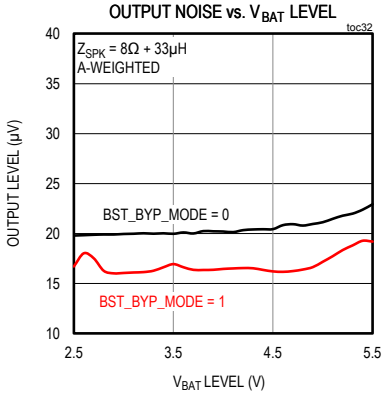
OUTPUT POWER vs. V_{BAT} SUPPLY LEVEL



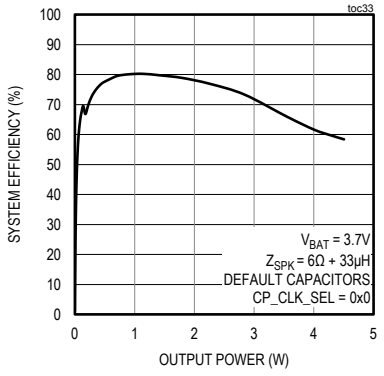
OUTPUT POWER vs. V_{BAT} SUPPLY LEVEL



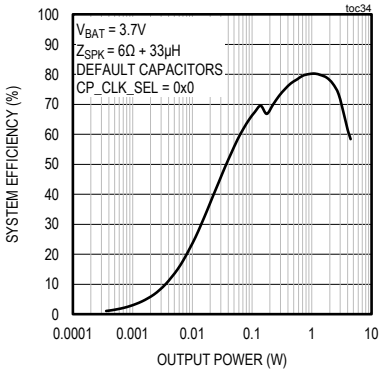
OUTPUT NOISE vs. V_{BAT} LEVEL



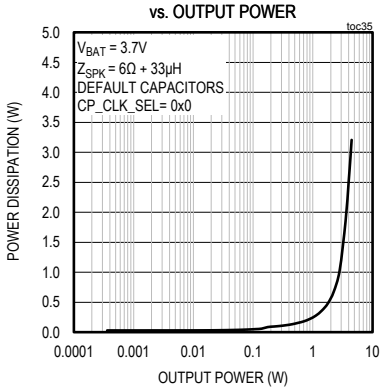
EFFICIENCY vs. OUTPUT POWER



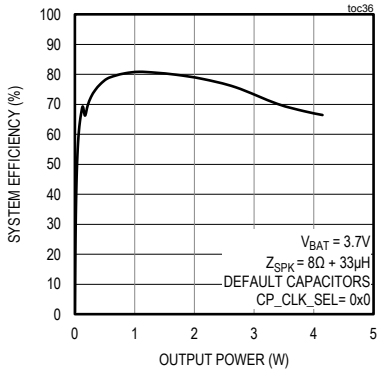
EFFICIENCY vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



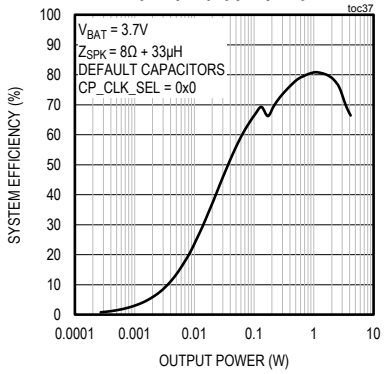
EFFICIENCY vs. OUTPUT POWER



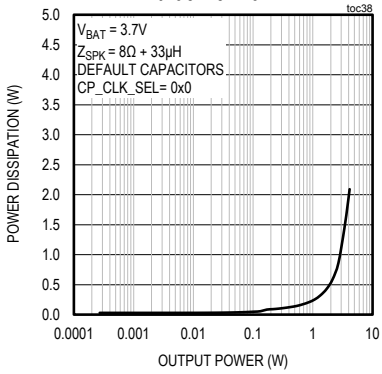
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

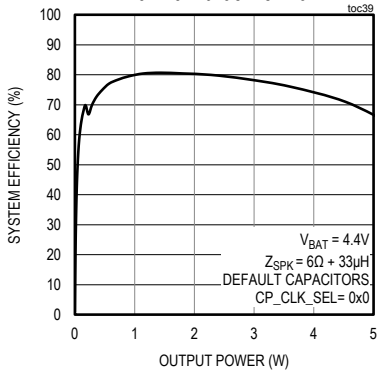
EFFICIENCY vs. OUTPUT POWER



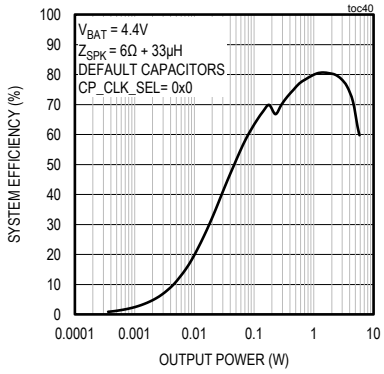
POWER DISSIPATION vs. OUTPUT POWER



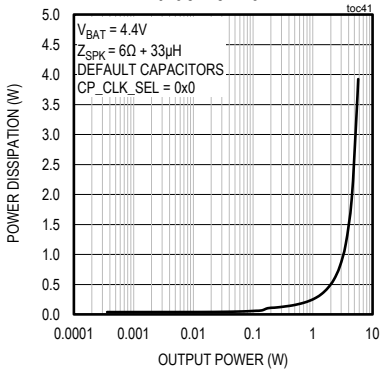
EFFICIENCY vs. OUTPUT POWER



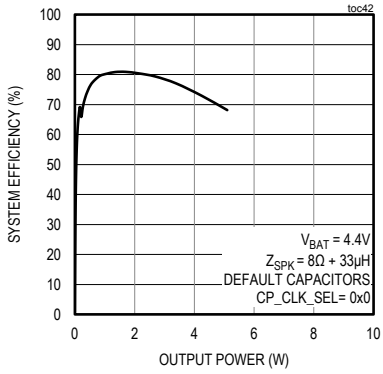
EFFICIENCY vs. OUTPUT POWER



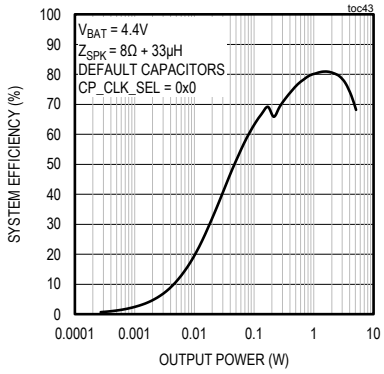
POWER DISSIPATION vs. OUTPUT POWER



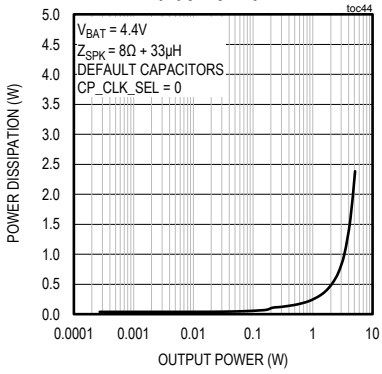
EFFICIENCY vs. OUTPUT POWER



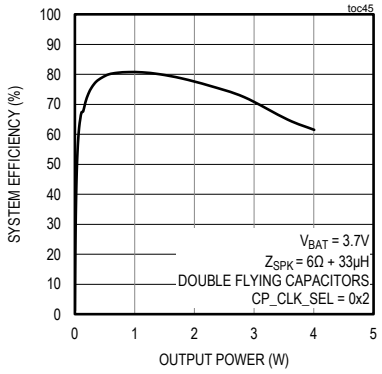
EFFICIENCY vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



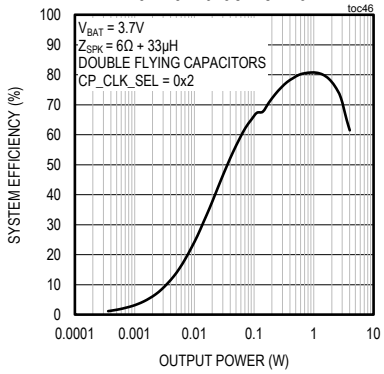
EFFICIENCY vs. OUTPUT POWER



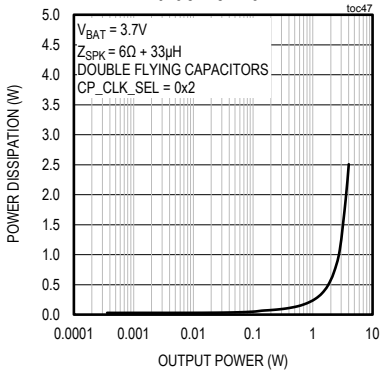
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

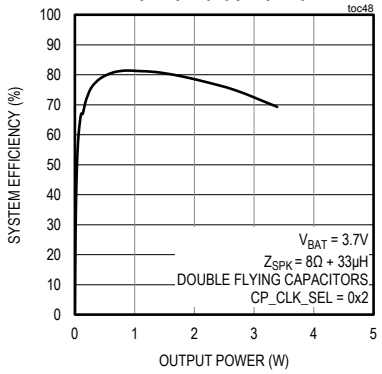
EFFICIENCY vs. OUTPUT POWER



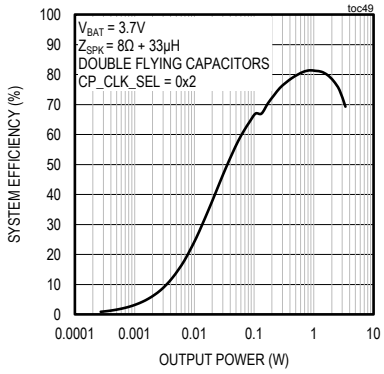
POWER DISSIPATION vs. OUTPUT POWER



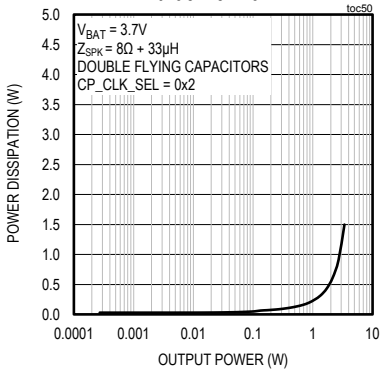
EFFICIENCY vs. OUTPUT POWER



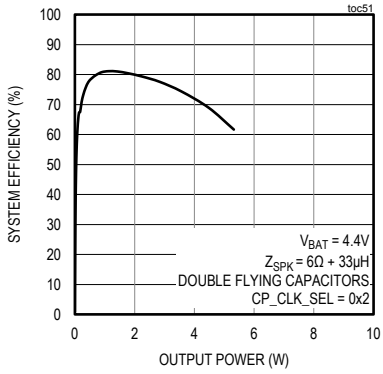
EFFICIENCY vs. OUTPUT POWER



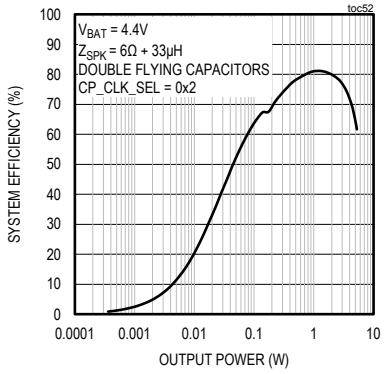
POWER DISSIPATION vs. OUTPUT POWER



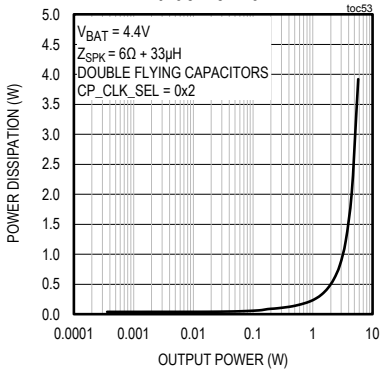
EFFICIENCY vs. OUTPUT POWER



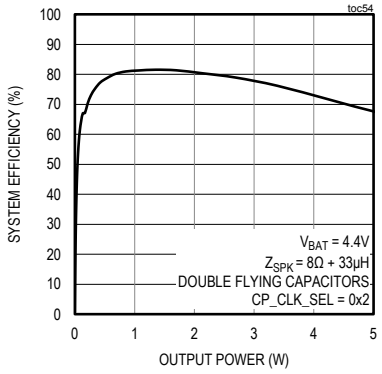
EFFICIENCY vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



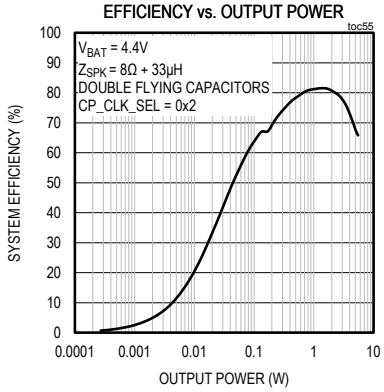
EFFICIENCY vs. OUTPUT POWER



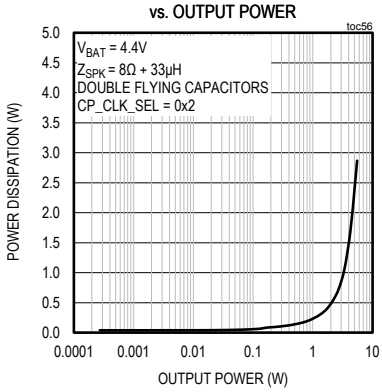
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

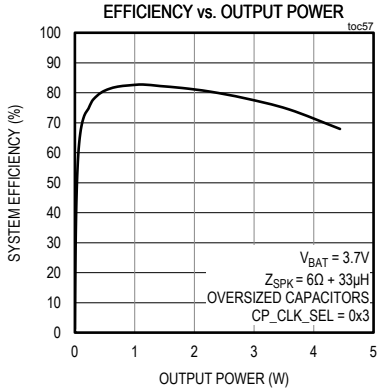
EFFICIENCY vs. OUTPUT POWER



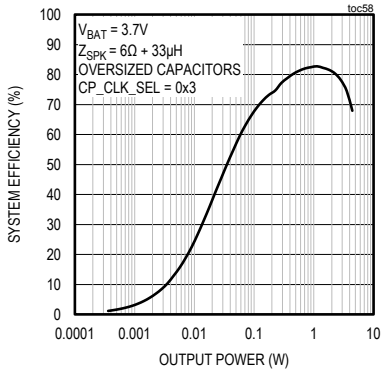
POWER DISSIPATION vs. OUTPUT POWER



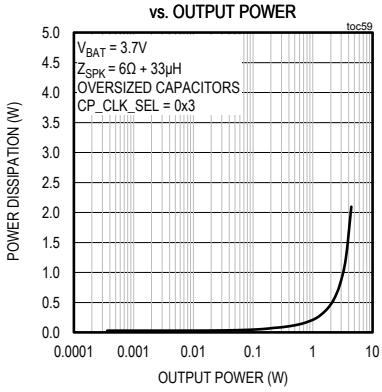
EFFICIENCY vs. OUTPUT POWER



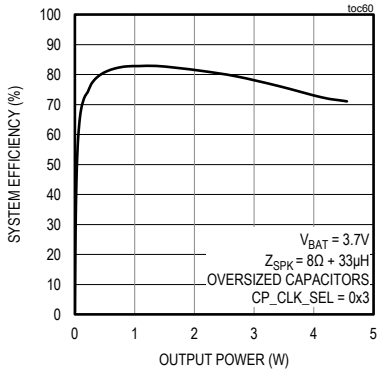
EFFICIENCY vs. OUTPUT POWER



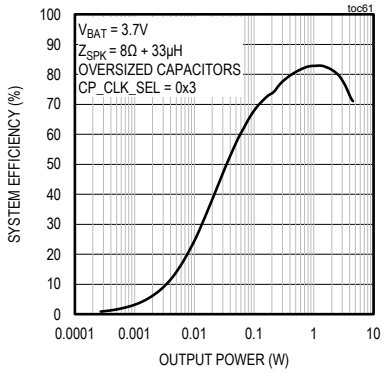
POWER DISSIPATION vs. OUTPUT POWER



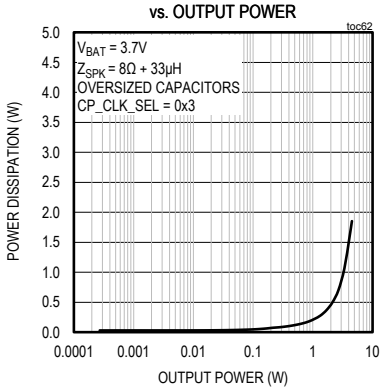
EFFICIENCY vs. OUTPUT POWER



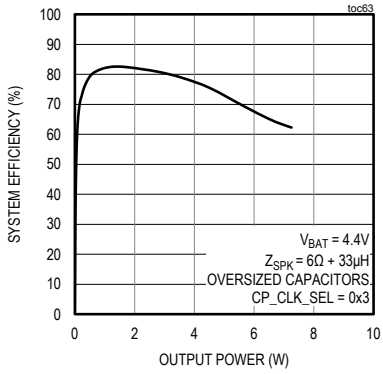
EFFICIENCY vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



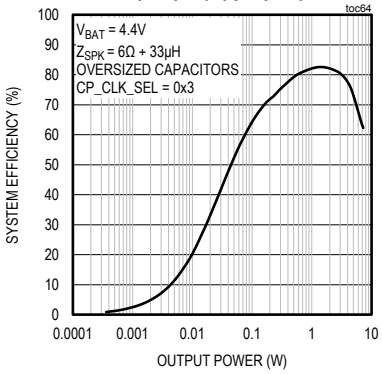
EFFICIENCY vs. OUTPUT POWER



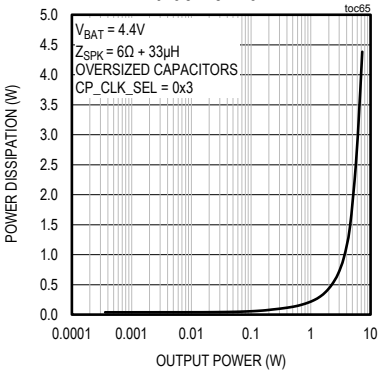
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

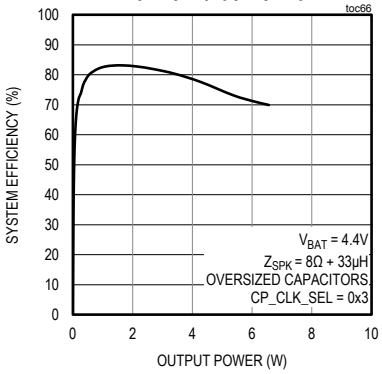
EFFICIENCY vs. OUTPUT POWER



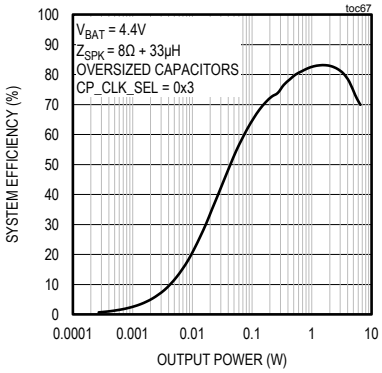
POWER DISSIPATION vs. OUTPUT POWER



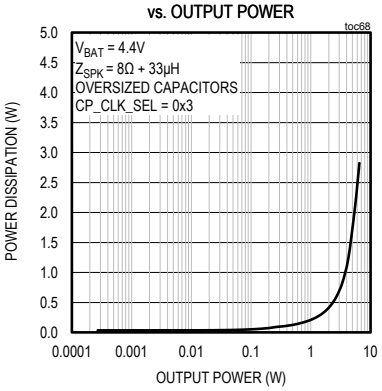
EFFICIENCY vs. OUTPUT POWER



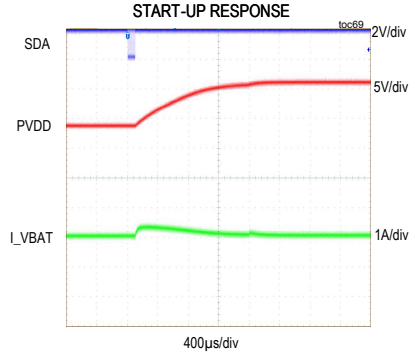
EFFICIENCY vs. OUTPUT POWER



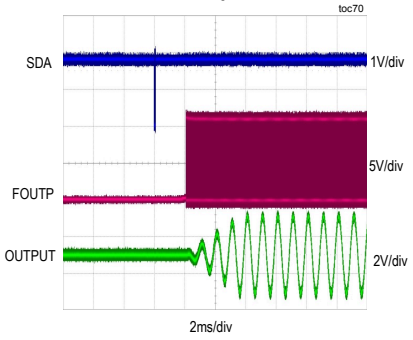
POWER DISSIPATION vs. OUTPUT POWER



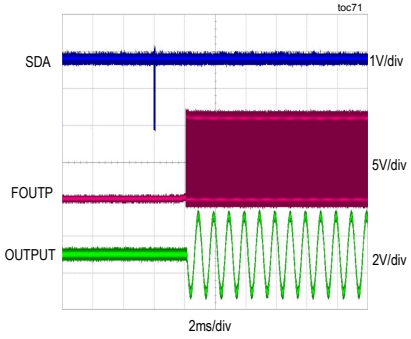
CHARGE PUMP START-UP RESPONSE



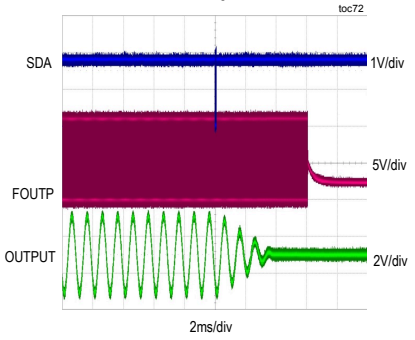
TURN-ON RESPONSE WITH RAMPING ENABLED



TURN-ON RESPONSE WITH RAMPING DISABLED



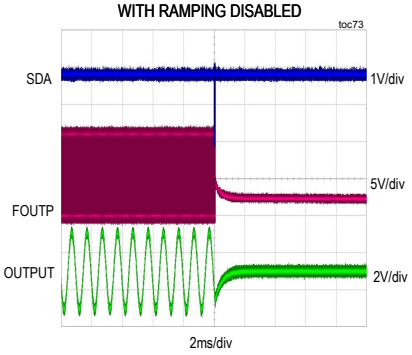
TURN-OFF RESPONSE WITH RAMPING ENABLED



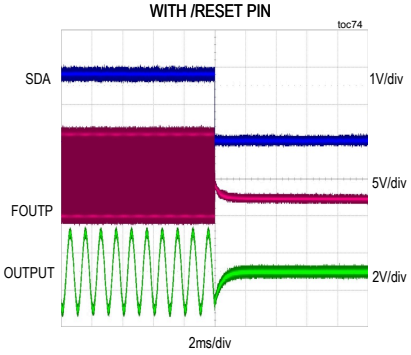
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

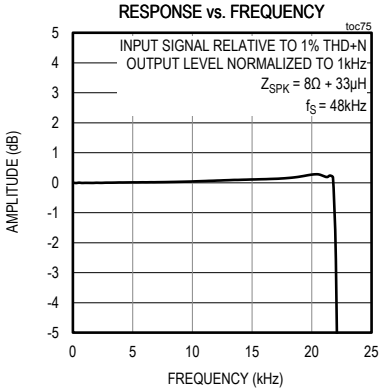
TURN-OFF RESPONSE WITH RAMPING DISABLED



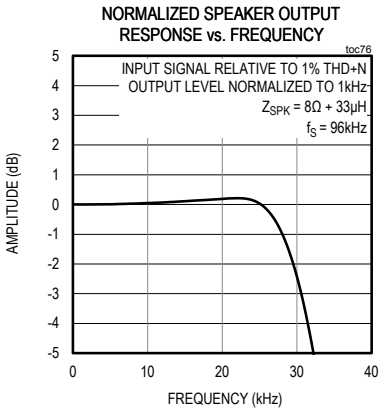
TURN-OFF RESPONSE WITH /RESET PIN



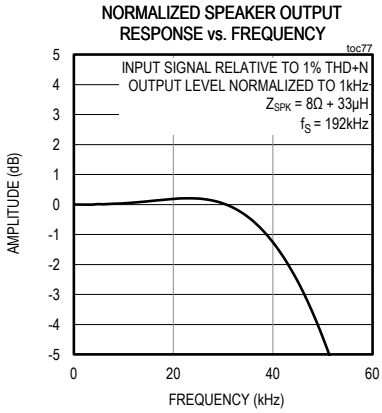
NORMALIZED SPEAKER OUTPUT RESPONSE vs. FREQUENCY



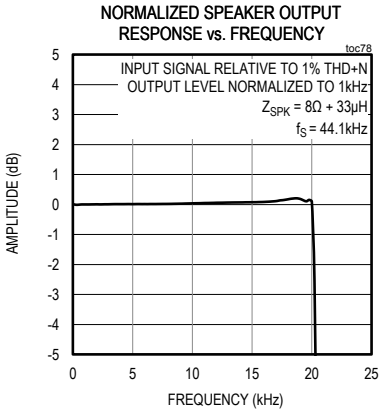
NORMALIZED SPEAKER OUTPUT RESPONSE vs. FREQUENCY



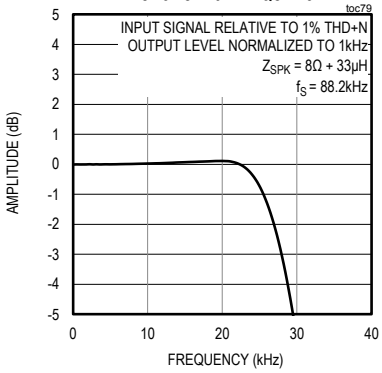
NORMALIZED SPEAKER OUTPUT RESPONSE vs. FREQUENCY



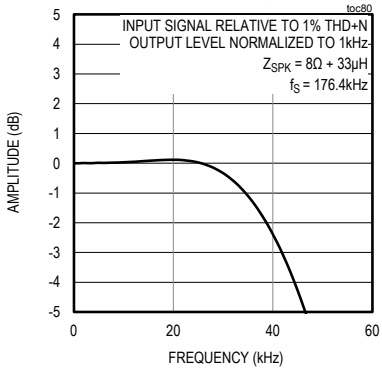
NORMALIZED SPEAKER OUTPUT RESPONSE vs. FREQUENCY



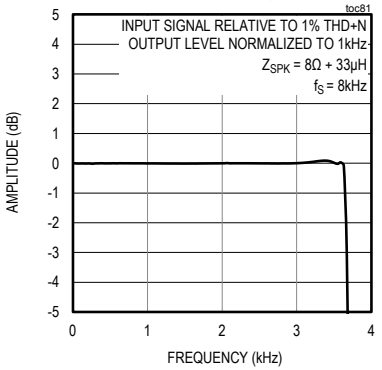
NORMALIZED SPEAKER OUTPUT RESPONSE vs. FREQUENCY



NORMALIZED SPEAKER OUTPUT RESPONSE vs. FREQUENCY

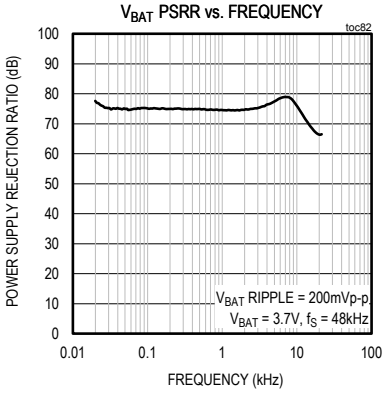


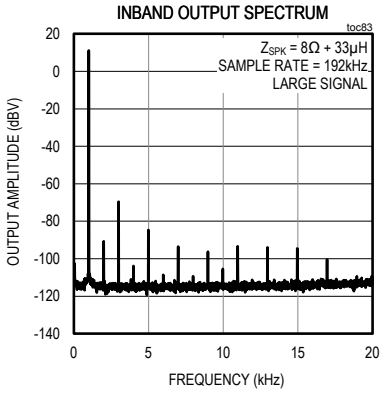
NORMALIZED SPEAKER OUTPUT RESPONSE vs. FREQUENCY

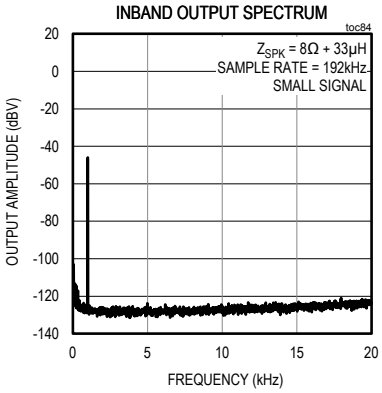


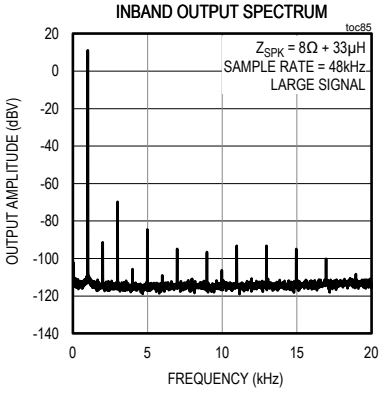
Typical Operating Characteristics (continued)

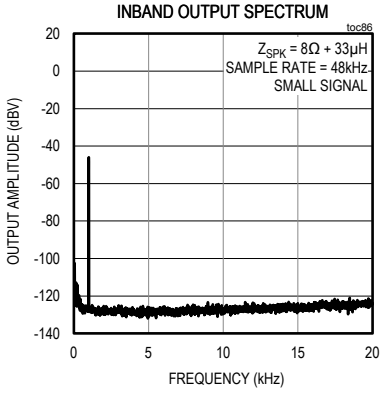
(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

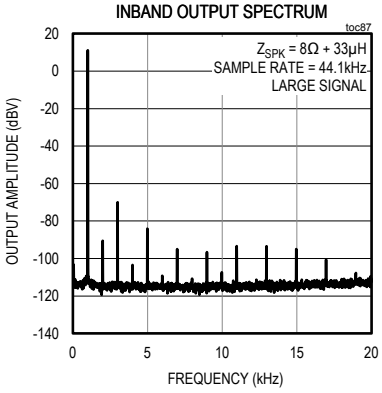


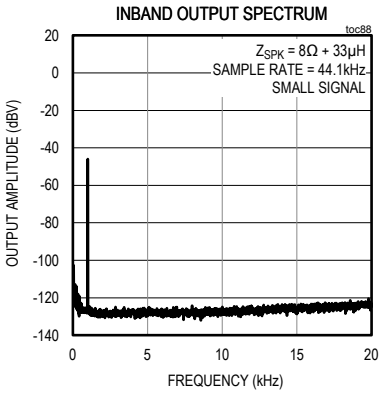


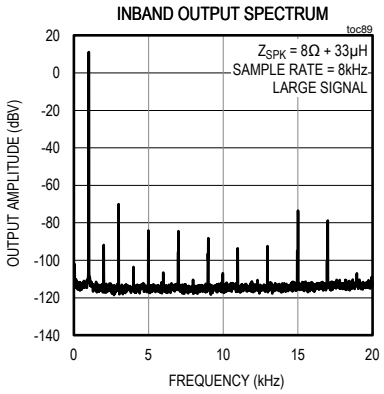


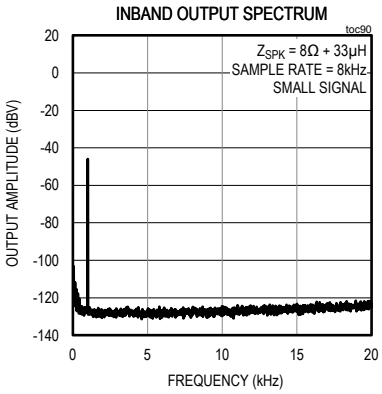








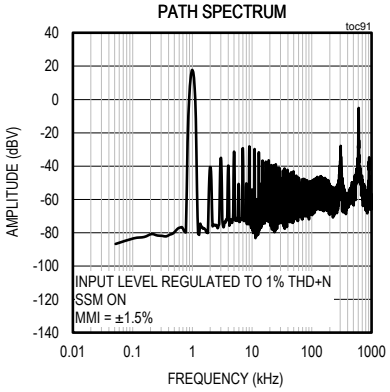




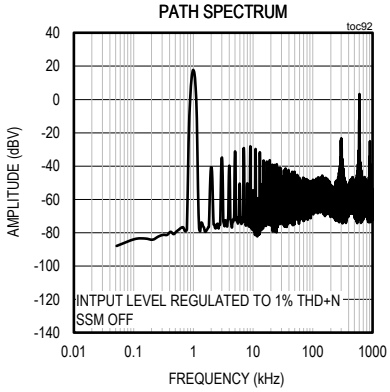
Typical Operating Characteristics (continued)

(V_{BAT} = 3.7V, V_{VDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, C_{VBAT} = 1 x 10µF, 1 x 0.1µF, C_{VDD} = 1µF, C_{PVDD} = 2 x 10µF, 1 x 0.1µF, C_{CPBYP} = 2 x 2.2µF, 1 x 0.1µF, C_{CP1} = 2 x 2.2µF, C_{CP2} = 2 x 2.2µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C))

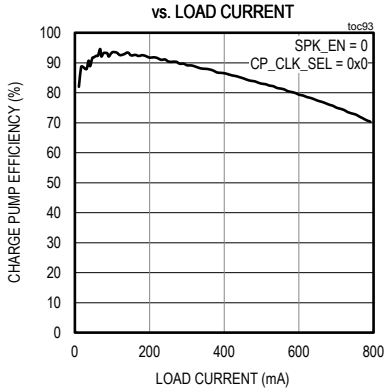
WIDEBAND PLAYBACK PATH SPECTRUM



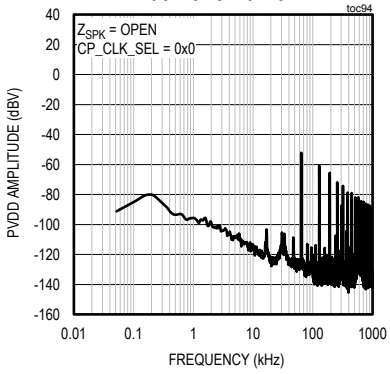
WIDEBAND PLAYBACK PATH SPECTRUM



CHARGE PUMP EFFICIENCY vs. LOAD CURRENT

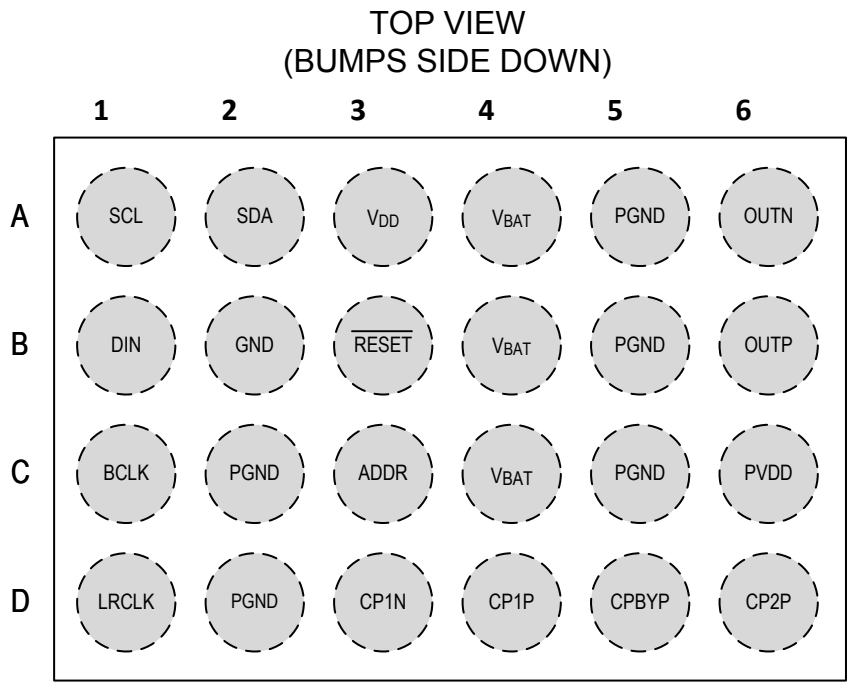


PVDD WIDEBAND OUTPUT SPECTRUM



Pin Configuration

MAX98380



(2.138mm x 1.468mm, 0.35mm PITCH)

Pin Description

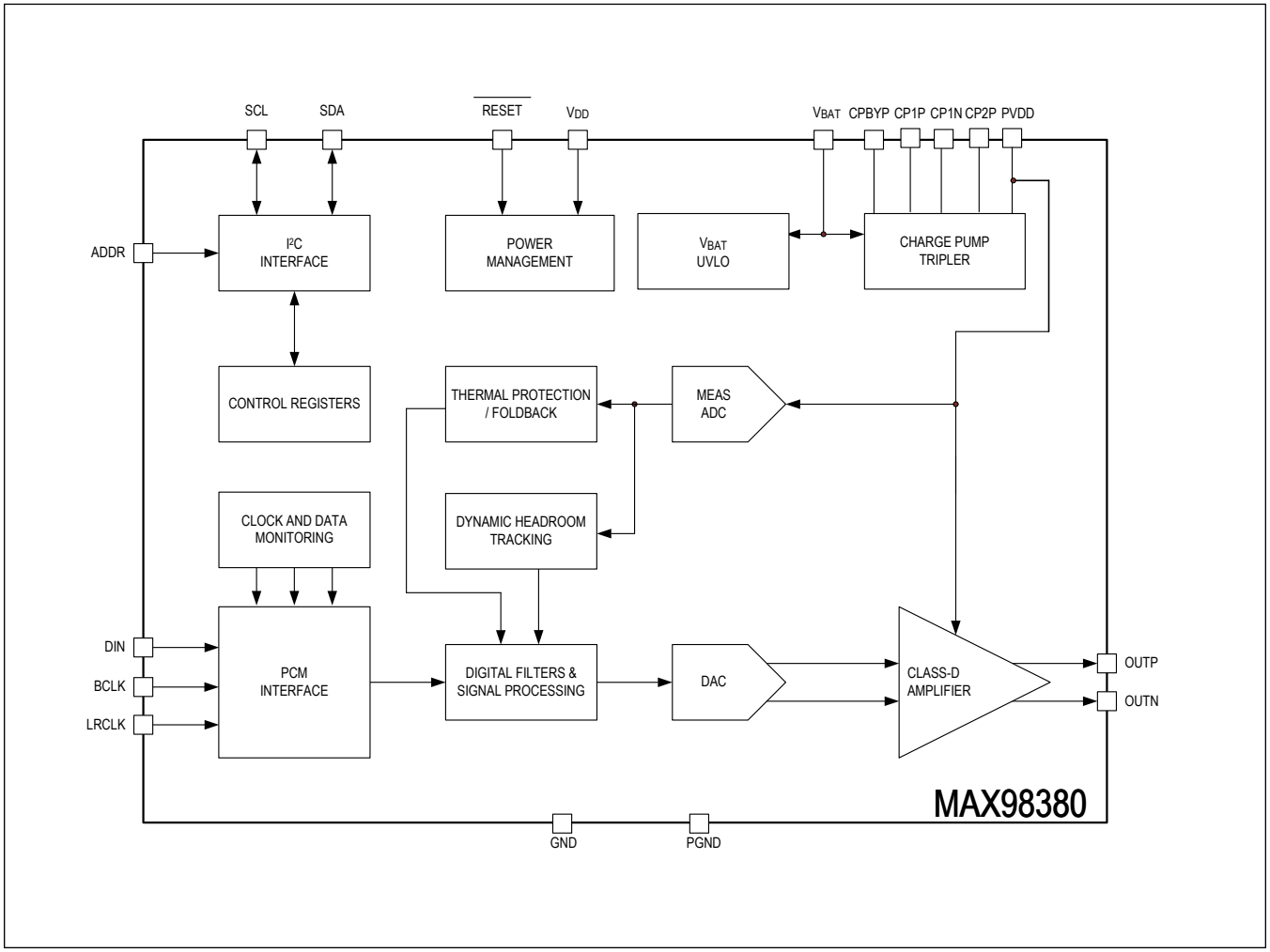
PIN	NAME	FUNCTION	REF SUPPLY	TYPE
B3	$\overline{\text{RESET}}$	Hardware Enable (Active-Low). Resets all digital portions of the device and all registers to default PoR settings.	V_{DD}	Digital Input
A4, B4, C4	V_{BAT}	Battery Voltage Input. V_{BAT} supplies the boost converter and other analog circuit blocks. Bypass V_{BAT} to PGND with a 10µF capacitor and to GND with a 0.1µF capacitor.	—	Supply
A3	V_{DD}	Power Supply Input. Bypass to GND with a 1µF capacitor placed as close as possible.	—	Supply
D4	CP1P	Charge Pump 1st Flying Capacitor Positive Terminal	—	
D3	CP1N	Charge Pump 1st and 2nd Flying Capacitor Negative Terminal	—	
D6	CP2P	Charge Pump 2nd Flying Capacitor Positive Terminal	—	
D5	CPBYP	Charge Pump Bypass	—	
C6	PVDD	Charge Pump Output. Speaker amplifier power supply.	—	Supply

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
C2, D2, A5, B5, C5	PGND	Power Ground. Grounding for the boost converter and Class-D amplifier. Connect all PGND bumps together as close as possible to the IC.	—	Supply
B2	GND	Ground	—	Supply
B6	OUTP	Positive Class-D Amplifier Output	PVDD	Analog Output
A6	OUTN	Negative Class-D Amplifier Output	PVDD	Analog Output
A2	SDA	I^2C-Compatible Serial-Data Input/Output. Connect a pullup resistor to V_{DD} for full output swing.	V_{DD}	Digital I/O (Open Drain)
A1	SCL	I^2C-Compatible Serial-Clock Input. Connect a pullup resistor to V_{DD} for full output swing.	V_{DD}	Digital Input (Open Drain)
C3	ADDR	I^2C Address Select. Selects one of four I^2C slave addresses.	V_{DD}	Digital Input
C1	BCLK	PCM Interface BCLK Input. Internally pulled down to GND through R_{PD}.	V_{DD}	Digital Input
D1	LRCLK	PCM Interface Frame Clock Input/Output. LRCLK frequency matches the PCM interface sample rate. Internally pulled down to GND through R_{PD}.	V_{DD}	Digital Input
B1	DIN	PCM Interface Data Input. Internally pulled down to GND through R_{PD}.	V_{DD}	Digital Input

Functional Diagrams

Detailed Block Diagram



Detailed Description

Device State Control

Hardware Shutdown State

When the device is first powered up or after a hardware reset event, the device always initializes into the hardware shutdown state. In hardware shutdown, the device is configured to its lowest power state. Upon entering hardware shutdown, the device is globally placed into a reset condition. As a result, the I^2C control interface is disabled and all device registers are returned to their PoR states. When exiting hardware shutdown, the device initializes and then transitions into the software shutdown state. During this transition (as part of initialization), the OTP register trim settings are loaded.

When the hardware reset input ($\overline{RESET}$) is asserted low, the device enters (or remains in) hardware shutdown. The device is also placed into hardware shutdown anytime the V_{BAT} supply drops below its UVLO threshold.

The device only exits hardware shutdown when the V_{BAT} supply is above its UVLO threshold, and the hardware reset input ($\overline{RESET}$) is asserted high. Once all of these conditions are met, the device automatically exits hardware shutdown, and transitions into software shutdown provided V_{DD} is supplied and in the valid range.

Software Shutdown State

The device enters the software shutdown state after it transitions out of the hardware shutdown state and when exiting the active state. In the software shutdown state, all blocks are automatically disabled except for the I^2C control interface. In the software shutdown state, all device registers can be programmed without restriction and all programmed register states are retained.

The global enable bit (EN) is used to transition the device into and out of software shutdown. When global enable (EN) is set high, the device transitions to the active state. When the device is in the active state and global enable (EN) is set low, the device transitions to the software shutdown state. Additionally, the device is reset and enters software shutdown anytime the software reset bit (RST) is written with a 1.

Active State

The device enters the active state through a transition from the software shutdown state when valid clocks are applied to the device. In the active state, all enabled device blocks are active and speaker amplifier playback is possible when audio data is applied to the device. In the active state, only dynamic register settings (or those restricted to disabled blocks) can be programmed safely.

The only non-fault state transitions to or from the active state are those initiated through the global enable bit (EN). All other transitions to or from the active state are the result of fault events and can result in audible glitches if they occur during active playback.

PCM Interface

The flexible PCM slave interface supports common audio playback sample rates from 8kHz to 192kHz. The PCM interface also supports standard I^2S, left-justified, and TDM data formats. The PCM interface is disabled and powered down when the PCM data input (DIN) is disabled.

PCM Clock Configuration

The PCM slave interface requires the host to supply both BCLK and LRCLK. To configure the PCM interface clock inputs, the host must program both the device interface sample rate (*PCM_SR*) and BCLK to LRCLK (*PCM_BSEL*) ratio. The PCM interface sample rate must be configured to match the frequency of the frame clock (LRCLK) using the *PCM_SR* registers. The speaker path sample rate is also set by the *PCM_SR* setting. The device supports a range of BCLK to LRCLK clock ratios (*PCM_BSEL*) ranging from 32 to 512. However, based on the selected PCM interface sample rate (LRCLK frequency), the configured clock ratio cannot result in a BLCK frequency that exceeds 24.576MHz.

PCM Data Format Configuration

The device supports the standard I^2S, left-justified, and TDM data formats, and the operating mode is configured using

the *PCM_FORMAT* bit field.

I²S/Left-Justified Mode

I²S and left-justified formats support two channels that can be 16-, 24-, or 32-bits in length. The BCLK to LRCLK ratio (*PCM_BSEL*) must be configured to be twice the desired channel length. The audio data word size is configurable to 16-, 24-, or 32-bits in length (*PCM_CHANSZ*), but must be programmed to be less than or equal to the channel length. If the resulting channel length exceeds the configured data word size, then the data input LSBs are truncated.

Table 1. Supported I²S/Left-Justified Mode Configurations

CHANNELS	CHANNEL LENGTH	BCLK TO LRCLK RATIO (PCM_BSEL)	SUPPORTED DATA WORD SIZES (PCM_CHANSZ)
2	16	32	16
	24	48	16, 24
	32	64	16, 24, 32

With the default PCM settings, falling LRCLK indicates the start of a new frame and the left channel data (Channel 0) while rising LRCLK indicates the right channel data (Channel 1). In I²S mode, the MSB of the audio word is latched on the second active BCLK edge after an LRCLK transition. In left-justified mode, the MSB of the audio word is latched on the first active BCLK edge after an LRCLK transition.

The *PCM_BCLKEDGE* register bit selects either the rising or falling edge of BCLK as the active edge that is used for data capture (DIN). The *PCM_CHANSEL* bit configures which LRCLK edge indicates the start of a new frame (channel 0), and LRCLK transitions always align with the inactive BCLK edge. The data output is valid on the same active BCLK edge as the data input.

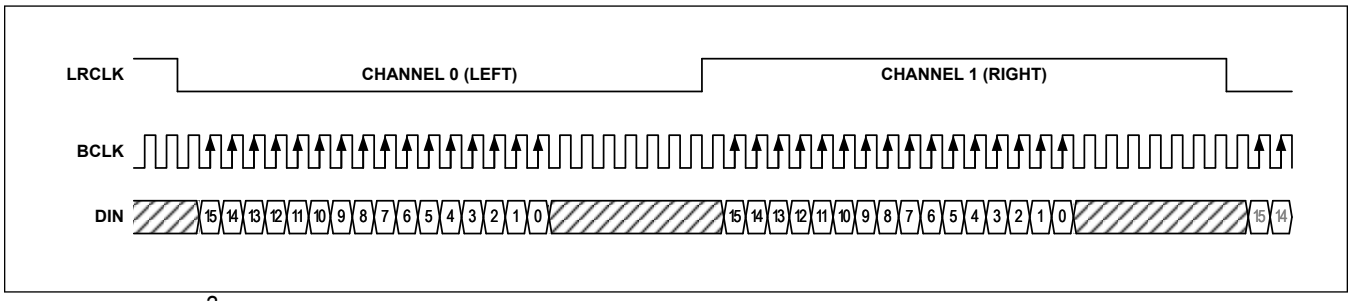


Figure 1. Standard I²S Mode

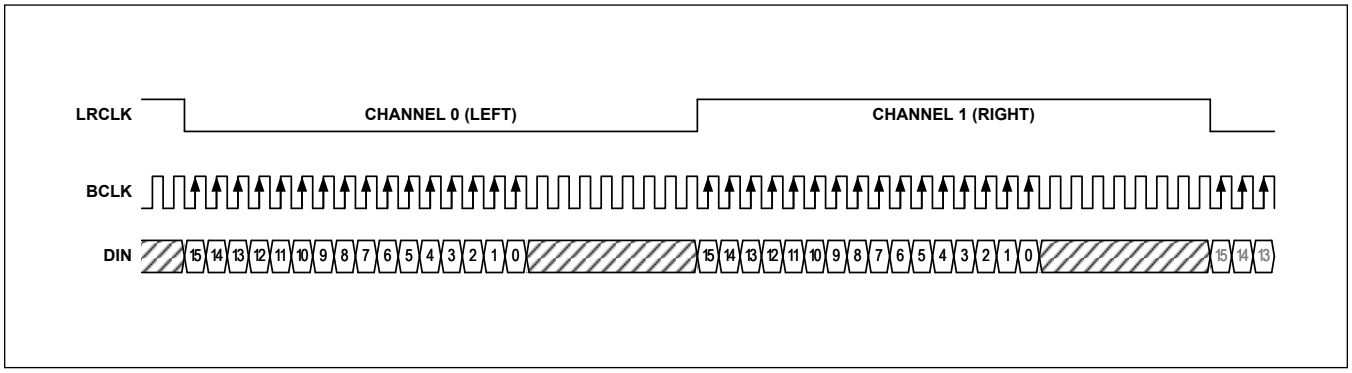


Figure 2. Left-Justified Mode

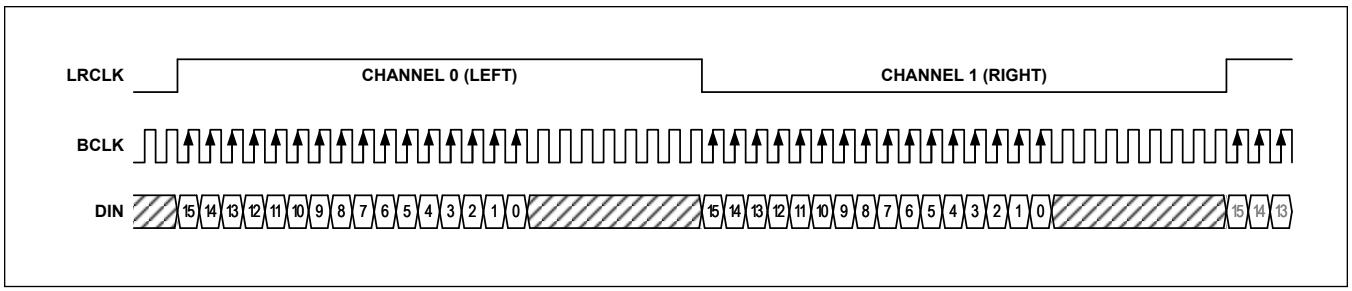


Figure 3. Left-Justified Mode (LRCLK Inverted)

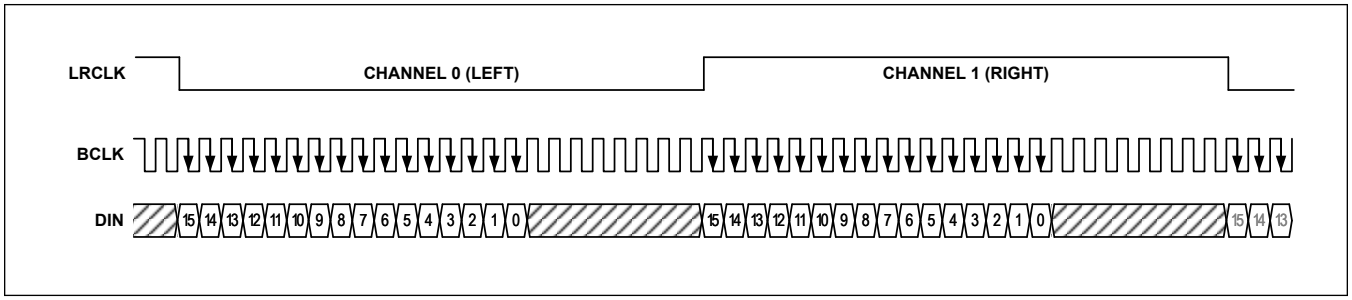


Figure 4. Left-Justified Mode (BCLK Inverted)

TDM Modes

The provided TDM modes support timing for up to 16 digital audio input channels (from DIN) each containing 16-, 24-, or 32-bits of data. The number of TDM input channels is determined by both the selected BCLK to LRCLK ratio (*PCM_BSEL*) and the selected data word and channel length (*PCM_CHANSZ*).

For a given valid configuration, the number of available data input channels per frame is calculated as follows:

Number of Available Data Input Channels = BCLK to LRCLK Ratio/Channel Length

For a given valid configuration, the number of available 8-bit data output slots per frame is calculated as follows:

Number of Available Data Output Slots = BCLK to LRCLK Ratio/8

Table 2 shows the supported TDM mode configurations for each combination of input data channels and output data slots. In some configurations, the maximum PCM interface and speaker amplifier playback sample rate are limited to less than 96kHz to avoid violating the BCLK frequency limit of 24.576MHz.

Table 2. Supported TDM Mode Configurations

INPUT DATA CHANNELS	DATA WORD SIZES (PCM_DATA_WIDTH)	BCLK TO LRCLK RATIO (PCM_BSEL)	MAXIMUM SPEAKER PLAYBACK SAMPLE RATE (FLRCLK)
2	16	32	192kHz
	24	48	
	32	64	
3	32	125	
4	16	64	
	24	96	
	32	128	
5	24	125	
7	16	125	
2	16	32	96kHz

Table 2. Supported TDM Mode Configurations (continued)

INPUT DATA CHANNELS	DATA WORD SIZES (PCM_DATA_WIDTH)	BCLK TO LRCLK RATIO (PCM_BSEL)	MAXIMUM SPEAKER PLAYBACK SAMPLE RATE (FLRCLK)
	24	48	
	32	64	
3	32	125	
4	16	64	
	24	96	
	32	128	
5	24	125	
7	16	125	
	32	250	
8	16	128	
	24	192	
	32	256	
10	24	250	
15	16	250	
16	16	256	
7	32	250	48kHz
10	24	250	
	32	320	
15	16	250	
16	24	384	
	32	512	

With the default PCM interface settings, in TDM mode a rising frame clock (LRCLK) edge acts as the frame sync pulse and indicates the start of a new frame. The frame sync pulse width must be equal to at least one bit clock period however the falling edge can occur at any time as long as it does not violate the setup time of the next frame sync pulse rising edge. The *PCM_CHANSEL* bit can be used to invert the LRCLK edges (sync pulse) used to start a TDM frame.

In TDM mode, the MSB of the first audio word can be latched on the first (TDM Mode 0), second (TDM Mode 1), or third (TDM mode 2) active BCLK edge after the sync pulse and is programmed by the PCM_FORMAT bits. Additionally, the *PCM_BCLKEDGE* register bit allows for the programmability of the BCLK edge that is used for data capture and data output. The data output is valid on the same active BCLK edge as the data input. The data output also transitions on the same edge as data input.

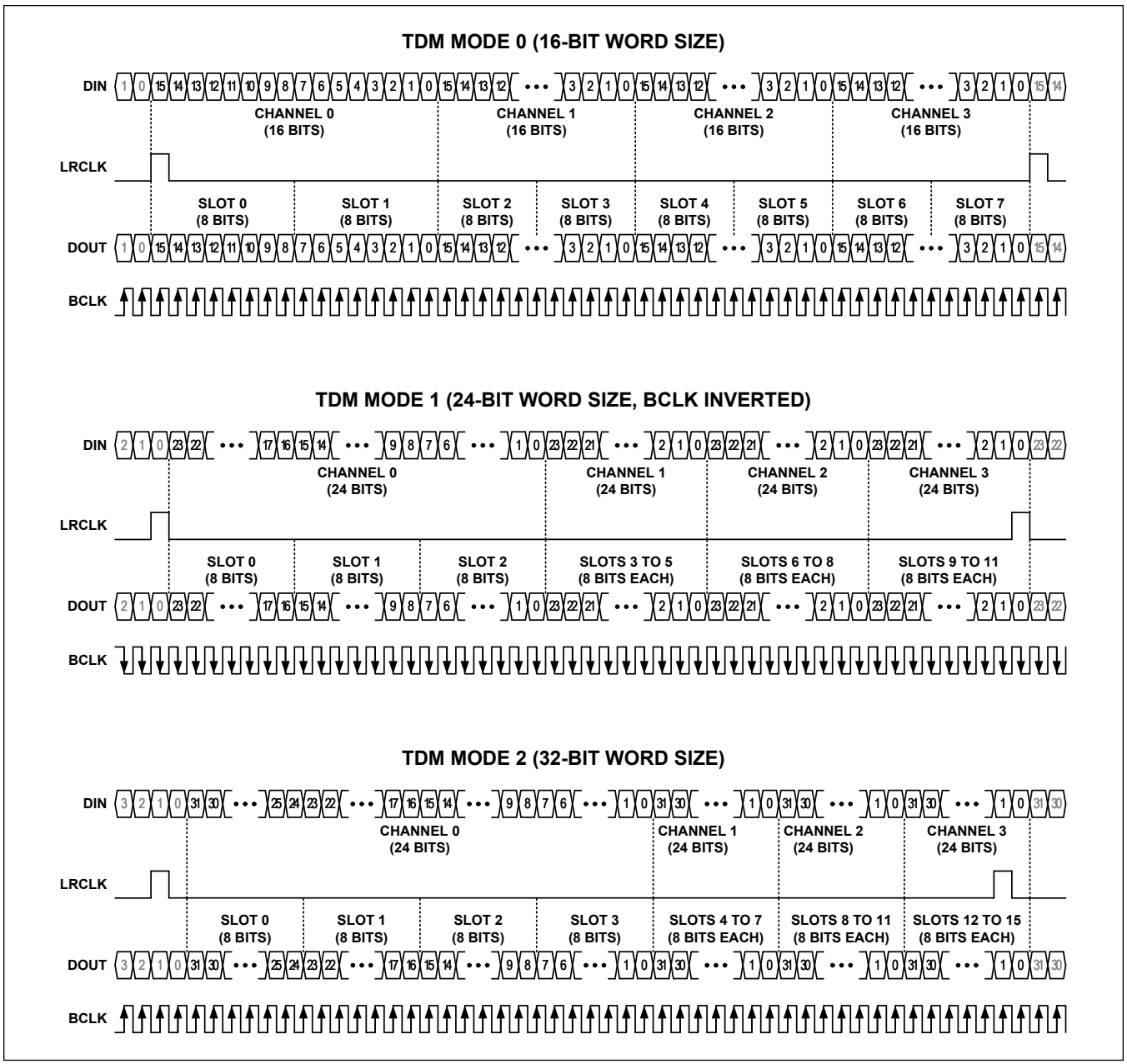


Figure 5. TDM Modes

PCM Data Path Configuration

The PCM interface data input (DIN) receives the source data for the speaker amplifier path.

PCM Data Input

The PCM interface data input (DIN) is enabled with the PCM_RX_EN bit and can accept data from any valid input data channel. The device provides an input digital mono mixer that can route a single channel or can mix two PCM input channels to create a mono input to the speaker playback path. The PCM_DMMIX_CFG bit is used to configure the mixer, while the PCM_DMMIX_CH0_SOURCE and PCM_DMMIX_CH1_SOURCE bits select which of the 16 PCM input channels are used as the input to the mono mixer. In I^2S and left-justified modes, only 2 input data channels are available

while in TDM mode, up to 16 channels of input data may be available. If the PCM data input is disabled (PCM_RX_EN = 0), a zero-code value is driven into the speaker amplifier path.

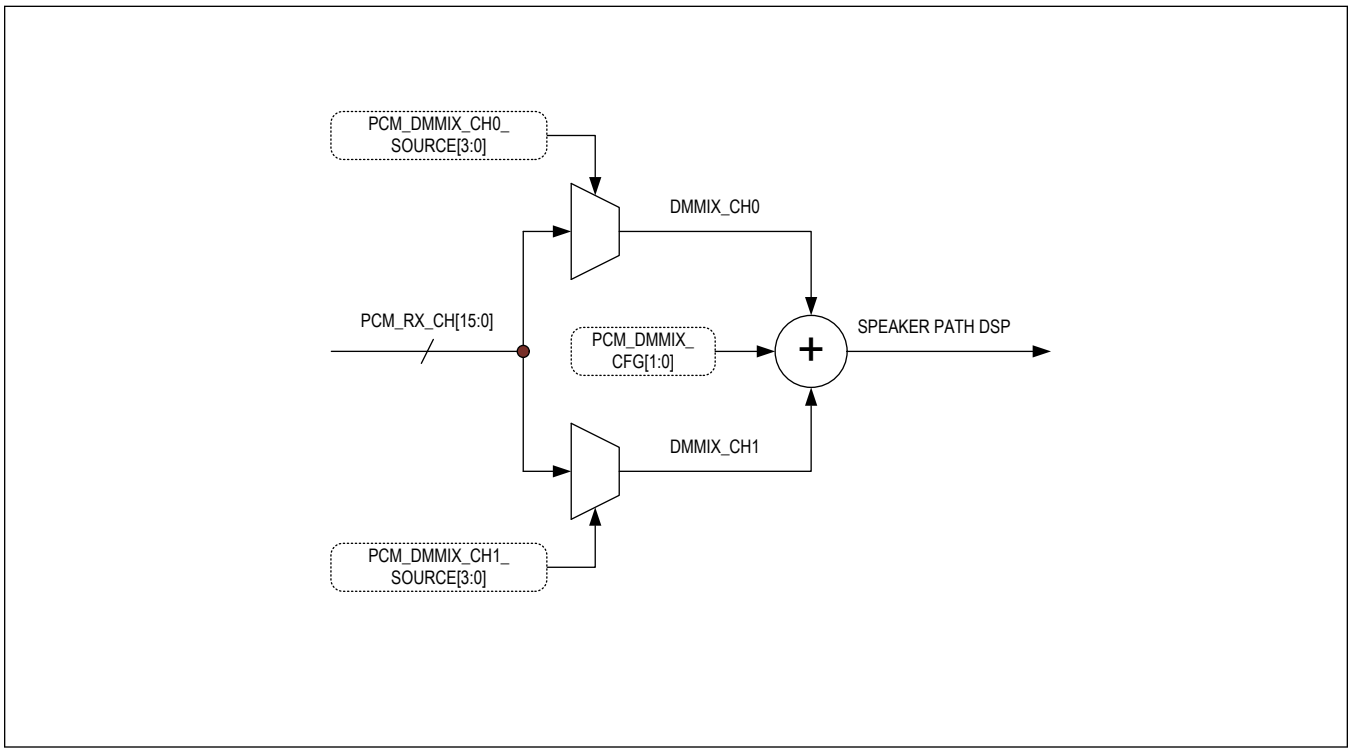


Figure 6. PCM Data Input

PCM Interface Timing

Figure 7 shows timing for BCLK, LRCLK, and DIN. See the *Electrical Characteristics* table for more details.

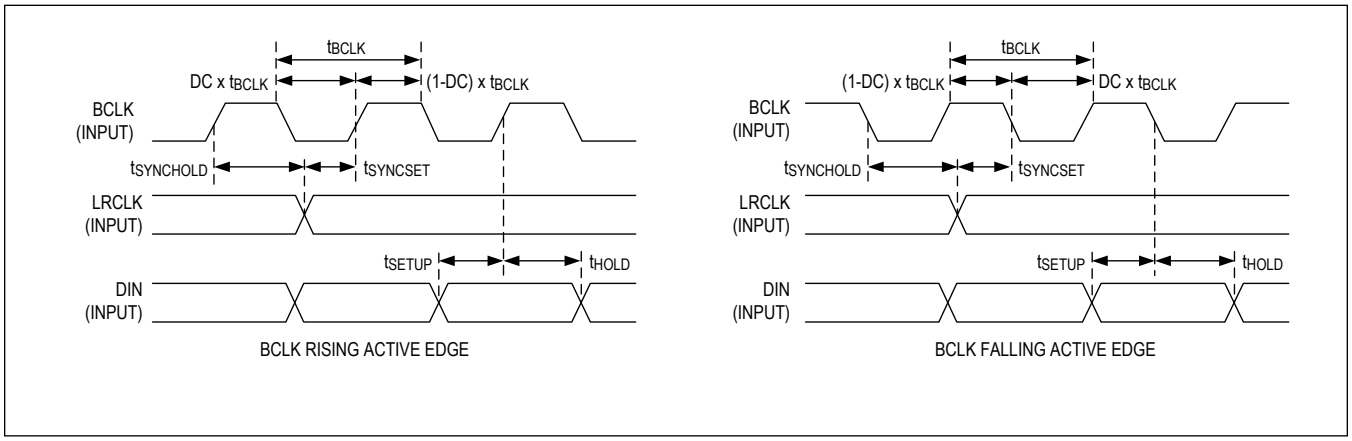


Figure 7. PCM Interface Timing/Slave Mode—LRCLK, BCLK, DIN Timing Diagram

Device Status Bits

The IC uses the status register to report the status of various device functions. The status register bits are set when their respective events occur, and are cleared upon reading the register. Device status can be determined by poling the status

register. See Table 3 for the status bit event sources.

Table 3. Status Bit Event Sources

STATUS BIT EVENT SOURCES	BIT FIELD	DESCRIPTION
Thermal Shutdown Event	*THERMSHDN*	Indicates that the thermal-shutdown threshold temperature has been exceeded.
Thermal Warning Event	*THERMWARN*	Indicates that the thermal-warning threshold temperature has been exceeded.
Thermal Foldback Begin Event	*THERMFB_BGN*	Indicates that the die temperature is above the thermal-warning threshold and the device is attenuating the output.
Thermal Foldback End Event	*THERMFB_END*	Indicates that die temperature is below thermal-warning threshold and the device has stopped attenuating the output.
OTP Load Fail Event	*OTP_FAIL*	Indicates that the OTP load routine that runs when exiting hardware shutdown has failed to complete successfully. If the OTP load routine fails, the device is held in software shutdown.
Speaker Over Current Event	*SPK_OVC*	Indicates that the speaker amplifier current limit has been exceeded.
FLL CLK Error	*FLL_ERR*	Indicates a clock stop error in the internal clocks of the device.
External CLK (BCLK/LRCLK) Error	*CLK_ERR*	Indicates a frequency or framing error in the input BCLK or LRCLK.
Speaker Amplifier Monitor Error	*SPKMON_ERR*	Indicates an amplifier output stuck high or low error.
Power-Up Done Event	*PWRUP_DONE*	Indicates that the device has entered the active state and the device is ready to play audio.
Power-Down Done Event	*PWRDN_DONE*	Indicates that the device has entered the software shutdown state.
V_{BAT} UVLO Shutdown Event	*VBAT_UVLO_SHDN*	Indicates that V_{BAT} is below the minimum allowed voltage when the device is in the active state.
DHT Active Event	*DHT_ACTIVE*	Indicates that the DHT circuit is active and is applying attenuation to the signal.

Speaker Path

The source input data to the speaker amplifier path is routed from the PCM interface. The data is then routed through digital filters, signal processing, and volume/gain control blocks before reaching the Class-D speaker amplifier.

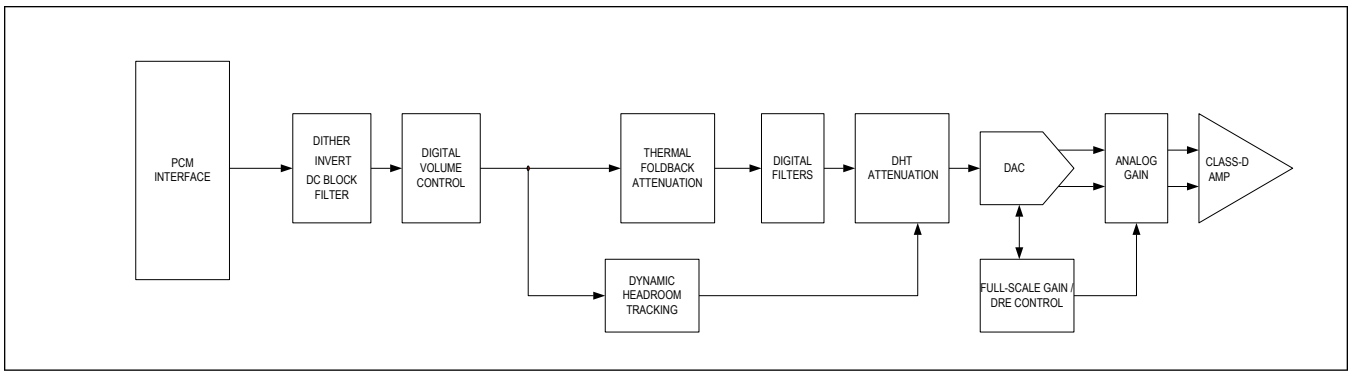


Figure 8. Speaker Amplifier Path

Speaker Path Dither

The input data to the speaker path can optionally have dither (±1LSB peak-to-peak) applied if *SPK_DITH_EN* is set to 1. No dither is applied when *SPK_DITH_EN* is set to 0.

Speaker Path Data Inversion

The input data to the speaker path can optionally be inverted by setting the *SPK_INVERT* bit to 1.

Speaker Path DC Blocking Filter

A DC blocking filter can be enabled on the speaker path by setting the *SPK_DCBLK_EN* bit to 1.

Speaker Path Digital Volume Control

The device provides a dynamically programmable speaker path digital volume control. The digital volume control provides an attenuation range of 0dB to -63dB in 0.5dB steps that is configured with the *SPK_VOL* bit field. A digital mute is also provided and is enabled when *SPK_VOL* is set to 0x7F.

Digital volume ramping during speaker path start-up, speaker path shutdown, and digital mute (*SPK_VOL* = 0x7F) is disabled by default. However, both the volume ramp up and ramp down can be individually enabled with the *SPK_VOL_RMPUP_BYPASS* and *SPK_VOL_RMPDN_BYPASS* bit fields respectively. When volume ramp up or ramp down is enabled, the device turn-on and turn-off times are longer.

Speaker Safe Mode

The device provides a safe mode bit (*SPK_SAFE_EN*). When this bit is enabled, the *SPK_VOL* and *SPK_GAIN_MAX* settings are ignored and the amplifier output is set to -18dBFS. By default, speaker safe mode is enabled to protect any speaker connected to the device on power-up. While speaker safe mode is enabled, the digital volume control (*SPK_VOL*) settings are ignored.

Speaker Path Maximum Peak Output Voltage Scaling

The full-scale output of the speaker path DAC is 0.48dBV (typical). The speaker path no-load maximum peak output voltage level (V_{MPO}) is then programmable relative to this baseline level. The peak output scaling range is from 6dB to 21dB and is set with the SPK_GAIN_MAX bit field.

The speaker output signal level (in dBV) for a given digital input signal level (in dBFS) is calculated as follows:

Output Signal Level (dBV) = Input Signal Level (dBFS) + 0.48 (dBV) + SPK_GAIN_MAX (dB) (0dBFS is referenced to 0dBV) The peak output voltage scaling is applied to the signal path using a combination of digital gain and analog gain adjustments.

DAC Digital Filters

The DAC features a digital lowpass filter that is automatically configured based on the sample rate that is used. This filter eliminates the effect of aliasing and any other high-frequency noise that might otherwise be present. See the *DAC Digital Filters* section of the *Electrical Characteristics* table.

Dynamic Headroom Tracking (DHT)

The device features DHT that can preserve consistent signal distortion and listening levels in the presence of a varying supply level. The DHT features a limiter that can operate as either a signal distortion limiter (SDL) or a standard signal level limiter (SLL).

The DHT block is enabled with the DHT_EN bit. Before enabling the DHT, the measurement ADC PVDD channel should be configured and enabled. The DHT block uses the measured supply level and the current signal level to calculate the attenuation (if any) that is applied to the signal path. Also, the DHT block should not be disabled by setting the DHT_EN bit to 0 when the DHT is active (i.e., attenuation is being applied).

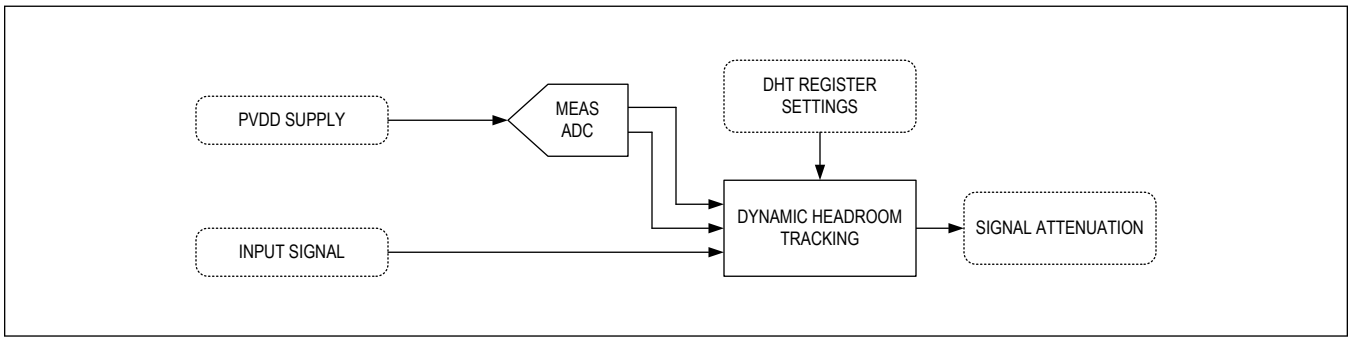


Figure 9. Simplified Dynamic Headroom Tracking System Block Diagram

DHT Supply Tracking and Headroom

The DHT block uses three parameters to track the target peak output level (V_{TPO}) relative to the maximum peak output voltage (V_{MPO}) as the active speaker amplifier supply level varies.

The first is the speaker amplifier full-scale gain setting (SPK_GAIN_MAX bit field). This control selects the maximum (no-load) peak output voltage level (V_{MPO}) that is output by the Class-D amplifier with a full-scale input signal (0dBFS). Most DHT thresholds and parameters are calculated relative to the full-scale V_{MPO}.

The second parameter is the measured speaker amplifier supply voltage level (V_{SUP}). The measurement ADC provides the DHT block with the PVDD supply voltage level (V_{PVDD}).

The third parameter is the speaker amplifier supply headroom (SUP_{HR}). The supply headroom is a positive or negative percentage offset relative to the measured V_{SUP} conversion result. It is configured using the DHT_HR bit field and can be set from +20% to -20% of V_{SUP} in 2.5% step sizes.

The DHT target peak output voltage level (V_{TPO}) is equal to the measured supply voltage (V_{SUP}) scaled to include the selected supply headroom percentage, and is actively calculated with the following equation:

$V_{TPO} = V_{SUP} \times (100\% – SUP_{HR})$ The target peak output attenuation (or ratio) from V_{TPO} to V_{MPO} is calculated as follows: $A_{TPO} = 20 \times \log (V_{TPO}/V_{MPO})$ If A_{TPO} exceeds 0dB (V_{SUP} with headroom > V_{MPO}), then the DHT block assumes that there is sufficient supply voltage to reproduce the audio signals as configured without attenuation. In this case, A_{TPO} = 0dB is used for all further calculations. This is important as the DHT functions only apply attenuation, and never apply positive gain. Once the calculated V_{TPO} drops below V_{MPO}, the calculated target peak output attenuation (A_{TPO}) is less than 0dB, and the DHT functions are applied appropriately as the input signal level changes.

For example, if V_{MPO} = 13.63V, V_{SUP} = 8.04V, and SUP_{HR} = -20%, then solving for V_{TPO} yields a target peak output level of ~9.65V. Next, solving for the target peak output attenuation (A_{TPO}) yields approximately -3dB.

Figure 10 shows the default transfer function (with no DHT attenuation applied), where the current target peak output level (V_{TPO}) is based on the current V_{SUP} and the supply headroom settings. The tracked V_{TPO} and the resulting peak output attenuation (A_{TPO}) are then used in the attenuation calculations for the DHT functions. Note that this and all subsequent figures are not drawn to a precise scale and that the x-axis input signal level (dBFS) is on a linear scale, while the y-axis peak output voltage level is on a log scale.

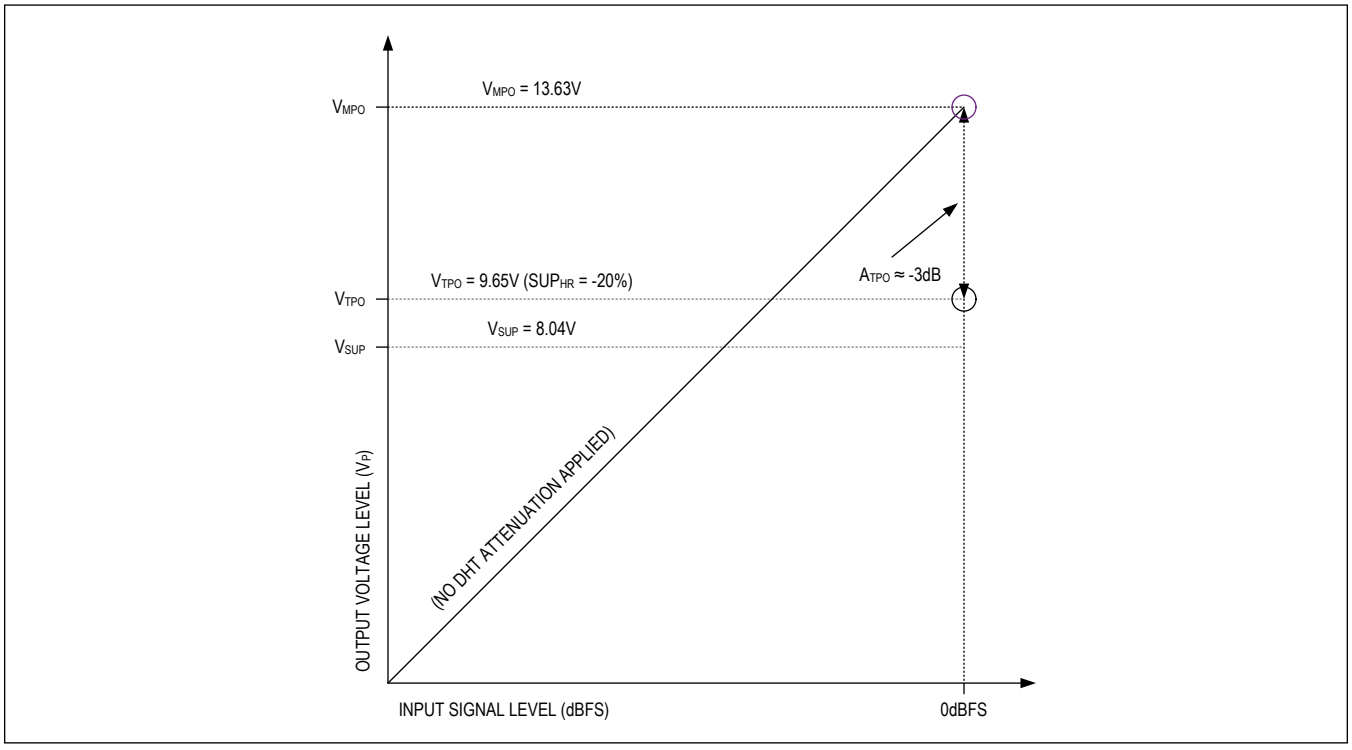


Figure 10. V_{TPO} and A_{TPO} Calculation Example

DHT Mode 1—Signal Distortion Limiter (SDL)

The DHT signal distortion limiter (SDL) maintains a consistent level of signal distortion at the amplifier output as the supply voltage (V_{SUP}) changes. To use DHT mode 1 (just the signal distortion limiter active), set the DHT_LIM_MODE bit low (default) to place the limiter function in supply tracking mode (SDL). The signal distortion limiter function is a compressor with a ratio of infinity to 1 that actively sets its threshold (V_{SDL} in voltage) equal to the calculated target peak output voltage level (V_{TPO}). The output-referred SDL threshold (SDL_{THR}) and the input-referred SDL knee or rotation point (SDL_{RP}) are equal in mode 1 and can be calculated relative to full-scale (in dBFS) as a ratio of V_{TPO} to V_{MPO}: $SDL_{RP} = SDL_{THR} = 20 \times \log (A_{TPO}) = 20 \times \log (V_{TPO}/V_{MPO})$

The transfer function for input signal levels below the SDL rotation point (SDL_{RP}) is unchanged. When the input signal level exceeds SDL_{RP}, the signal distortion limiter function is applied to the signal path. As the input signal level increases, the distortion limiter attenuation continues to increase as well and can be calculated for a given input signal level (A_{INPUT} in dBFS) as follows:

$SDL\ ATTENUATION = SDL_{RP} – A_{INPUT}$

By actively recalculating SDL_{RP} (or SDL_{THR}) as the target peak output level (V_{TPO}) changes, the DHT SDL maintains a consistent limit and level of amplifier output distortion relative to the available supply voltage (V_{SUP}).

When the target peak output voltage (V_{TPO}) exceeds the amplifier maximum peak output voltage (V_{MPO}), there is sufficient headroom and no SDL attenuation is applied. However, as soon as V_{TPO} falls below V_{MPO}, the input signal amplitude can exceed the calculated SDL_{RP}. The following examples show the transfer function when $V_{SUP} \geq V_{MPO}$ with the minimum (-20%), no (0%), and maximum (+20%) supply headroom (SUP_{HR}) settings. Note that in the case with positive headroom (+20%), the SDL_{RP} falls below the input signal full-scale level even though $V_{SUP} = V_{MPO}$.

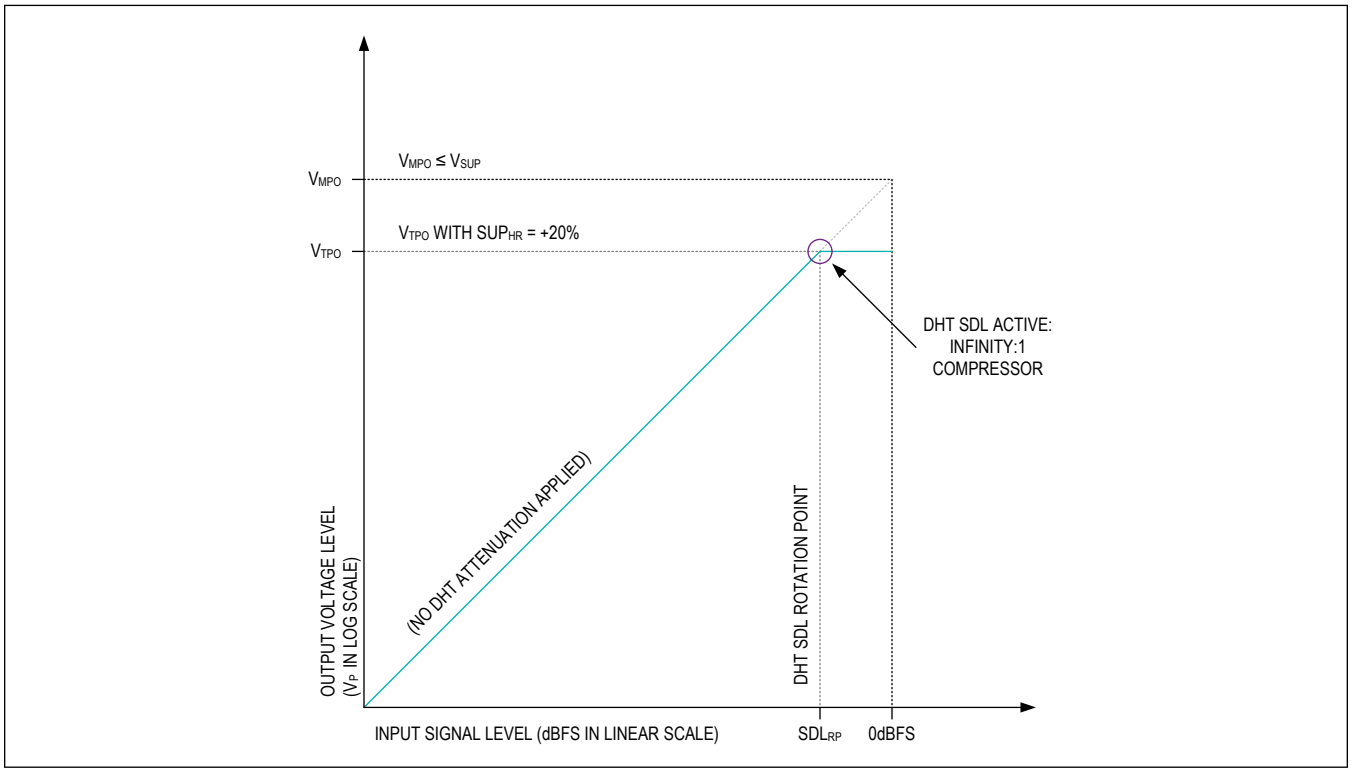


Figure 11. Signal Distortion Limiter with $V_{MPO} \leq V_{SUP}$ and +20% Headroom (SUP_{HR})

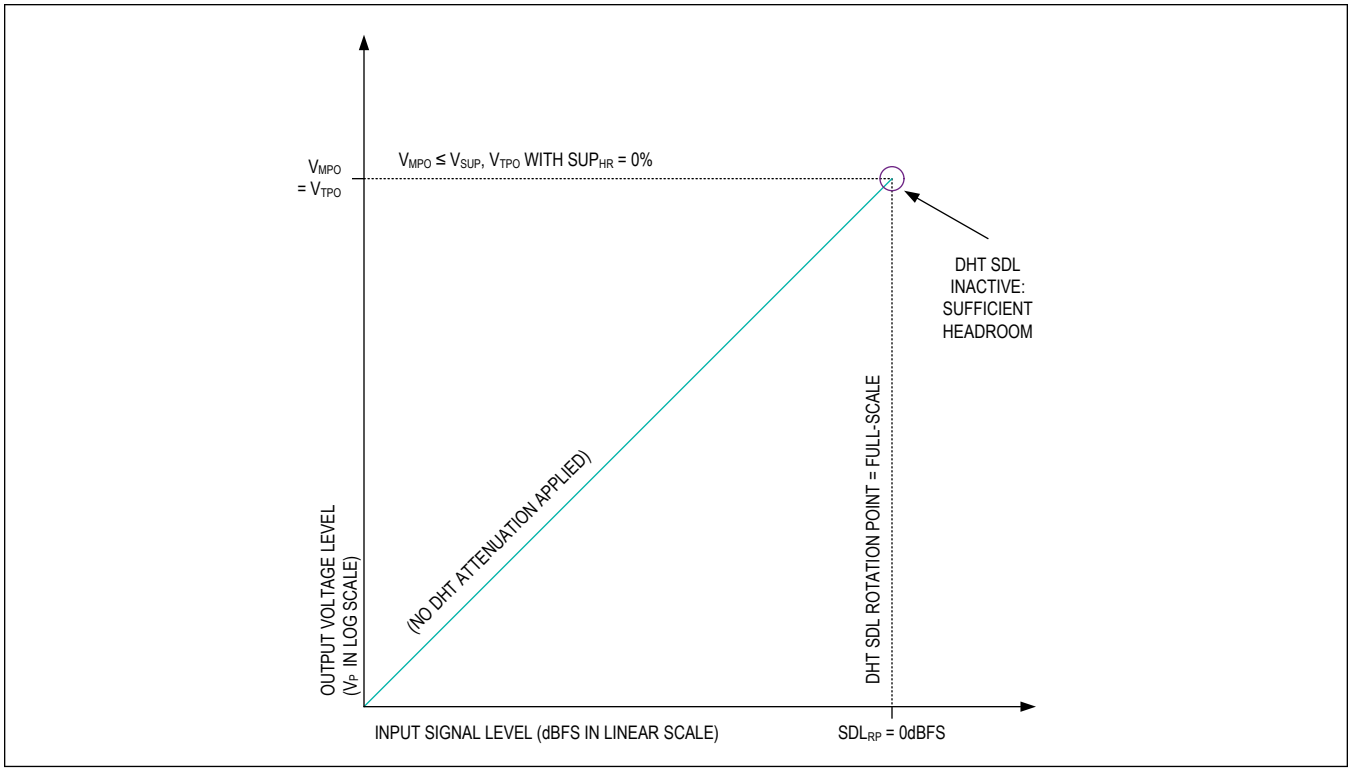


Figure 12. Signal Distortion Limiter with $V_{MPO} \le V_{SUP}$ and 0% Headroom (SUP_{HR})

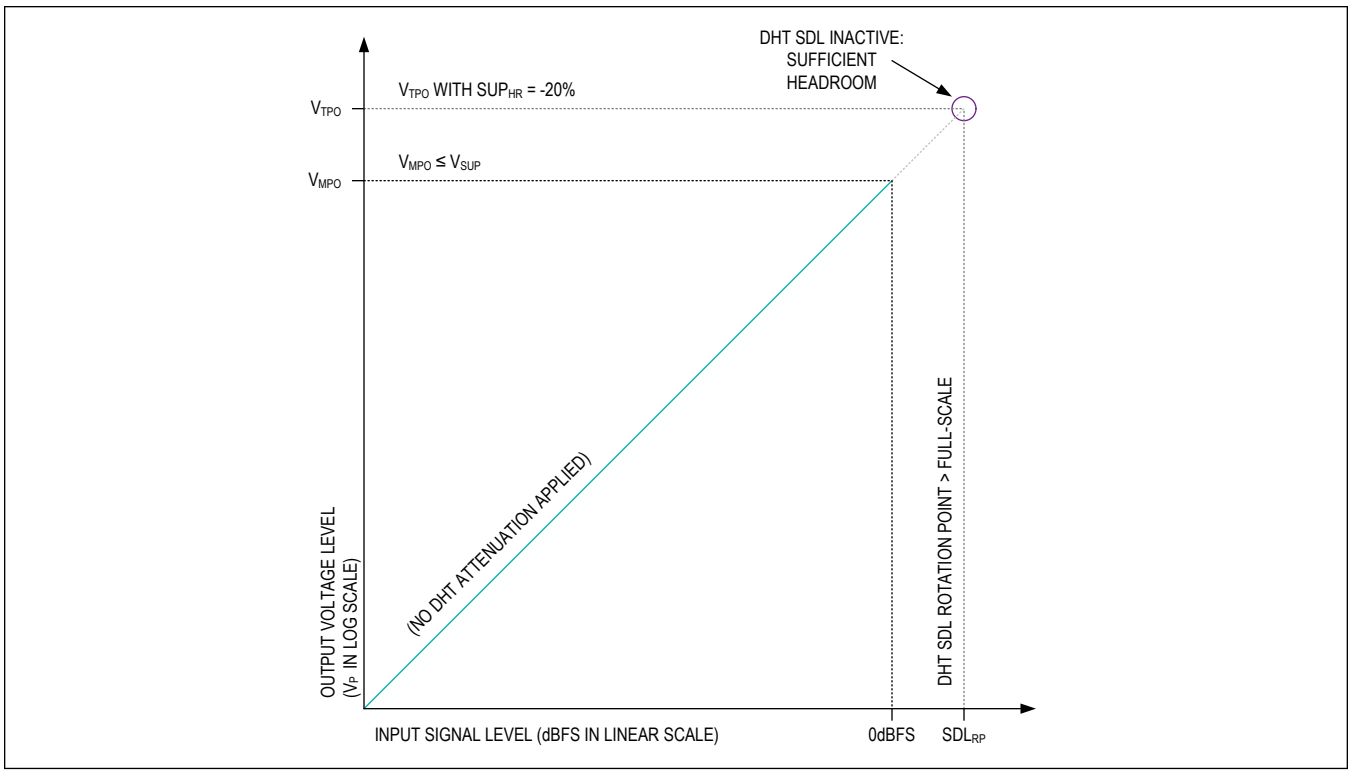


Figure 13. Signal Distortion Limiter with $V_{MPO} \leq V_{SUP}$ and -20% Headroom (SUP_{HR})

As the supply voltage (V_{SUP}) drops further below the maximum peak output voltage (V_{MPO}), the DHT target peak output voltage (V_{TPO}) proportionally scales down. In cases with zero or positive amplifier supply headroom settings (+20% ≥ SUP_{HR} ≥ 0%), the input signal level can exceed the SDL rotation point (SDL_{RP}) before the peak output exceeds V_{SUP}. In this case, amplifier output clipping can be prevented.

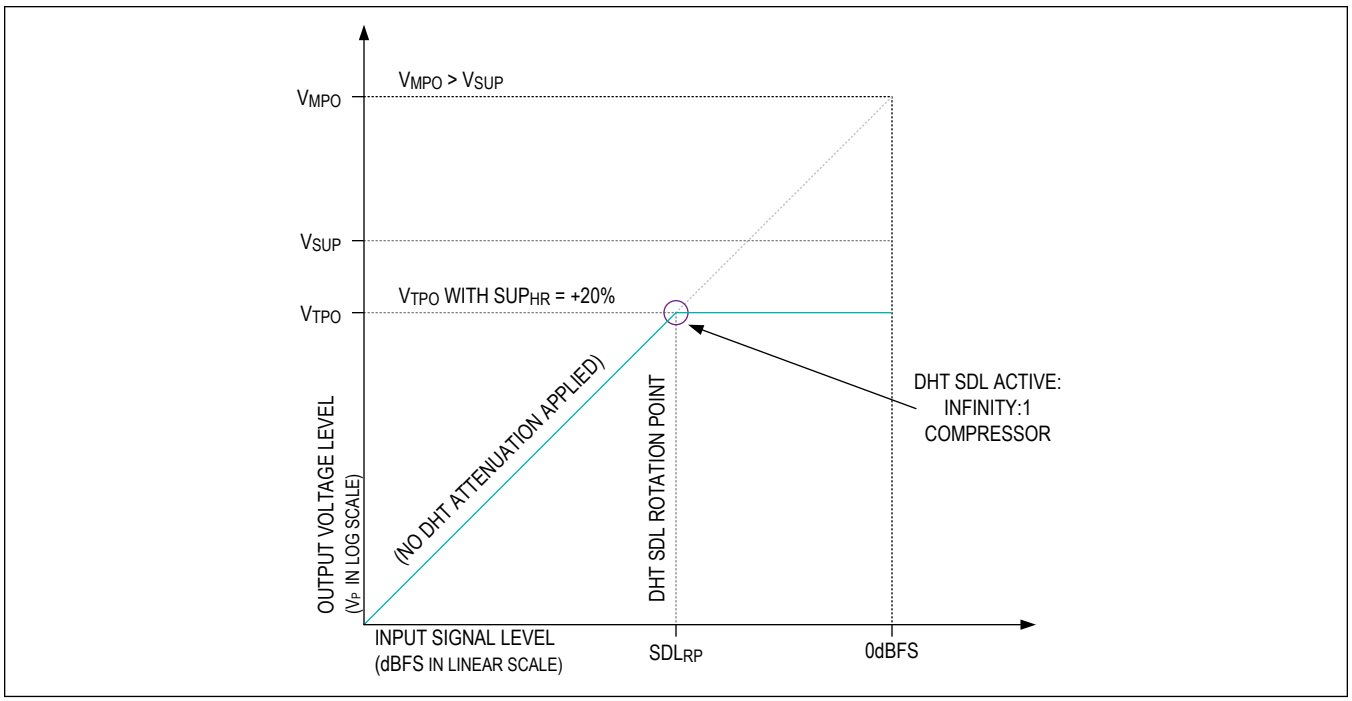


Figure 14. Signal Distortion Limiter with V_{MPO} > V_{SUP} and +20% Headroom (SUP_{HR})

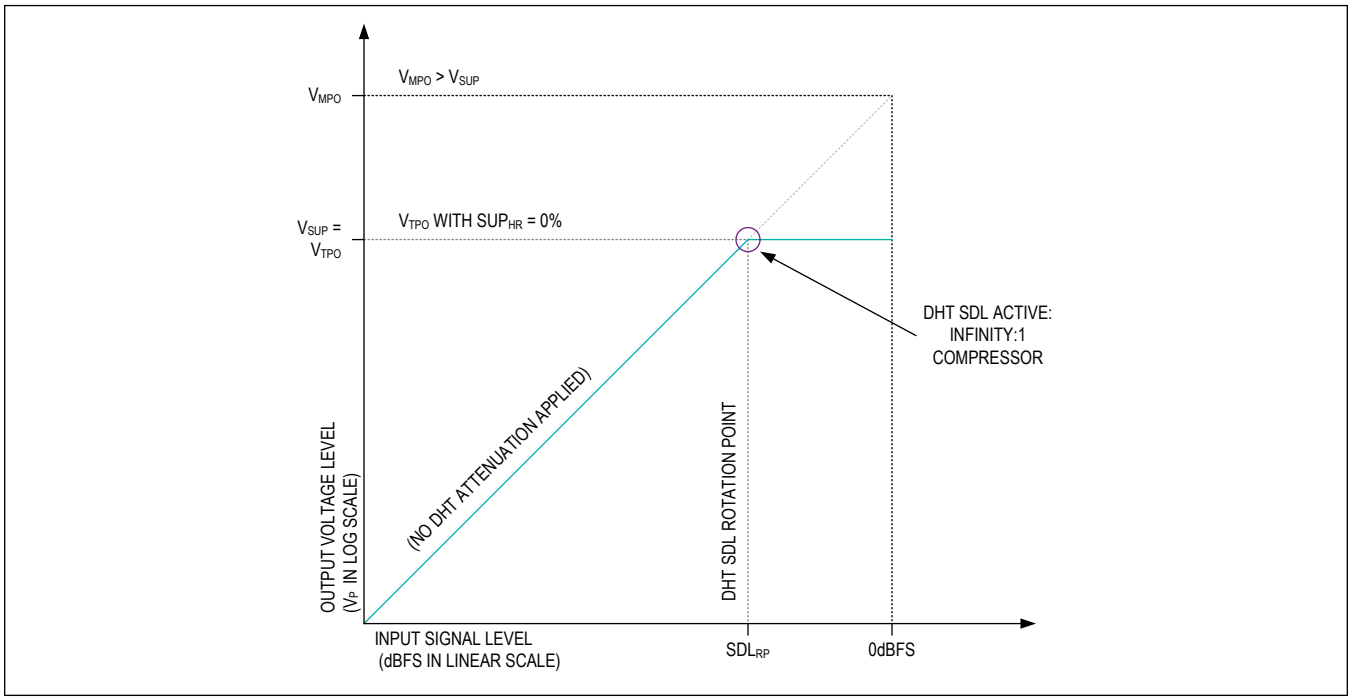


Figure 15. Signal Distortion Limiter with V_{MPO} > V_{SUP} and 0% Headroom (SUP_{HR})

In cases with a negative supply headroom setting (0% > SUP_{HR} ≥ -20%), the input signal does not exceed the SDL_{RP} until after the peak output reaches V_{SUP}. As a result, clipping occurs at the amplifier output. However, once the input signal level exceeds the SDL_{RP}, the audio signal level is digitally limited by the SDL preventing the amplifier output clipping from worsening further.

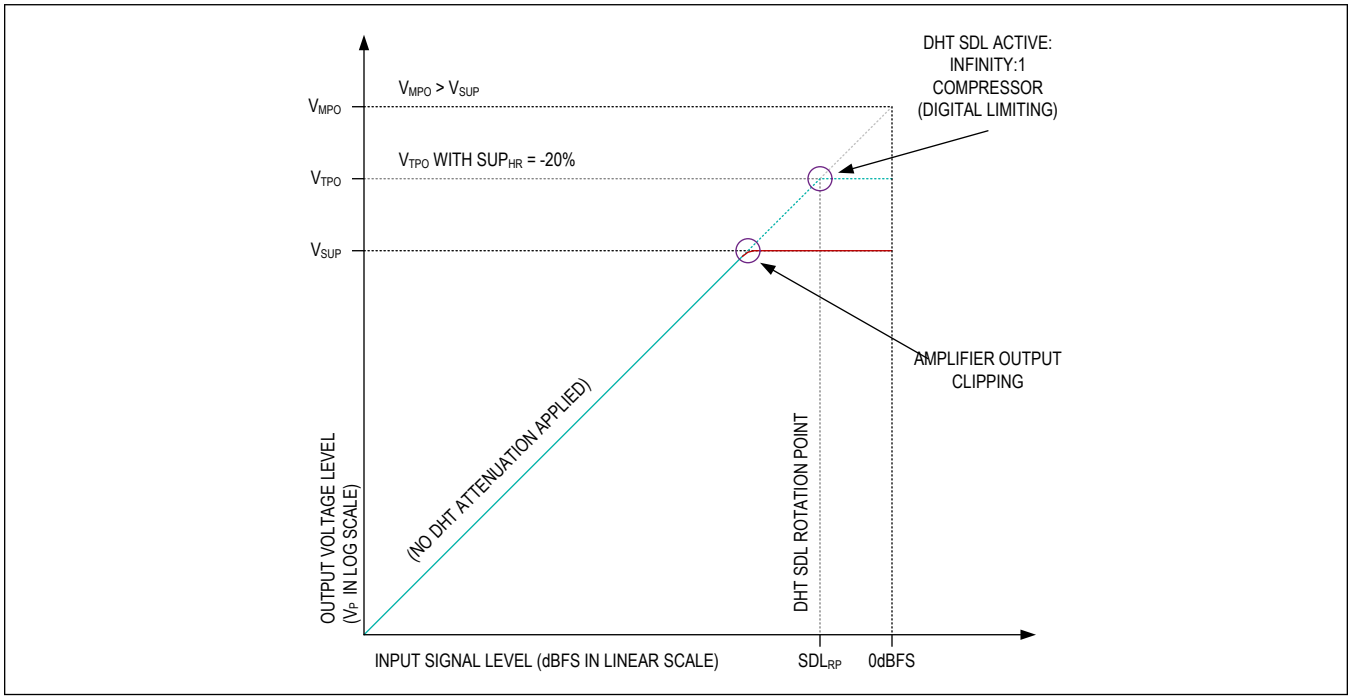


Figure 16. Signal Distortion Limiter with V_{MPO} > V_{SUP} and -20% Headroom (SUPHR)

DHT Mode 2—Signal Level Limiter (SLL)

In DHT mode 2, the limiter is configured as a fixed threshold signal level limiter (SLL). Set the DHT_LIM_MODE bit high to place the limiter function in SLL mode.

Like the signal distortion limiter, the signal level limiter function is a compressor with a ratio of infinity to 1. However, unlike the SDL, the SLL output-referred threshold (SLL_{THR}) is configured to a set level. The SLL_{THR} is selected with the DHT_LIM_THRES bit field from a range of 0dBFS to -15dBFS. The SLL threshold can also be expressed as an input-referred knee or rotation point (SLL_{RP}) which is equal to SLL_{THR} in mode 2. The SLL amplifier peak output voltage limit (V_{SLL}) is calculated from the selected SLL threshold (SLL_{THR}) and maximum peak output voltage (V_{MPO}) with the following equation:

SLL PEAK OUTPUT VOLTAGE LIMIT = V_{SLL} = V_{MPO} x 10 ^(SLL_{THR}/20)

The transfer function for signal levels below the SLL threshold (SLL_{THR}) is unchanged. When the signal level exceeds the SLL_{THR}, the signal level limiter function is applied to the signal path. As the input signal level increases, the limiter attenuation continues to increase as well and can be calculated for a given input signal level (A_{INPUT} in dBFS) relative to SLL_{RP} (= SLL_{THR}) as follows:

SLL ATTENUATION = SLL_{RP}–A_{INPUT}

When V_{TPO} is greater than V_{SLL}, the amplifier peak output level is limited to V_{SLL} whenever the signal amplitude exceeds the SLL threshold (SLL_{THR}). As a result of the fixed SLL threshold and rotation point, the transfer function is identical for any V_{SUP} level and corresponding V_{TPO} that is greater than V_{SLL}.

This is illustrated in Figure 17 for decreasing V_{SUP} and V_{TPO} levels. As V_{SUP} decreases, V_{TPO} is recalculated and decreases as well. Three different, progressively lower V_{TPO} levels are shown (V_{TPO1}, V_{TPO2}, and V_{TPO3}). Due to the fixed SLL threshold, V_{SLL} is the same in all three cases. Since all three V_{TPO} values are greater than V_{SLL}, the transfer function for each case is identical and is limited at V_{SLL}.

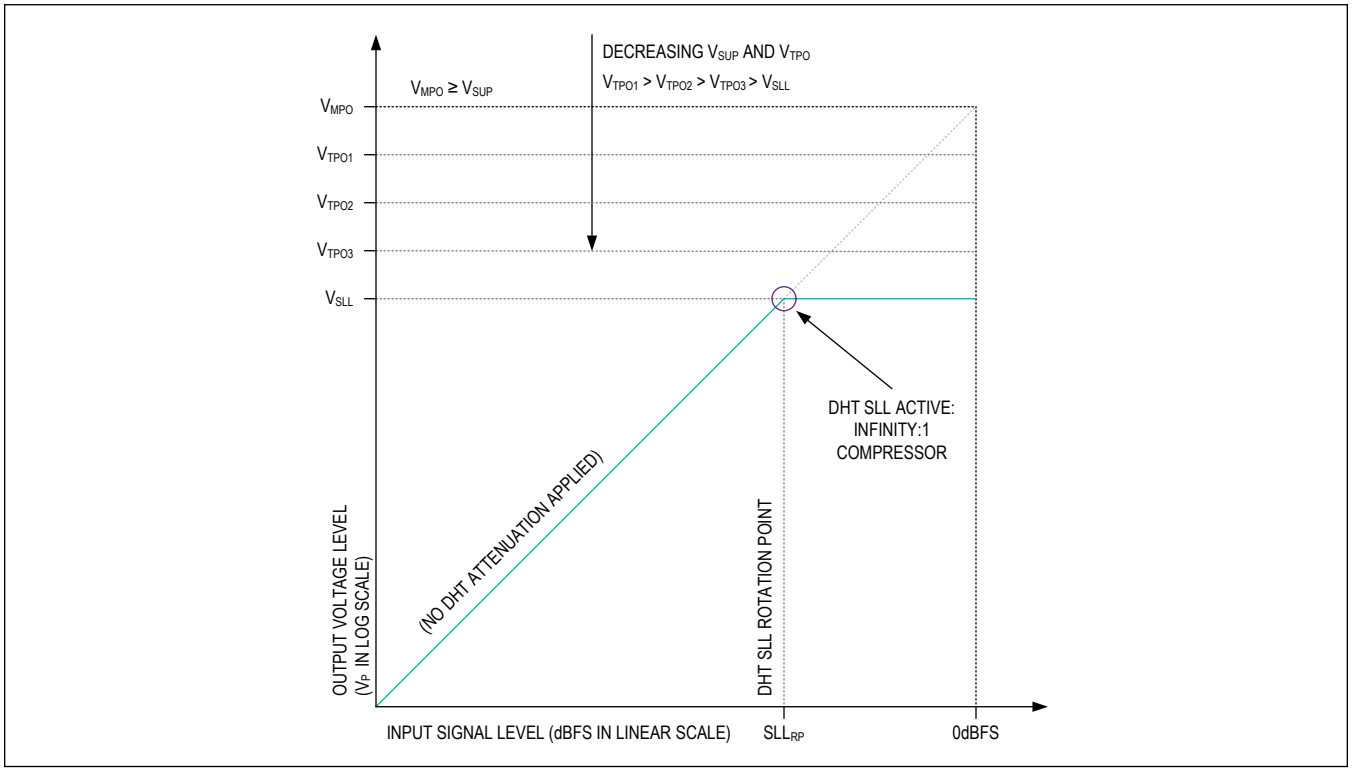


Figure 17. Signal Level Limiter with $V_{TPO} > V_{SLL}$ as V_{SUP} Decreases

When the V_{TPO} is less than V_{SLL}, the amplifier output can clip before the input signal amplitude exceeds the SLL rotation point ($SLL_{RP} = SLL_{THR}$). As the input signal level continues to increase, once it exceeds SLL_{RP} the signal level is digitally limited preventing the amplifier output clipping from worsening further. Because both the SLL threshold and rotation point are fixed relative to full-scale, as V_{SUP} continues to decrease, the clipping at the amplifier output grows progressively worse before the input signal exceeds SLL_{RP} (= SLL_{THR}).

Figure 18 has the same SLL settings as Figure 17 (same SLL_{THR}). For simplicity, $V_{TPO} = V_{SUP}$ (SUP_{HR} = 0%), and V_{TPO} has decreased further and is now less than V_{SLL}. As a result, the amplifier output clips before the SLL digitally limits the signal level.

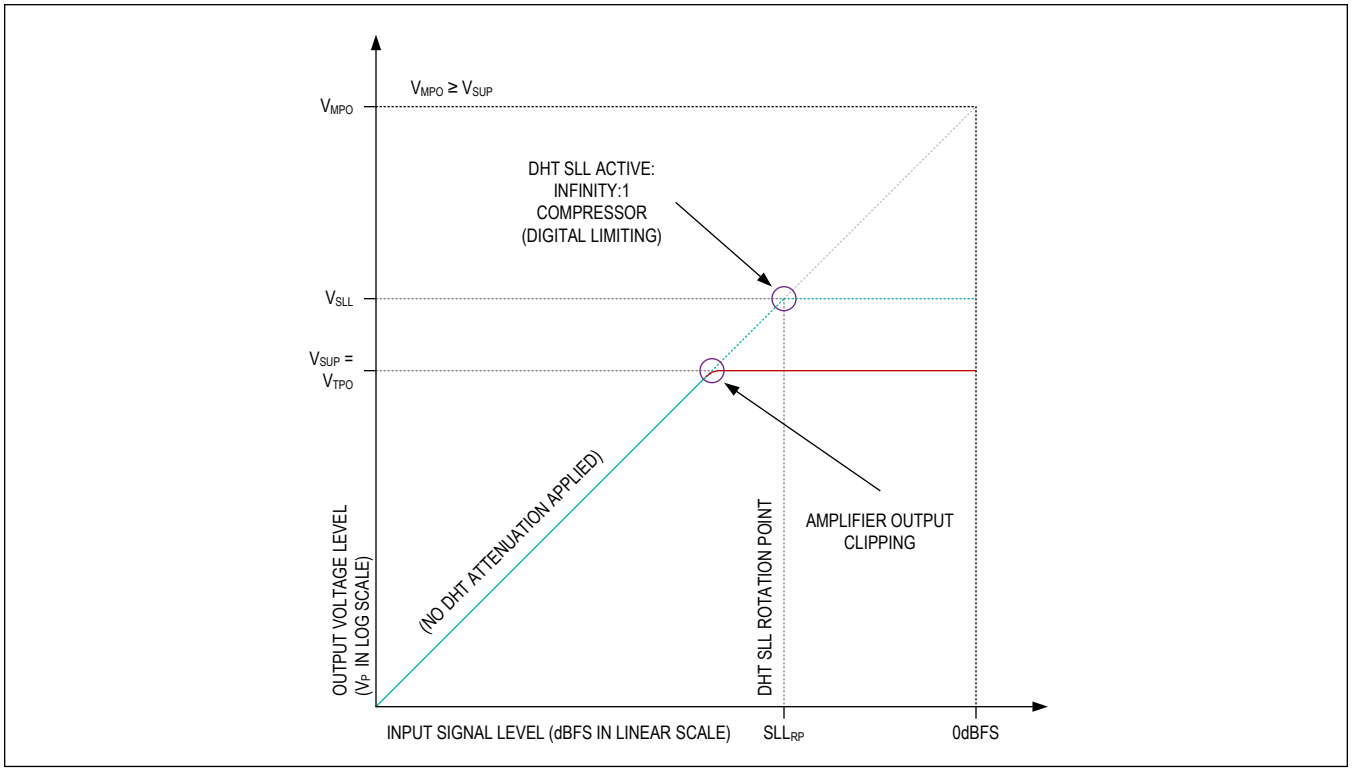


Figure 18. Signal Level Limiter with V_{TPO} < V_{SLL} Showing Amplifier Output Clipping

DHT Attenuation

When the DHT block first applies attenuation, an interrupt is generated (DHT_ACTIVE_BGN_*). When the DHT block fully releases all applied attenuation (i.e., DHT is inactive), an interrupt is generated (DHT_ACTIVE_END_*). Interrupts are not generated when DHT is actively adjusting the level of attenuation.

The maximum attenuation (A_{MAX}) applied to the audio signal by the DHT functions is selected with the DHT_MAX_ATN bit field. The maximum attenuation can be set from -1dB to -15dB with a 1dB step size. The configured DHT functions stop further attenuation of the audio signal once the calculated attenuation (relative to the unattenuated input signal level) reaches the selected maximum attenuation (A_{MAX}). If the calculated attenuation (based on input signal level and measured V_{SUP}) exceeds the selected maximum attenuation (A_{MAX}), the applied attenuation is set equal to (limited at) A_{MAX}. This can occur anytime the target peak output (V_{TPO}) to maximum peak output (V_{MPO}) ratio or peak output attenuation (denoted A_{TPO}) is less than (or has a larger absolute value than) A_{MAX}.

All previous examples showcase where the peak output attenuation (A_{TPO}) did not exceed the selected maximum attenuation (A_{MAX}). The following figures show signal distortion limiter use cases where V_{SUP} has decreased until A_{TPO} < A_{MAX}.

In Figure 19, the SUP_{HR} is set to -20%. Since A_{TPO} < A_{MAX}, the attenuation applied by the distortion limiter reaches the programmed maximum attenuation level before the input signal reaches full-scale. For input signals past the point where calculated attenuation is equal to A_{MAX}, the attenuation stops increasing and is now fixed at A_{MAX}. As a result, past this point, the audio signal (in the digital domain) begins to increase. This results in the distortion increasing at the amplifier output (which was already clipping at the limited level of distortion).

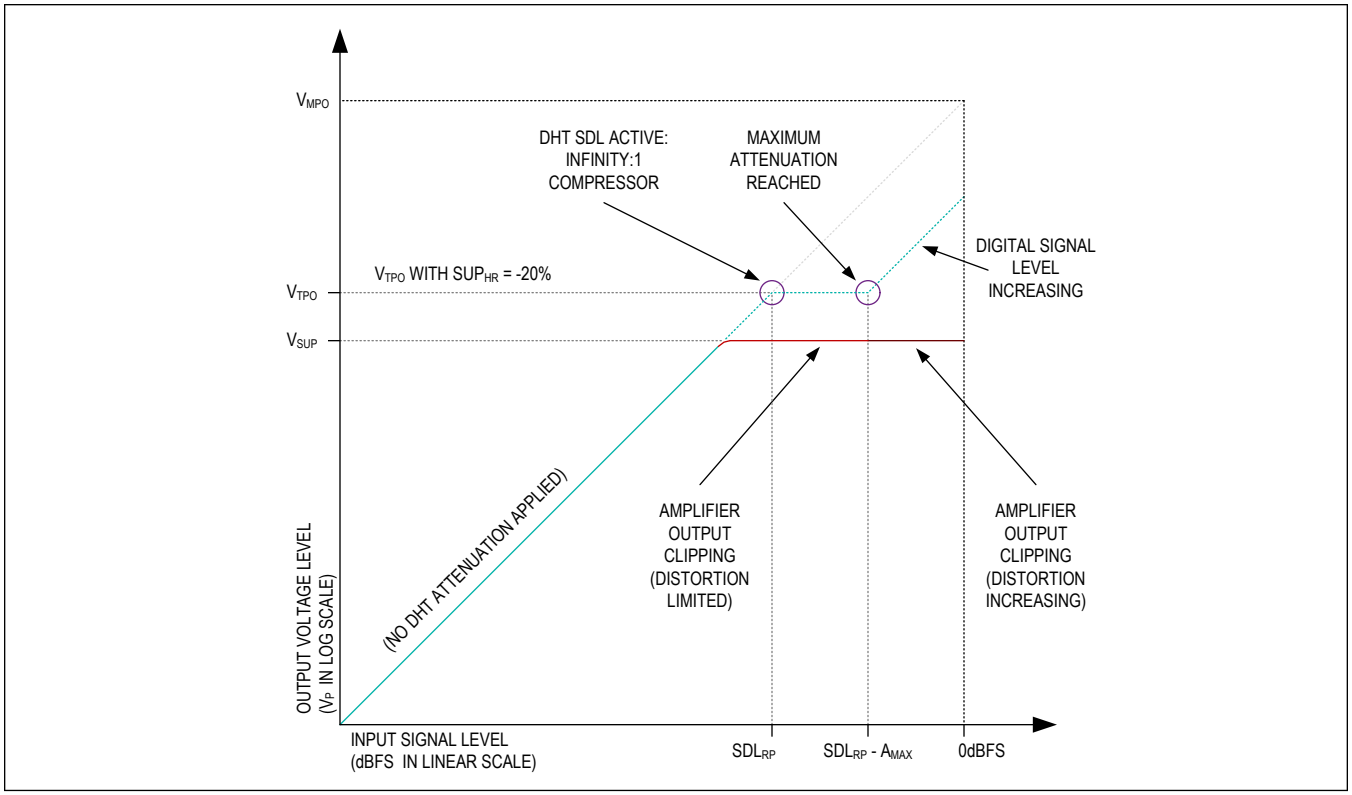


Figure 19. Distortion Limiter Case with -20% Headroom and A_{MAX} Exceeded

In Figure 20, the supply headroom is set to +20%. As before, the attenuation applied by the SDL reaches the selected maximum attenuation (A_{MAX}) before the input signal reaches full-scale. Past this point, the audio signal (in the digital domain) begins increasing and the signal level (and any distortion) at the amplifier output increases as well. In this case, the amplifier output was not clipping until after A_{MAX} was exceeded.

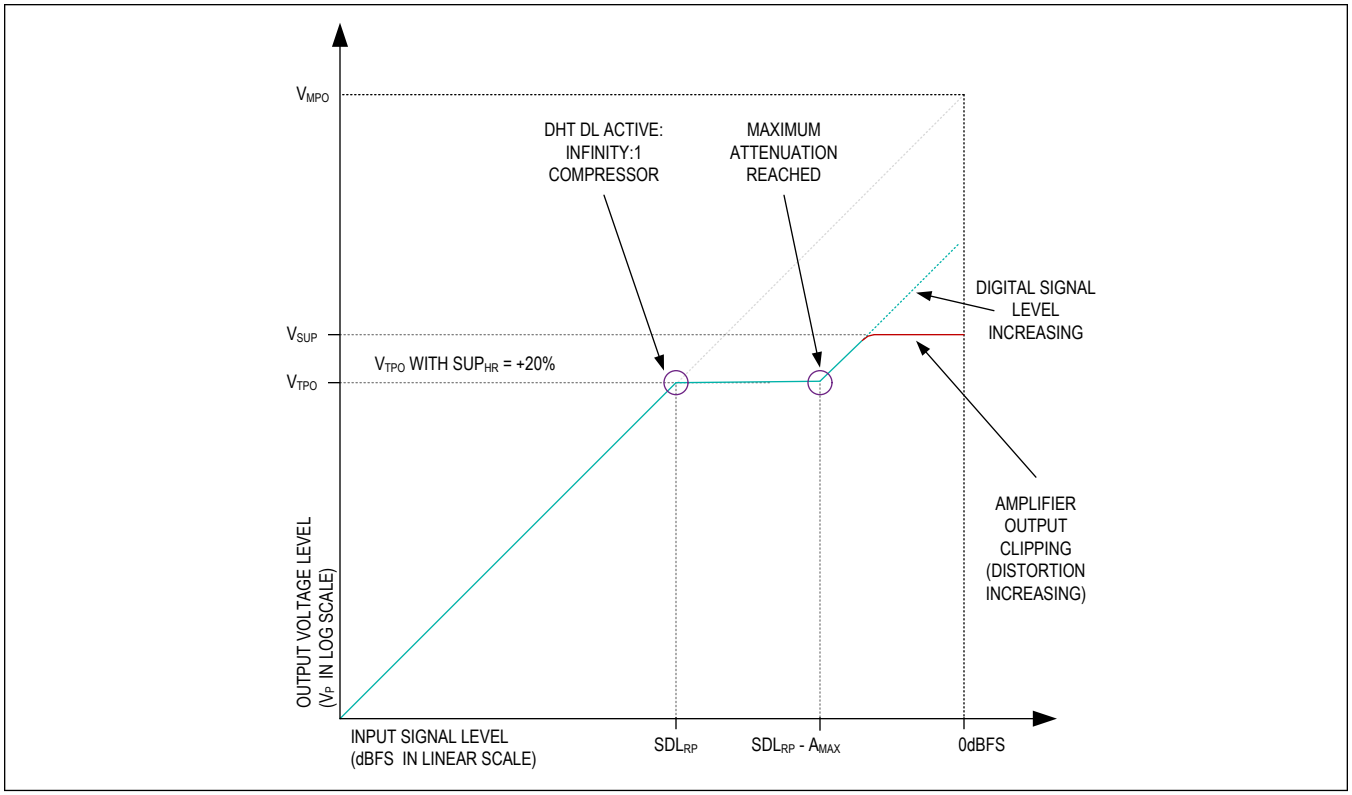


Figure 20. Distortion Limiter Case with +20% Headroom and A_{MAX} Exceeded

DHT Ballistics

When the signal level exceeds the threshold for a configured DHT function (SDL or SLL) or continues to increase beyond this point, the appropriate level of attenuation is applied to the signal level at the programmed attack rate. The DHT attack rate is selected with the DHT_ATK_RATE bit field.

The change in input signal level is detected by a peak detect circuit which has a fixed 3.5ms release time. When the signal level decreases or drops below the threshold for a configured DHT function (SDL or SLL), the appropriate level of applied attenuation is released. The DHT release rate is selected with the DHT_RLS_RATE bit field. However, due to the 3.5ms/dB peak detector, the 2ms/dB release rate is effectively 3.5ms/dB. All other release rates have a fixed delta of 3.5ms compared to the programmed release rate.

The attack-and-release behavior is a bit different when triggered by a change in the active amplifier supply level. When the supply level decreases and triggers a DHT function attack, the attenuation is applied quickly at the configured attack rate. Likewise, as the supply level increases, the attenuation is released at the configured release rate. However, if DHT supply hysteresis is enabled (DHT_SUPPLY_HYST_EN = 1), then as the supply increases, the applied DHT function does not release attenuation until the increase in the supply level exceeds the programmed DHT supply hysteresis level (DHT_SUPPLY_HYST). Once the supply increase exceeds the hysteresis, the appropriate level of applied attenuation is released at the configured release rate.

Charge Pump Boost

The MAX98380 features a charge pump tripler that boosts the V_{BAT} supply voltage to PVDD to power the Class-D speaker amplifier. The device features a soft-start sequence to minimize inrush current and voltage overshoot on power-up. When the IC is enabled, the soft-start ramps the charge pump output (PVDD) to its final value in a fixed time (set by CP_SOFT_TIMER) while maintaining a current limit of $I_{STARTUP}$ (see the *Electrical Characteristics* table). Maximum load current is available after the soft-start is completed. The CP_SOFT_TIMER setting is dependent on the effective capacitance of the flying capacitor and PVDD decoupling capacitor. If the timer is set too low, the PVDD does not settle

to its final value at the end of the soft-start time, and the device sees a high inrush current thereafter. The recommended soft timer settings for different capacitors is shown in Table 4.

Table 4. Charge Pump Soft Timer Settings

FLYING CAPACITOR VALUES	CAPACITOR TYPE	CP_SOFT_TIMER SETTING	SOFT TIMER (ms)
Nominal (2x2.2µF/2x2.2µF)	0402	0x3	1.5
Double flying caps (4x2.2µF/4x2.2µF)	0402	0x4	2.0
Oversized capacitors (22µF/22µF)	0805	0x6	3.0

The charge pump clock frequency can be configured by setting the *CP_CLK_SEL* bits. However, the charge pump frequency is automatically changed in quiescent conditions to get the lowest power consumption.

The part also features a boost bypass mode that is set using the *BST_BYPASS_MODE* bit field. By default, the *BST_BYPASS_MODE* bit field is set to 0 and the charge pump tripler is enabled and the Class-D amplifier is powered by the voltage V_{PVDD} (see the *Electrical Characteristics* table). When the *BST_BYPASS_MODE* bit field is set to 1, the charge pump operates in bypass mode, and the PVDD voltage is set to the V_{BAT} supply.

Dynamic Boost Control (DBC)

For increased efficiency, the charge pump boost can be configured to operate in the dynamic boost control (DBC) mode. In DBC mode, the boost bypass is controlled dynamically using the LSB of the digital audio stream sourced from a host DSP. Using a simple software routine, the host DSP analyzes the incoming digital audio, and based on a predetermined threshold level, modifies the LSB to 0 or 1 before sending it to the amplifier. This results in significant power savings, both during quiescent, and active playback.

Speaker Amplifier

The filterless Class-D amplifier offers much higher efficiency than Class-AB amplifiers. The high efficiency of a Class-D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class-D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Class-D Output Short-Circuit Protection

If the output current limit of the Class-D amplifier (I_{LIM}) is exceeded (see the *Electrical Characteristics* table), the outputs are disabled for approximately 27ms. At the end of the 27ms, the outputs are re-enabled. If the fault condition still exists, the outputs continue to disable and re-enable until the fault condition is removed.

Click-and-Pop Suppression

The speaker amplifier features ADI's comprehensive click-and-pop suppression. During turn-on, the click-and-pop suppression circuitry reduces audible transient sources internal to the device. When entering shutdown or standby, the differential speaker outputs simultaneously go to Hi-Z.

The comprehensive click-and-pop suppression of the MAX98380 is unaffected by power-up or power-down sequencing. Applying or removing the clocks before or after the transition of $\overline{RESET}$ yields the same click-and-pop performance. However, when volume ramping is enabled, the clocks and V_{DD} must remain valid for 13ms after $\overline{RESET}$ goes high to allow for volume ramping to complete for best click-and-pop performance.

Ultra-Low EMI Filterless Output Stage

Traditional Class-D amplifiers require the use of external LC filters or shielding to meet EN55022B electromagnetic interference (EMI) regulation standards. ADI's active emissions-limiting, edge-rate control circuitry, and spread-spectrum modulation reduce EMI emissions while maintaining high efficiency.

ADI's spread-spectrum modulation mode flattens wideband spectral components while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The device's spread-spectrum modulator randomly varies the switching frequency by f_{SSM} around the center frequency (f_{SW}). Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Measurement ADC

The device features a configurable measurement ADC. By default, the ADC has a 9-bit resolution but can be configured for 8-bit resolution by programming the ADC_MODE bit field to 1 (by default ADC_MODE = 0). This allows the user to trade accuracy for faster ADC conversion speed. The measurement ADC has two channels, one for die temperature measurement (measurement ADC thermal channel) and one for PVDD supply voltage measurement (measurement ADC PVDD channel). Enabled channels are measured sequentially and continuously. Each channel separately provides an optional programmable lowpass IIR filter.

Measurement ADC Thermal Channel

When the device is clocked and in the active state (EN = 1), the measurement ADC thermal channel automatically activates. When active, it continuously measures and reports the device die temperature over the range from -29°C to +150°C)

The output of the thermal ADC channel can be read back through the MEAS_ADC_THERM_DATA bit field and is the input to both the thermal protection and thermal foldback blocks. By default (*MEAS_ADC_THERM_RD_MODE* = 0), the thermal readback value is automatically updated after each conversion is completed. Setting *MEAS_ADC_THERM_RD_MODE* to 1 places thermal readback into manual mode. In manual mode, the thermal readback result is updated manually when a 1 is written to the *MEAS_ADC_THERM_RD_UPD* bit field. The ADC thermal channel data readback in manual mode is 9 bits (by default) and 8 bits (when ADC_MODE = 1). In the automatic readback mode, for the 9 bit ADC resolution mode, since the data readback is from two registers, the LSB register is not guaranteed to be synchronous with the MSB register and can result in higher noise in automatic mode.

The thermal ADC channel also provides an optional lowpass IIR filter with a programmable bandwidth that scales relative to the measurement ADC sample rate. The filter is enabled with the MEAS_ADC_TEMP_FILT_EN bit field, and the bandwidth is set with the MEAS_ADC_TEMP_FILT_COEFF bit field.

Measurement ADC PVDD Channel

When the device is clocked and in the active state (EN = 1), the measurement ADC PVDD channel can be enabled. The PVDD channel is manually enabled by setting the *MEAS_ADC_PVDD_EN* bit to 1 and must be manually enabled for the DHT to operate. When the channel is enabled, it continuously measures and reports the PVDD supply voltage level over the range of 2.5V to 15V.

The output of the measurement ADC PVDD channel can be readback through the MEAS_ADC_PVDD_DATA bit field and is routed to the DHT. By default (*MEAS_ADC_PVDD_RD_MODE* = 0), the PVDD readback value is automatically updated after each conversion is completed. Setting *MEAS_ADC_PVDD_RD_MODE* to 1 places PVDD readback into manual mode. In manual mode, the readback result is updated when a 1 is written to the *MEAS_ADC_PVDD_RD_UPD* bit field. The ADC PVDD channel data read back in manual mode is 9 bits (by default) and 8 bits (when ADC_MODE = 1). In the automatic readback mode, for the 9 bit ADC resolution mode, since the data readback is from two registers, the LSB register is not guaranteed to be synchronous with the MSB register and can result in higher noise in automatic mode.

The lowest measured PVDD measurement result is read back through the *LOWEST_PVDD_DATA_MSB* and LOWEST_PVDD_DATA_LSB bit fields. These bit fields both automatically clear and are reset to the value of the current measurement result immediately after LSB readback is completed.

The PVDD channel also provides an optional lowpass IIR filter with a programmable bandwidth that scales relative to the measurement ADC sample rate. The filter is enabled with the MEAS_ADC_PVDD_FILT_EN bit and the bandwidth is set with the MEAS_ADC_PVDD_FILT_COEFF bit field. When DHT operation is desired, it is recommended to enable the filter (MEAS_ADC_PVDD_FILT_EN = 1) and set the filter bandwidth to 300kHz (MEAS_ADC_PVDD_FILT_COEFF = 0x4).

Thermal Protection

When the device is active, the measurement ADC thermal channel is automatically enabled and monitors die temperature to ensure that it does not exceed the configured thermal thresholds.

Thermal Warning and Thermal Shutdown Configuration

The thermal-warning threshold is configured by the *THERMWARN_THRESH[5:0]* bit field and the thermal-shutdown

threshold is configured by the *THERMSHDN_THRESH*[5:0] bit field. When die temperature is decreasing, hysteresis is applied to both thresholds. The temperature hysteresis is configured by the *THERM_HYST* bit field.

Thermal Shutdown Recovery Configuration

The device thermal-shutdown-recovery behavior is determined by the state of the *THERM_AUTORESTART_EN* bit. When the *THERM_AUTORESTART_EN* bit is set to 0, the thermal-shutdown recovery is in manual mode. In manual mode, when the die temperature exceeds the thermal-shutdown threshold, the amplifier output is automatically disabled. Once the die temperature drops below the thermal-warning threshold minus the hysteresis, the device is placed into software shutdown (*EN* is set to 0) and remains in that state until the host manually re-enables the device.

When the *THERM_AUTORESTART_EN* bit is set to 1, the thermal-shutdown recovery is in automatic mode. In automatic mode, when the die temperature exceeds the thermal-shutdown threshold, the amplifier is automatically disabled. Once the die temperature drops below the thermal-warning threshold minus the hysteresis, the amplifier is automatically re-enabled.

Thermal Foldback

The device features thermal foldback to allow for a smoother audio response to high-temperature events. Thermal foldback is enabled by setting the *THERMFB_EN* bit to 1. Once enabled, when the die temperature exceeds the configured thermal-warning threshold (+120°C by default), attenuation is applied to the speaker amplifier path. As the die temperature increases, the level of attenuation also increases proportionally up to a maximum level of -12dB (unless the thermal-shutdown threshold is exceeded first). Likewise, as die temperature decreases (including hysteresis and hold time), the applied attenuation also proportionally decreases. The slope of the thermal-foldback attenuation is programmed with the *THERMFB_SLOPE* bit field.

When thermal foldback is active, the attack time for a gain change can be a maximum of 2 samples. Additionally, there is up to a 7 sample delay in the signal path attenuation due to the group delay of the amplifier. The attenuation release rate (for decreasing temperature) is programmable and is configured with the *THERMFB_RLS* bit field. When the die temperature starts to decrease and drops below the maximum temperature minus the programmed hysteresis level, the attenuation starts to release after the programmed hold time (set with the *THERMFB_HOLD* bit field, thermal foldback settings).

I²C Serial Interface

The I²C serial control interface is activated when the device detects a valid I²C start condition at the SCL and SDA pins.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. The seven most significant bits are programmable through the ADDR connection as shown in Table 5. The device does not communicate if ADDR is unconnected. Setting the read/write bit to 1 configures the device for read mode. Setting the read/write bit to 0 configures the device for write mode. The address is the first byte of information sent to the IC after the START condition.

Table 5. I²C Slave Address

ADDR CONNECTION	I²C SLAVE ADDRESS (BINARY)	I²C WRITE ADDRESS (BINARY)	I²C READ ADDRESS (BINARY)
Connected to DVDD	0111000x	01110000	01110001
Connected to GND	0111001x	01110010	01110011
Connected to SDA	0111010x	01110100	01110101
Connected to SCL	0111011x	01110110	01110111

The IC features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 1MHz. Figure 21 shows the 2-wire interface timing diagram. The master generates SCL and initiates a data transfer on the bus. The master device writes data to the IC by transmitting the proper slave address followed by two register address bytes (most significant byte first) and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL

pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

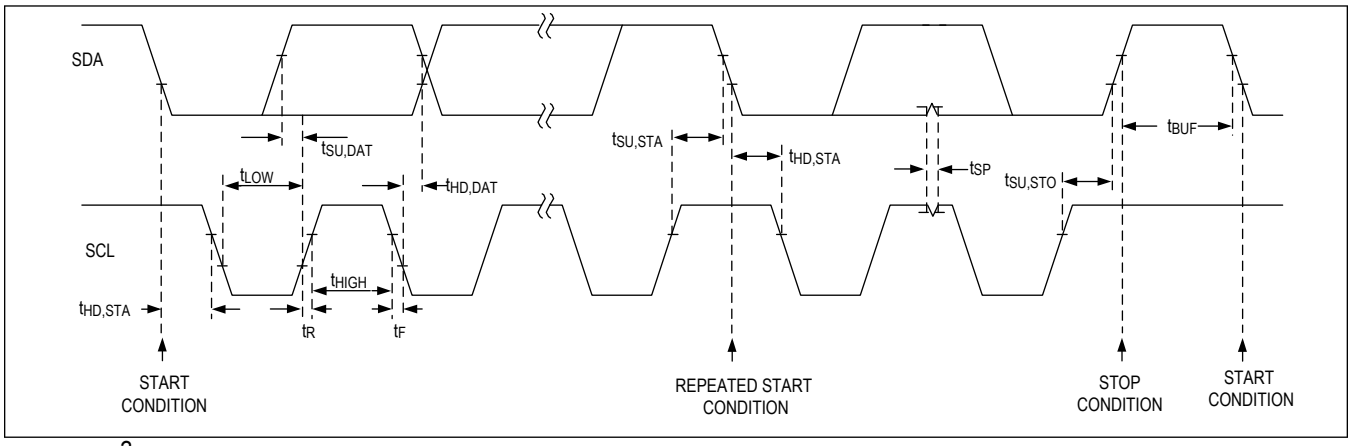


Figure 21. I²C Interface Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

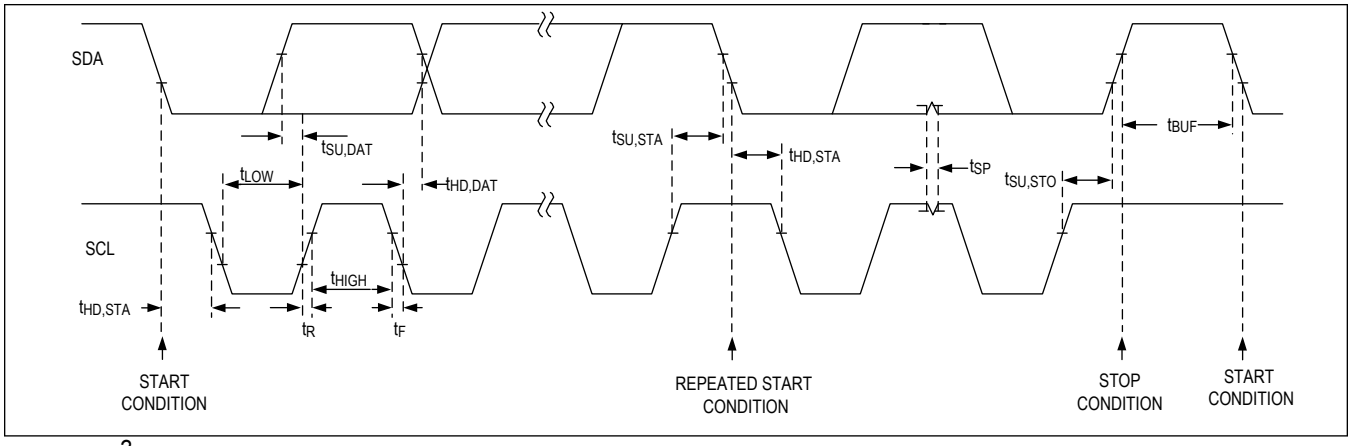


Figure 22. I²C START, STOP, and REPEATED START Conditions

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt each byte of data when in write mode. The IC pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

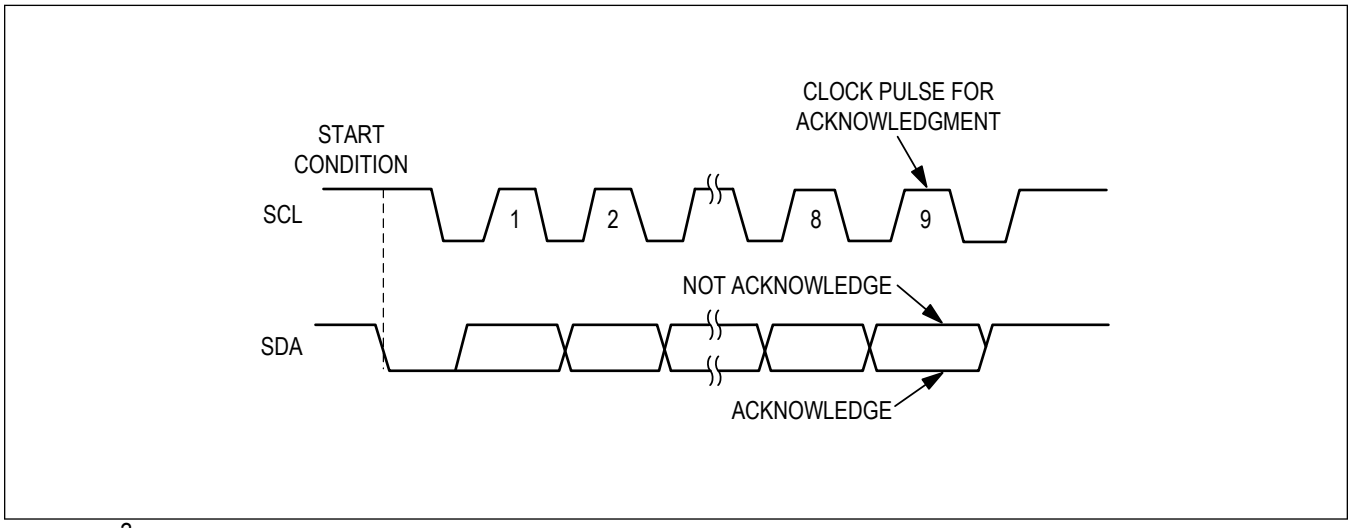


Figure 23. I^2C Acknowledge

Write Data Format

A write to the IC includes the transmission of a START condition, the slave address with the R/W bit set to 0, two bytes of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second and third bytes transmitted from the master configure the ICs internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that is written to the chosen register. An acknowledge pulse from the IC signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

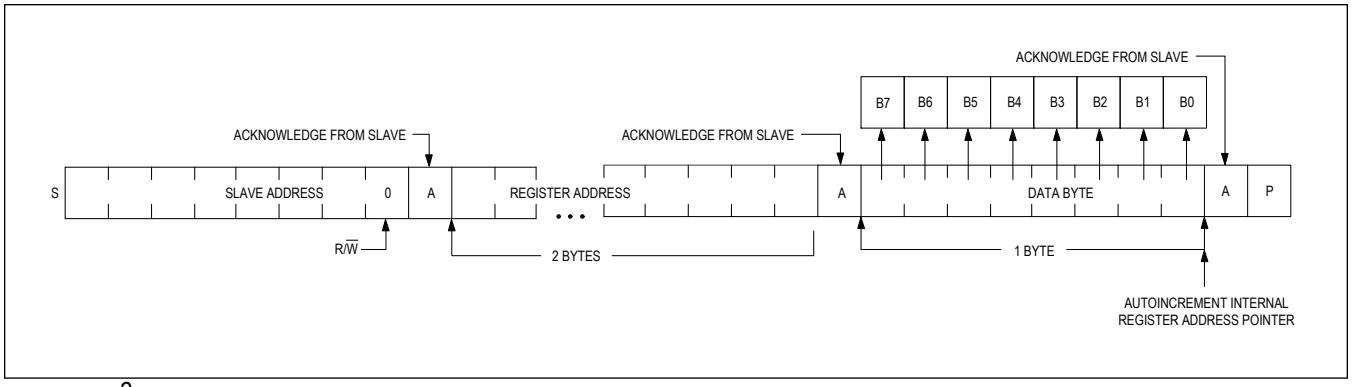


Figure 24. I²C Writing One Byte of Data to the Slave

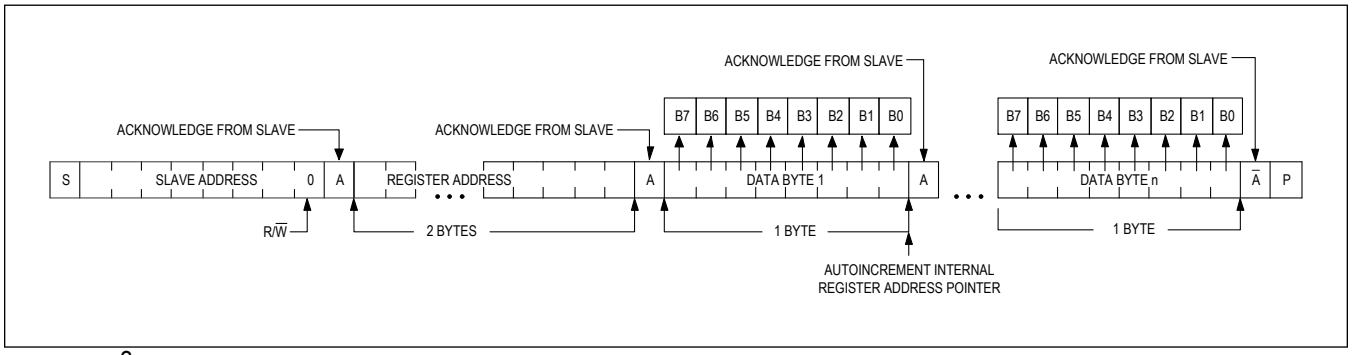


Figure 25. I²C Writing n-Bytes of Data to the Slave

Read Data Format

Send the slave address with the R/W bit set to 1 to initiate a read operation. The IC acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x2000.

The first byte transmitted from the IC is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the ICs slave address with the R/W bit set to 0 followed by the two-byte register address. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The IC then transmits the contents of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition.

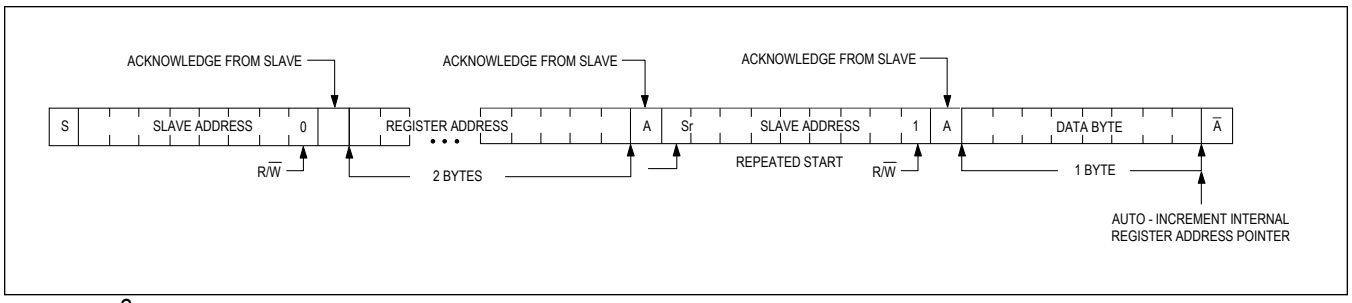


Figure 26. I²C Reading One Byte of Data from the Slave

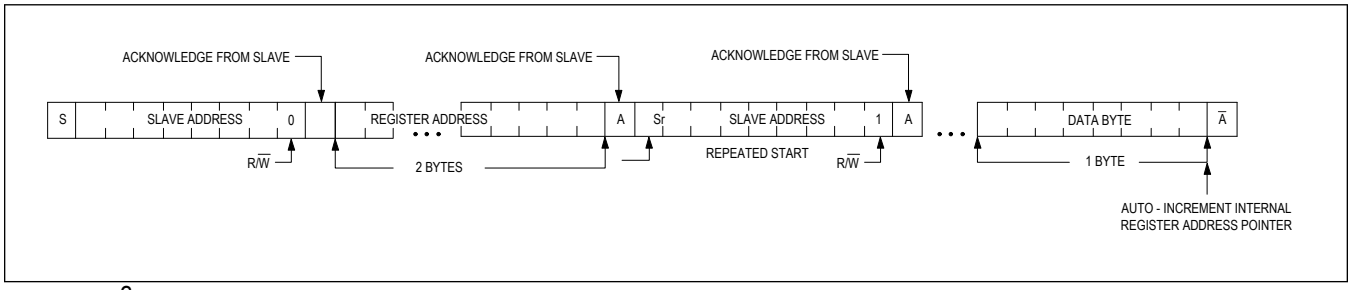


Figure 27. I²C Reading n-Bytes of Data from the Slave

I²C Register Map

Control Bit Field Types and Write Access Restrictions

The device control bit fields fall into one of three basic types: read, write, or read and write. There are no read restrictions, and any read-enabled bit field can be read back anytime the I²C control interface is active. However, there are write restrictions, and every write-enabled bit field falls into one of two write access subtypes.

The first write access subtype is dynamic. Dynamic bit fields effectively have no write access restrictions and can be safely changed (written) in any device state where the I²C control interface is active. The second bit field access subtype is restricted. Restricted bit fields should only be changed (written) when the related functional block (as shown in Table 6) is powered down.

If the write access is restricted to the global enable (restrictions EN and ENL), then the restricted bit field should only be changed (written) when the device is in software shutdown. As a form of system protection, write access to some critical global enable restricted bit fields (ENL) is locked out by the hardware when the device is not in the software-shutdown state. Attempting to change (write to) these locked restricted bit fields when the device is not in the software-shutdown state has no effect (read access is still allowed).

The bit field type and write access subtype are provided for every bit field in the detailed register description tables. For all bit fields with the restricted subtype, the dependency is also denoted in the "RES" column.

Table 6 provides a detailed description of all device register types, access subtypes, and restriction dependencies that are used by this device. The write access restrictions describe the specific device condition(s) that should be met (and the corresponding bit field settings) before the system attempts to change (write to) bit fields with that restriction type.

Table 6. Control Bit Types and Write Access Restrictions

BIT FIELD TYPE	WRITE ACCESS	WRITE ACCESS RESTRICTIONS		"RES" SYMBOL
		DESCRIPTION	CONDITION	
Read	Read Only	—	—	—
Write or Read/ Write	Dynamic	—	—	—
	Restricted	Device in Software Shutdown	EN = 0	**EN**

Table 6. Control Bit Types and Write Access Restrictions (continued)

		Write Access Locked Out by Hardware Unless the Device is in Software Shutdown	EN = 0	**ENL**
		Speaker Amplifier Output and Feedback Disabled	SPK_EN = 0	**SPK**
		Thermal Foldback Disabled	THERMFB_EN = 0	**TFB**
		Dynamic-Headroom Tracking Disabled	DHT_EN = 0	**DHT**
		PCM Interface Data Input and Output Disabled	PCM_RX_EN = 0	**PCM**

Register Map

Register Map

ADDRESS	NAME	MSB							LSB
Reset									
0x2000	Software Reset[7:0]	–	–	–	–	–	–	–	RST
Status Registers									
0x2001	Status Registers 1[7:0]	VBAT_UVLO_SHDN	FLL_ERR_RAW	CLK_ERR	SPKMON_ERR	SPK_OVC	OTP_FAIL	PWRDN_DONE	PWRUP_DONE
0x2002	Status Registers 2[7:0]	–	–	–	DHT_ACTIVE	THERMSHDN	THERMWARN	THERMFB_BGN	THERMFB_END
Thermal Protection									
0x2020	Thermal Warning Threshhold[7:0]	–	THERMWARN_THRESH[6:0]						
0x2021	Thermal Shutdown Threshold[7:0]	–	THERMSHDN_THRESH[6:0]						
0x2022	Thermal Hysteresis[7:0]	–	–	–	–	–	–	THERM_HYST[1:0]	
0x2023	Thermal Foldback Settings[7:0]	–	–	THERMFB_HOLD[1:0]		THERMFB_RLS[1:0]		THERMFB_SLOPE[1:0]	
0x2027	Thermal Foldback Enable[7:0]	–	–	–	–	–	–	–	THERMFB_EN
Error Monitor									
0x2030	Clock Monitor Config[7:0]	–	–	–	–	–	–	–	CMON_AUTORESTART_EN
0x2037	Error Monitor Control[7:0]	–	–	–	–	SPKMON_EN	–	–	CMON_EN
PCM Registers									
0x2040	PCM Mode Config[7:0]	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]			–	PCM_CHANSEL	–
0x2041	PCM Clock Setup[7:0]	–	–	–	PCM_BCLKEDGE	PCM_BSEL[3:0]			
0x2042	PCM Sample Rate Setup 1[7:0]	–	–	–	–	PCM_SR[3:0]			
0x2043	PCM RX Source 1[7:0]	–	–	–	–	–	–	PCM_DMMIX_CFG[1:0]	
0x2044	PCM RX Source 2[7:0]	PCM_DMMIX_CH1_SOURCE[3:0]				PCM_DMMIX_CH0_SOURCE[3:0]			
0x204F	PCM Rx Enables[7:0]	–	–	–	–	–	–	–	PCM_RX_EN
ChargePump Control									
0x2082	SS TIMER ADJUST[7:0]	CP_CLK_SEL[1:0]		CP_SOFT_TIMER[5:0]					
Speaker Path Control									
0x2090	AMP volume control[7:0]	–	SPK_VOL[6:0]						
0x2091	AMP Path Gain[7:0]	–	–	–	–	–	SPK_GAIN_MAX[2:0]		

ADDRESS	NAME	MSB							LSB
0x2092	AMP DSP Config[7:0]	–	–	SPK_SAFE_EN	SPK_VOL_RMPDN_BYPASS	SPK_VOL_RMPUP_BYPASS	SPK_INVERT	SPK_DITH_EN	SPK_DCBLK_EN
0x2094	AMP SSM Configuration[7:0]	–	–	–	–	BST_BYP_MODE	SPK_SSM_MOD[1:0]		AMP_SSM_EN
0x2095	AMP Configuration[7:0]	AMP_CFG[7:0]							
0x209F	AMP Enable[7:0]	–	–	–	–	–	–	–	SPK_EN
Meas ADC Control									
0x20B0	Meas ADC Sample Rate[7:0]	–	–	–	–	–	–	MEAS_ADC_SR[1:0]	
0x20B1	Meas ADC Resolution[7:0]	–	–	–	–	–	–	ADC_TEMP_RES	ADC_PVDD_RES
0x20B2	Meas ADC PVDD Config[7:0]	–	–	–	MEAS_ADC_PVDD_FILT_EN	MEAS_ADC_PVDD_FILT_COEFF[3:0]			
0x20B3	Meas ADC Thermal Config[7:0]	–	–	–	MEAS_ADC_TEMP_FILT_EN	MEAS_ADC_TEMP_FILT_COEFF[3:0]			
0x20B4	Meas ADC Readback Control[7:0]	–	–	–	–	–	MEAS_ADC_THERM_RD_MODE	–	MEAS_ADC_PVDD_RD_MODE
0x20B5	Meas ADC Readback update[7:0]	–	–	–	–	–	MEAS_ADC_THERM_RD_UPD	–	MEAS_ADC_PVDD_RD_UPD
0x20B6	Meas ADC PVDD Readback MSB[7:0]	MEAS_ADC_PVDD_DATA[8:1]							
0x20B7	Meas ADC PVDD Readback LSB[7:0]	–	–	–	–	–	–	–	MEAS_ADC_PVDD_DATA[0]
0x20B8	Meas ADC Temp Readback MSB[7:0]	MEAS_ADC_THERM_DATA[8:1]							
0x20B9	Meas ADC Temp Readback LSB[7:0]	–	–	–	–	–	–	–	MEAS_ADC_THERM_DATA[0]
0x20BA	Meas ADC Lowest PVDD Readback MSB[7:0]	LOWEST_PVDD_DATA[7:0]							
0x20BB	Meas ADC Lowest PVDD Readback LSB[7:0]	–	–	–	–	–	–	–	LOWEST_PVDD_DATA
0x20BC	Meas ADC Highest Temp Readback MSB[7:0]	HIGHEST_TEMP_DATA[7:0]							

ADDRESS	NAME	MSB							LSB
0x20BD	Meas ADC Highest Temp Readback LSB[7:0]	–	–	–	–	–	–	–	HIGHEST_TEMP_DATA
0x20CF	Meas ADC Config[7:0]	–	–	–	–	–	–	–	MEAS_ADC_PVDD_EN
Dynamic Headroom Tracking									
0x20D1	Limiter Configuration 1[7:0]	–	–	–	DHT_HR[4:0]				
0x20D2	Limiter Configuration 2[7:0]	–	–	DHT_LIM_THRESH[4:0]					DHT_LIM_MODE
0x20D3	DHT Configuration 2[7:0]	–	–	–	DHT_MAX_ATN[4:0]				
0x20D4	DHT Configuration 3[7:0]	–	–	–	–	DHT_ATK_RATE[3:0]			
0x20D5	DHT Configuration 4[7:0]	–	–	–	–	DHT_RLS_RATE[3:0]			
0x20D6	DHT Supply Hysteresis Configuration[7:0]	–	–	–	–	DHT_SUPPLY_HYST[2:0]			DHT_SUPPLY_HYST_EN
0x20D8	DHT Enable[7:0]	–	–	–	–	–	–	–	DHT_EN
System Configuration									
0x210E	Auto-Restart Behavior[7:0]	–	–	–	OVC_RETRY_EN	THERM_AUTORESTART_EN	VBAT_UVLO_AUTORESTART_EN	PVDD_OVLO_AUTORESTART_EN	–
0x210F	Global Enable[7:0]	–	–	–	–	–	–	–	EN
Device and Revision ID									
0x21FF	Revision ID[7:0]	REV_ID[7:0]							

Register Details

Software Reset (0x2000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RST
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
RST	0	This bit field is used to trigger a software reset event. Writing a 1 resets the device and returns the control registers to their power-on reset states. Writing a 0 has no effect, and readback always returns 0.	0: No action. 1: Triggers a software reset event.

Status Registers 1 (0x2001)

BIT	7	6	5	4	3	2	1	0
Field	VBAT_UVLO_SHDN	FLL_ERR_RAW	CLK_ERR	SPKMON_ERR	SPK_OVC	OTP_FAIL	PWRDN_DONE	PWRUP_DONE
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read Only	Read, Ext	Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
VBAT_UVLO_SHDN	7	V_{BAT} UVLO Error Status	0x0: V_{BAT} UVLO is not triggered during normal operation. 0x1: V_{BAT} UVLO is triggered during normal operation.
FLL_ERR_RAW	6	Internal FLL Error Status	0x0: FLL LOCK signal set high as expected during playback operation. 0x1: FLL LOCK is deasserted during playback.
CLK_ERR	5	Clock Monitor Error Status	0x0: No external clock error detected. 0x1: BCLK or LRCLK is stopped during normal operation.
SPKMON_ERR	4	DC Level Detection Status	0x0: DC level is not presented, or lower than the setting threshold level. 0x1: DC level is greater than the setting threshold level.
SPK_OVC	3	Speaker Overcurrent Fault Status	0x0: Speaker overcurrent is inactive. 0x1: Speaker overcurrent is detected.
OTP_FAIL	2	OTP Load Status	0x0: OTP loading is successful. 0x1: OTP load routine did not complete succesfully.
PWRDN_DONE	1	Device Power-Down Status	0x0: Device is not reporting a power-down into software shutdown event. 0x1: Device is reporting a power-down into software shutdown event.
PWRUP_DONE	0	Device Power-Up Status	0x0: Device is not reporting a power-up event. 0x1: Device is reporting a power-up into the active state with the speaker amplifier enabled. This bit is asserted when device transitions from software shutdown (EN = 0) into active state (EN = 1) with the speaker amplifier enabled (SPK_EN = 1) or in the active state when the speaker amplifier enable bit is set to 1 (SPK_EN = 1). The bit is also set when the device enters active state when recovering from a UVLO event when auto-restart bit is set to 1 (VBAT_UVLO_AUTORESTART = 1 or PVDD_UVLO_AUTORESTART = 1).

Status Registers 2 (0x2002)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DHT_ACTIVE	THERMSHDN	THERMWARN	THERMFB_BGN	THERMFB_END
Reset	–	–	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	–	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_ACTIVE	4	DHT Active Status	0x0: DHT is inactive. 0x1: DHT is active.
THERMSHDN	3	Thermal Shutdown Status	0x0: Die temperature is lower than thermal shutdown setting level. 0x1: Die temperature is greater than thermal shutdown setting level.
THERMWARN	2	Thermal Warning Status	0x0: Die temperature is lower than thermal warning level setting. 0x1: Die temperature is higher than thermal warning level setting.
THERMFB_BGN	1	Thermal Foldback Begin Status	0x0: Thermal foldback is not active. 0x1: Thermal foldback is active.
THERMFB_END	0	Thermal Foldback End Status	0x0: Thermal foldback is active. 0x1: Thermal foldback has ended.

Thermal Warning Threshhold (0x2020)

BIT	7	6	5	4	3	2	1	0
Field	–	THERMWARN_THRESH[6:0]						
Reset	–	0x46						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
THERMWARN_THRESH	6:0	Sets the thermal warning threshold temperature.	0x00: 50°C 0x01: 51°C 0x02: 52°C ...: ... 0x62: 148°C 0x63: 149°C 0x64-0x7F: 150°C

Thermal Shutdown Threshold (0x2021)

BIT	7	6	5	4	3	2	1	0
Field	–	THERMSHDN_THRESH[6:0]						
Reset	–	0x64						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_THRESH	6:0	Sets the thermal shutdown threshold temperature.	0x00: 50°C 0x01: 51°C 0x02: 52°C ...: ... 0x30: 98°C 0x31: 99°C 0x64 to 0x7F: 150°C

Thermal Hysteresis (0x2022)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	THERM_HYST[1:0]	
Reset	–	–	–	–	–	–	0x2	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
THERM_HYST	1:0	Controls the amount of hysteresis applied to the thermal threshold measurements.	0x0: 2°C 0x1: 5°C 0x2: 7°C 0x3: 10°C

Thermal Foldback Settings (0x2023)

BIT	7	6	5	4	3	2	1	0
Field	–	–	THERMFB_HOLD[1:0]		THERMFB_RLS[1:0]		THERMFB_SLOPE[1:0]	
Reset	–	–	0x3		0x0		0x1	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
THERMFB_HOLD	5:4	The thermal foldback hold time controls how long the device temperature must remain below the configured thermal threshold hysteresis before thermal foldback release begins.	0x0: 0ms 0x1: 20ms 0x2: 40ms 0x3: 80ms
THERMFB_RLS	3:2	This sets the release rate of the thermal foldback attenuation.	0x0: 3ms/dB 0x1: 10ms/dB 0x2: 100ms/dB 0x3: 300ms/dB
THERMFB_SLOPE	1:0	This sets the slope of the thermal foldback attenuation when die temperature exceeds thermal-warning threshold.	0x0: 0.25dB/°C 0x1: 0.5dB/°C 0x2: 1.0dB/°C 0x3: 2.0dB/°C

Thermal Foldback Enable (0x2027)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	THERMFB_EN
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
THERMFB_EN	0	Enables Thermal Foldback	0: Thermal foldback disabled. 1: Thermal foldback enabled.

Clock Monitor Config (0x2030)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CMON_AUTORESTART_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CMON_AUTORESTART_EN	0	Controls whether or not the device automatically resumes playback when the clocks become valid after the device is disabled due to a clock monitor error. It is not valid to use the auto restart mode when the device boost bypass mode is controlled by toggling the PCM interface input LSB.	0x0: Device does not automatically restart after valid clocks are reapplied. 0x1: Device automatically restarts after valid clocks are reapplied.

Error Monitor Control (0x2037)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPKMON_EN	–	–	CMON_EN
Reset	–	–	–	–	0x0	–	–	0x1
Access Type	–	–	–	–	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPKMON_EN	3	Enables the internal speaker protection monitor.	0x0: Disables internal speaker data monitor. 0x1: Enables internal speaker data monitor.
CMON_EN	0	Enables the clock monitor to monitor PCM input clocks for clock errors.	0x0: Disable 0x1: Enable

PCM Mode Config (0x2040)

BIT	7	6	5	4	3	2	1	0
Field	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]			–	PCM_CHANSEL	–
Reset	0x3		0x0			–	0b0	–
Access Type	Write, Read		Write, Read			–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_CHANSZ	7:6	Configures the PCM data word size for each channel.	00: Reserved 01: 16-bit 10: 24-bit 11: 32-bit
PCM_FORMAT	5:3	Selects the PCM data format.	0x0: I²S mode 0x1: Left-justified 0x2: Reserved 0x3: TDM mode 0 (0 BCLK delay from LRCLK) 0x4: TDM mode 1 (1 BCLK delay from LRCLK) 0x5: TDM mode 2 (2 BCLK delay from LRCLK) 0x6 to 0x7: Reserved
PCM_CHANSEL	1	Selects which LRCK edge starts a new frame (channel 0 or slot 0).	0: I²S and LJ mode: Falling LRCLK edge starts a new frame. In TDM modes: Rising LRCLK edge starts a new frame. 1: In I²S and LJ mode: Rising LRCLK edge starts a new frame. In TDM modes: Falling LRCLK edge starts a new frame.

PCM Clock Setup (0x2041)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PCM_BCLKEDGE	PCM_BSEL[3:0]			
Reset	–	–	–	0b0	0x4			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_BCLKEDGE	4	Selects the active BCLK edge.	0: Input data captured and output data valid on rising edge of BCLK. 1: Input data captured and output data valid on falling edge of BCLK.

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_BSEL	3:0	Selects the number of BCLKs per LRCLK expected by the PCM Interface.	0x0 to 0x1: Reserved 0x2: 32 0x3: 48 0x4: 64 0x5: 96 0x6: 128 0x7: 192 0x8: 256 0x9: 384 0xA: 512 0xB: 320 0xC to 0xF: Reserved

PCM Sample Rate Setup 1 (0x2042)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PCM_SR[3:0]			
Reset	–	–	–	–	0x8			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_SR	3:0	Sets the sample rate of the PCM interface. This corresponds to the expected LRCLK frequency.	0x0: 8kHz 0x1: 11.025kHz 0x2: 12kHz 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9: 88.2kHz 0xA: 96kHz 0xB: 176.4kHz 0xC: 192kHz 0xD to 0xF: Reserved

PCM RX Source 1 (0x2043)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PCM_DMMIX_CFG[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_DMMIX_CFG	1:0	Determines the behavior of the mono mixer circuit.	0x0: Output of mono mixer is Channel 0. 0x1: Output of mono mixer is Channel 1. 0x2: Output of mono mixer is (Channel 0 + Channel 1)/2. 0x3: Reserved.

PCM RX Source 2 (0x2044)

BIT	7	6	5	4	3	2	1	0
Field	PCM_DMMIX_CH1_SOURCE[3:0]				PCM_DMMIX_CH0_SOURCE[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_DMMIX_CH1_SOURCE	7:4	Selects the PCM data input channel that is routed to the channel 1 of the digital mono mixer.	0x0: PCM Input Channel 0 0x1: PCM Input Channel 1 0x2: PCM Input Channel 2 ...: ... 0xE: PCM Input Channel 14 0xF: PCM Input Channel 15
PCM_DMMIX_CH0_SOURCE	3:0	Selects the PCM data input channel that is routed to the channel 0 of the digital mono mixer.	0x0: PCM Input Channel 0 0x1: PCM Input Channel 1 0x2: PCM Input Channel 2 ...: ... 0xE: PCM Input Channel 14 0xF: PCM Input Channel 15

PCM Rx Enables (0x204F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PCM_RX_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_RX_EN	0	Enables the speaker amplifier playback path.	0: PCM data input disabled. 1: PCM data input enabled.

SS TIMER ADJUST (0x2082)

BIT	7	6	5	4	3	2	1	0
Field	CP_CLK_SEL[1:0]		CP_SOFT_TIMER[5:0]					
Reset	0x0		0x03					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
CP_CLK_SEL	7:6	Configures the frequency of the charge pump clock.	0x0: 1.024Mhz (normal mode) and 64kHz (low-power mode) 0x1: 2/3 x Default frequency 0x2: 1/2 x Default frequency 0x3: 1/3 x Default frequency

BITFIELD	BITS	DESCRIPTION	DECODE
CP_SOFT_TIMER	5:0	Selects duration of soft-start time.	0x0: Reserved 0x1: 0.5mS 0x2: 1.0mS 0x3: 1.5mS 0x4: 2.0mS 0x5: 2.5mS 0x6: 3.0mS 0x7: 3.5mS 0x8: 4.0mS 0x9: 4.5mS 0xA: 5.0mS 0xB: 5.5mS 0xC: 6.0mS 0xD: 6.5mS 0xE: 7.0mS 0xF: 7.5mS 0x10: 8.0mS 0x11: 8.5mS 0x12: 9.0mS 0x13: 9.5mS 0x14: 10.0mS 0x15: 10.5mS 0x16: 11.0mS 0x17: 11.5mS 0x18: 12.0mS 0x19: 12.5mS 0x1A: 13.0mS 0x1B: 13.5mS 0x1C: 14.0mS 0x1D: 14.5mS 0x1E: 15.0mS 0x1F: 15.5mS 0x20: 16.0mS 0x21 - 0x3F: Reserved

AMP volume control (0x2090)

BIT	7	6	5	4	3	2	1	0
Field	–	SPK_VOL[6:0]						
Reset	–	0x0						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_VOL	6:0	Sets the digital volume level of the speaker amplifier path.	0x00: 0dB 0x01: -0.5dB 0x02: -1.0dB ...: (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63dB 0x7F: Mute

AMP Path Gain (0x2091)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SPK_GAIN_MAX[2:0]		
Reset	–	–	–	–	–	0x3		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_GAIN_MAX	2:0	Sets the maximum peak output voltage level (V_{MPO}) for the speaker path (no-load). Values in dB are relative to the baseline speaker path DAC full-scale output level of 0.48dBV.	0x00: 2.98V_P (6dB) 0x01: 4.22V_P (9dB) 0x02: 5.96V_P (12dB) 0x03: 8.41V_P (15dB) 0x04: 11.88V_P (18dB) 0x05: 16.79V_P (21dB) 0x06-0x07: Reserved

AMP DSP Config (0x2092)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SPK_SAFE_EN	SPK_VOL_RMPDN_BYPASS	SPK_VOL_RMPUP_BYPASS	SPK_INVERT	SPK_DITH_EN	SPK_DCBLK_EN
Reset	–	–	0x1	0b0	0b0	0b0	0b1	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_SAFE_EN	5	The safe mode bit protects any speaker connected to the device on power up. When this setting is enabled the amplifier output is set to -18dBFS or less.	0: Speaker safe mode disabled. 1: Speaker safe mode enabled.
SPK_VOL_RMPDN_BYPASS	4	Controls whether the speaker amplifier path volume is internally ramped down during shutdown and during volume changes.	0: Volume ramp down enabled. 1: Volume ramp down bypassed.
SPK_VOL_RMPUP_BYPASS	3	Controls whether the speaker amplifier path volume is internally ramped up during startup and during volume changes.	0: Volume ramp up enabled. 1: Volume ramp up bypassed.
SPK_INVERT	2	Inverts the speaker amplifier path output.	0: Output is normal. 1: Output is inverted.
SPK_DITH_EN	1	Selects whether or not dither is applied to data in the speaker amplifier path.	0: Dither disabled. 1: Dither enabled.
SPK_DCBLK_EN	0	Controls the DC blocking filter in the speaker amplifier path.	0: DC blocking filter disabled. 1: DC blocking filter enabled.

AMP SSM Configuration (0x2094)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BST_BYP_MODE	SPK_SSM_MOD[1:0]		AMP_SSM_EN
Reset	–	–	–	–	0x0	0x0		0x1
Access Type	–	–	–	–	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BST_BYP_MODE	3	Configures the charge pump boost bypass mode.	0x0: Charge pump boost is in normal operation. 0x1: Charge pump boost is bypassed.
SPK_SSM_MOD	2:1		0x0: ±1.5% 0x1: ±3.0% 0x2: ±4.5% 0x3: ±6.0%
AMP_SSM_EN	0	Enable AMP SSM	0x0: SSM Disabled 0x1: SSM Enabled

AMP Configuration (0x2095)

BIT	7	6	5	4	3	2	1	0
Field	AMP_CFG[7:0]							
Reset	0x70							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AMP_CFG	7:0	Configuration bits for device when using dynamic boost control (DBC).	AMP_CFG<7:5>: Reserved AMP_CFG<4>: 0 = Boost bypass and aplifier receiver mode controlled via PCM interface. 1 = Boost bypass and aplifier receiver mode controlled via I^2C control. AMP_CFG<3>: 0 = AMP_RCVR_MODE register bit controls the boost bypass and amplifier receiver mode. 1= Overrides the AMP_RCVR_MODE register and forces the class-D amplifier to always operate in the boost mode. This bit must be set to 1 when device is suing dynamic boost control. AMP_CFG<2:0>: Reserved

AMP Enable (0x209F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SPK_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_EN	0	Enables the speaker amplifier.	0x0: Speaker amplifier is disabled. 0x1: Speaker amplifier is enabled.

Meas ADC Sample Rate (0x20B0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MEAS_ADC_SR[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_SR	1:0	Configures the sample rate of the PVDD and thermal channel of the measurement ADC.	0x0: PVDD channel sample rate = 992KHz, temperature channel sample rate = 32kHz 0x1: PVDD channel sample rate = 960KHz, temperature channel sample rate = 64kHz 0x2: PVDD channel sample rate = 896KHz, temperature channel sample rate = 128kHz 0x3: PVDD channel sample rate = 768KHz, temperature channel sample rate = 256kHz

Meas ADC Resolution (0x20B1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	ADC_TEMP_RES	ADC_PVDD_RES
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_TEMP_RES	1	Configures the temperature channel resolution.	0x0: 9-Bit resolution. 0x1: 8-Bit resolution.
ADC_PVDD_RES	0	Configures the PVDD channel resolution.	0x0: 9-Bit resolution. 0x1: 8-Bit resolution.

Meas ADC PVDD Config (0x20B2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEAS_ADC_PVDD_FILT_EN	MEAS_ADC_PVDD_FILT_COEFF[3:0]			
Reset	–	–	–	0x0	0x2			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_PVDD_FILT_EN	4	Controls whether filtering is applied to the PVDD channel output.	0: Filter is bypassed. 1: Filter is applied.
MEAS_ADC_PVDD_FILT_COEFF	3:0	Sets the PVDD channel lowpass filter bandwidth.	Value: Measurement ADC channel cutoff frequencies 0x0: 7.5kHz 0x1: 20kHz 0x2: 75kHz (default) 0x3: 150kHz 0x4: 300kHz 0x5 to 0xF: Reserved

Meas ADC Thermal Config (0x20B3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEAS_ADC_TEMP_FILT_EN	MEAS_ADC_TEMP_FILT_COEFF[3:0]			
Reset	–	–	–	0x0	0x02			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_TEMP_FILT_EN	4	Controls whether filtering is applied to the thermal channel output.	0: Filter is bypassed. 1: Filter is applied.
MEAS_ADC_TEMP_FILT_COEFF	3:0	Sets the thermal channel lowpass filter bandwidth.	Value: Measurement ADC channel cutoff frequencies 0x0: 7.5kHz 0x1: 20kHz 0x2: 75kHz (default) 0x3: 150kHz 0x4: 300kHz 0x5 to 0xF: Reserved

Meas ADC Readback Control (0x20B4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MEAS_ADC_THERM_RD_MODE	–	MEAS_ADC_PVDD_RD_MODE
Reset	–	–	–	–	–	0x0	–	0x0
Access Type	–	–	–	–	–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_THERM_RD_MODE	2	Controls whether the thermal ADC channel output readback is updated automatically or manually after each conversion is completed.	0: Measurement ADC channel readback data is automatically updated. 1: Inititates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_PVDD_RD_MODE	0	Controls whether the PVDD ADC channel output readback is updated automatically or manually after each conversion is completed.	0: Measurement ADC channel readback data is automatically updated. 1: Inititates a measurement and locks the result into the measurement ADC channel readback register.

Meas ADC Readback update (0x20B5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MEAS_ADC_THERM_RD_UPD	–	MEAS_ADC_PVDD_RD_UPD
Reset	–	–	–	–	–	0x0	–	0x0
Access Type	–	–	–	–	–	Write Only	–	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_THERM_RD_UPD	2	Write 1 to inititate a measurement and lock the result into the measurement ADC thermal channel readback register.	0x0: No effect. 0x1: Inititates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_PVDD_RD_UPD	0	Write 1 to inititate a measurement and lock the result into the measurement ADC PVDD channel readback register.	0x0: No effect. 0x1: Inititates a measurement and locks the result into the measurement ADC channel readback register.

Meas ADC PVDD Readback MSB (0x20B6)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_PVDD_DATA[8:1]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_PVDD_DATA	7:0	Provides the measured PVDD value.	To convert the ADC code into a real voltage, use the following: 9-Bit mode: Measured V_{PVDD}(V) = MEAS_ADC_PVDD_DATA[8:0] x 29.3mV 8-Bit mode: Measured V_{PVDD}(V) = MEAS_ADC_PVDD_DATA[8:1] x 58.6mV

Meas ADC PVDD Readback LSB (0x20B7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_PVDD_DATA[0]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_PVDD_DATA	0	Provides the measured PVDD value.	To convert the ADC code into a real voltage, use the following: 9-Bit mode: Measured V_{PVDD}(V) = MEAS_ADC_PVDD_DATA[8:0] x 29.3mV

Meas ADC Temp Readback MSB (0x20B8)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_THERM_DATA[8:1]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_THERM_DATA	7:0	Provides the measured temperature value.	To convert the ADC code into a real temperature, use the following: 8-Bit mode: Measured temp = -255°C + (MEAS_ADC_THERM_DATA[8:1] x 2°C) 9-Bit mode: Measured temp = -255°C + (MEAS_ADC_THERM_DATA[8:0] x 1°C)

Meas ADC Temp Readback LSB (0x20B9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_THERM_DATA[0]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_THERM_DATA	0	Provides the measured temperature value.	To convert the ADC code into real temperature, use the following: 9-Bit mode: Measured temp = -255°C + (MEAS_ADC_THERM_DATA[8:0] x 1°C)

Meas ADC Lowest PVDD Readback MSB (0x20BA)

BIT	7	6	5	4	3	2	1	0
Field	LOWEST_PVDD_DATA[7:0]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
LOWEST_PVDD_DATA	7:0	Provides the lowest measured PVDD value.	To convert the ADC code into a real voltage, use the following: 9-Bit mode: Measured V_{PVDD}(V) = MEAS_ADC_PVDD_DATA[8:0] x 29.3mV 8-Bit mode: Measured V_{PVDD}(V) = MEAS_ADC_PVDD_DATA[8:1] x 58.6mV

Meas ADC Lowest PVDD Readback LSB (0x20BB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOWEST_PVDD_DATA
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
LOWEST_PVDD_DATA	0	Provides the lowest measured PVDD value.	To convert the ADC code into a real voltage, use the following: 9-Bit mode: Measured V_{PVDD}(V) = MEAS_ADC_PVDD_DATA[8:0] x 29.3mV

Meas ADC Highest Temp Readback MSB (0x20BC)

BIT	7	6	5	4	3	2	1	0
Field	HIGHEST_TEMP_DATA[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHEST_TEMP_DATA	7:0	Provides the highest temperature measured.	To convert the ADC code into a real temperature, use the following: 8-Bit mode: Measured temp = -255°C + (MEAS_ADC_THERM_DATA[8:1] x 2°C) 9-Bit mode: Measured temp = -255°C + (MEAS_ADC_THERM_DATA[8:0] x 1°C)

Meas ADC Highest Temp Readback LSB (0x20BD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HIGHEST_TEMP_DATA
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHEST_TEMP_DATA	0	Provides the highest temperature measured.	To convert the ADC code into a real temperature, use the following: 9-Bit mode: Measured temp = -255°C + (MEAS_ADC_THERM_DATA[8:0] x 1°C)

Meas ADC Config (0x20CF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_PVDD_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_PVDD_EN	0	Manually enables the measurement ADC PVDD channel.	0: Do not manually enable the measurement ADC channel (can be automatically enabled). 1: Manually force the measurement ADC channel to be enabled anytime the device is in the active state.

Limiter Configuration 1 (0x20D1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DHT_HR[4:0]				
Reset	–	–	–	0x8				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_HR	4:0	Selects the DHT supply headroom for the limiter functions.	0x0: -20% 0x1: -17.5% 0x2: -15% 0x3: -12.5% 0x4: -10% 0x5: -7.5% 0x6: -5.0% 0x7: -2.5% 0x8: 0% 0x9: +2.5% 0xA: +5.0% 0xB: +7.5% 0xC: +10% 0xD: +12.5% 0xE: +15% 0xF: +17.5% 010: +20%

Limiter Configuration 2 (0x20D2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DHT_LIM_THRESH[4:0]					DHT_LIM_MODE
Reset	–	–	0x0					0x0
Access Type	–	–	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_LIM_THRESH	5:1	Selects the fixed threshold level for signal level limiter mode (SLL). Has no effect in signal distortion limiter mode (SDL).	00000: 0dBFS 00001: -1dBFS 00010: -2dBFS ...: (-1dBFS steps) 01110: -14dBFS 01111: -15dBFS 10000 to 11111: Reserved
DHT_LIM_MODE	0	Selects whether the DHT limiter is in signal distortion or signal level limiter mode.	0: Signal distortion limiter mode where limiter threshold tracks supply. 1: Signal level limiter mode where limiter uses fixed thresholds.

DHT Configuration 2 (0x20D3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DHT_MAX_ATN[4:0]				
Reset	–	–	–	0x14				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_MAX_ATN	4:0	Selects the maximum attenuation that can be applied to the audio signal by the DHT.	0x0: Reserved 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4: -4dB 0x5: -5dB 0x6: -6dB 0x7: -7dB 0x8: -8dB 0x9: -9dB 0xA: -10dB 0xB: -11dB 0xC: -12dB 0xD: -13dB 0xE: -14dB 0xF: -15dB 0x10: -16dB 0x11: -17dB 0x12: -18dB 0x13: -19dB 0x14: -20dB 0x15-0x1F: Reserved

DHT Configuration 3 (0x20D4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_ATK_RATE[3:0]			
Reset	–	–	–	–	0x2			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_ATK_RATE	3:0	Selects the DHT attack rate.	0x0: 20µs/dB 0x1: 40µs/dB 0x2: 80µs/dB 0x3: 160µs/dB 0x4: 320µs/dB 0x5: 640µs/dB 0x6: 1.28ms/dB 0x7: 2.56ms/dB 0x8: 5.12ms/dB 0x9: 10.24ms/dB 0xA: 20.48ms/dB 0xB: 40.96ms/dB 0xC: 81.92ms/dB 0xD: 163.84ms/dB 0xE: Reserved 0xF: Reserved

DHT Configuration 4 (0x20D5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_RLS_RATE[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_RLS_RATE	3:0	Selects the DHT release rate.	0x0: 2ms/dB 0x1: 4ms/dB 0x2: 8ms/dB 0x3: 16ms/dB 0x4: 32ms/dB 0x5: 64ms/dB 0x6: 128ms/dB 0x7: 256ms/dB 0x8: 512ms/dB 0x9: 1.024s/dB 0xA: 2.048s/dB 0xB: 4.096s/dB 0xC: 8.192s/dB 0xD: 16.384s/dB 0xE: Reserved 0xF: Reserved

DHT Supply Hysteresis Configuration (0x20D6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_SUPPLY_HYST[2:0]			DHT_SUPPLY_HYST_EN
Reset	–	–	–	–	0x3			0x1
Access Type	–	–	–	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_SUPPLY_HYST	3:1	Selects the supply hysteresis for DHT attenuation release when supply increases.	0x0: 1 LSB 0x1: 2 LSB 0x2: 3 LSB 0x3: 4 LSB 0x4: 6 LSB 0x5: 8 LSB 0x6: 10 LSB 0x7: 12 LSB 0x8: Reserved
DHT_SUPPLY_HYST_EN	0	Select whether PVDD DHT hysteresis is enabled or disabled.	0: DHT is disabled. 1: DHT is enabled.

DHT Enable (0x20D8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DHT_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_EN	0	Select whether DHT is enabled or disabled.	0: DHT is disabled. 1: DHT is enabled.

Auto-Restart Behavior (0x210E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	OVC_RETRY_EN	THERM_AUTORESTART_EN	VBAT_UVLO_AUTORESTART_EN	PVDD_OVLO_AUTORESTART_EN	–
Reset	–	–	–	0x0	0x0	0x0	0b0	–
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
OVC_RETRY_EN	4	Controls whether or not the speaker amplifier is automatically reenabled after an OVC fault condition.	0x0: Overcurrent recovery is in manual retry mode. 0x1: Overcurrent recovery is in auto-retry mode.
THERM_AUTORESTART_EN	3	Controls whether or not the device automatically returns to the active state when the die temp recovers from thermal shutdown.	0x0: Thermal shutdown recovery is in manual mode. 0x1: Thermal shutdown recovery is in auto mode.
VBAT_UVLO_AUTORESTART_EN	2	Controls whether or not the device automatically returns to the active state when it recovers from a V_{BAT} UVLO event.	0x0: Manual mode 0x1: Auto mode
PVDD_OVLO_AUTORESTART_EN	1	Controls whether or not the device automatically returns to the active state when PVDD recovers from an OVLO event.	0: PVDD OVLO recovery is in manual mode. 1: PVDD OVLO recovery is in auto mode.

Global Enable (0x210F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
EN	0	Disable or enable all blocks and reset all logic except the I^2C interface and control registers.	0: Device powered down. 1: Device enabled.

Revision ID (0x21FF)

BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0x40							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
REV_ID	7:0	Revision of the device. Updated at every device revision.	0x41: Device revision — RevA0 silicon

Applications Information

Layout and Grounding

Proper layout and grounding are essential for optimal performance; use at least four PCB layers and add thermal vias to the ground/power plane close to the device to ensure good thermal performance and high-end output power. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal. Ground the power signals and the analog signals of the IC separately at the system ground plane to prevent switching interference from corrupting sensitive analog signals. Place the recommended supply decoupling capacitors as close as possible to the IC. The PVDD to PGND connection must be kept short and should have minimal trace length and loop area to ensure optimal performance. Use wide, low-resistance output, supply, and ground traces. As load impedance decreases, the current drawn from the device outputs increase. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through a 100mΩ trace, 1.95W is being delivered to the speaker. If power is delivered through a 10mΩ trace, 1.99W is being delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device. The device is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on the top and bottom PCB planes.

Recommended External Components

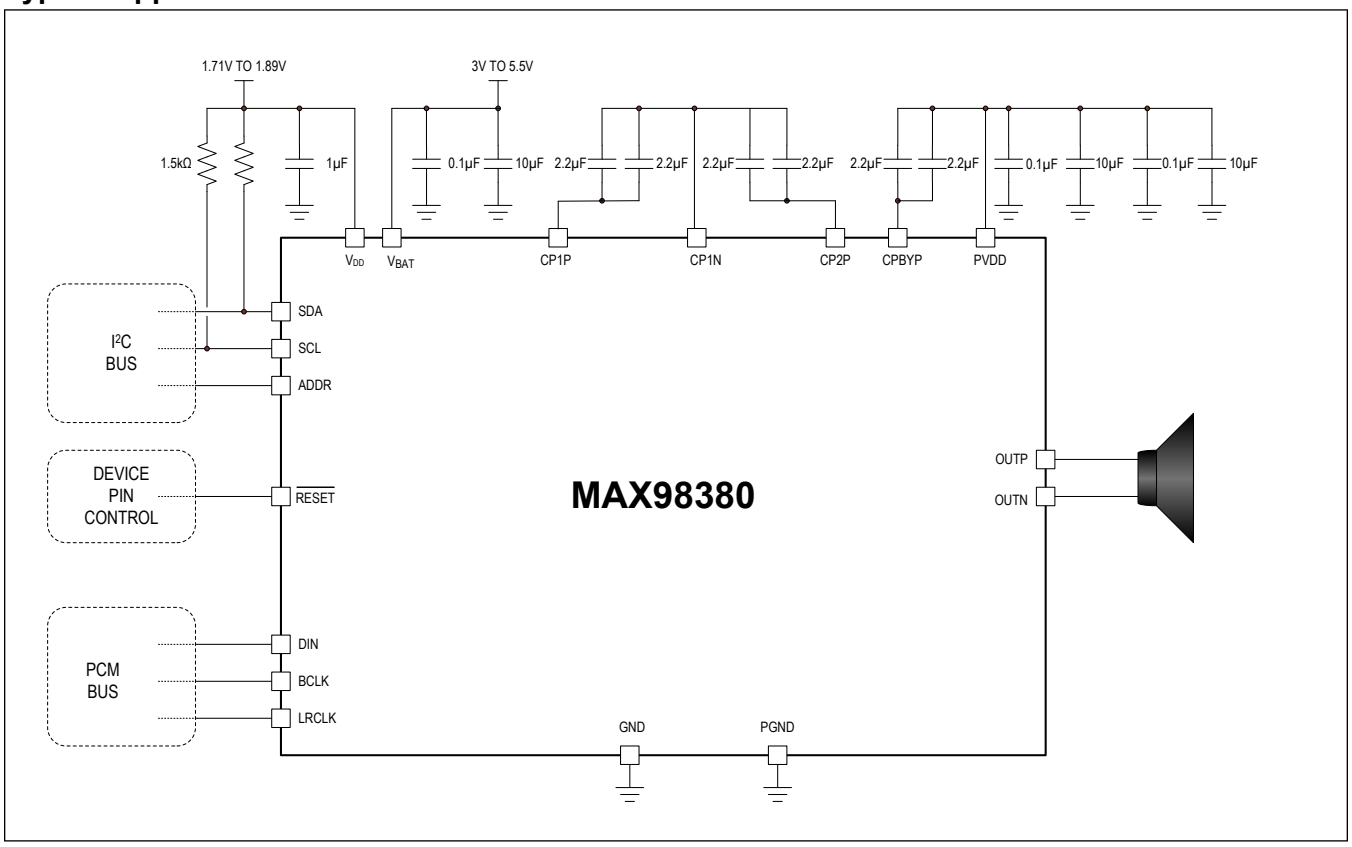
Table 7 shows the recommended external components. See the *Typical Application Circuits* for more details.

Table 7. Component List

BUMP	VALUE	SIZE	VOLTAGE RATING (V)	DIELECTRIC
PVDD	100µF ± 20%	—	25	Alum-Elec
PVDD	10µF ± 20%	0603	25	X5R
PVDD	10µF ± 20%	0603	25	X5R
PVDD	0.1µF ± 10%	0402	25	X5R
PVDD	0.1µF ± 10%	0402	25	X5R
V_{BAT}	0.1µF ± 10%	0201	16	X5R
V_{BAT}	10µF ± 20%	0603	25	X5R
CP1P	2.2µF ± 10%	0402	16	X5R
CP1P	2.2µF ± 10%	0402	16	X5R
CP2P	2.2µF ± 10%	0402	16	X5R
CP2P	2.2µF ± 10%	0402	16	X5R
CPBYP	0.1µF ± 10%	0201	16	X5R
CPBYP	2.2µF ± 10%	0402	16	X5R
CPBYP	2.2µF ± 10%	0402	16	X5R
V_{DD}	1µF ± 20%	0201	6.3	X5R

Typical Application Circuits

Typical Applications Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX98380EWG+	-40°C to +85°C	24 WLP	KAA
MAX98380EWG+T	-40°C to +85°C	24 WLP	KAA

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/22	Release for Market Intro	—