VL53L4ED

Datasheet

Time-of-Flight high accuracy proximity sensor with extended temperature capability

Product status link
VL53L4ED

Features

High accuracy proximity ranging

- High performance proximity sensor
- Short distance linearity down to 1 mm
- From 0 to 1300 mm with full field of view (FoV)
- Extended effective temperature range of -40°C to 105°C
- Up to 800 mm ranging under 5 klx
- FoV of 18°
- Autonomous low power mode with interrupt programmable threshold to wake up the host
- Fast ranging frequency up to 100 Hz

Fully integrated miniature module

- 940 nm invisible laser emitter (VCSEL) and analog driver
- Low power microcontroller running advanced digital firmware
- 4.4 x 2.4 x 1 mm size
- Pin-to-pin compatible with VL53L4CD

Easy integration

- Reflowable component
- Single power supply 2v8
- It can be hidden behind the cover glass
- I²C interface (up to 1 MHz)
- Full set of C software drivers (Linux compatible) for turnkey ranging
- Embedded processing for a very low memory footprint

Application

Proximity ranging applications under strong light conditions such as:

- Robotic and industrial applications including collision avoidance.
- System activation, occupancy, and presence detection (public buildings and car parks).
- Smart lighting systems for outdoor lighting control.
- Biometric distance measurement (security systems and health monitoring).

High temperature range for extreme environment applications:

- Industrial automation and security systems.
- Touchless button for industrial tools.
- Industrial manufacturing assistance.
- Liquid level monitoring (container and tank).

Description

The VL53L4ED is specifically designed for high-accuracy, short-range measurements requiring extended temperature capability. It offers an 18° field of view for measurements from 1 mm up to 1300 mm in standard conditions, and up to 1150 mm under its extended temperature. Special settings also provide an accurate distance measurement up to 800 mm under ambient light conditions (5 klx).

This sensor has an effective temperature range of -40°C to 105°C, ensuring reliable measurement, even in extreme temperature conditions. It is the ideal product for industrial devices requiring proximity sensing. Examples include presence detection and system activation applications. The VL53L4ED is a direct derivative of the VL53L4CD with which it is pin-to-pin compatible. Its fully embedded on-chip processing helps to reduce design complexity and BOM cost because less powerful and less expensive microcontrollers can be used.

Like all Time-of-Flight (ToF) sensors based on STMicroelectronics' FlightSense technology, the VL53L4ED records an absolute distance measurement regardless of the target color and reflectance.

The VL53L4ED is housed in a miniature reflowable package. It integrates a SPAD (single photon avalanche diode) array, and consequently achieves the best ranging performance in various ambient lighting conditions, for a wide range of cover glass materials.

This sensor integrates a VCSEL (vertical-cavity surface-emitting laser). It emits a fully invisible 940 nm IR light that is totally safe for eyes (Class 1 certification).

1 Acronyms and abbreviations

Acronym/abbreviation	Definition
AF	autofocus
API	application programming interface
BOM	bill of material
ESD	electrostatic discharge
FoV	field of view
FoI	field of illumination
FW BOOT	firmware boot
HW STANDBY	hardware standby
I²C	inter-integrated circuit (serial bus)
MSB	most significant bit
NA	not applicable
PCB	printed circuit board
PDAF	phase-detection autofocus
SCL	serial clock line
SDA	serial data line
SW STANDBY	software standby
SPAD	single photon avalanche diode
ToF	Time-of-Flight
ULD	ultra lite driver
VCSEL	vertical-cavity surface-emitting laser

2 Product overview

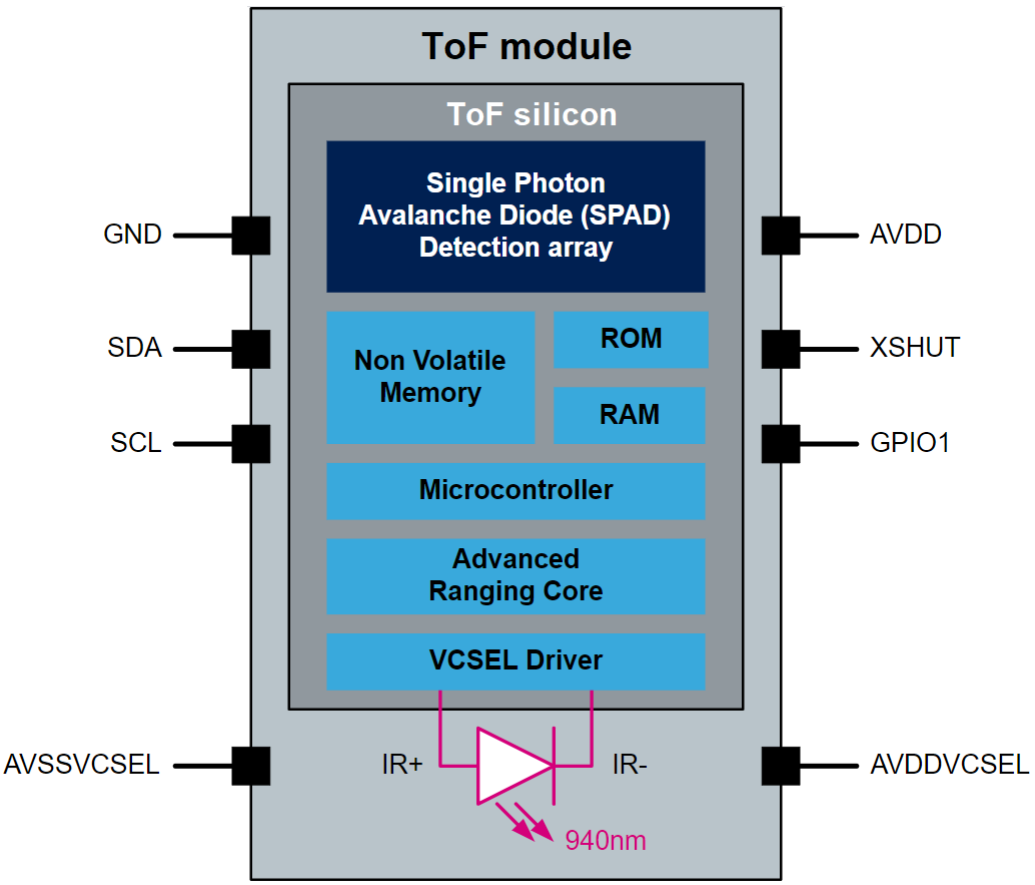
2.1 Technical specification

Table 1. Technical specification

Feature	Detail
Package	Optical LGA12
Size	4.4 x 2.4 x 1 mm
Operating voltage	2.7 to 3.4 V
Operating temperature	-40 to 105°C
Infrared emitter	940 nm
I²C	Up to 1 MHz (fast mode plus) serial bus Address: 0x52

2.2 System block diagram

Figure 1. VL53L4ED block diagram



2.3 Device pinout

The following figure shows the pinout of the VL53L4ED (see also Section 8: Outline drawings).

Figure 2. VL53L4ED pinout (bottom view)

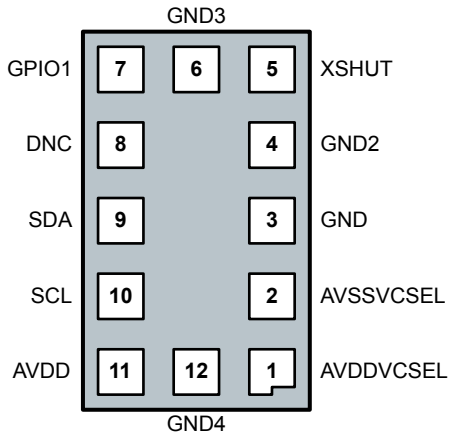


Table 2. VL53L4ED pin description

Pin number	Signal name	Signal type	Signal description
1	AVDDVCSEL	Supply	VCSEL supply, to be connected to main supply
2	AVSSVCSEL	Ground	VCSEL ground, to be connected to main ground
3	GND		To be connected to main ground
4	GND2		
5	XSHUT	Digital input	Xshutdown pin, active low
6	GND3	Ground	To be connected to main ground
7	GPIO1	Digital output	Interrupt output. Open drain output
8	DNC	Digital input	Do not connect, must be left floating
9	SDA	Digital input/output	I²C serial data
10	SCL	Digital input	I²C serial clock input
11	AVDD	Supply	Supply, to be connected to main supply
12	GND4	Ground	To be connected to, the main ground

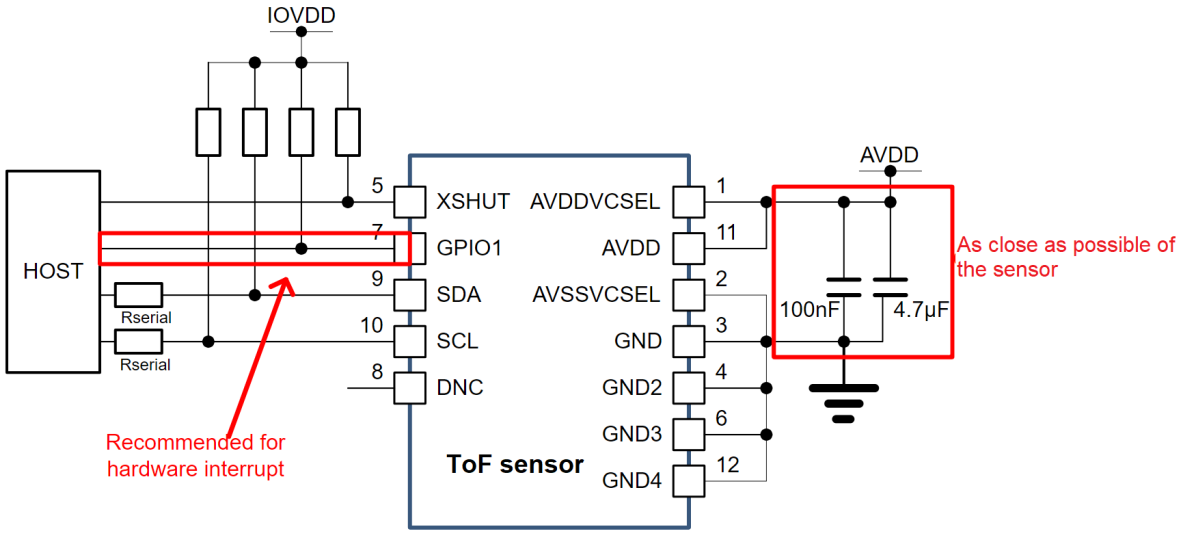
Note: AVSSVCSEL and GND are ground pins that can be connected in the application schematics.

Note: GND2, GND3, and GND4 are standard pins that are forced to the ground domain in the application schematics. This is to avoid possible instabilities which might arise if set in other states.

2.4 Application schematic

The following figure shows the application schematic of the VL53L4ED.

Figure 3. VL53L4ED schematic



Capacitors on the external supply AVDD should be placed as close as possible to the AVDDVCSEL and AVSSVCSEL module pins.

The external pull-up resistor values can be found in the I2C-bus specification. Pull-ups are typically fitted only once per bus, near the host. For suggested values, see Table 3. Suggested pull-up and series resistors for I²C fast mode and Table 4. Suggested pull-up and series resistors for I²C fast mode plus.

The XSHUT pin must always be driven to avoid leakage current. A pull-up is needed if the host state is not known. XSHUT is needed to use hardware standby mode (there is no I²C communication).

The recommended value of the XSHUT and GPIO1 pull-up is 10 kohms.

The GPIO1 should be left unconnected if not used.

The following tables list recommended values for pull-up and series resistors. Values are for an AVDD of 1.8 V to 2.8 V, in I²C fast mode (up to 400 kHz) and fast mode plus (up to 1 MHz).

Table 3. Suggested pull-up and series resistors for I²C fast mode

I²C load capacitance (CL)(1)	Pull up resistor (ohms)	Series resistor (àhms)
$C_L \leq 90$ pF	3.6 k	0
90 pF < $C_L \leq 140$ pF	2.4 k	0
140 pF < $C_L \leq 270$ pF	1.2 k	0
270 pF < $C_L \leq 400$ pF	0.8 k	0

1. *For each bus line, CL is measured in the application PCB by the customer.*

Table 4. Suggested pull-up and series resistors for I²C fast mode plus

I²C load capacitance (CL)[1]	Pull up resistor (ohms)	Series resistor (ohms)
$C_L \leq 90$ pF	1.5 k	100
90 pF < $C_L \leq 140$ pF	1 k	50
140 pF < $C_L \leq 270$ pF	0.5 k	50
270 pF < $C_L \leq 400$ pF	0.3 k	50

1. *For each bus line, CL is measured in the application PCB by the customer.*

3 Functional description

3.1 System functional description

Figure 4. VL53L4ED system functional description shows the system level functional description.

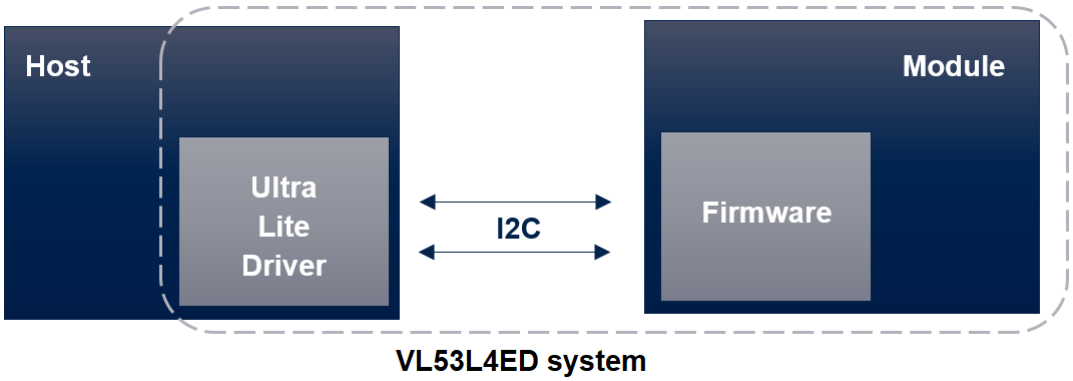
The host customer application controls the VL53L4ED device using an ultra lite driver (ULD). The ULD contains a set of high level functions that allow control of the VL53L4ED firmware. Tasks such as initialization, start/stop ranging, and setting the system accuracy can be controlled.

The driver is a turnkey solution. It consists of a set of “C” functions that enable fast development of end-user applications. This helps to avoid complications with direct multiple register access. The driver is structured so that it can be compiled on any kind of platform. However, STMicroelectronics advise a good abstracted platform layer. The driver package allows the user to take full advantage of the VL53L4ED capabilities.

The firmware fully manages the hardware registers access.

Section 3.2: State machine description details the firmware state machine.

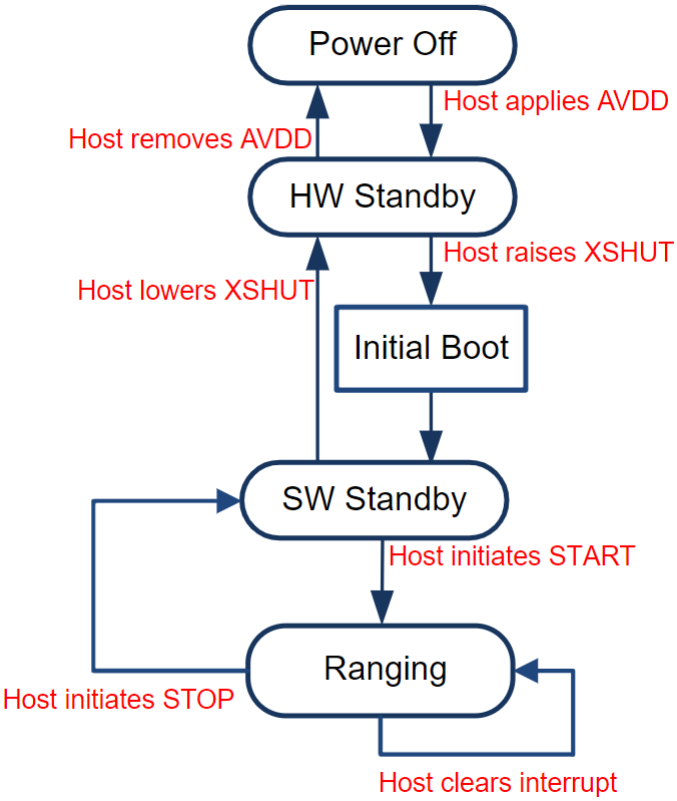
Figure 4. VL53L4ED system functional description



3.2 State machine description

The following figure shows the device state machine.

Figure 5. Device state machine



3.3 Customer manufacturing calibration flow

Up to two calibrations are needed to ensure the best sensor performance. Offset is needed in all applications. If a cover glass is used, crosstalk calibration is also needed.

3.4 Device programming and control

The I²C is the physical control interface of the device. It is described in Section 4: Control interface.

A software layer (driver) is also provided to control the device. This avoids complex I²C register operations. There are turnkey functions to start, stop, and read the ranging values.

3.5 Digital processing and reading the results

Digital processing is the final operation of the ranging sequence that computes, validates, or rejects a ranging measurement. All the processing is performed by the VL53L4ED internal firmware. The software driver allows reading the results when they are valid.

If the distance cannot be measured (because there is no target, or a weak signal), a corresponding status error code is generated. Te host can read this code.

3.6 Reading the results

The software driver provides turnkey functions to read output results after the measurement:

- Signal rate
- Ranging distance
- Min. and max. distances where an object is located
- Ambient light level
- Measurement status

3.7 Power sequence

There are two options available for device power-up and boot sequence.

Note: In all cases, XSHUT is raised only when AVDD is tied on.

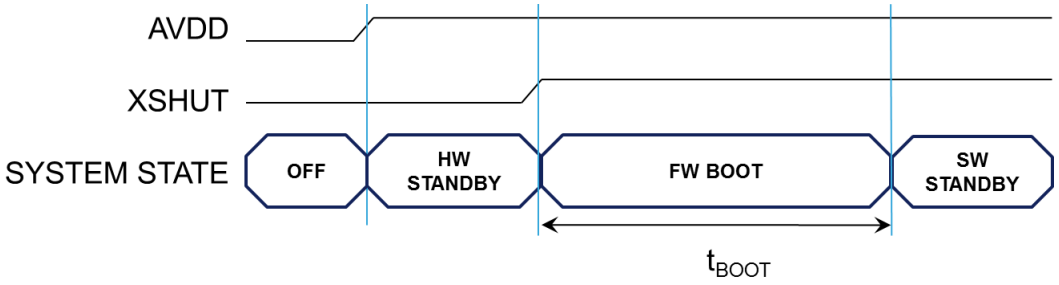
Option 1

The XSHUT pin is connected and controlled from the host.

This option optimizes power consumption. The device can be completely powered off when not used, and then woken up through the host (using the XSHUT pin).

Hardware standby (HW STANDBY) mode is the period when AVDD is present and XSHUT is low.

Figure 6. Power up and boot sequence



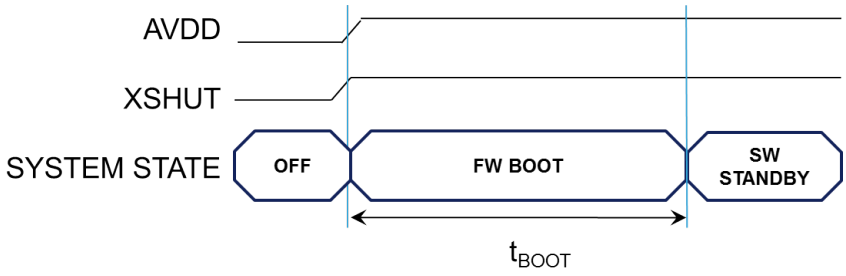
Note: t_{BOOT} is 1.2 ms maximum.

Option 2

The host does not control the XSHUT pin. This pin is tied to AVDD through the pull-up resistor.

When the XSHUT pin is not controlled, the power-up sequence is presented in the following figure. In this case, the device goes automatically to software standby (SW STANDBY) after firmware boot (FW BOOT), without entering HW STANDBY.

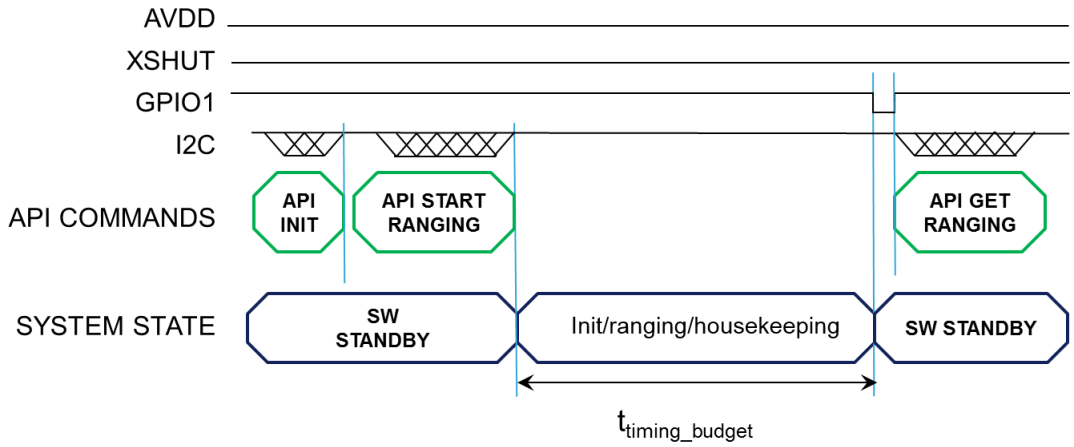
Figure 7. Power up and boot sequence with XSHUT not controlled



Note: t_{BOOT} is 1.2 ms maximum.

3.8 Ranging sequence

Figure 8. **Ranging sequence**



Note: API in the figure above means application programmable interface.

Note: t_{timing_budget} is a parameter set by the user, using a dedicated driver function.

3.9 Handshake management

Once a ranging measurement is available, an interrupt is generated. The driver communicates this to the host as a physical signal on the GPIO1 pin, which is then driven low. The former operating method is called a “hardware interrupt”, and the latter is referred to as a “polling mode”.

Once the host reads the result, the driver clears the interrupt, and the ranging sequence can continue. If the interrupt is not cleared, the ranging operation inside the device is on hold. The interrupt behavior allows good synchronization between the device and the host. This avoids results being lost if the host is not available to acquire or process the data.

It is strongly recommended to use the hardware interrupt pin to manage this handshake.

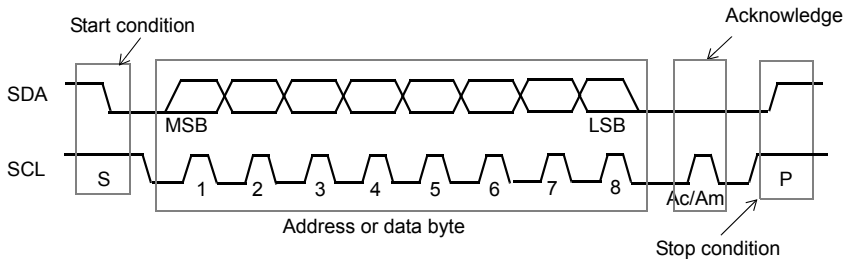
4 Control interface

This section specifies the control interface. The I²C interface uses two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus uses a unique address and a simple controller/target relationship exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high.

Clock signal generation is performed by the controller device. The controller device initiates data transfer. The I²C bus has a maximum speed of 1 Mbits/s and uses a default device address of 0x52.

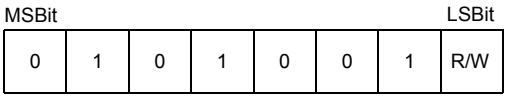
Figure 9. Data transfer protocol



Information is packed in 8-bit packets (bytes) and is always followed by an acknowledge bit, Ac for VL53L4ED acknowledge and Am for controller acknowledge (host bus controller). The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

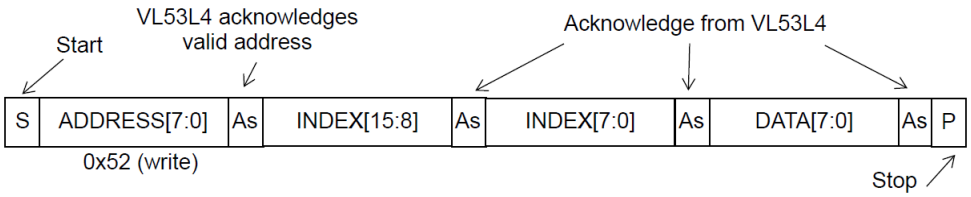
A message contains a series of bytes preceded by a start condition, and followed by either a stop or repeated start (another start condition but without a preceding stop condition), followed by another message. The first byte contains the device address (0x52) and also specifies the data direction. If the least significant bit is low (that is, 0x52) the message is a controller-write-to-the-target. If the LSB is set (that is, 0x53) then the message is a controller-read-from-the-target.

Figure 10. I²C device address: 0x52



All serial interface communications with the Time-of-Flight sensor must begin with a start condition. The VL53L4ED module acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (LSB of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence, the second byte received provides a 16-bit index, which points to one of the internal 8-bit registers.

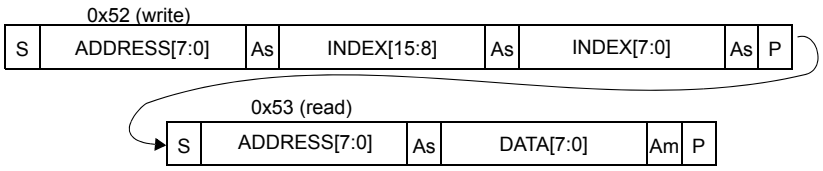
Figure 11. Data format (write)



As data are received by the target, they are written bit by bit to a serial/parallel register. After each data byte has been received by the target, an acknowledge is generated, the data are then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 12. Data format (read)



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the VL53L4ED for a write, and the host for a read).

A message can only be terminated by the bus controller, either by issuing a stop condition or by a negative acknowledge (that is, not pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The controller can therefore send data bytes continuously to the target until the target fails to provide an acknowledge, or the controller terminates the write communication with a stop condition. If the auto increment feature is used, the controller does not have to send address indexes to accompany the data bytes.

Figure 13. Data format (sequential write)

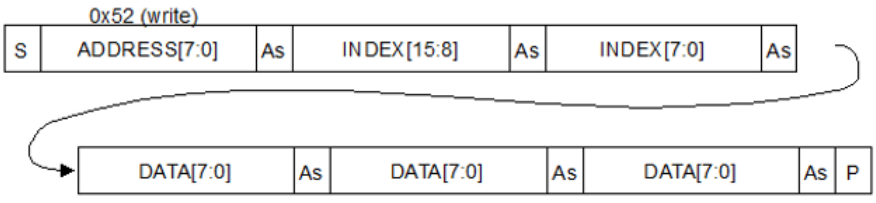
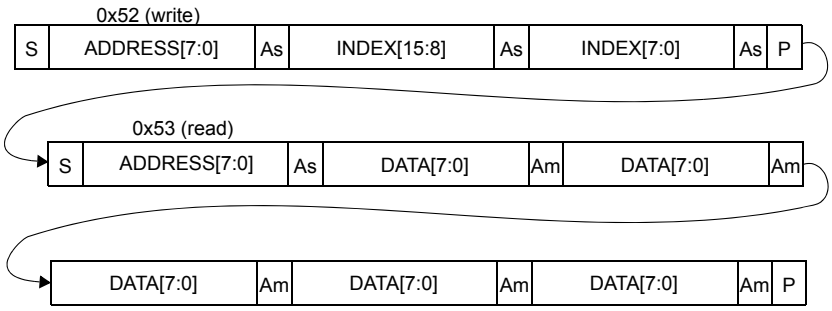


Figure 14. **Data format (sequential read)**



4.1 I²C interface - timing characteristics

Timing characteristics are shown in the following tables. Refer to Figure 15. I²C timing characteristics for an explanation of the parameters used.

Timings are given for all PVT conditions.

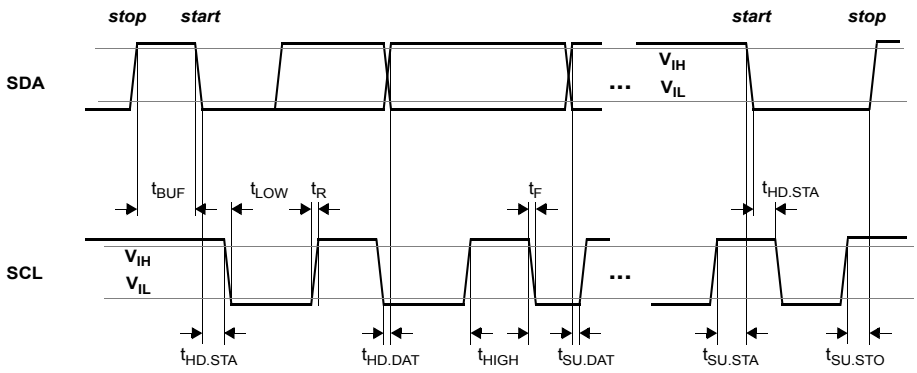
Table 5. **I²C interface - timing characteristics for fast mode plus (1 MHz)**

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	1000	kHz
t_{LOW}	Clock pulse width low	0.5	—	—	µs
t_{HIGH}	Clock pulse width high	0.26	—	—	
t_{SP}	Pulse width of spikes that are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	0.5	—	—	µs
$t_{HD.STA}$	Start hold time	0.26	—	—	
$t_{SU.STA}$	Start setup time	0.26	—	—	
$t_{HD.DAT}$	Data in hold time	0	—	0.9	
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	120	
t_F	SCL/SDA fall time	—	—	120	
$t_{SU.STO}$	Stop set-up time	0.26	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
CIN	Input capacitance (SCL)	—	—	4	
C_L	Load capacitance	—	140	550	

Table 6. I²C interface - timing characteristics for fast mode (400 kHz)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	400	kHz
t_{LOW}	Clock pulse width low	1.3	—	—	µs
t_{HIGH}	Clock pulse width high	0.6	—	—	
t_{SP}	Pulse width of spikes that are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	1.3	—	—	µs
$t_{HD.STA}$	Start hold time	0.26	—	—	
$t_{SU.STA}$	Start setup time	0.26	—	—	
$t_{HD.DAT}$	Data in hold time	0	—	0.9	
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	300	
t_F	SCL/SDA fall time	—	—	300	
$t_{SU.STO}$	Stop set-up time	0.6	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
CIN	Input capacitance (SCL)	—	—	4	
C_L	Load capacitance	—	125	400	

Figure 15. I²C timing characteristics



IL or V_{IH}.

All timings are measured from either V_{IL} or V_{IH}.

4.2 I²C interface - reference registers

The registers shown in the table below can be used to validate the user I²C interface.

Table 7. Reference registers

Register name	Index	Value
Model_ID	0x010F	0xEC
Module_Type	0x0110	0xAA

Note: The I²C read/writes can be 8, 16 or 32-bit. Multibyte reads/writes are always addressed in ascending order with MSB first as shown in the following table.

The customer must use the VL53L4ED software driver for easy and efficient ranging operations to match performance and accuracy criteria. Hence, full register details are not exposed.

Table 8. 32-bit register example

Register address	Byte
Address	MSB
Address + 1	—
Address + 2	—
Address + 3	LSB

5 Thermal characteristics

5.1 Absolute maximum rating (T_{STG})

Warning: *Stresses above those listed in the following table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device is not implied at these or any other conditions above those indicated in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

The storage temperature (T_{STG}) is the ambient temperature at which the device can be stored with no voltage applied.

Table 9. Absolute maximum rating conditions

Parameter	Min.	Max.	Unit
Storage temperature (T_{STG})	-40	125	°C

5.2 Ambient operating temperature

The ambient operating temperature is the temperature at which the device may be powered and can operate without any damage.

Table 10. Recommended operating temperature

Parameter	Min.	Max.	Unit
Ambient operating temperature	-40	105	°C

6 Electrical characteristics

6.1 Absolute maximum ratings

Warning: *Stresses above those listed in the following table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device is not implied at these or any other conditions above those indicated in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Table 11. Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
AVDD	-0.5	—	3.4	V
SCL, SDA, XSHUT, and GPIO1				

6.2 Recommended operating conditions

There are no power supply sequencing requirements. The I/Os may be high, low, or floating when AVDD is applied. The I/Os are internally failsafe with no diode connecting them to AVDD.

Table 12. Recommended operating conditions

Parameter	Min.	Typ.	Max.	Unit
Voltage (AVDD)	2.7	2.8	3.4	V
IO (IOVDD) (1)	1.7	1.8/2.8	3.4	

1. *XSHUT should be high only when AVDD is on.*

6.3 Electrostatic discharge

The VL53L4ED is compliant with the electrostatic discharge (ESD) values presented in the following table.

Table 13. ESD performances

Parameter	Specification	Conditions
Human body model	JS-001-2012	± 2 kV, 1500 ohms, 100 pF
Charged device model	JESD22-C101	± 500 V

6.4 Current consumption

Table 14. Power consumption at ambient temperature

All current consumption values include silicon process variations. Temperature and voltage are nominal conditions (23°C and 2v8). All values include AVDD and AVDDVCSEL.

Parameter	Min.	Typ.	Max.	Unit
HW STANDBY	3	5	7	µA
SW STANDBY	4	6	9	
Active ranging average consumption (including VCSEL) (1) (2)		22	24	mA

1. *Active ranging is an average value, measured using the default driver settings.*
2. *Peak current (including VCSEL) can reach 40 mA.*

6.5 Digital input and output

Table 15. Digital I/O electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
Interrupt pin (GPIO1)					
VIL	Low level input voltage	—	—	0.3 IOVDD	V
VIH	High level input voltage	0.7 IOVDD		—	
VOL	Low level output voltage (IOUT = 4 mA)	—		0.4	
VOH	High level output voltage (IOUT = 4 mA)	IOVDD-0.4		—	
FGPIO	Operating frequency (CLOAD = 20 pF)	0		108	MHz
I²C interface (SDA/SCL)					
VIL	Low level input voltage	-0.5	—	0.6	V
VIH	High level input voltage	1.12		3.5	
VOL	Low level output voltage (IOUT = 4 mA)	—		0.4	
IIL/IH	Leakage current (1)	—		10	
	Leakage current (2)	—		0.15	µA

1. *AVDD = 0 V*
2. *AVDD = 2.85 V, and I/O voltage = 1.8 V*

7 Ranging performances

7.1 Measurement conditions

In all the measurement tables of this document, it is considered that:

- All ranging performances are measured with the target covering the full FoV.
- Targets used are Munsell N4.75 (17%), Munsell N8.25 (54%), and Munsell N9.5 (88%).
- Nominal voltage is 2.8 V.
- The device is controlled through the driver using the default settings.
- Indoor (no IR) means that there is no contribution of light in the band 940 nm ± 30 nm.
- Light, outdoor overcast corresponds to an ambient light level of 10 kcps/SPAD. For reference, this corresponds to a 1.2 W/m^2 at 940 nm following the AM1.5G spectrum. It is equivalent to 5 kLux of daylight as reflected by a gray 17% chart at 40 cm.
- No cover glass is present.
- Typical and corner samples are used.
- An offset correction is made at 100 mm from the sensor with a gray 17% target.

7.2 Minimum ranging distance

The minimum detection distance is 0 mm. The minimum ranging distance with a linear response is 1 mm.

7.3 Maximum ranging distance at nominal temperature

The table below shows the ranging specification for the VL53L4ED bare module. This is without a cover glass, at room temperature (23°C), with nominal voltage (2.8 V), and the full FoV covered.

The timing budget enables control over the quantity of emitted signals. A higher timing budget results in the emission of more signals, thereby increasing the temperature variation robustness. It is strongly recommended to use a minimum timing budget of 100 ms to ensure consistent data over the temperature range. All measurements have been made using 100 ms integration time.

Table 16. Nominal maximum ranging distance mode for typical parts (100 ms timing budget)

Target reflectance level, full FoV (reflectance %)	Indoor (detection rate %)	Outdoor detection rate (%)
White target (88%)	Typical: 1250 mm @ 90% min. Typical: 1300 mm @ 50% min.	Typical: 750 mm @ 90% min. Typical: 800 mm @ 50% min.
Light gray target (54%)	Typical: 950 mm @ 90% min. Typical: 1000 mm @ 50% min.	Typical: 700 mm @ 90% min. Typical: 750 mm @ 50% min.
Gray target (17%)	Typical: 450 mm @ 90% min. Typical: 500 mm @ 50% min.	Typical: 400 mm @ 90% min. Typical: 450 mm @ 50% min.

The detection rate is a statistical value indicating the worst case percentage of measurements that return a valid ranging. For example, taking 1000 measurements with a 90% detection rate, gives 900 valid distances. The 100 other distances may be outside of the specification, and are flagged with an error status.

7.4 Evolution of maximum ranging distance over temperature

The figures below show the evolution of the maximum ranging distance over all temperatures for the VL53L4ED bare module. This is without a cover glass at nominal voltage (2.8 V), and with the full FoV covered.

Figure 16. Evolution of maximum ranging distance over temperature for typical parts (100 ms timing budget, 0 klx)

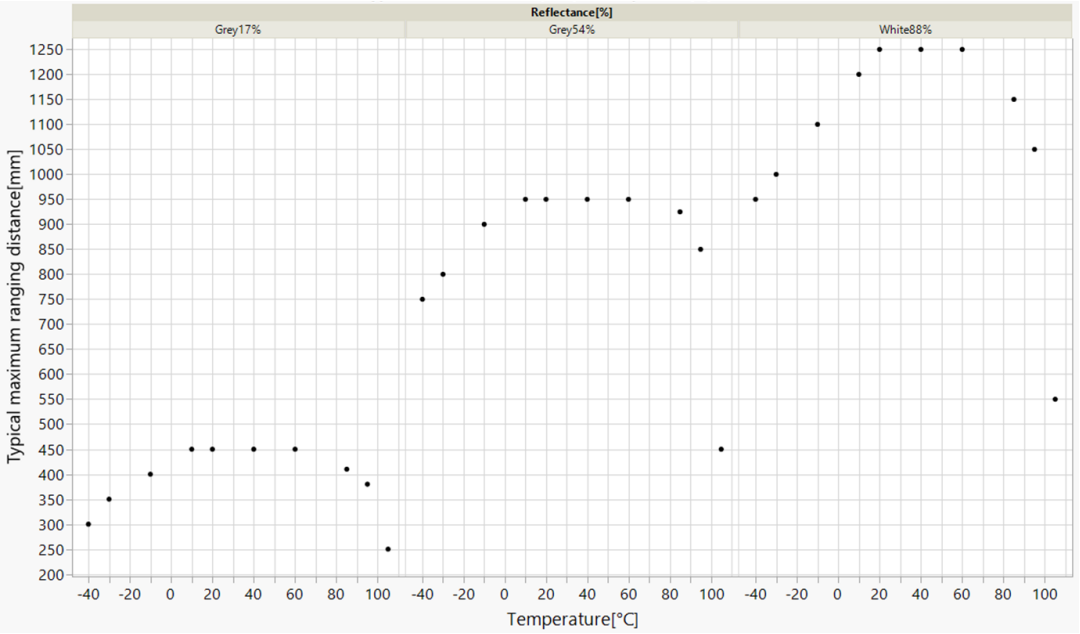
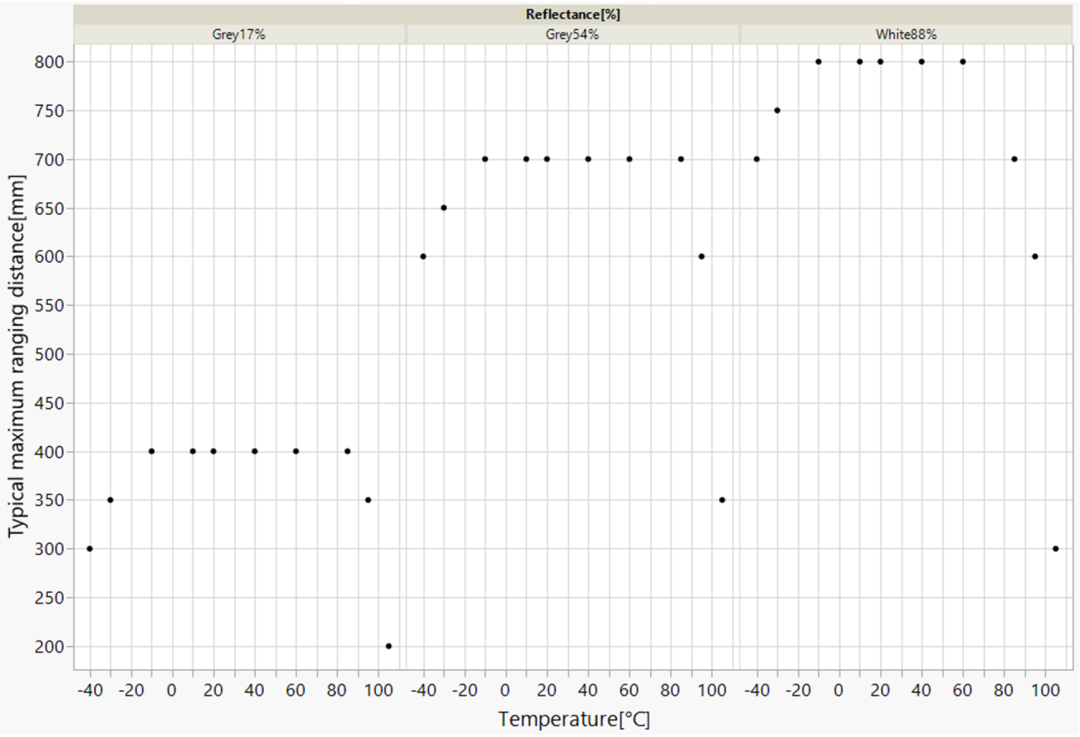


Figure 17. Evolution of maximum ranging distance over temperature for typical parts (100 ms timing budget, 5 klx)

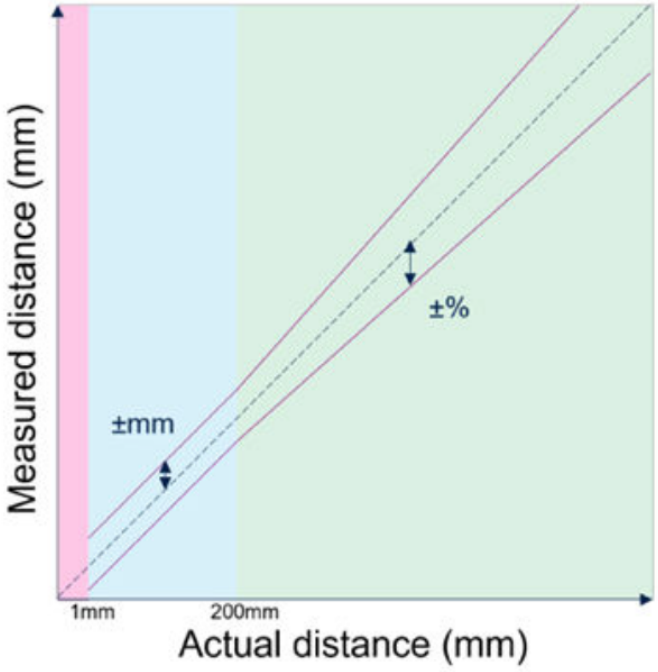


7.5 Ranging accuracy

7.5.1 Ranging accuracy definition

The figure below illustrates how range accuracy is defined over distance.

Figure 18. Ranging accuracy vs. distance



The ranging accuracy is a direct evaluation of the measurement error, including offset errors and output noise. At least 90% of the ranging values are within the declared ranges. This quality indicator includes measure-to-measure and part-to-part dispersion.

7.5.2 Ranging accuracy at nominal temperature

The following table shows the ranging accuracy for the VL53L4ED bare module. This is without a cover glass, at room temperature (23°C), with nominal voltage (2.8 V), and the full FoV covered.

Table 17. Ranging accuracy for a typical part at 100 ms timing budget

Target reflectance level with full FoV (reflectance %)	Distance (mm)	Indoor (0 klx)	Outdoor (5 klx)
White target (88%)	1-100	± 6 mm	± 7 mm
	101-200	± 7 mm	± 7 mm
	>200	± 2%	± 5%
Light gray target (54%)	1-100	± 5 mm	± 6 mm
	101-200	± 6 mm	± 7 mm
	>200	± 3%	± 5%
Gray target (17%)	1-100	± 5 mm	± 6 mm
	101-200	± 6 mm	± 7 mm
	>200	± 3%	± 4%

7.5.3 Evolution of accuracy over temperature

Figure 19. Evolution of accuracy over temperature for a typical part (100 ms timing budget, 0 klx) and Figure 20. Evolution of accuracy over temperature for a typical part (100 ms timing budget, 5 klx) show the evolution of accuracy over all temperatures for the VL53L4ED bare module. Measurements were taken without a cover glass at nominal voltage (2.8 V), and with the full FoV covered. Both figures represent 100 measurements made at a single reference distance of 300 mm.

Figure 21. Box plot range definition shows the data spread compared to the real distance.

Figure 19. Evolution of accuracy over temperature for a typical part (100 ms timing budget, 0 klx)

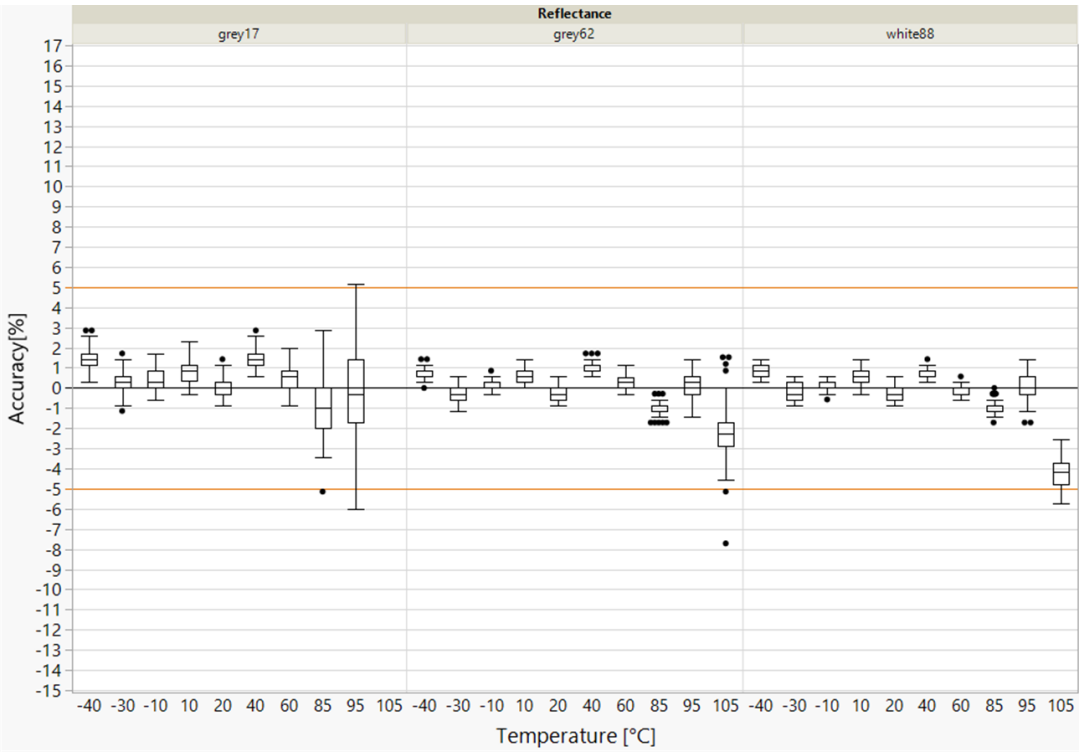


Figure 20. **Evolution of accuracy over temperature for a typical part (100 ms timing budget, 5 klx)**

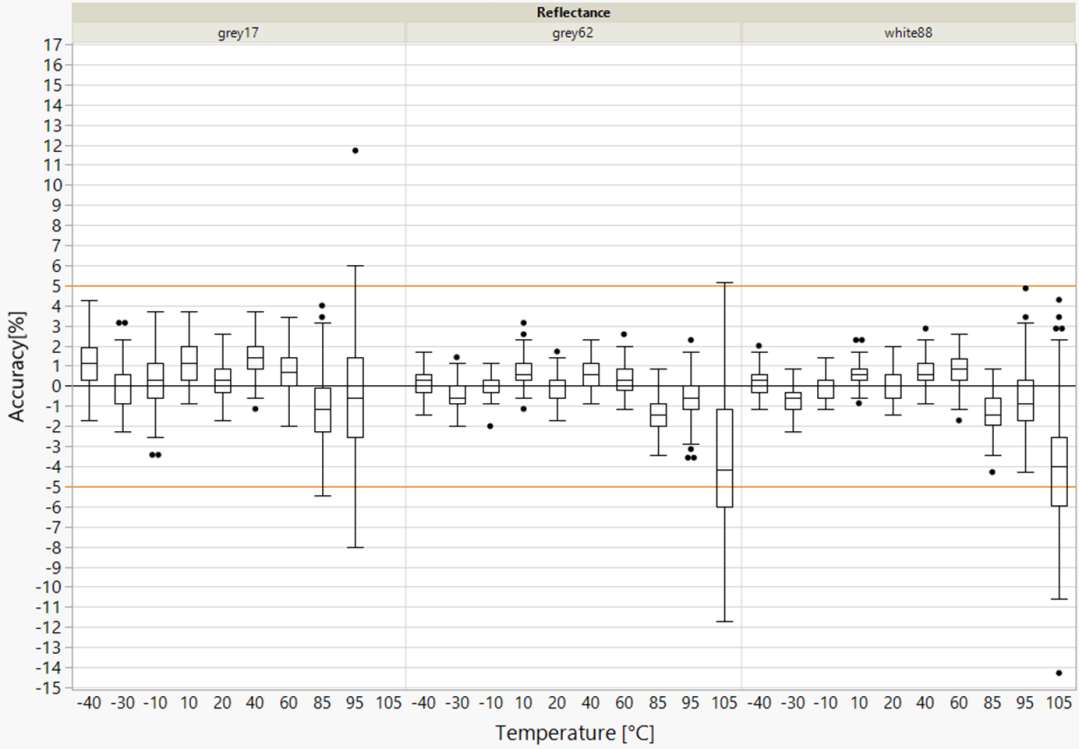
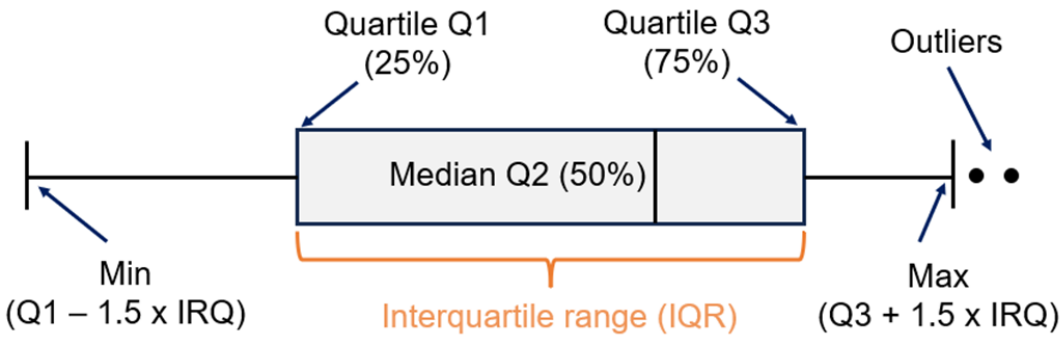


Figure 21. **Box plot range definition**



7.6 Ranging drift with temperature

When the temperature increases, the ranging value may be affected.

This value is an offset and not a gain, and it does not depend on the target distance.

The device embeds a feature that allows compensation of the temperature variation effect.

To get the most accurate performances, perform a manual temperature update when temperature varies. This operation is done using a dedicated driver function.

8 Outline drawings

STMicroelectronics delivers any of the dual source cap assemblies shown below. Both versions are transparent for the customer, since the pad and substrate design are identical for both versions and have no impact on the customer PCB design. Ranging performances, reflow, and technical parameters are identical for both module designs presented in the second figure below.

Note: The module drawings below are based on DM00726192, rev 4.0.

Figure 22. Outline drawing (1/5)

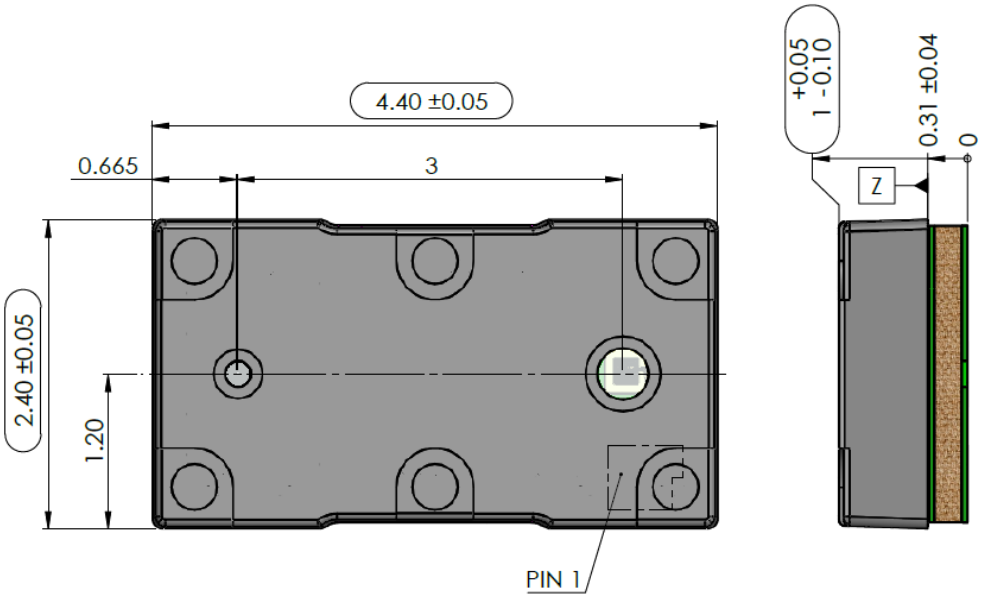


Figure 23. Outline drawing (2/5)

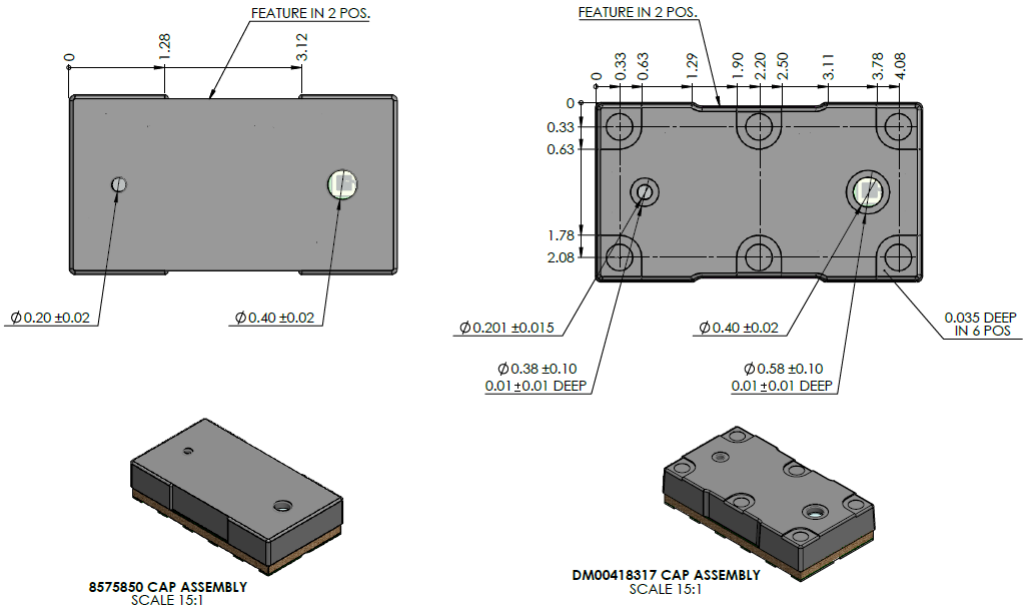
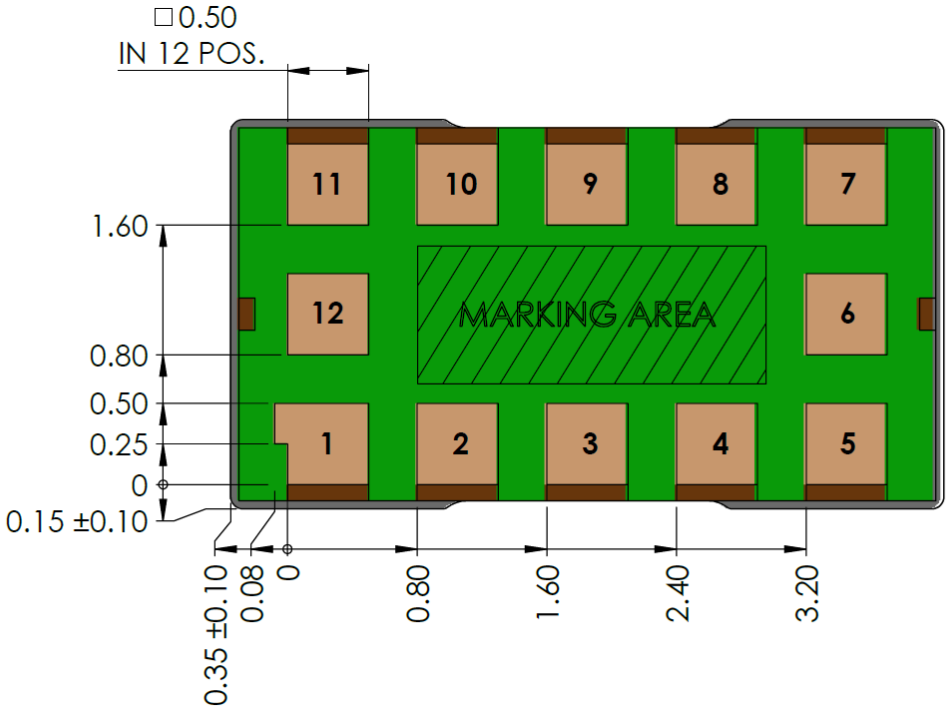


Figure 24. **Outline drawing (3/5)**



Note: For more information, refer to Table 2. VL53L4ED pin description.

Figure 25. **Outline drawing - option with liner (4/5)**

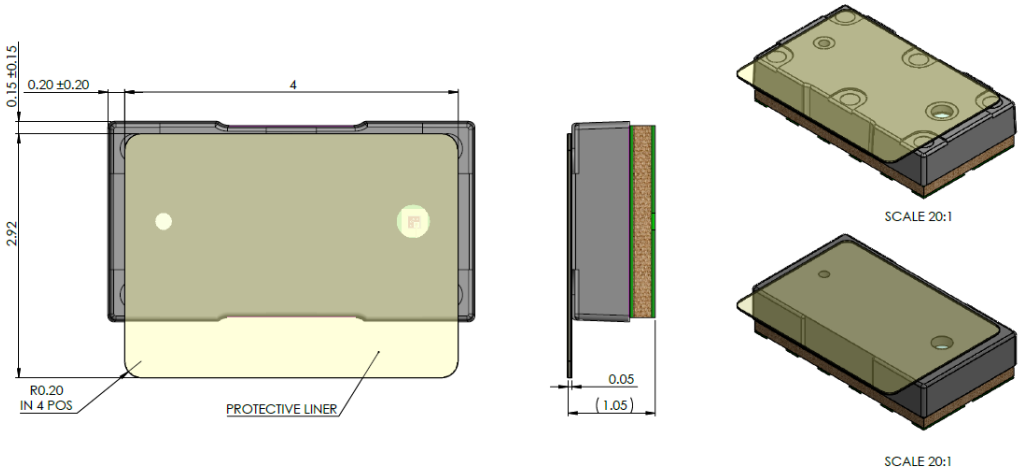
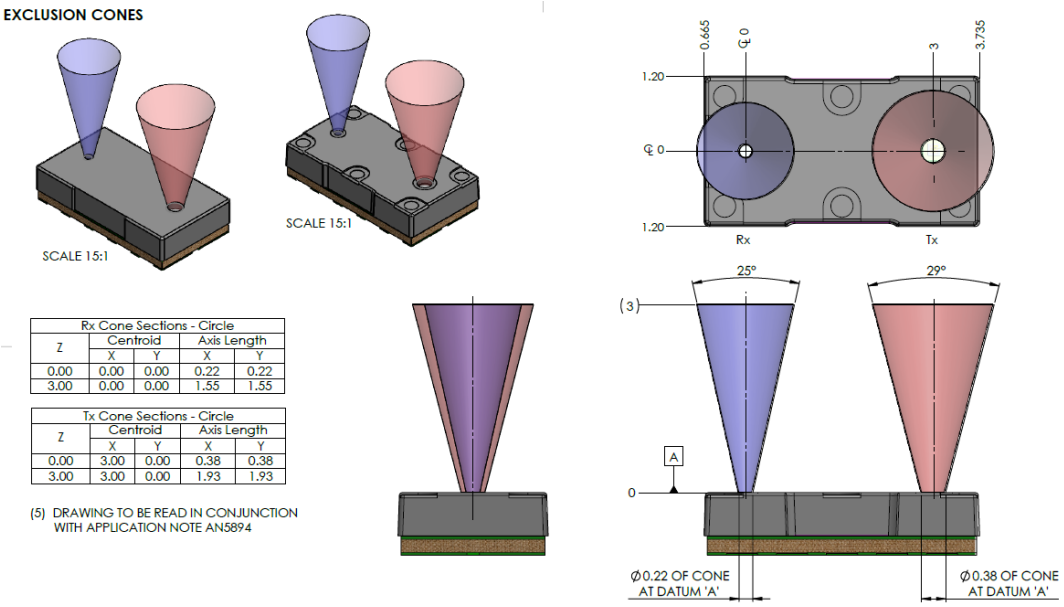


Figure 26. **Outline drawing (5/5)**



Rx Cone Sections - Circle				
Z	Centroid		Axis Length	
	X	Y	X	Y
0.00	0.00	0.00	0.22	0.22
3.00	0.00	0.00	1.55	1.55

Tx Cone Sections - Circle				
Z	Centroid		Axis Length	
	X	Y	X	Y
0.00	3.00	0.00	0.38	0.38
3.00	3.00	0.00	1.93	1.93

(5) DRAWING TO BE READ IN CONJUNCTION WITH APPLICATION NOTE AN5894

9 Field of view and field of illumination

The Rx (or collector) exclusion zone includes all module assembly tolerances and is used to define the cover glass dimensions. The cover glass opening must be equal to or wider than the exclusion zone.

The detection volume represents the applicative or system FoV in which a target is detected, and a distance measured. It is determined by the Rx lens or the Rx aperture, and is narrower than the exclusion zone.

Figure 27. System FoV and exclusion zone description (not to scale)

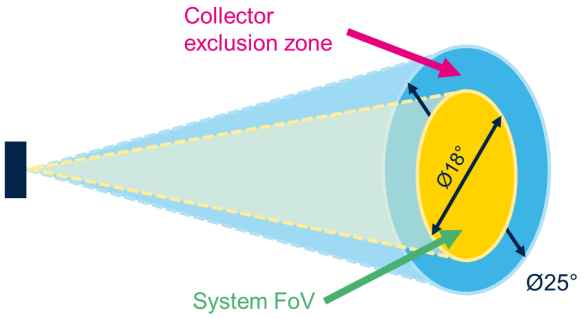


Table 18. FoV angles

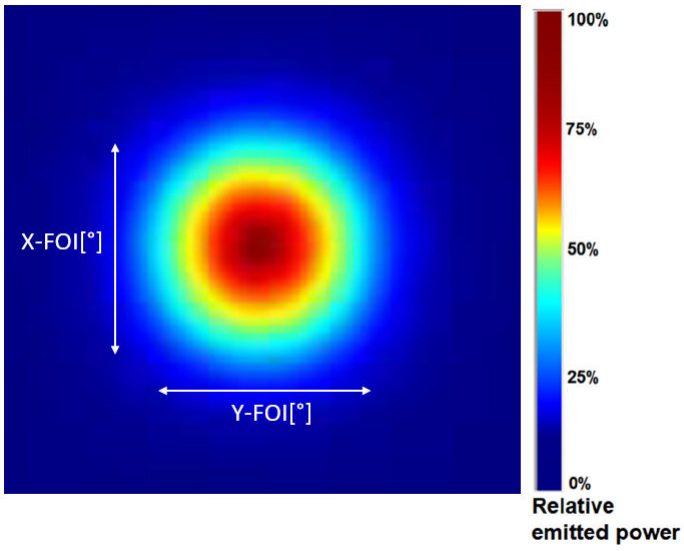
Setting	Target at 100 mm (white 88%)	Target at 1000 mm (white 88%)
Detection volume (°)	22°	18°
Collector exclusion cone (°)	25°	25°

Note: Detection volume depends on the environment and sensor configuration as well as target distance, reflectance, ambient light level, sensor timing budget, distance mode, and tuning parameters.

Note: The detection volume of Table 18. FoV angles has been measured with a white 88% reflectance perpendicular target in full FoV, located at 100 mm and 1000 mm from the sensor, without ambient light (dark conditions), using the default driver configuration.

The VCSEL FoI is shown in the figure below. The X-axis is 16° and the Y-axis is 16° (1/e²).

Figure 28. VL53L4ED FoI



10 Laser safety

This product contains a laser emitter and corresponding drive circuitry. The laser output is designed to meet Class 1 laser safety limits under all reasonably foreseeable conditions including single faults in compliance with IEC 60825-1:2014.

Do not increase the laser output power by any means. Do not use any optics to focus the laser beam.

Caution: Use of controls or adjustments, or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Figure 29. Class 1 laser label

This product complies with:

- IEC 60825-1:2014
- 21 CFR 1040.10 and 1040.11, except for conformance with IEC 60825-1:2014 as described in the laser notice number 56, dated May 8, 2019.
- EN 60825-1:2014 including EN 60825-1:2014/A11:2021
- EN 50689:2021, however STMicroelectronics does not guarantee compliance with the requirement of clause 5 from EN50689 regarding child appealing products. If designing a child appealing product, contact STMicroelectronics' technical application support.

11 Packing and labeling

11.1 Product marking

A two line product marking is applied on the backside of the module (on the substrate). The first line is the silicon product code, and the second line, the internal tracking code.

11.2 Inner box labeling

The labeling follows the STMicroelectronics' standard packing acceptance specification.

The following information is on the inner box label:

- Assembly site
- Sales type
- Quantity
- Trace code
- Marking
- Bulk ID number

11.3 Packing

At customer level, it is recommended to mount the device in a clean environment to avoid foreign material deposition.

To help avoid any foreign material contamination at product assembly level, the module is shipped in a tape and reel format. The tape is described in Section 11.4: Tape outline drawing.

The packing is vacuum sealed and includes a desiccant.

11.4 Tape outline drawing

The pictures below show the tape outline drawings for modules without and with liner. The pin1 of the module is referenced by a red star in the figures.

Figure 30. Tape outline drawing - option modules without liner

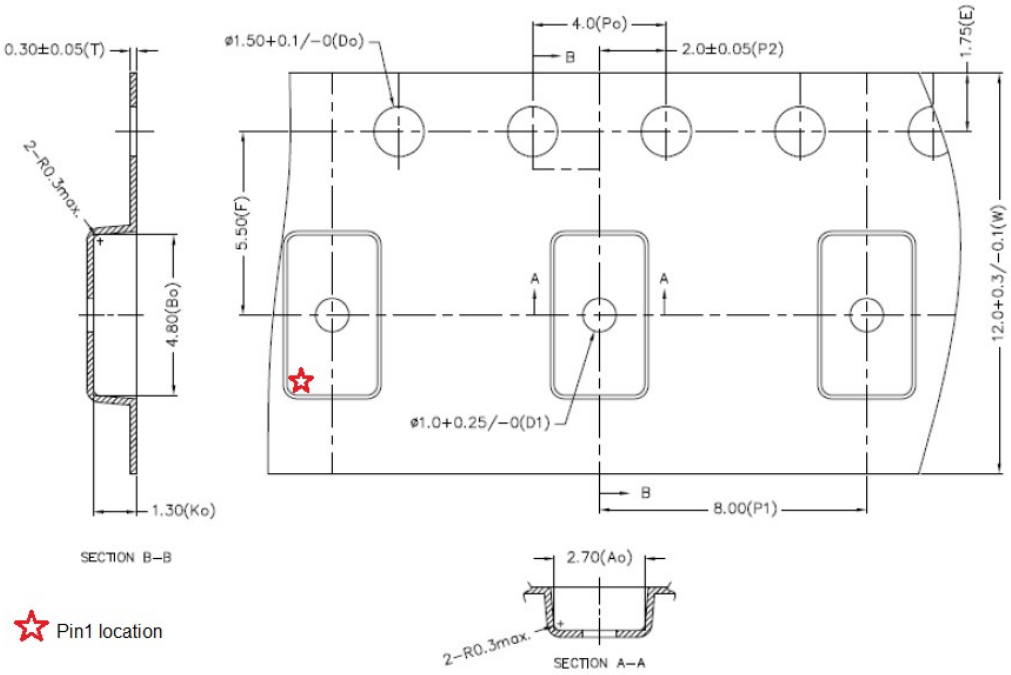
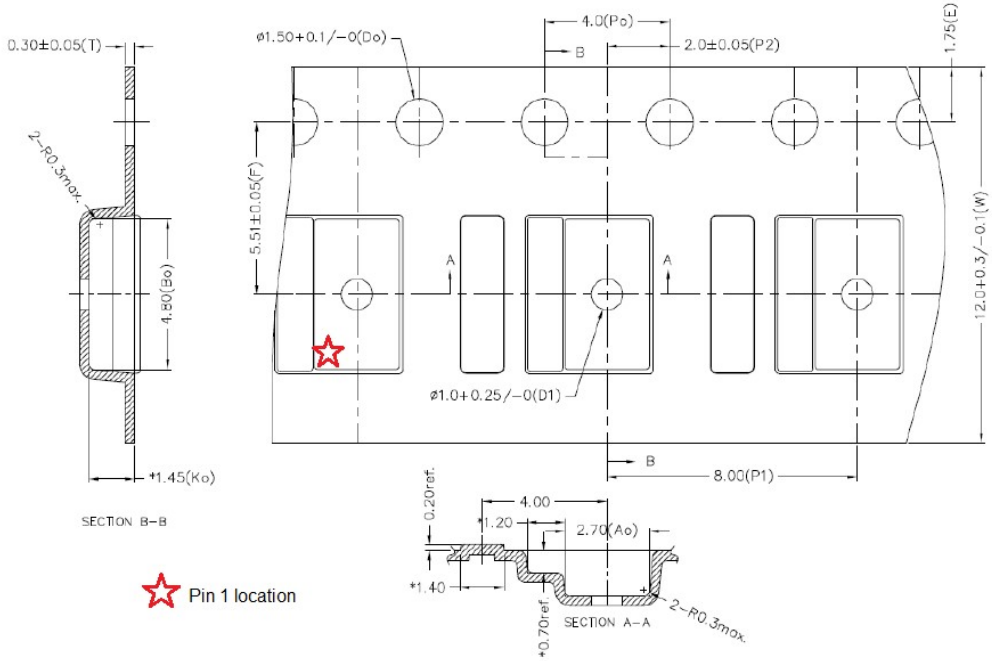


Figure 31. Tape outline drawing - option modules with liner



Caution: For sensors with the liner option, the liner must be removed during assembly of the customer device, just before mounting the cover glass. The liner is compliant with a reflow at 260°C (as per JEDEC-JSTD-020-C).

12 Handling, moisture, and reflow precautions

12.1 Shock precaution

Sensor modules house numerous internal components that are susceptible to shock damage. If a unit is subject to excessive shock, it must be rejected even if no apparent damage is visible. For example, if it is dropped on the floor, or if a tray/reel of units is dropped on the floor.

12.2 Part handling

Handling must be done with nonmarring, ESD, safe carbon, plastic, or Teflon™ tweezers. Ranging modules are susceptible to damage or contamination. The customer is advised to use a clean assembly process after removing the tape from the parts, and until a protective cover glass is mounted.

12.3 Compression force

A maximum compressive load of 25 N should be applied on the module.

12.4 Moisture sensitivity level

Moisture sensitivity is level 3 (MSL) as described in JEDEC JSTD-020-C.

For devices that are classified to the levels defined in JEDEC JSTD-020-C, JEDEC JSTD-033-C provides:

- Manufacturers and users with standardized methods for handling, packing, and shipping.
- Standardized methods for using moisture/reflow and process sensitive devices.

12.5 Pb-free solder reflow process

Table 19. Recommended solder profile and Figure 32. Solder profile show the recommended and maximum values for the solder profile.

Customers have to tune the reflow profile depending on the PCB, solder paste, and material used. We expect customers to follow the recommended reflow profile, which is specifically tuned for the VL53L4ED package.

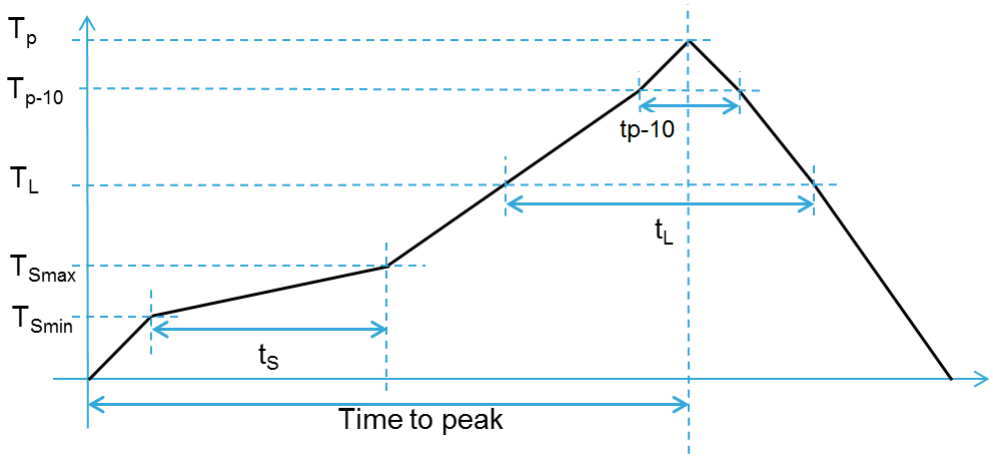
If a customer must perform a reflow profile which is different from the recommended one, the new profile must be qualified by the customer at their own risk. This is especially true for peak >240°C. In any case, the profile must be within the “maximum” profile limit described in JEDEC JSTD-020-C and in the table below.

Note: Temperatures mentioned in the following table are measured at the top of the VL53L4ED package.

Table 19. Recommended solder profile

Parameters	Recommended	Maximum	Unit
Minimum temperature (TS min)	130	150	°C
Maximum temperature (TS max)	200	200	
Time ts (TS min to TS max)	90-110	60-120	s
Temperature (TL)	217	217	°C
Time (tL)	55-65	55-65	s
Ramp up	2	3	°C/s
Temperature (Tp-10)	—	250	°C
Time (tp-10)		10	s
Ramp up		3	°C/s
Peak temperature (Tp)	240	260 max	°C
Time to peak	30	300	s
Ramp down (peak to Tl)	-4	-6	°C/s

Figure 32. **Solder profile**



Note: The component should be limited to a maximum of three passes through this solder profile.

Note: As the VL53L4ED package is not sealed, only a dry reflow process should be used (such as convection reflow). Vapor phase reflow is not suitable for this type of optical component.

Note: The VL53L4ED is an optical component and as such, it should be treated carefully. This would typically include using a 'no wash' assembly process.

13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

14 Ordering information

The VL53L4ED is currently available in the formats below. More detailed information is available on request.

Table 20. Order codes

Order codes	Package	Packing	Minimum order quantity
VL53L4EDV0DH/1	Optical LGA12 with liner	Tape and reel	4500 pcs
VL53L4EDV9DH/1	Optical LGA12 without liner	Tape and reel	4500 pcs

Revision history

Table 21. **Document revision history**

Date	Version	Changes
14-Dec-2023	1	Initial release
26-Apr-2024	2	Section 8: Outline drawings: Updated text, added two notes, modified outline drawings 1-4, and added Figure 26. Outline drawing (5/5). Table 15. Digital I/O electrical characteristics: Updated the maximum value of VIH for the I²C interface (SDA/SCL). Updated Section 10: Laser safety. Section 11.3: Packing: Added a note. Updated Section 11.4: Tape outline drawing. Section 14: Ordering information: Added new text and updated Table 20. Order codes.
12-Jul-2024	3	Added Section 5: Thermal characteristics. Updated Section 11: Packing and labeling. Added Section 12: Handling, moisture, and reflow precautions.

Contents

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