74LVC1G66

Bilateral switch

Rev. 14.1 — 3 September 2024 Product data sheet

1. General description

The 74LVC1G66 is a single-pole, single-throw analog switch with two input/output terminals (nY and nZ) and a digital enable input (nE). When nE is LOW, the analog switch is turned off. Control inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at control inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
  - 7.5 Ω (typical) at V_{CC} = 2.7 V
  - 6.5 Ω (typical) at V_{CC} = 3.3 V
  - 6 Ω (typical) at V_{CC} = 5 V
- Switch current capability of 32 mA
- High noise immunity
- CMOS low power consumption
- TTL interface compatibility at 3.3 V
- Overvoltage tolerant control inputs to 5.5 V
- Latch-up performance meets requirements of JESD78 Class I
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G66GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G66GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G66GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G66GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G66GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G66GZ	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	SOT8065-1

4. Marking

Table 2. Marking

Type number	Marking code [1]
74LVC1G66GW	VL
74LVC1G66GV	V66
74LVC1G66GM	VL
74LVC1G66GN	VL
74LVC1G66GS	VL
74LVC1G66GZ	VL

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

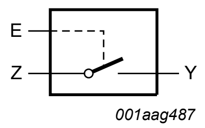


Fig. 1. Logic symbol

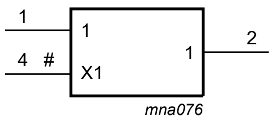


Fig. 2. IEC logic symbol

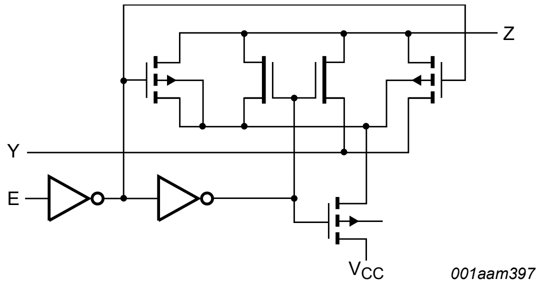
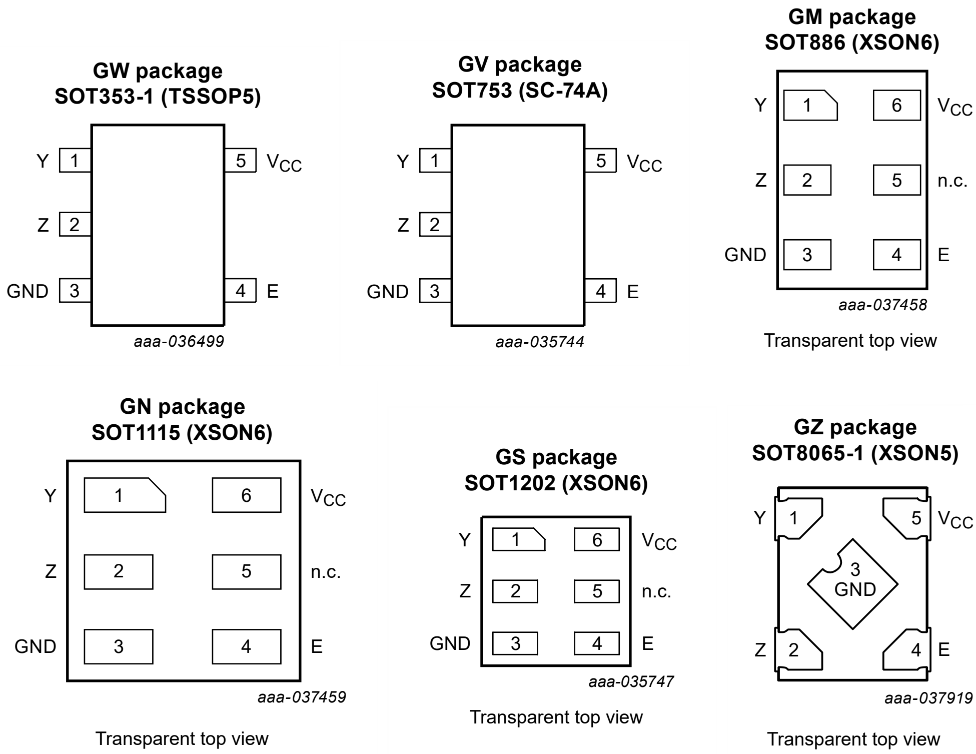


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT353-1, SOT753, SOT8065-1	SOT886, SOT1115 and SOT1202	
Y	1	1	independent input or output
Z	2	2	independent output or input
GND	3	3	ground (0 V)
E	4	4	enable input (active HIGH)
n.c.	-	5	not connected
V_{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input E	Switch
L	OFF-state
H	ON-state

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-50	-	mA
I_{SK}	switch clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±50	mA
V_{SW}	switch voltage	enable and disable mode [2]	-0.5	V_{CC} + 0.5	V
I_{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 ° C to +125 °C [3]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.
For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT8065-1 (XSON5) package: P_{tot} derates linearly with 3.2 mW/K above 72 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_{SW}	switch voltage	[1]	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V [2]	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V [2]	-	-	10	ns/V

[1] To avoid sinking GND current from terminal Z when switch current flows in terminal Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Y. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

10. Static characteristics

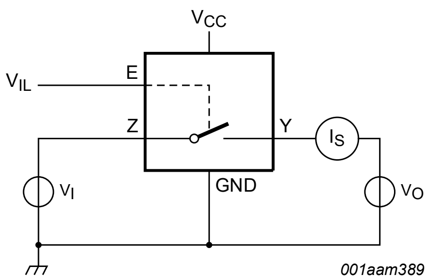
Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		V_{CC} = 2.3 V to 2.7 V		1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V		$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V		-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V		-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
I_I	input leakage current	pin E; V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	[2]	-	±0.1	±1	-	±1	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 5.5 V; see Fig. 4	[2]	-	±0.1	±0.2	-	±0.5	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 5.5 V; see Fig. 5	[2]	-	±0.1	±1	-	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{SW} = GND or V_{CC}; V_{CC} = 1.65 V to 5.5 V	[2]	-	0.1	4	-	4	μA
ΔI_{CC}	additional supply current	pin E; V_I = V_{CC} - 0.6 V; V_{SW} = GND or V_{CC}; V_{CC} = 5.5 V	[2]	-	5	500	-	500	μA
C_I	input capacitance			-	2.0	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance			-	6.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance			-	11	-	-	-	pF

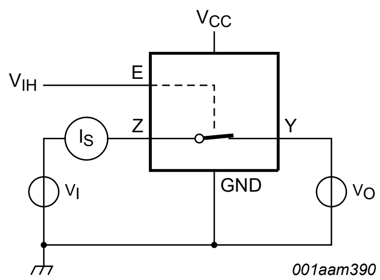
[1] All typical values are measured at T_{amb} = 25 °C.
[2] These typical values are measured at V_{CC} = 3.3 V.

10.1. Test circuits



V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Fig. 4. Test circuit for measuring OFF-state leakage current



V_I = V_{CC} or GND and V_O = open circuit.

Fig. 5. Test circuit for measuring ON-state leakage current

10.2. ON resistance

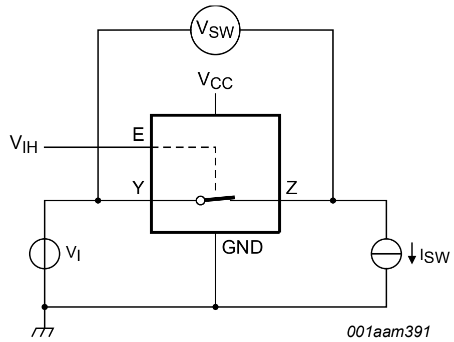
Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 6; for graphs see Fig. 7 to Fig. 12.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}						
		I_{SW} = 4 mA; V_{CC} = 1.65 V to 1.95 V	-	34.0	130	-	195	Ω
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	12.0	30	-	45	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	10.4	25	-	38	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	7.8	20	-	30	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	6.2	15	-	23	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND						
		I_{SW} = 4 mA; V_{CC} = 1.65 V to 1.95 V	-	8.2	18	-	27	Ω
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	7.1	16	-	24	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	6.9	14	-	21	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	6.5	12	-	18	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	5.8	10	-	15	Ω
		V_I = V_{CC}						
		I_{SW} = 4 mA; V_{CC} = 1.65 V to 1.95 V	-	10.4	30	-	45	Ω
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	7.6	20	-	30	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	7.0	18	-	27	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	6.1	15	-	23	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	4.9	10	-	15	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = GND to V_{CC} [2]						
		I_{SW} = 4 mA; V_{CC} = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	3.5	-	-	-	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	2.0	-	-	-	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

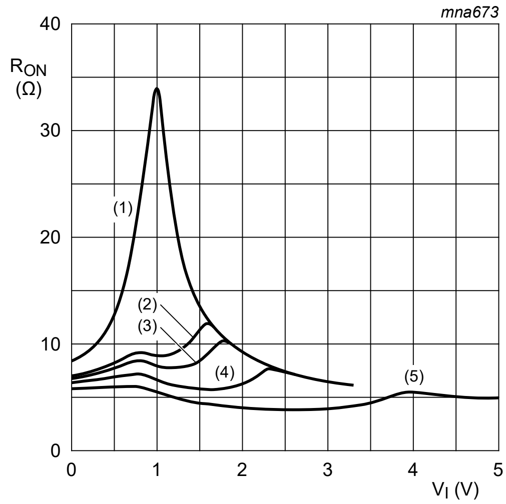
[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3. ON resistance test circuit and graphs



$R_{ON} = V_{SW}/I_{SW}$.

Fig. 6. Test circuit for measuring ON resistance



(1) V_{CC} = 1.8 V.

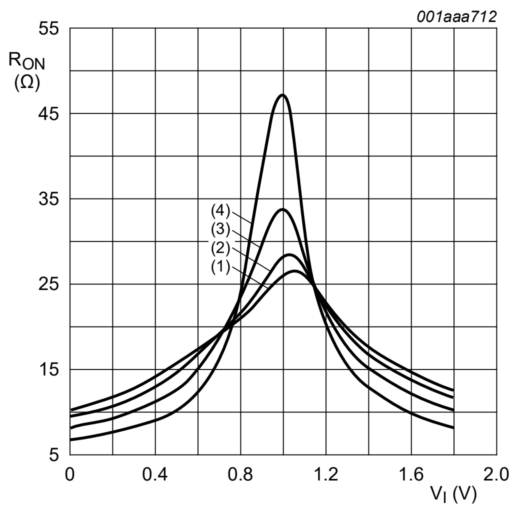
(2) V_{CC} = 2.5 V.

(3) V_{CC} = 2.7 V.

(4) V_{CC} = 3.3 V.

(5) V_{CC} = 5.0 V.

Fig. 7. Typical ON resistance as a function of input voltage; T_{amb} = 25 °C



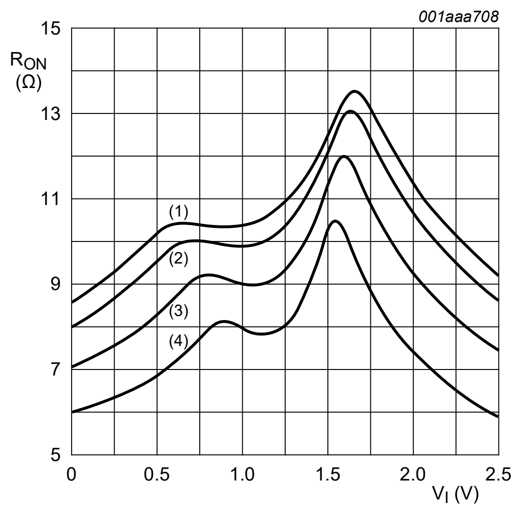
(1) T_{amb} = 125 °C.

(2) T_{amb} = 85 °C.

(3) T_{amb} = 25 °C.

(4) T_{amb} = -40 °C.

Fig. 8. ON resistance as a function of input voltage; V_{CC} = 1.8 V



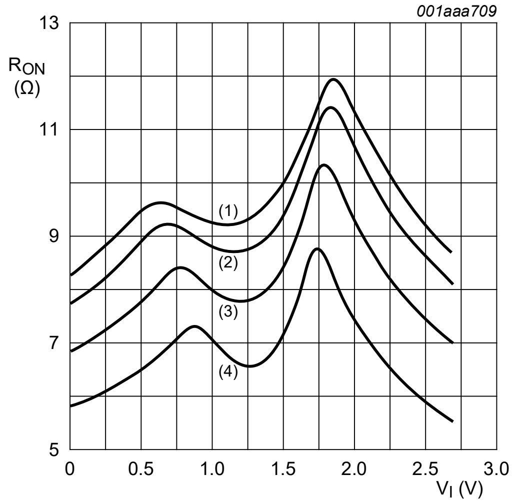
(1) T_{amb} = 125 °C.

(2) T_{amb} = 85 °C.

(3) T_{amb} = 25 °C.

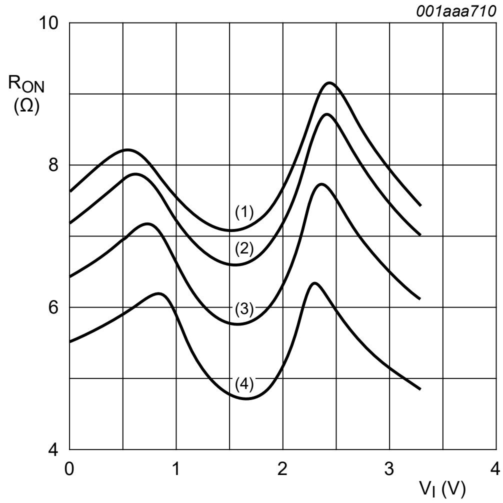
(4) T_{amb} = -40 °C.

Fig. 9. ON resistance as a function of input voltage; V_{CC} = 2.5 V



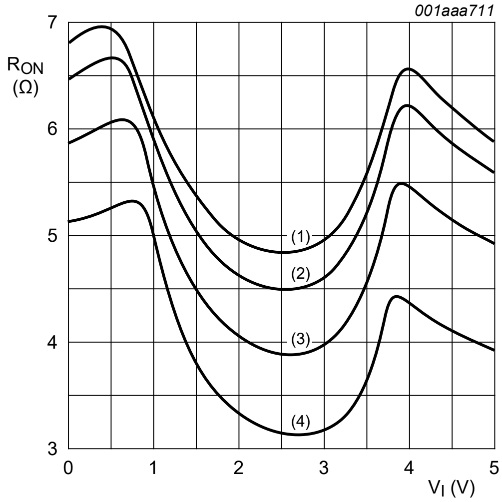
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = -40 °C.

Fig. 10. ON resistance as a function of input voltage; V_{CC} = 2.7 V



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = -40 °C.

Fig. 11. ON resistance as a function of input voltage; V_{CC} = 3.3 V



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = -40 °C.

Fig. 12. ON resistance as a function of input voltage; V_{CC} = 5.0 V

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 15.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	Y to Z or Z to Y; see Fig. 13 [2] [3]						
		V_{CC} = 1.65 V to 1.95 V	-	0.8	2.0	-	3.0	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.4	1.2	-	2.0	ns
		V_{CC} = 2.7 V	-	0.4	1.0	-	1.5	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.3	0.8	-	1.5	ns
		V_{CC} = 4.5 V to 5.5 V	-	0.2	0.6	-	1.0	ns
t_{en}	enable time	E to Y or Z; see Fig. 14 [4]						
		V_{CC} = 1.65 V to 1.95 V	1.0	5.3	12	1.0	15.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.0	6.5	1.0	8.5	ns
		V_{CC} = 2.7 V	1.0	2.6	6.0	1.0	8.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.5	5.0	1.0	6.5	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	1.9	4.2	1.0	5.5	ns
t_{dis}	disable time	E to Y or Z; see Fig. 14 [5]						
		V_{CC} = 1.65 V to 1.95 V	1.0	4.2	10	1.0	13	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.4	6.9	1.0	9.0	ns
		V_{CC} = 2.7 V	1.0	3.6	7.5	1.0	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.4	6.5	1.0	8.5	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.5	5.0	1.0	6.5	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 10 MHz; V_I = GND to V_{CC} [6]						
		V_{CC} = 2.5 V	-	9.8	-	-	-	pF
		V_{CC} = 3.3 V	-	12.0	-	-	-	pF
		V_{CC} = 5.0 V	-	17.3	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}
[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).
[4] t_{en} is the same as t_{PZH} and t_{PZL}
[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}
[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

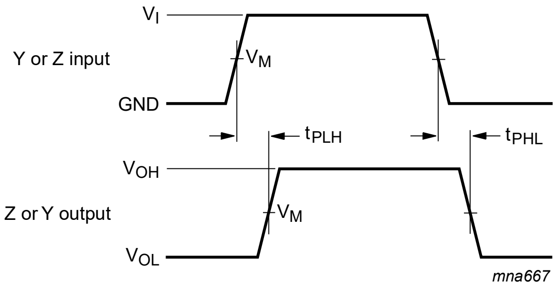
$C_{S(ON)}$ = maximum ON-state switch capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ = sum of the outputs.

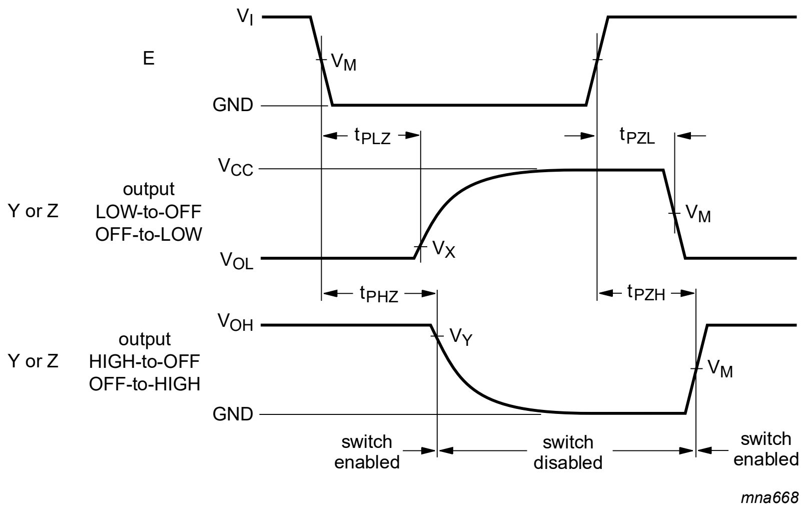
11.1. Waveforms and test circuit



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 13. Input (Y or Z) to output (Z or Y) propagation delays



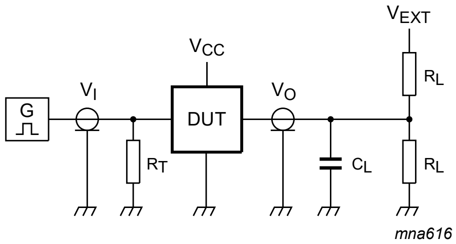
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 14. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 11.
Definitions for test circuit:
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;
C_L = Load capacitance including jig and probe capacitance;
R_L = Load resistance;
V_{EXT} = External voltage for measuring switching times.

Fig. 15. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

11.2. Additional dynamic characteristics

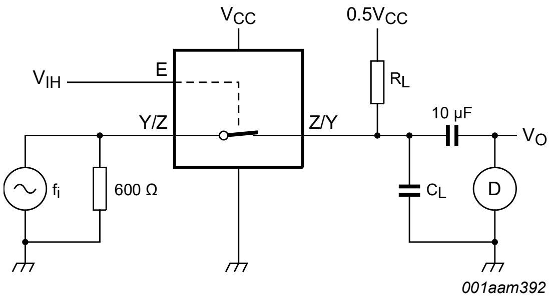
Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	R_L = 10 kΩ; C_L = 50 pF; f_i = 1 kHz; see Fig. 16				
		V_{CC} = 1.65 V	-	0.032	-	%
		V_{CC} = 2.3 V	-	0.008	-	%
		V_{CC} = 3.0 V	-	0.006	-	%
		V_{CC} = 4.5 V	-	0.001	-	%
		R_L = 10 kΩ; C_L = 50 pF; f_i = 10 kHz; see Fig. 16				
		V_{CC} = 1.65 V	-	0.068	-	%
		V_{CC} = 2.3 V	-	0.009	-	%
		V_{CC} = 3.0 V	-	0.008	-	%
		V_{CC} = 4.5 V	-	0.006	-	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(-3dB)}$	-3 dB frequency response	R_L = 600 Ω; C_L = 50 pF; see Fig. 17				
		V_{CC} = 1.65 V	-	135	-	MHz
		V_{CC} = 2.3 V	-	145	-	MHz
		V_{CC} = 3.0 V	-	150	-	MHz
		V_{CC} = 4.5 V	-	155	-	MHz
		R_L = 50 Ω; C_L = 5 pF; see Fig. 17				
		V_{CC} = 1.65 V	-	> 500	-	MHz
		V_{CC} = 2.3 V	-	> 500	-	MHz
		V_{CC} = 3.0 V	-	> 500	-	MHz
		V_{CC} = 4.5 V	-	> 500	-	MHz
		R_L = 50 Ω; C_L = 10 pF; see Fig. 17				
		V_{CC} = 1.65 V	-	200	-	MHz
		V_{CC} = 2.3 V	-	350	-	MHz
		V_{CC} = 3.0 V	-	410	-	MHz
		V_{CC} = 4.5 V	-	440	-	MHz
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Fig. 18				
		V_{CC} = 1.65 V	-	-46	-	dB
		V_{CC} = 2.3 V	-	-46	-	dB
		V_{CC} = 3.0 V	-	-46	-	dB
		V_{CC} = 4.5 V	-	-46	-	dB
		R_L = 50 Ω; C_L = 5 pF; f_i = 1 MHz; see Fig. 18				
		V_{CC} = 1.65 V	-	-37	-	dB
		V_{CC} = 2.3 V	-	-37	-	dB
		V_{CC} = 3.0 V	-	-37	-	dB
		V_{CC} = 4.5 V	-	-37	-	dB
V_{ct}	crosstalk voltage	between digital input and switch; R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; t_r = t_f = 2 ns; see Fig. 19				
		V_{CC} = 1.65 V	-	69	-	mV
		V_{CC} = 2.3 V	-	87	-	mV
		V_{CC} = 3.0 V	-	156	-	mV
		V_{CC} = 4.5 V	-	302	-	mV
Q_{inj}	charge injection	C_L = 0.1 nF; V_{gen} = 0 V; R_{gen} = 0 Ω; f_i = 1 MHz; R_L = 1 MΩ; see Fig. 20				
		V_{CC} = 1.8 V	-	3.3	-	pC
		V_{CC} = 2.5 V	-	4.1	-	pC
		V_{CC} = 3.3 V	-	5.0	-	pC
		V_{CC} = 4.5 V	-	6.4	-	pC
		V_{CC} = 5.5 V	-	7.5	-	pC

11.3. Test circuits



Test conditions:

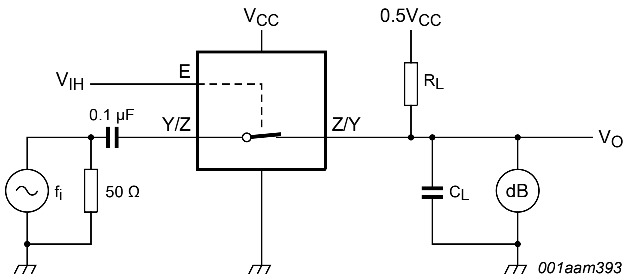
V_{CC} = 1.65 V: V_i = 1.4 V (p-p).

V_{CC} = 2.3 V: V_i = 2 V (p-p).

V_{CC} = 3 V: V_i = 2.5 V (p-p).

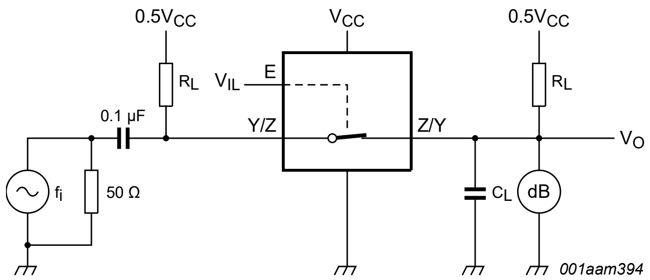
V_{CC} = 4.5 V: V_i = 4 V (p-p).

Fig. 16. Test circuit for measuring total harmonic distortion



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 17. Test circuit for measuring the frequency response when switch is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 18. Test circuit for measuring isolation (OFF-state)

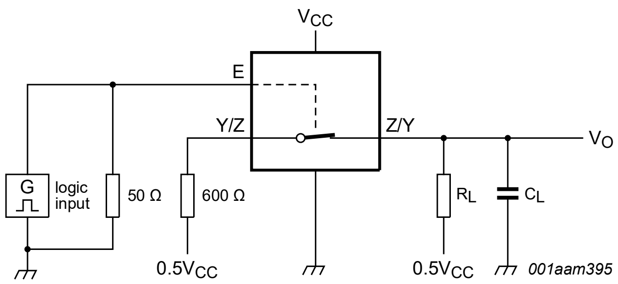
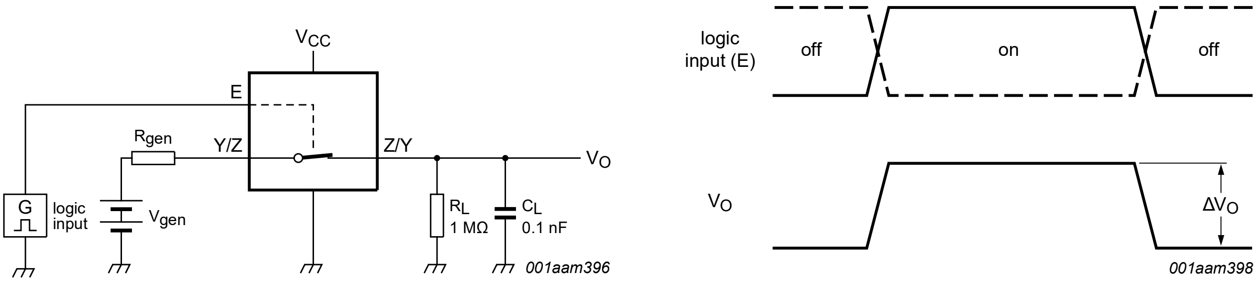


Fig. 19. Test circuit for measuring crosstalk between digital input and switch



$Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

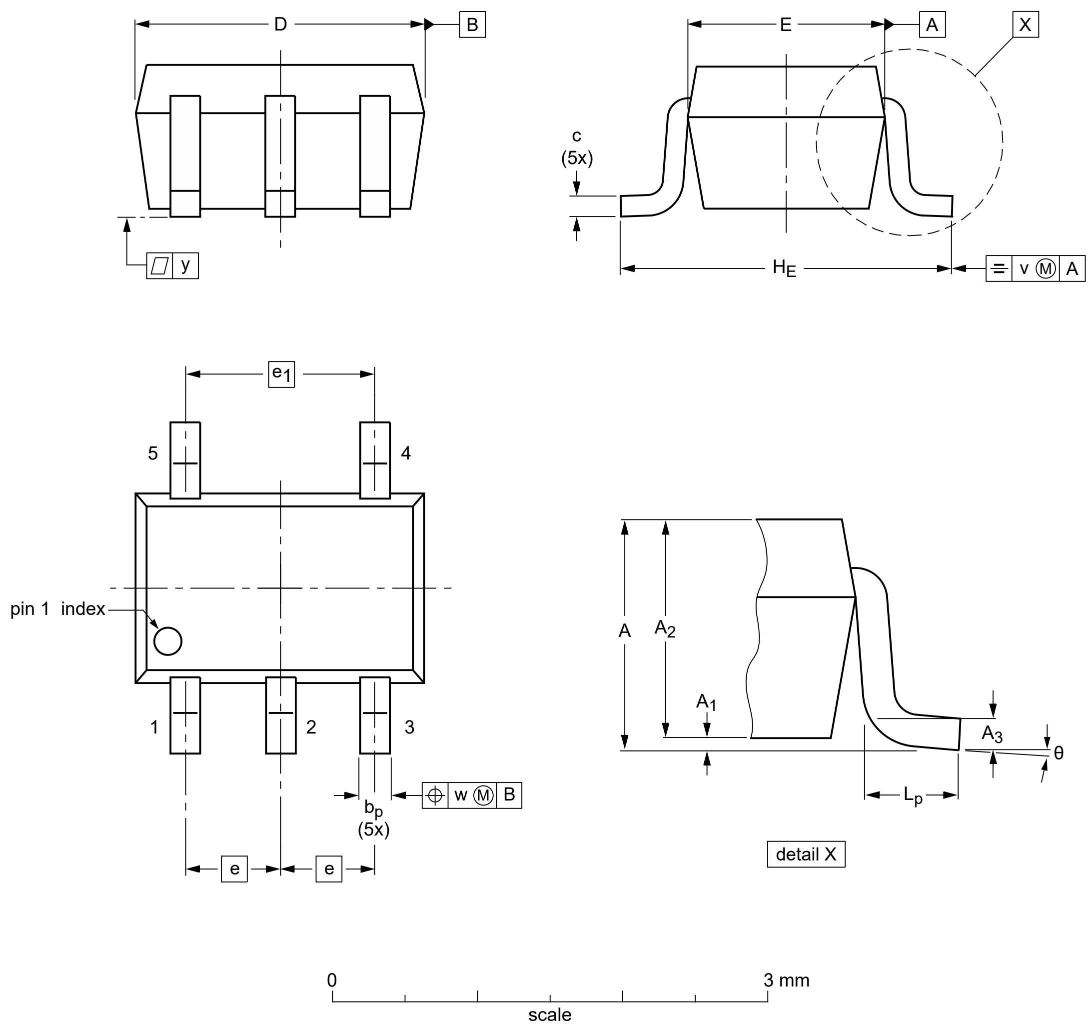
R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig. 20. Test circuit for measuring charge injection

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

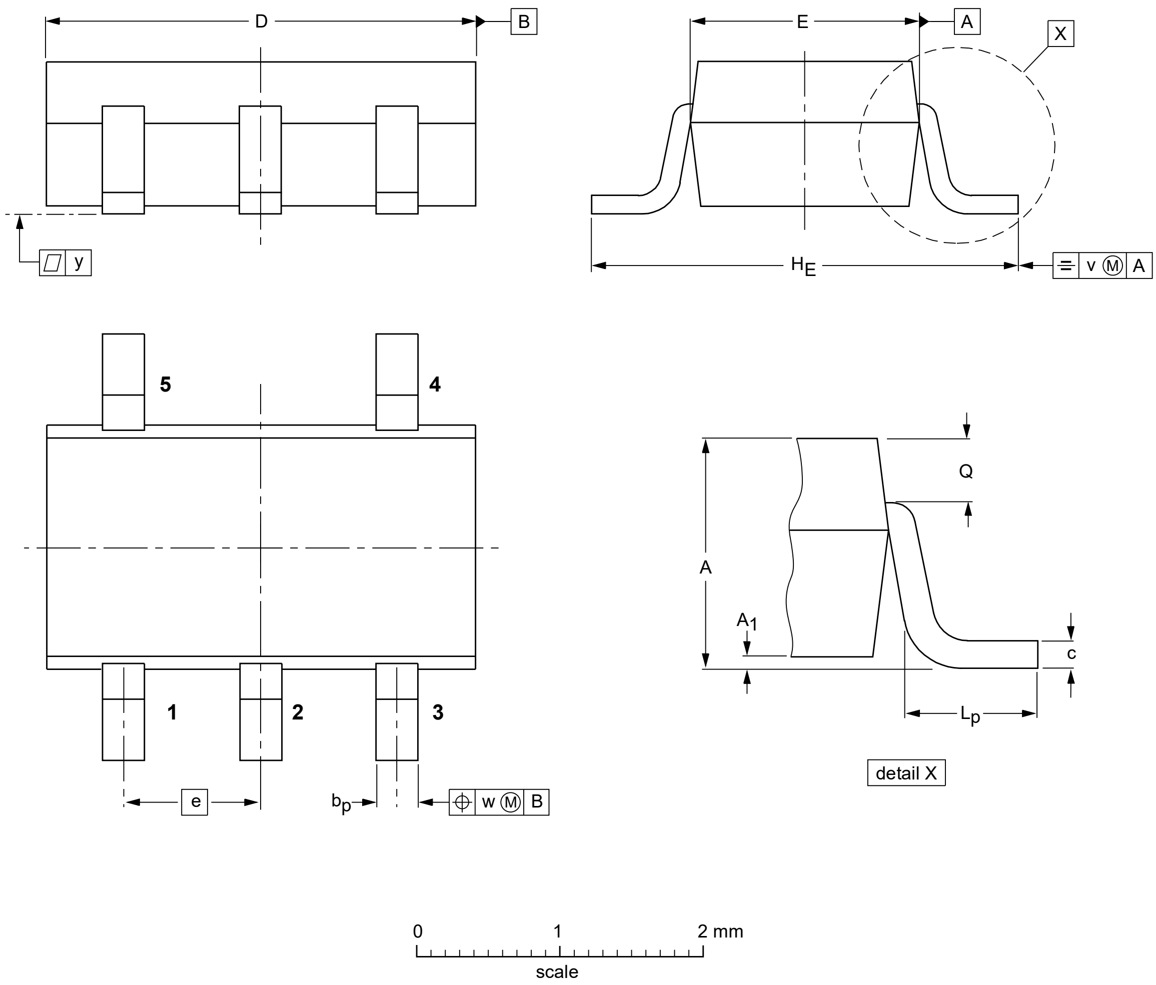
Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 21. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

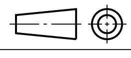
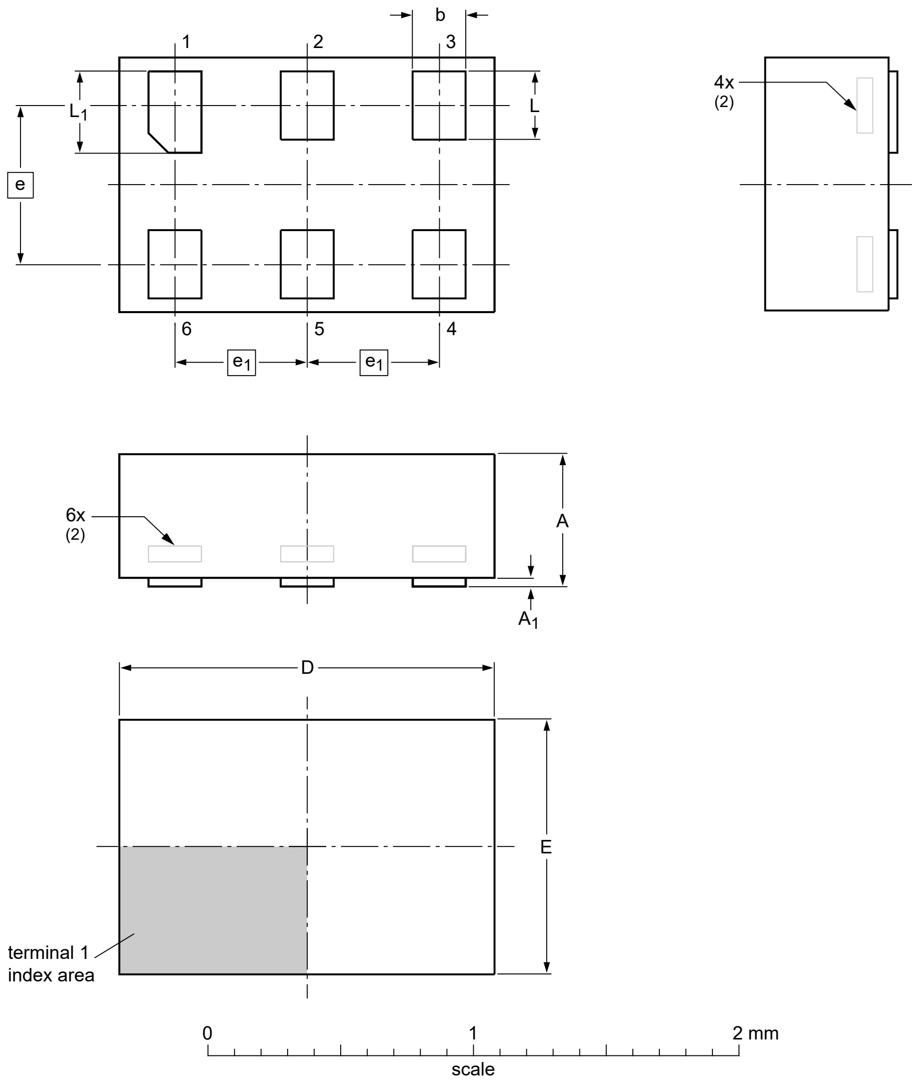
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 22. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

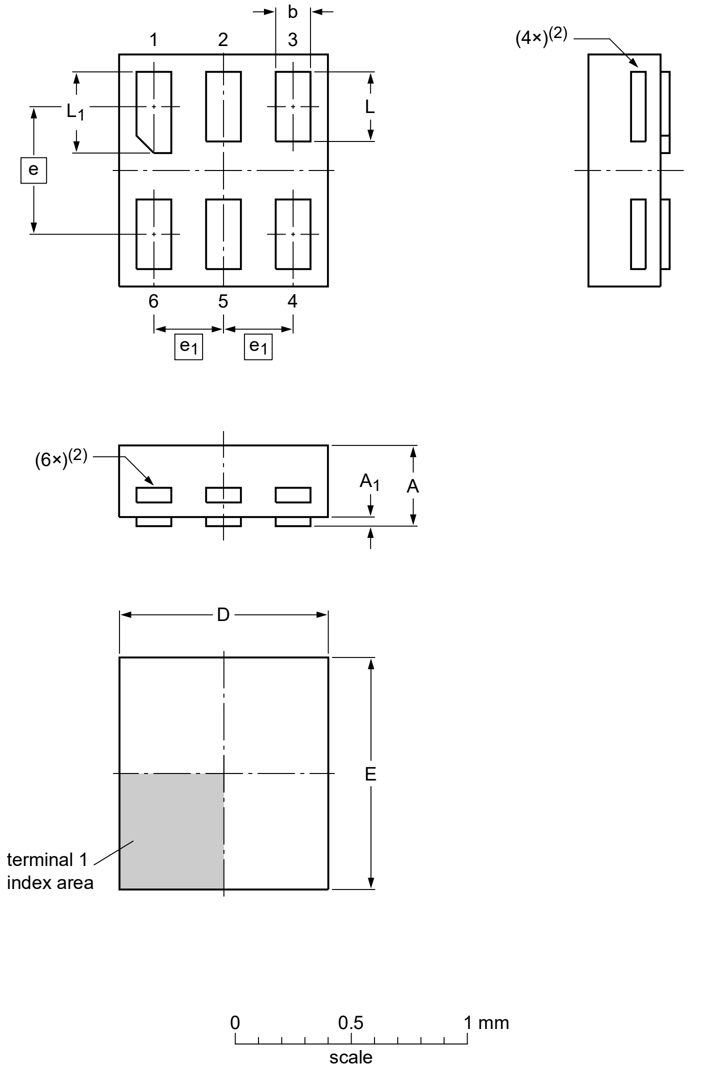
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig. 23. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm **SOT1115**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
mm	nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min			0.12	0.85	0.95			0.27	0.32

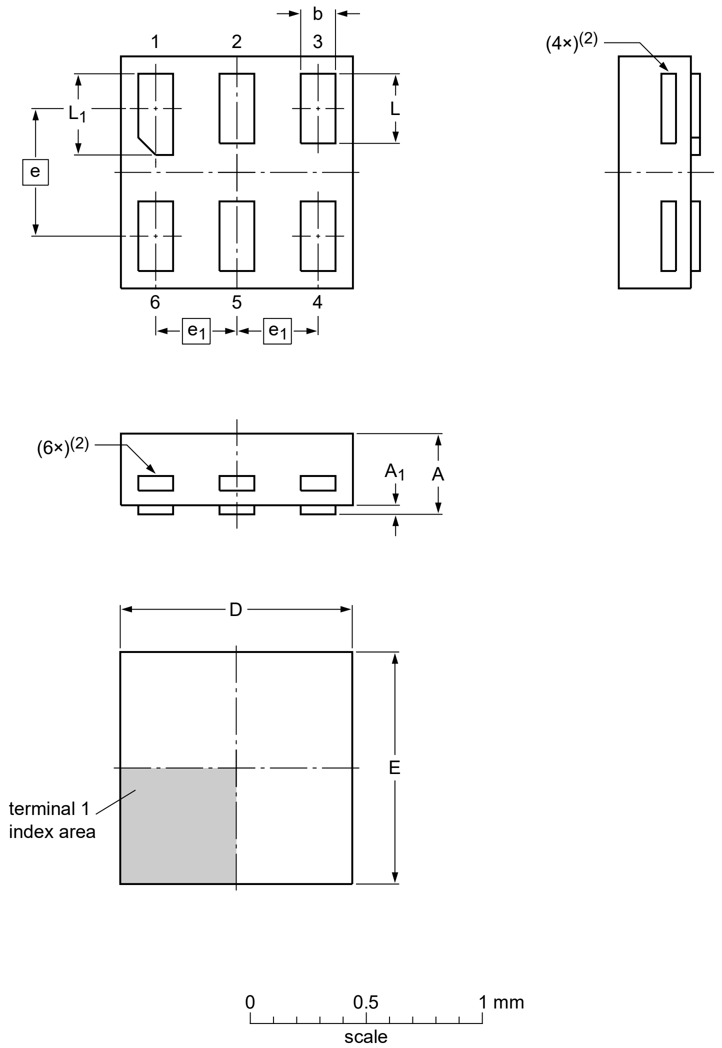
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						~~10-04-02~~ 10-04-07

Fig. 24. Package outline SOT1115 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm** **SOT1202**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
mm	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

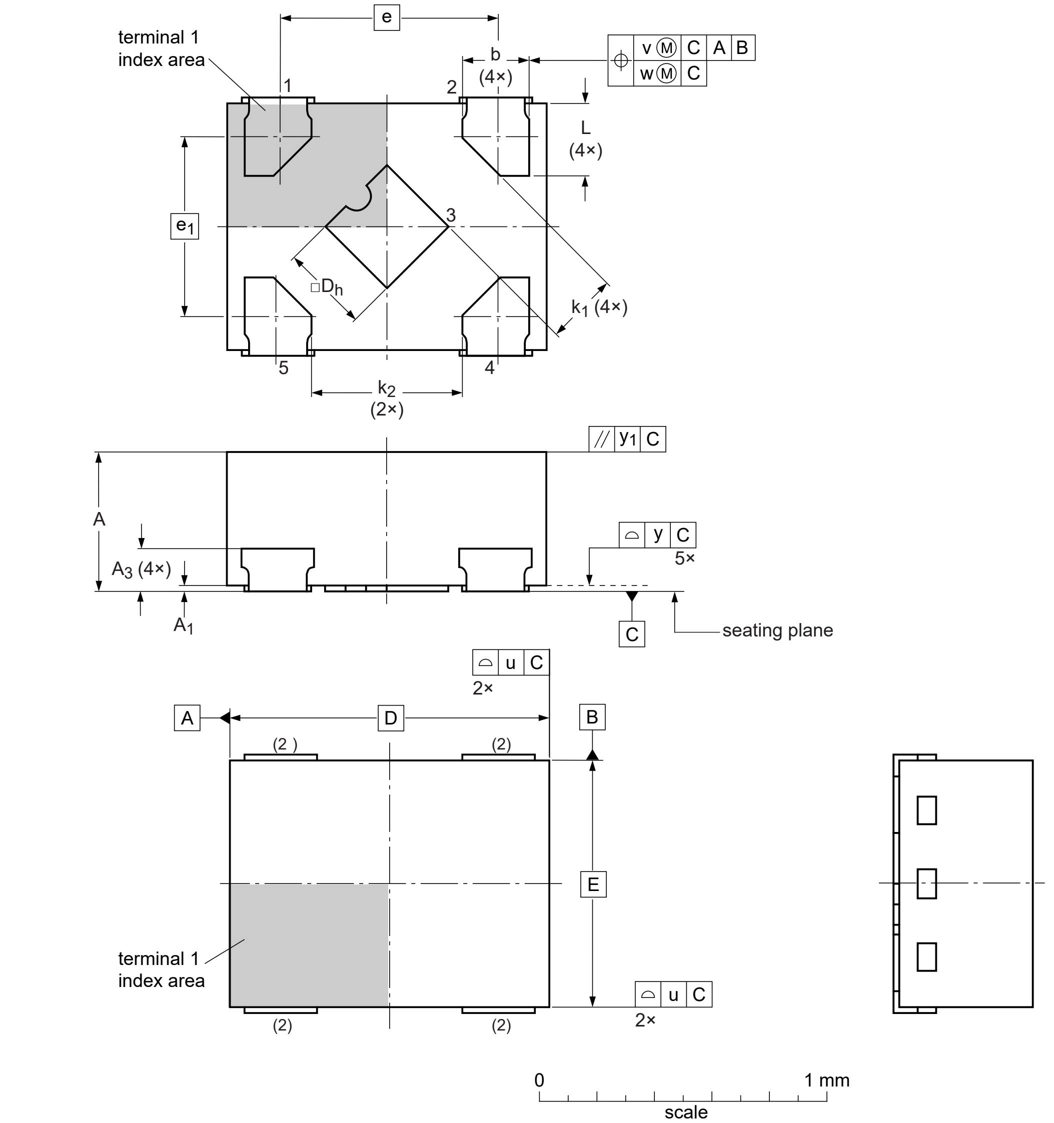
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Fig. 25. Package outline SOT1202 (XSON6)

XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm **SOT8065-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	A_3	b	$D^{(1)}$	D_h	$E^{(1)}$	e	e_1	k_1	k_2	L	u	v	w	y	y_1
mm	max	0.50	0.040	0.135 (typ)	0.28		0.35						0.30					
	nom	0.47	0.020		0.23	1.10	0.30	0.85	0.75	0.6			0.25	0.05	0.1	0.05	0.05	0.05
	min	0.44	0.005		0.20		0.27				0.2	0.45	0.22					

Note:
1. Plastic or metal protrusions per side are not included.
2. Side wettable flanks (SWF), protrusion max. 0.02 mm.

sot8065-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8065-1		MO-340				~~24-07-09~~ 24-08-27

Fig. 26. Package outline SOT8065-1 (XSON5)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G66 v.14.1	20240903	Product data sheet	-	74LVC1G66 v.14
Modifications:	• Fig. 26: Added JEDEC reference MO-340 to SOT8065-1 package outline drawing.			
74LVC1G66 v.14	20240715	Product data sheet	-	74LVC1G66 v.13
Modifications:	• Type number 74LVC1G66GZ (SOT8065-1/XSON5) added.			
74LVC1G66 v.13	20230824	Product data sheet	-	74LVC1G66 v.12
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC1G66 v.12	20220112	Product data sheet	-	74LVC1G66 v.11
Modifications:	• Fig. 21: Package outline drawing SOT353-1 (TSSOP5) has changed.			
74LVC1G66 v.11	20210608	Product data sheet	-	74LVC1G66 v.10
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74LVC1G66GF (SOT891 / XSON6) removed. • Section 1 updated. • Section 8: Derating values for P_{tot} total power dissipation updated.			
74LVC1G66 v.10	20161207	Product data sheet	-	74LVC1G66 v.9
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC1G66 v.9	20150115	Product data sheet	-	74LVC1G66 v.8
Modifications:	• SOT886 (XSON6) package outline drawing modified.			
74LVC1G66 v.8	20111202	Product data sheet	-	74LVC1G66 v.7
Modifications:	• Legal pages updated.			
74LVC1G66 v.7	20100730	Product data sheet	-	74LVC1G66 v.6
74LVC1G66 v.6	20070827	Product data sheet	-	74LVC1G66 v.5
74LVC1G66 v.5	20070807	Product data sheet	-	74LVC1G66 v.4
74LVC1G66 v.4	20040413	Product specification	-	74LVC1G66 v.3
74LVC1G66 v.3	20021115	Product specification	-	74LVC1G66 v.2

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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