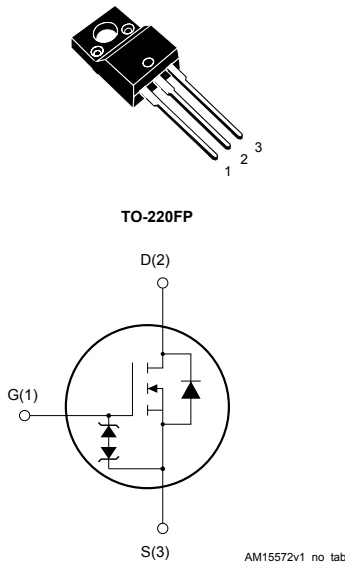


## N-channel 800 V, 1.0 $\Omega$ typ., 5 A MDmesh K6 Power MOSFET in a TO-220FP package



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STF80N1K1K6	800 V	1.1 $\Omega$	5 A

- Worldwide best  $R_{DS(on)}$  x area
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Flyback converter
- Adapters for tablets, notebook and AIO
- LED lighting

### Description

This very high voltage N-channel Power MOSFET is designed using the ultimate MDmesh K6 technology based on 20 years STMicroelectronics experience on super junction technology. The result is the best-in-class on-resistance per area and gate charge for applications requiring superior power density and high efficiency.

#### Product status link

[STF80N1K1K6](#)

#### Product summary

<b>Order code</b>	STF80N1K1K6
<b>Marking</b>	80N1K1K6
<b>Package</b>	TO-220FP
<b>Packing</b>	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3	
$I_{DM}^{(2)}$	Drain current (pulsed)	8	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	21	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	5	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	100	A/ $\mu\text{s}$
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	120	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ , $T_C = 25\text{ }^\circ\text{C}$ )	2.5	kV
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Limited by package.
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 2.5\text{ A}$ ,  $V_{DS}(\text{peak}) = 400\text{ V}$ .
4.  $V_{DS} \leq 640\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	6	$^\circ\text{C/W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C/W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max.)	1.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	60	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			50	
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 1$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3.0	3.5	4.0	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1.7\text{ A}$		1.0	1.1	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 400\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	300	-	$\mu\text{F}$
$C_{oss}$	Output capacitance		-	4.5	-	$\mu\text{F}$
$C_{o(er)}^{(1)}$	Equivalent capacitance energy related	$V_{DS} = 0\text{ to }640\text{ V}$ , $V_{GS} = 0\text{ V}$	-	7	-	$\mu\text{F}$
$C_{o(tr)}^{(2)}$	Equivalent capacitance time related		-	37	-	$\mu\text{F}$
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	4.2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}$ , $I_D = 2.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 18. Test circuit for gate charge behavior)	-	5.7	-	nC
$Q_{gs}$	Gate-source charge		-	1.7	-	nC
$Q_{gd}$	Gate-drain charge		-	1.8	-	nC

1.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

2.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

**Table 6. Switching times**

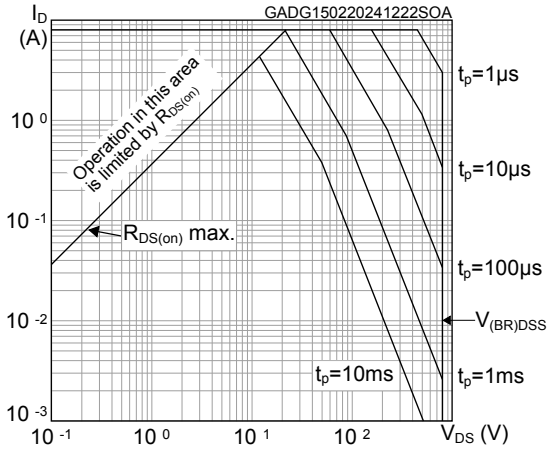
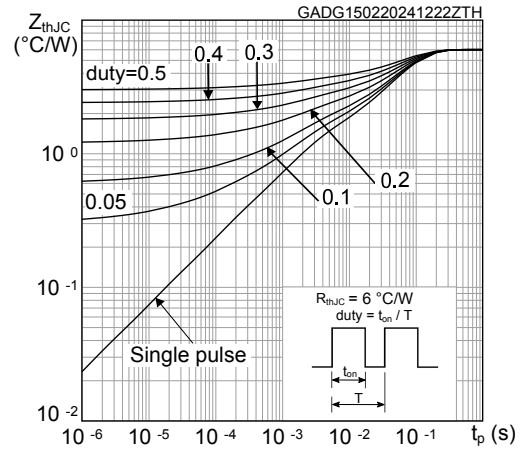
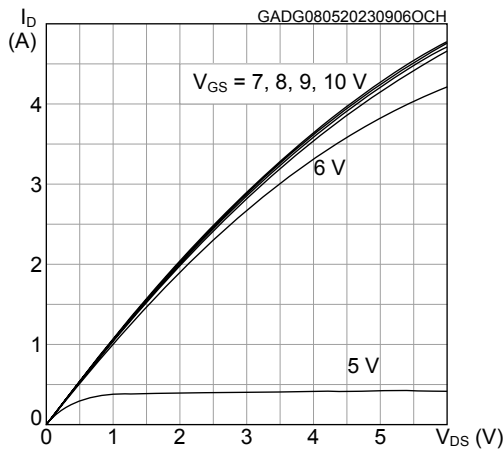
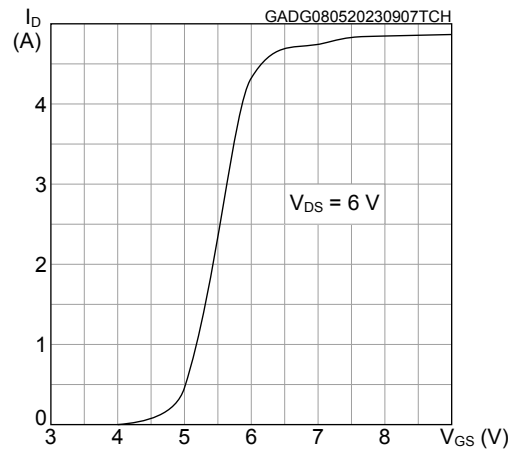
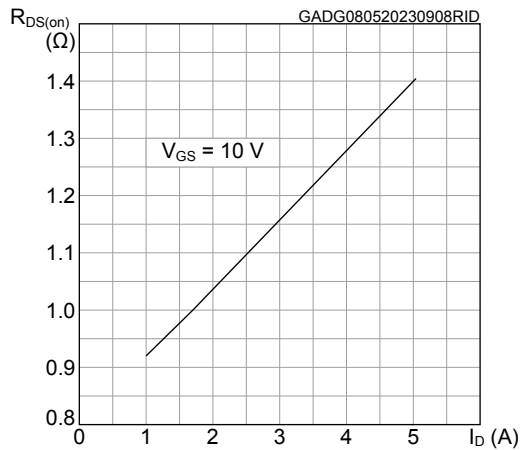
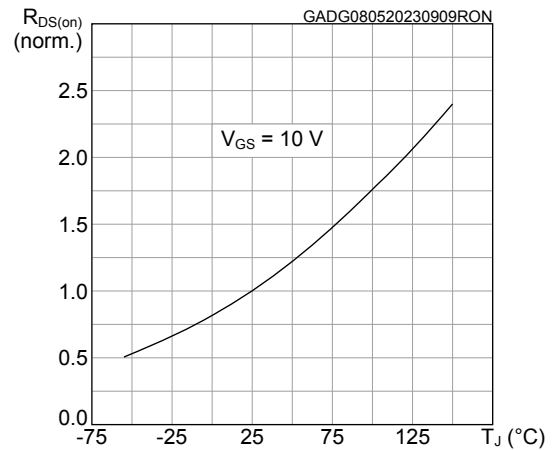
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 2.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	7.4	-	ns
$t_r$	Rise time		-	4.3	-	ns
$t_{d(off)}$	Turn-off delay time	see (Figure 16. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	22	-	ns
$t_f$	Fall time		-	14	-	ns

**Table 7. Source-drain diode**

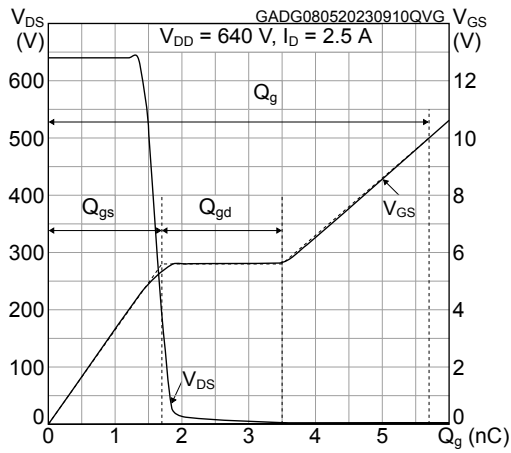
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		5	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		8	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 5\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	217		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	1.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	11.8		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	333		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	2.3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	10.2		A

1. Limited by package.
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

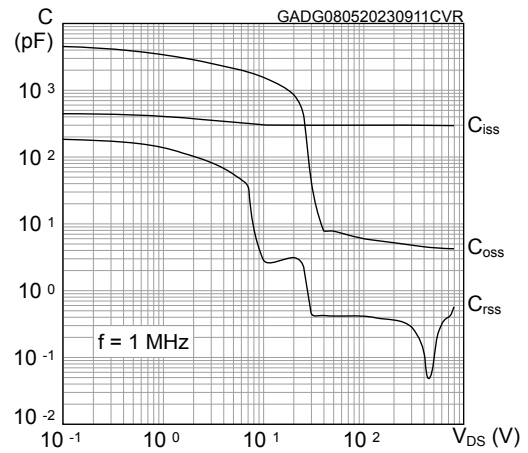
## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

**Figure 2. Maximum transient thermal impedance**

**Figure 3. Typical output characteristics**

**Figure 4. Typical transfer characteristics**

**Figure 5. Typical drain-source on-resistance**

**Figure 6. Normalized on-resistance vs temperature**


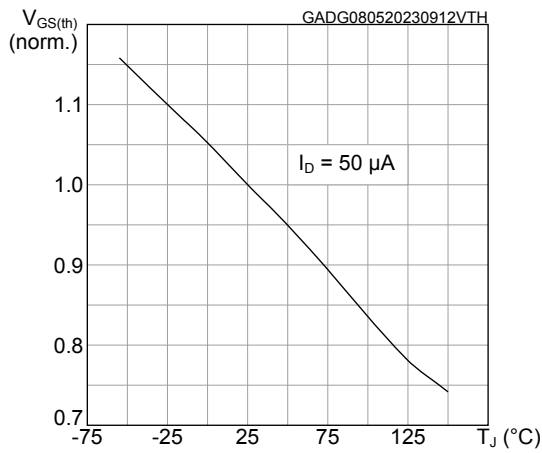
**Figure 7. Typical gate charge characteristics**



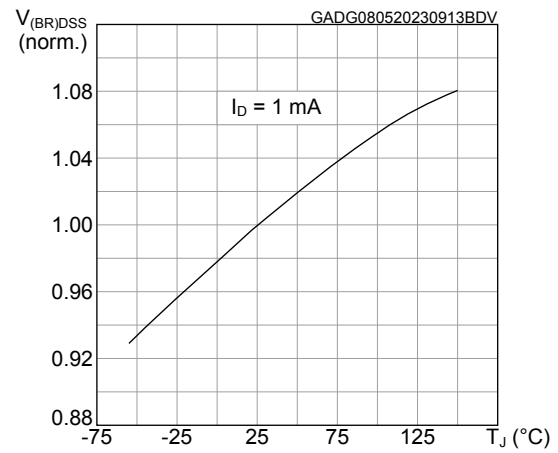
**Figure 8. Typical capacitance characteristics**



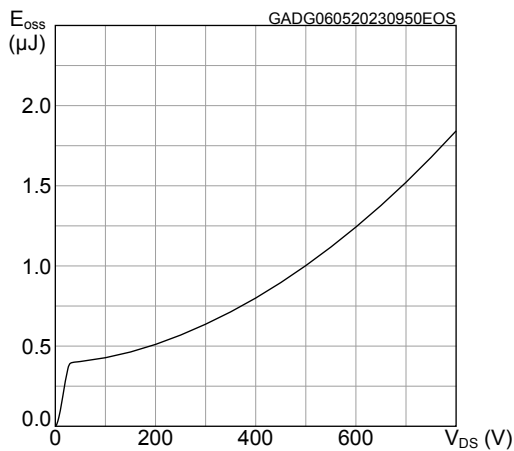
**Figure 9. Normalized gate threshold vs temperature**



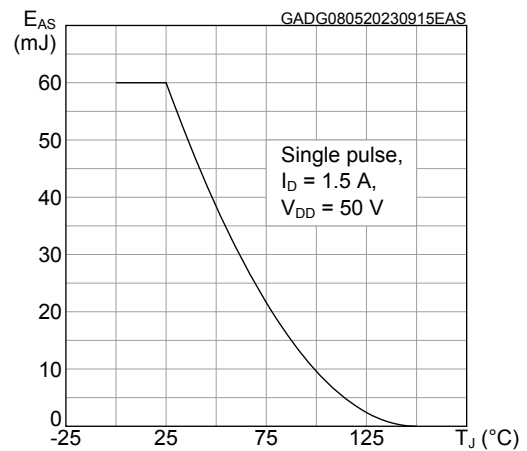
**Figure 10. Normalized breakdown voltage vs temperature**



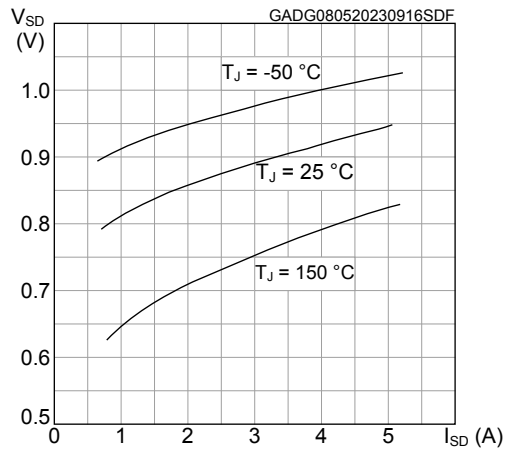
**Figure 11. Typical output capacitance stored energy**



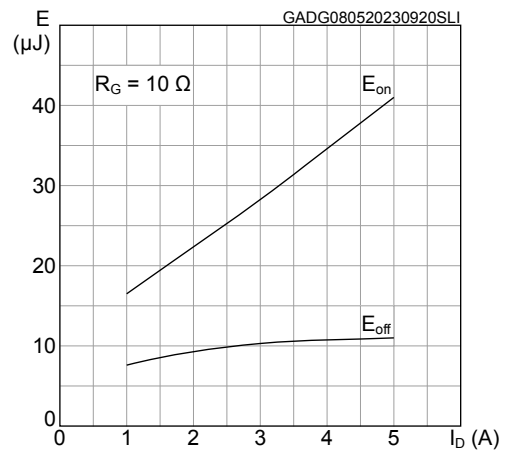
**Figure 12. Maximum avalanche energy vs temperature**



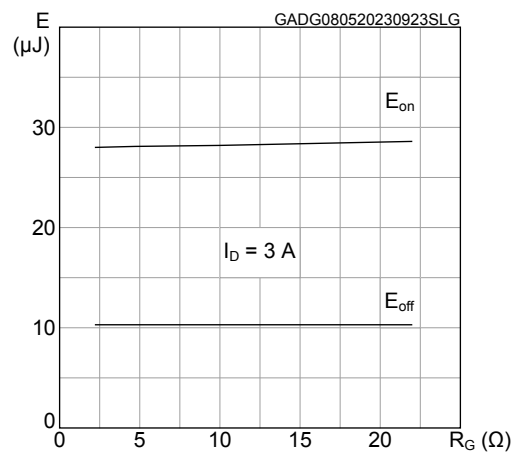
**Figure 13. Typical reverse diode forward characteristics**



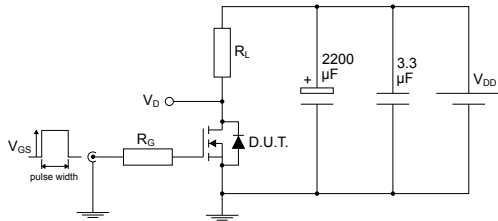
**Figure 14. Typical inductive load switching energy vs  $I_D$**



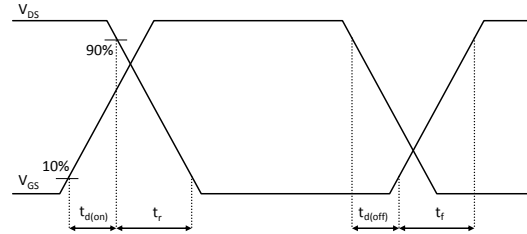
**Figure 15. Typical inductive load switching energy vs  $R_G$**



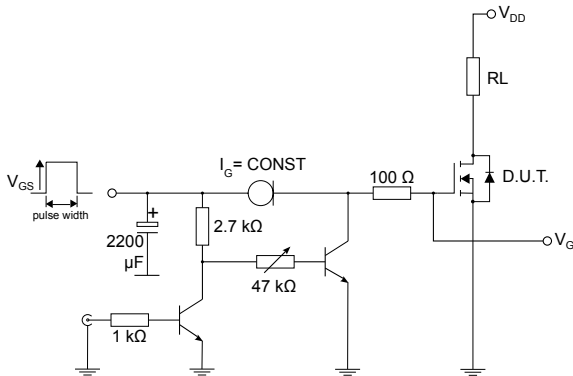
### 3 Test circuits

**Figure 16. Test circuit for resistive load switching times**


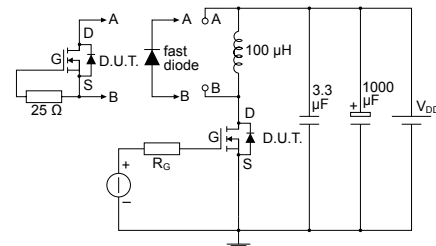
AM01468v1

**Figure 17. Switching time waveform**


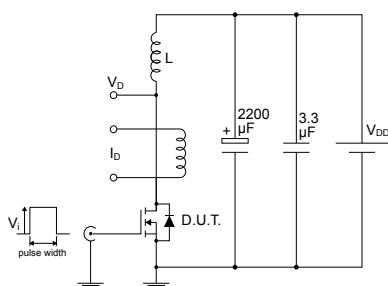
GADG280620211209SA

**Figure 18. Test circuit for gate charge behavior**


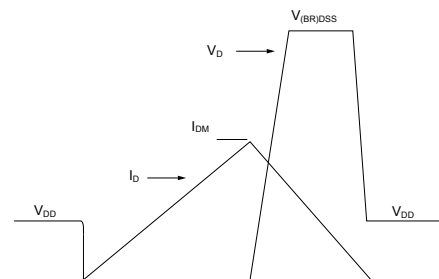
AM01469v10

**Figure 19. Test circuit for inductive load switching and diode recovery times**


AM01470v1

**Figure 20. Unclamped inductive load test circuit**


AM01471v1

**Figure 21. Unclamped inductive waveform**


AM01472v1

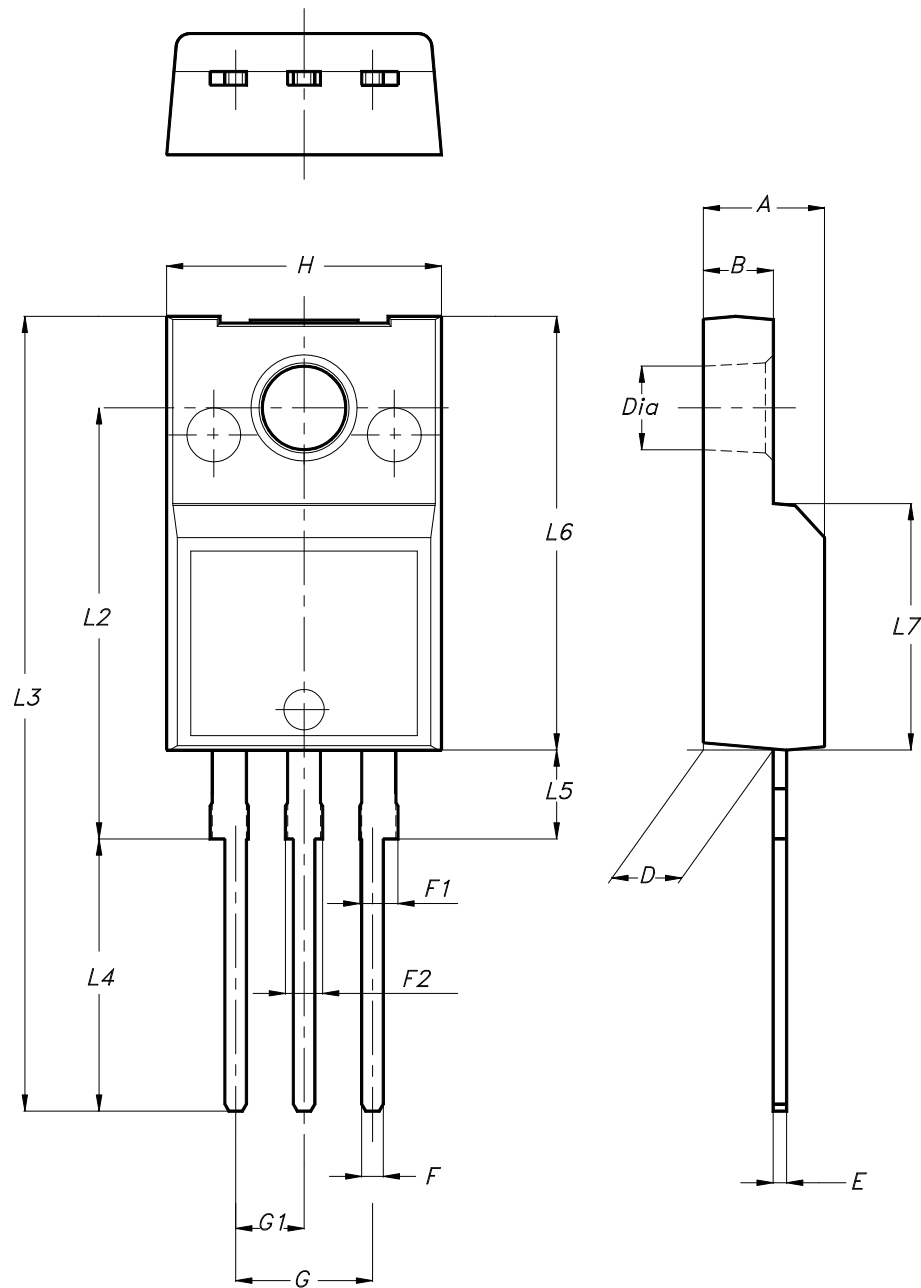


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220FP type B package information

Figure 22. TO-220FP type B package outline



7012510\_B\_rev.14

**Table 8. TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

## Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Feb-2024	1	First release.

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	<b>Electrical characteristics (curves)</b> .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package information</b> .....	<b>9</b>
<b>4.1</b>	<b>TO-220FP type B package information</b> .....	<b>9</b>
	<b>Revision history</b> .....	<b>11</b>

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2024 STMicroelectronics – All rights reserved