# CrossLink-NX-33 and CrossLinkU-NX

# Data Sheet

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---------|------------|
| AON | Always On |
| CDR | Clock and Data Recovery |
| CRC | Cycle Redundancy Code |
| DCC | Dynamic Clock Control |
| DCS | Dynamic Clock Select |
| DDR | Double Data Rate |
| DLL | Delay Locked Loop |
| DSP | Digital Signal Processing |
| EBR | Embedded Block RAM |
| ECC | Error Correction Coding |
| ECLK | Edge Clock |
| FFT | Fast Fourier Transform |
| FIFO | First In First Out |
| FIR | Finite Impulse Response |
| GPIO | General Purpose Input/Output |
| LC | Logic Cell |
| LRAM | Large RAM |
| LVCMOS | Low-Voltage Complementary Metal Oxide Semiconductor |
| LVDS | Low-Voltage Differential Signaling |
| LVPECL | Low Voltage Positive Emitter Coupled Logic |
| LVTTL | Low Voltage Transistor-Transistor Logic |
| LUT | Look Up Table |
| MPS | Maximum Packet Size |
| PCI | Peripheral Component Interconnect |
| PCLK | Primary Clock |
| PDPR | Pseudo Dual Port RAM |
| PFU | Programmable Functional Unit |
| PIC | Programmable I/O Cells |
| PIPE | PHY Interface for PCI Express |
| PLL | Phase Locked Loop |
| POR | Power On Reset |
| SER | Soft Error Rate |
| SEU | Single Event Upset |
| SLVS | Scalable Low-Voltage Signaling |
| SPI | Serial Peripheral Interface |
| SPR | Single Port RAM |
| SRAM | Static Random-Access Memory |
| TAP | Test Access Port |
| TDM | Time Division Multiplexing |
| USB | Universal Serial Bus |

# 1.   General Description

The CrossLink™-NX-33 and CrossLinkU™-NX devices (hereafter referred to as LIFCL-33 and LIFCL-33U respectively) can be used in a wide range of applications and are optimized for bridging and processing needs in Embedded Vision applications – supporting a variety of high bandwidth sensor and display interfaces, video processing and machine learning inferencing. It is built on the Lattice Nexus FPGA platform, using low-power 28 nm FD-SOI technology. It combines the extreme flexibility of an FPGA with the low power and high reliability (due to extremely low SER) of FD-SOI technology and offers small footprint package options.

LIFCL-33/33U devices support a variety of interfaces including MIPI D-PHY (CSI-2, DSI), LVDS, SLVS, subLVDS, and more. USB 2.0 and USB 3.2 Gen 1 are only supported in LIFCL-33U.

The processing features of the LIFCL-33U include up to 33k Logic Cells, sixty-four 18 × 18 multipliers, and 3.6 Mb of embedded memory (consisting of EBR and LRAM blocks), and distributed memory.

LIFCL-33/33U devices support fast configuration of its reconfigurable SRAM-based logic fabric. Security features to secure user designs include bitstream encryption and password protection. In addition to the high reliability inherent to FD-SOI technology (due to its extremely low SER), active reliability feature such as built-in frame-based SED/SEC (for SRAM-based logic fabric) is also supported.

Lattice Radiant™ design software allows large complex user designs to be efficiently implemented in LIFCL-33U device. Synthesis library support for the device is available for popular logic synthesis tools. Radiant tools use the synthesis tool output along with constraints from its floor planning tools to place and route the user design. The tools extract timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules. By using these configurable soft IP cores as standardized blocks, users are free to concentrate on the unique aspects of the design, increasing productivity.

## 1.1.   Features

Table 1.1 shows the key features of LIFCL-33/33U devices. Always On (AON), USB 2.0 and USB 3.2 Gen 1 are only supported in LIFCL-33U.

**Table 1.1. LIFCL-33/33U Key Features**

| Programmable Architecture | MIPI D-PHY |
|---|---|
| • 33k logic cells<br>• 64 multipliers (18 × 18 in sysDSP™ blocks)<br>• 3.6 Mb of embedded memory (EBR, LRAM)<br>• 60 programmable sysI/O<br>  (High Performance and Wide Range I/O) | • Soft D-PHY interfaces supported by High Performance (HP) sysI/O<br>• Transmit or receive<br>• Supports CSI-2, DSI<br>• Up to 1.2 Gbps per lane |
| **Programmable sysI/O Supports Wide Variety of Interfaces** | **Cryptographic Engine** |
| • High Performance (HP) on bottom I/O<br>  dual rank<br>   • Supports up to 1.8 V V$_{CCIO}$<br>   • Mixed voltage support (1.0 V, 1.2 V, 1.5 V, 1.8 V)<br>   • High-speed differential up to 1.2 Gbps<br>   • Supports soft D-PHY (Tx/Rx), LVDS 7:1 (Tx/Rx), SLVS (Tx/Rx), subLVDS (Rx)<br>• Wide Range (WR) on Top<br>  I/O Banks<br>   • Supports up to 3.3 V V$_{CCIO}$<br>   • Mixed voltage support (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V)<br>   • Programmable slew rate (slow, med, fast)<br>   • Controlled impedance mode<br>   • Emulated LVDS support<br>   • Hot Socketing Support | • Bitstream encryption – using AES-256<br>• Bitstream authentication – using ECDSA<br>• Hashing algorithms – SHA, HMAC<br>• True Random Number Generator<br>• AES 128/256 Encryption |

| sysDSP Enhanced DSP blocks | Single Event Upset (SEU) Mitigation Support |
|---|---|
| <ul><li>Hardened pre-adder</li><li>Dynamic Shift for AI/ML support</li><li>Four 18 × 18, eight 9 × 9, two 18 × 36, or 36 × 36 multipliers</li><li>Advanced 18 × 36, two 18 × 18, or four 8 × 8 MAC</li></ul> | <ul><li>Extremely low Soft Error Rate (SER) due to FD-SOI technology</li><li>Soft Error Detect – Embedded hard macro</li><li>Soft Error Correction – Without stopping user operation</li><li>Soft Error Injection – Emulate SEU event to debug system error handling</li></ul> |
| **sysCLOCK™ Analog PLL** | **Power Modes – Low Power versus High-Performance** |
| <ul><li>Six outputs per PLL</li><li>Fractional N</li><li>Programmable and dynamic phase control</li></ul> | <ul><li>User-selectable</li><li>Low-Power mode for power and/or thermal challenges</li><li>High-Performance mode for faster processing</li></ul> |
| **Flexible Memory Resources** | **Configuration – Fast, Secure** |
| <ul><li>Up to 1.1 Mb sysMEM™ Embedded Block RAM (EBR)</li><li>Programmable width</li><li>Single or dual clock FIFO</li><li>220k bits distributed RAM</li><li>Large RAM Blocks<ul><li>0.5 Mbits per block</li><li>Up to five blocks (2.5 Mb total) per device</li></ul></li></ul> | <ul><li>SPI – x1, x2, x4 up to 150 MHz<ul><li>Master and Slave SPI support</li></ul></li><li>JTAG</li><li>I$^2$C and I3C</li><li>Bitstream Security<ul><li>Encryption</li><li>Authentication</li></ul></li></ul> |
| **Internal Bus Interface Support** | **USB 2.0/USB 3.2 Gen 1 PHY and USB 3.2 Gen 1 Controller (LIFCL-33U)** |
| <ul><li>APB control bus</li><li>AHB-Lite for data bus</li><li>AXI protocol</li></ul> | <ul><li>USB 3.2 Gen 1 at 5 Gbps x1 (-9 speed grade only)</li><li>USB 3.2 Gen 1 PHY and Controller (-9 speed grade only)</li><li>USB 2.0 PHY and Controller (All speed grades)</li></ul> |
| **System Level Support** | **Always On (AON) Support for Low Power Applications** |
| <ul><li>IEEE 1149.1 and IEEE 1532 compliant</li><li>Reveal Logic Analyzer</li><li>On-chip oscillator for initialization and general use</li><li>1.0 V core power supply</li></ul> | <ul><li>AON timer and power management</li><li>Supports lowest FPGA power for AON applications</li><li>Typical standby power <70 uA</li></ul> |
| **Small Footprint Package Options** | |
| <ul><li>3.1 × 7.3 mm package options</li></ul> | |

**Table 1.2. LIFCL-33/33U Commercial/Industrial Family Selection Guide**

| Device | LIFCL-33 | LIFCL-33U |
|---|---|---|
| Logic Cells[1] | 33k | 33k |
| Embedded Memory (EBR) Blocks (18 kb) | 64 | 64 |
| Embedded Memory (EBR) Bits (kb) | 1,152 | 1,152 |
| Distributed RAM Bits (kb) | 220 | 220 |
| Large Memory (LRAM) Blocks | 5 | 5 |
| Large Memory (LRAM) Bits (kb) (512 kbits each) | 2560 | 2560 |
| 18 × 18 Multipliers | 64 | 64 |
| 450 MHz High Frequency Oscillator | 1 | 1 |
| 128 kHz Low Power Oscillator | 1 | 1 |
| GPLL[2] | 1 | 1 |
| Always On (AON) Block | — | 1 |
| USB 2.0/USB 3.2 Gen 1 Interface[3] | — | 1/1 |
| **Packages (Size, Ball Pitch)** | **Total I/O (Wide Range, High Performance)** | |
| 84 WLCSP (3.1 mm × 7.3 mm, 0.5 mm) | 60 (34, 26) | 44 (17, 27) |
| 104 FCCSP (5.5 mm x 8.5 mm, 0.65 mm) | — | 52 (20, 32) |

**Notes:**
1. Logic Cells = LUTs × 1.2 effectiveness.
2. GPLL is only supported in 104 package of LIFCL-33U.
3. USB 3.2 Gen 1 is supported by -9 speed grade only.

# 2. Architecture

## 2.1. Overview

Each LIFCL-33/33U device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR) and rows of sysDSP Digital Signal Processing blocks, as shown in Figure 2.1 and Figure 2.2. The sysMEM EBR blocks are large, dedicated 18 kb fast memory blocks and have FIFO support. Each sysMEM block can be configured to a single, pseudo dual or true dual port memory in a variety of depths and widths as RAM or ROM. Each DSP block supports a variety of multiplier and adder configurations with one 108-bit or two 54-bit accumulators supported, which are the building blocks for complex signal processing capabilities.

Each PIC block encompasses two PIO (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LIFCL-33/33U devices are arranged in seven banks allowing the implementation of a wide variety of I/O standards. The Wide Range (WR) I/O banks that are located on the top side of the device provide flexible ranges of general purpose I/O configurations up to 3.3 V VCCIOs. The banks located on the bottom side of the device are dedicated to High Performance (HP) interfaces such as LVDS, MIPI supporting up to 1.8 V VCCIOs.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. The registers in the PFU and sysI/O blocks in LIFCL-33/33U devices can be configured to be SET or RESET. After power up and configuration, it enters into user mode with these registers SET/RESET according to the user design, allowing the device to power up in a known state for predictable system function.

LIFCL-33U features like USB 3.2 Gen 1 and AON supports better system integration for host communications and low power applications.

LIFCL-33/33U devices also provide security features to help protect user designs and deliver more robust reliability by offering enhanced frame-based SED/SEC functions.

Other blocks provided include PLLs, DLLs, and configuration functions. The PLL and DLL blocks are located at the corners of each device. LIFCL-33/33U devices also include Lattice Memory Mapped Interface (LMMI) which is a Lattice standard to support simple read and write operations to control internal IP.

Every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LIFCL-33/33U devices use 1.0 V as their core voltage.
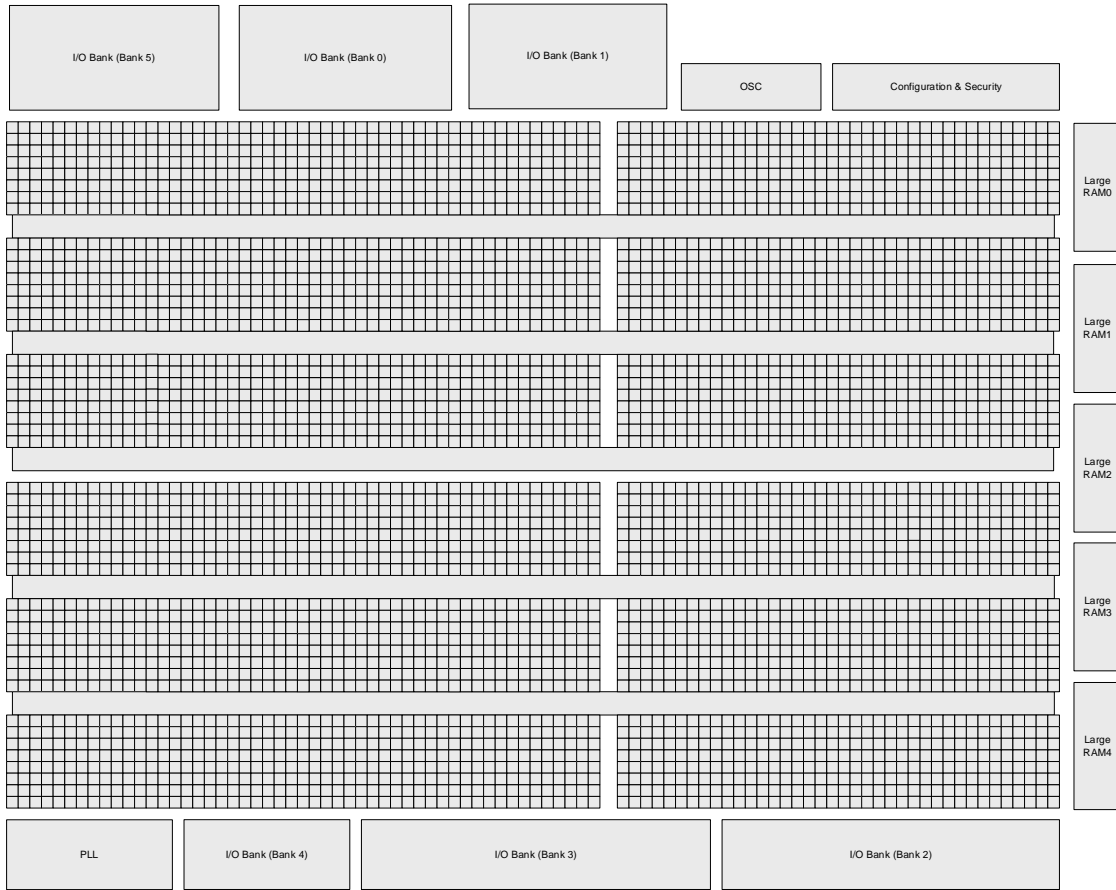
**Figure 2.1. LIFCL-33 Simplified Block Diagram**
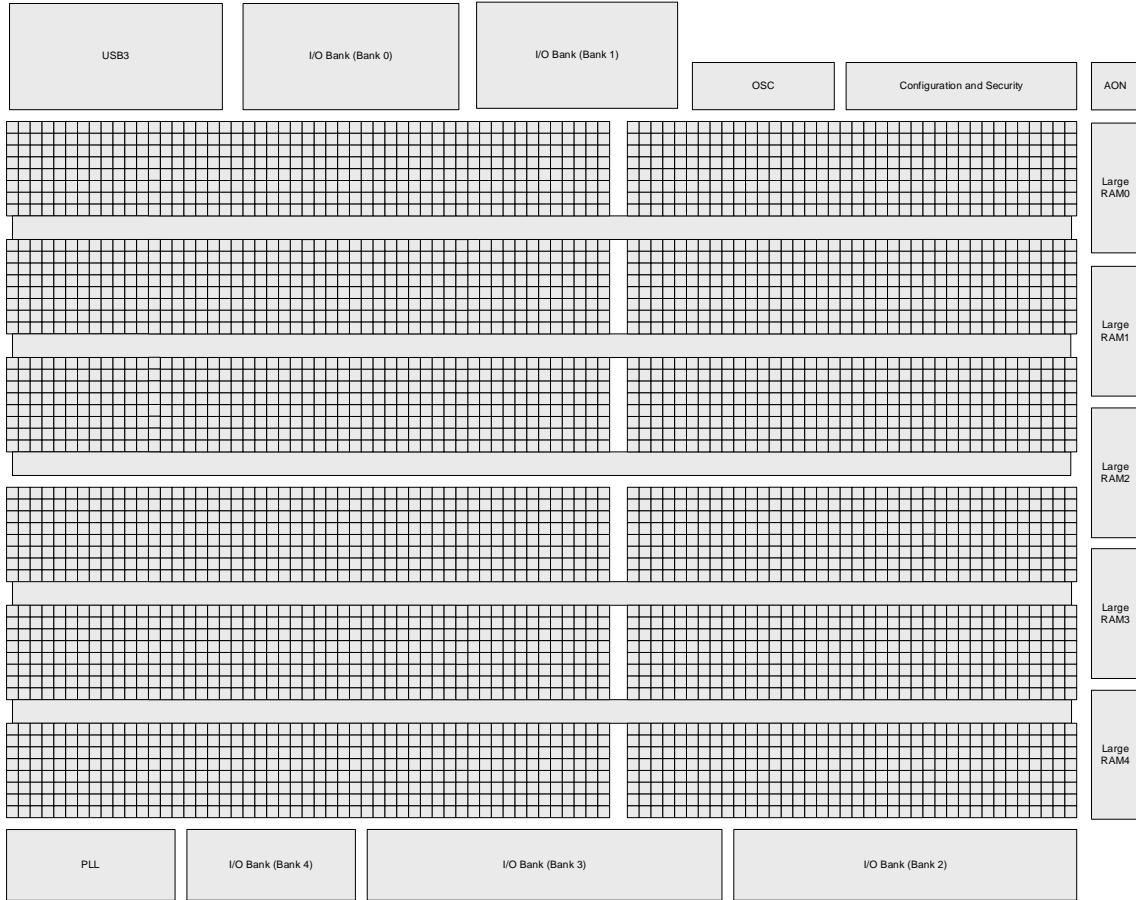
**Figure 2.2. LIFCL-33U Simplified Block Diagram**

## 2.2. PFU Blocks

The core of the LIFCL-33/33U devices consist of PFU blocks. Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2.3. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing.

The PFU block can be used to perform Logical, Arithmetic, RAM or ROM functions. Table 2.1 shows the functions each slice can perform in either Distributed SRAM or non-distributed SRAM modes.
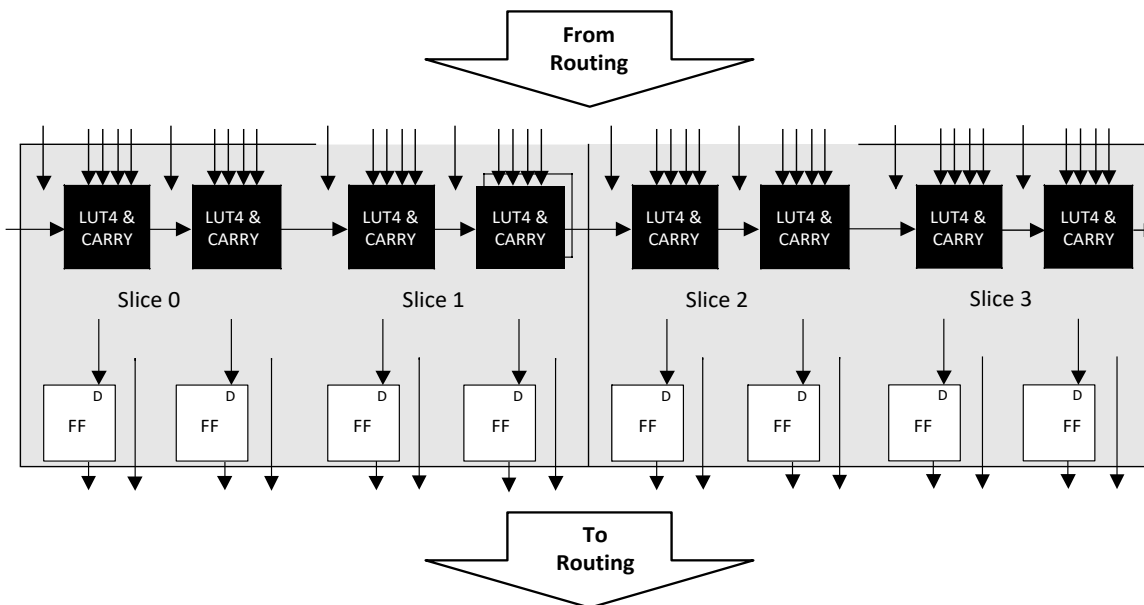
**Figure 2.3. PFU Diagram**

### 2.2.1. Slice

Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 and Slice 1 are configured as distributed memory and Slice 2 is not available as it is used to support Slice 0 and Slice 1, while Slice 3 is available as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each Slice contains logic that allows the LUTs to be combined to perform a LUT5 function. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions.

**Table 2.1. Resources and Modes Available per Slice**

| Slice | PFU (Used as Distributed SRAM) | | PFU (Not used as Distributed SRAM) | |
|---|---|---|---|---|
| | Resources | Modes | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | RAM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | RAM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | RAM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 3 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |

Figure 2.4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative edge clocking.

Each slice has 17 input signals: 16 signals from routing and one from the carry-chain (from the adjacent slice or PFU). Three of them are used for FF control and shared between two slices (0/1 or 2/3). There are five outputs: four to routing and one to carry-chain (to the adjacent PFU). Table 2.2 and Figure 2.4 list the signals associated with all the slices. Figure 2.5 shows the slice signals that support a LUT5 or two LUT5 functions. F0 can be configured to have a LUT4 or LUT5 output while F1 is for a LUT4 output.

FCO
(To different SLICE/PFU)

A1

B1

C1

D1

LUT4

LUT5
and
Carry

F1

F0

DI1

M1

FF

Q1

A0

B0

C0

D0

LUT4

DI0

M0/SEL

FF

Q0

Common to
SLICE 0/1 OR 2/3

CE

CLKIN

LSR

FF
CTRL

(From different SLICE/PFU)
FCI
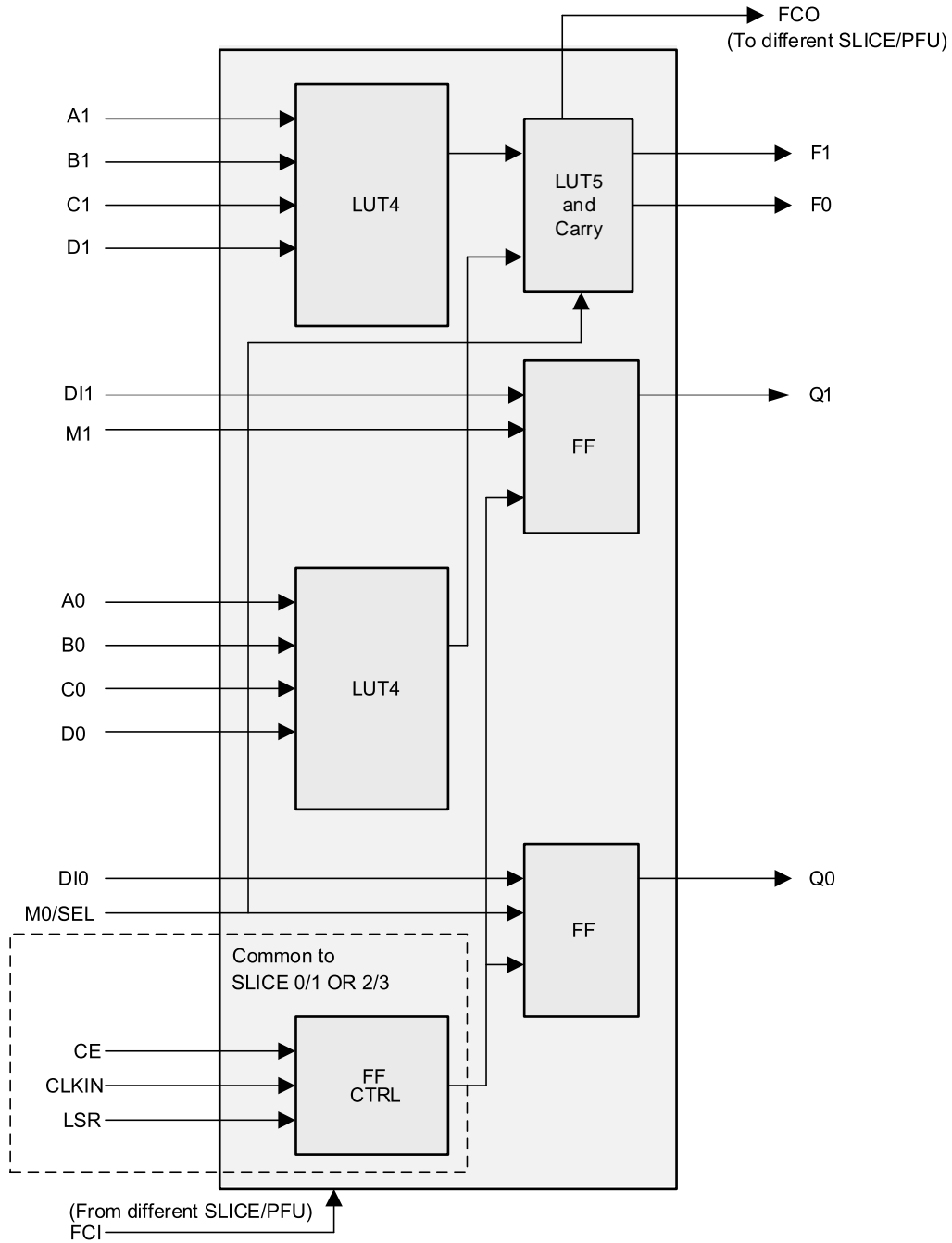
*Note: In RAM mode, LUT4s use the following signals:
QWD0/1
QWDN0/1
QWAS00~03, QWAS10~13

**Figure 2.4. Slice Diagram**
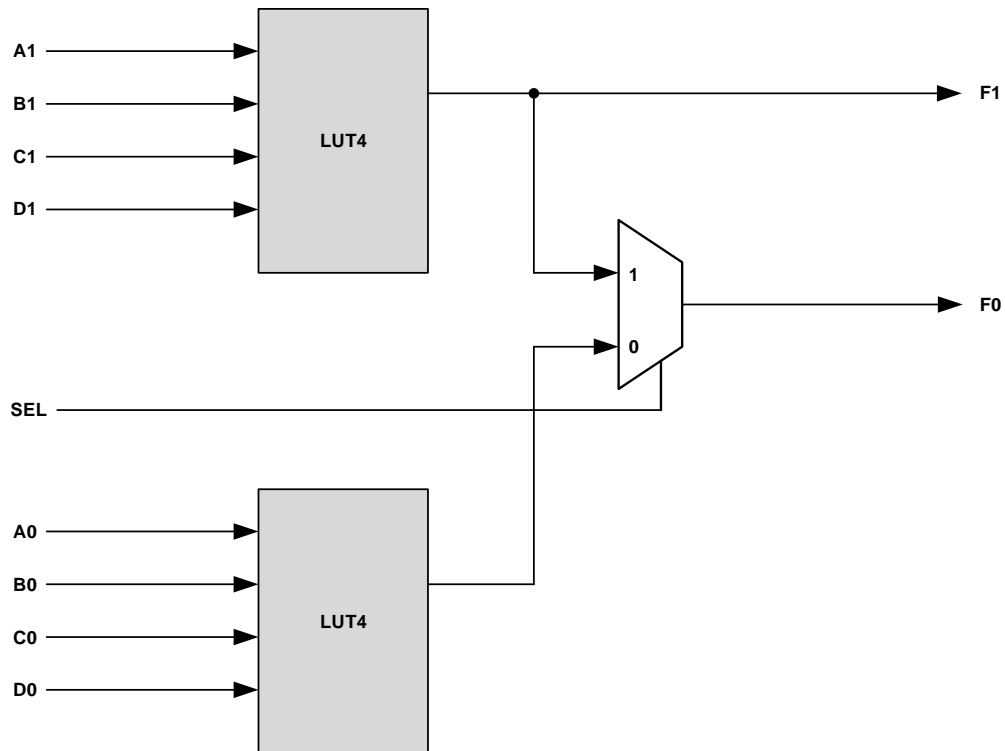
*Note: In RAM mode, LUT4s use the following signals:
QWD0/1
QWDN0/1
QWAS00~03, QWAS10~13

**Figure 2.5. Slice Configuration for LUT4 and LUT5**

**Table 2.2. Slice Signal Descriptions**

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Data signal | M0, M1 | Direct input to FF from fabric |
| Input | Control signal | SEL | LUT5 mux control input |
| Input | Data signal | DI0, DI1 | Inputs to FF from LUT4 F0/F1 outputs |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLKIN | System Clock |
| Input | Inter-PFU signal | FCI | Fast Carry-in[1] |
| Output | Data signals | F0 | LUT4/LUT5 output signal |
| Output | Data signals | F1 | LUT4 output signal |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Inter-PFU signal | FCO | Fast carry chain output[1] |

**Note**:
1. See Figure 2.4 for connection details.

## 2.2.2. Modes of Operation

Slices 0-2 have up to four potential modes of operation: Logic, Ripple, RAM and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

### Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice.

### Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear 2-bit using dynamic control
- Up/Down counter with preload (sync) 2-bit using dynamic control
- Comparator functions of A and B inputs 2-bit
    - A greater-than-or-equal-to B
    - A not-equal-to B
    - A less-than-or-equal-to B
- Up/Down counter with A greater-than-or-equal-to B comparator 2-bit using dynamic control
- Up/Down counter with A less-than-or-equal-to B comparator 2-bit using dynamic control
- Multiplier support $Ai \times Bj + 1 + Ai + 1 \times Bj$ in one logic cell with two logic cells per slice
- Serial divider 2-bit mantissa, shift 1bit/cycle
- Serial multiplier 2-bit, shift 1-bit/cycle or 2-bit/cycle

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

### RAM Mode

In this mode, a 16 × 4-bit distributed single or pseudo dual port RAM can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 × 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals. LIFCL-33/33U devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different sized memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LIFCL-33/33U devices, refer to Memory User Guide for Nexus Platform (FPGA-TN-02094).

**Table 2.3. Number of Slices Required to Implement Distributed RAM**

|  | SPR 16 × 4 | PDPR 16 × 4 |
|---|---|---|
| Number of slices | 3 | 3 |

**Note**: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

### ROM Mode

ROM mode uses the LUT logic; hence, Slice 0 through Slice 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to Memory User Guide for Nexus Platform (FPGA-TN-02094).

## 2.3.     Routing

There are many resources provided in the LIFCL-33/33U devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

LIFCL-33/33U devices have an enhanced routing architecture that produces a compact design. The Radiant software tool takes the output of the synthesis tool and places and routes the design.

## 2.4.     Clocking Structure

The LIFCL-33/33U clocking structure consists of clock synthesis blocks (PLLs), balanced clock tree networks (PCLK and ECLK), and efficient clock logic modules: Clock Dividers (PCLKDIV and ECLKDIV), Dynamic Clock Selection (DCS), Dynamic Clock Control (DCC), and DDRDLLs. Each of these functions is described as follows.

### 2.4.1.   Global PLL

The Global PLLs (GPLL) provide the ability to synthesize clock frequencies. The LIFCL-33/33U devices support two or three full-featured General Purpose GPLLs. The architecture of the GPLL is shown in Figure 2.6. A description of the GPLL functionality follows.

REFCLK is the reference frequency input to the PLL and its source can come from external CLK inputs or from internal routing. The CLKI input feeds into the input Clock Divider block.

CLKFB is the feedback signal to the GPLL which can come from a path internal to the PLL or from FPGA routing. The feedback divider is used to multiply the reference frequency and thus synthesize a higher or lower frequency clock output.

The PLL has six clock outputs CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, and CLKOS5. Each output has its own output divider, thus allowing the GPLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. Each GPLL output can be used to drive the primary clock or edge clock networks.

The setup and hold times of the device can be improved by programming a phase shift into the output clocks which advances or delays the output clock with reference to the un-shifted output clock. This phase shift can be either programmed during configuration or can be adjusted dynamically using the DIRSEL, DIR, DYNROTATE, and LOADREG ports.

The LOCK signal is asserted when the GPLL determines it has achieved lock and deasserted if a loss of lock is detected. The LOCK signal is asynchronous to the PLL clock outputs.
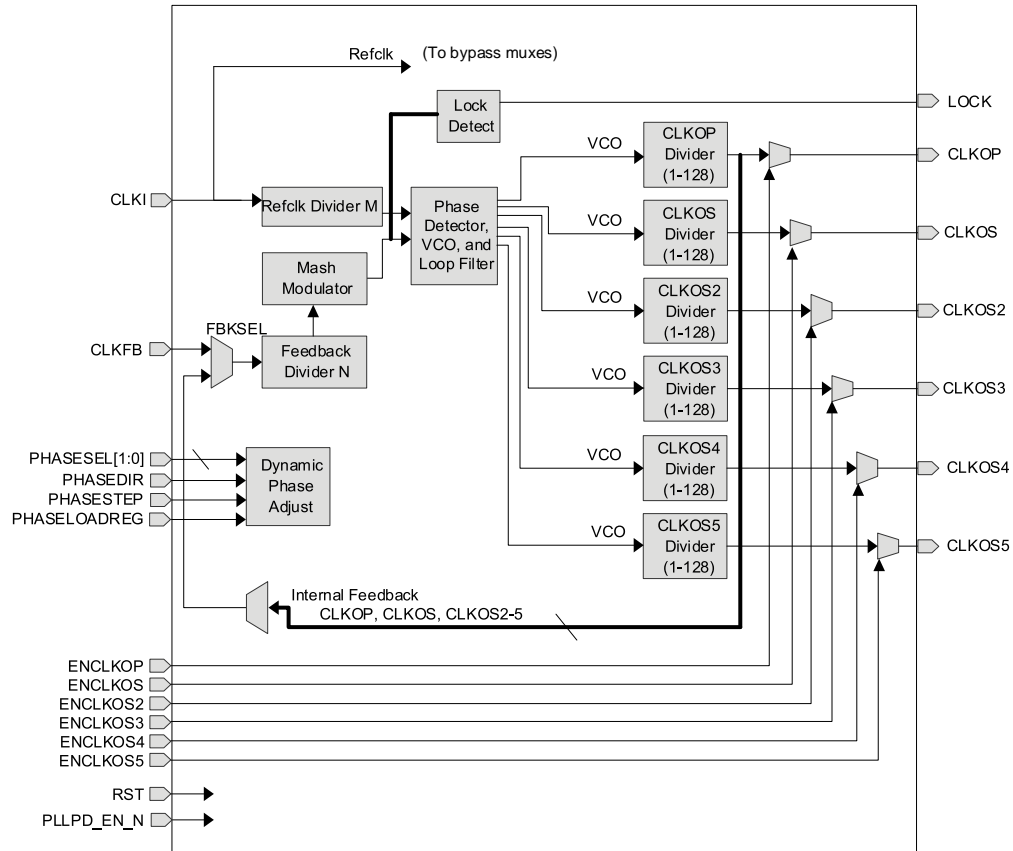
**Figure 2.6. General Purpose PLL Diagram**

For more details on the PLL, refer to the sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095).

## 2.4.2.    Clock Distribution Network

There are two main clock distribution networks for any member of the LIFCL-33/33U product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks can be driven from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, and Clock Divider outputs. There are Clock Divider blocks (ECLKDIV and PCLKDIV) to provide a slower clock from these clock sources.

LIFCL-33/33U devices support glitchless Dynamic Clock Control (DCC) for the PCLK Clock to save dynamic power. There are also Dynamic Clock Selection logic to allow glitchless selection between two clocks for the PCLK network (DCS).

An overview of the Clocking Network is shown in Figure 2.7 for the LIFCL-33/33U devices.
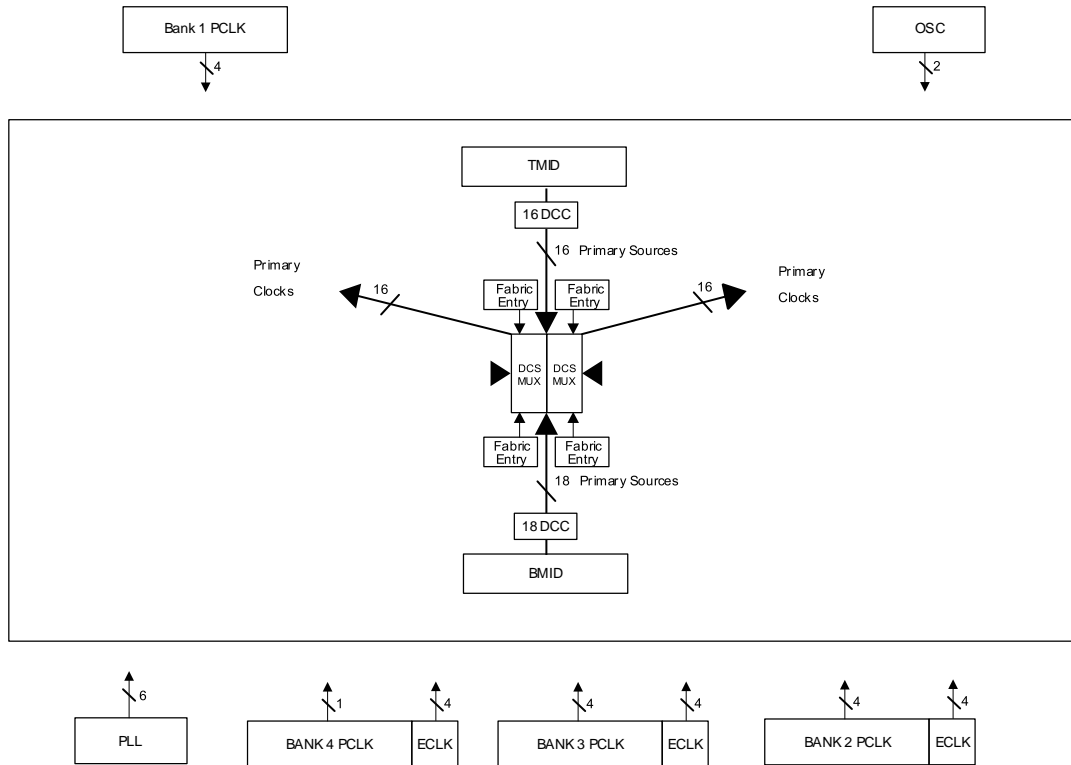
**Figure 2.7. Clocking**

### 2.4.3.    Primary Clocks

The LIFCL-33/33U devices provide low-skew, high fan-out clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network. The LIFCL-33/33U PCLK clock network is a balanced clock structure which is designed to minimize the clock skew across all destinations in the FPGA core.

The primary clock network is divided into two clock domains depending on the device density. Each of these domains has 16 clocks that can be distributed to the fabric in the domain.

The Lattice Radiant software can automatically route each clock to one of the domains up to a maximum of 16 clocks per domain. User can change how the clocks are routed by specifying a preference in the Lattice Radiant software to locate the clock to a specific domain. The LIFCL-33/33U devices provide the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

The primary clock sources are:
- Dedicated clock input pins
- PLL outputs
- PCLKDIV, ECLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- OSC clock

These sources are routed to each of four clock switches called a Mid Mux (LMID, RMID, TMID, BMID). The outputs of the Mid MUX are routed to the center of the FPGA where additional clock switches (DSC_CMUX) are used to route the primary clock sources to primary clock distribution to the LIFCL-33/33U fabric. These routing muxs are shown in Figure 2.7. There are potentially 64 unique clock domains that can be used in the largest LIFCL-33/33U device. For more information about the primary clock tree and connections, refer to sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095).

### 2.4.4. Edge Clock

LIFCL-33/33U FPGAs have several high-speed edge clocks that are intended for use with the PIO in the implementation of high-speed interfaces. There are four (4) ECLK networks per bank I/O on the Bottom side of the device. The Edge clock network is powered by a separate power domain (to reduce power noise injection from the core and reduce overall noise induced jitter) while controlled by the same logic that gates the FPGA core and PCLK domains for power management.

Each Edge Clock can be sourced from the following:

- Dedicated PIO Clock input pins (PCLK)
- DLLDEL output (PIO Clock delayed by 90°)
- PLL outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, and CLKOS5)
- Internal Nodes

Figure 2.8 illustrates the various ECLK sources. Bank 3 is shown in the example. Bank 2 and Bank 4 are similar.
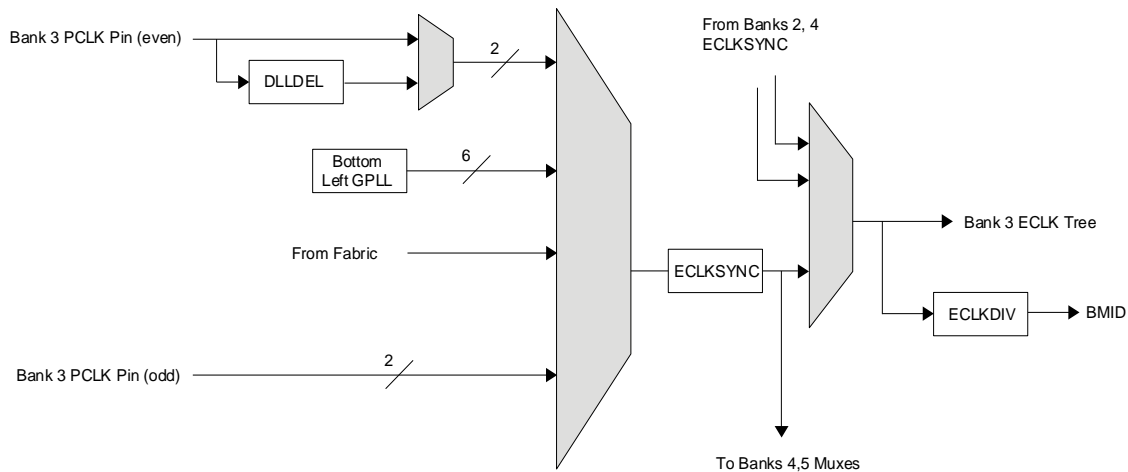


**Figure 2.8. Edge Clock Sources per Bank**

The edge clocks have low injection delay and low skew. They are typically used for Generic DDR interfaces. For detailed information on Edge Clock connections, refer to sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095).

### 2.4.5. Clock Dividers

LIFCL-33/33U devices have two distinct types of clock divider, Primary and Edge. There are from one (1) to eight (8) Primary Clock Dividers (PCLKDIV) and which are located in the DCS_CMUX block(s) at the center of the device. There are twelve (12) ECLKDIV dividers per device, locate near the bottom high-speed I/O banks.

The PCLKDIV supports ÷2, ÷4, ÷8, ÷16, ÷32, ÷64, ÷128, and ÷1 (bypass) operation. The PCLKDIV is fed from a DCSMUX within the DCS_CMUX block. The clock divider output drives one input of the DCS Dynamic Clock Select within the DSC_CMUX block. The Reset (RST) control signal is asynchronous and forces all outputs to low. The divider output starts at next cycle after the reset is synchronously released. The PCLKDIV is shown in context in Figure 2.8.

The ECLKDIV is intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷3.5, ÷4, or ÷5 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The ECLKDIV can be fed from selected PLL outputs, external primary clock pins (with or without DLLDEL Delay) or from routing. The clock divider outputs feed into the Bottom Mid-mux (BMID). The Reset (RST) control signal is asynchronous and forces all outputs to low. The divider output starts at next cycle after the reset is synchronously released.

The ECLKDIV block is shown in context in Figure 2.8. For further information on clock dividers, refer to sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095).

### 2.4.6. Clock Center Multiplexer Blocks

All clock sources are selected and combined for primary clock routing through the Dynamic Clock Selector Center Multiplexer logic (DCS_CMUX). There are one (1) or two (2) DCS_CMUX blocks per device. Each DCS_CMUX block contains 2 DCSMUX blocks, 1 PCLKDIV, 1 DCS block, and 1 or 2 CMUX blocks. See Figure 2.9 for a representative DCS_CMUX block diagram.

The heart of the DCS_CMUX is the Center Multiplexer (CMUX) block. It can accept up to 64 input clock sources (Mid-muxes (RMID, LMID, TMIC, BMID) and DCC) and to drive up to 16 primary clock trunk lines.

Up to two (2) clock inputs to the DCS_CMUX can be routed through a Dynamic Clock Select block then routed to the CMUX. One (1) input to the DCS can be optionally divided by the Primary Clock Divider (PCLKDIV). For more information about the DCS_CMUX, refer to sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095).
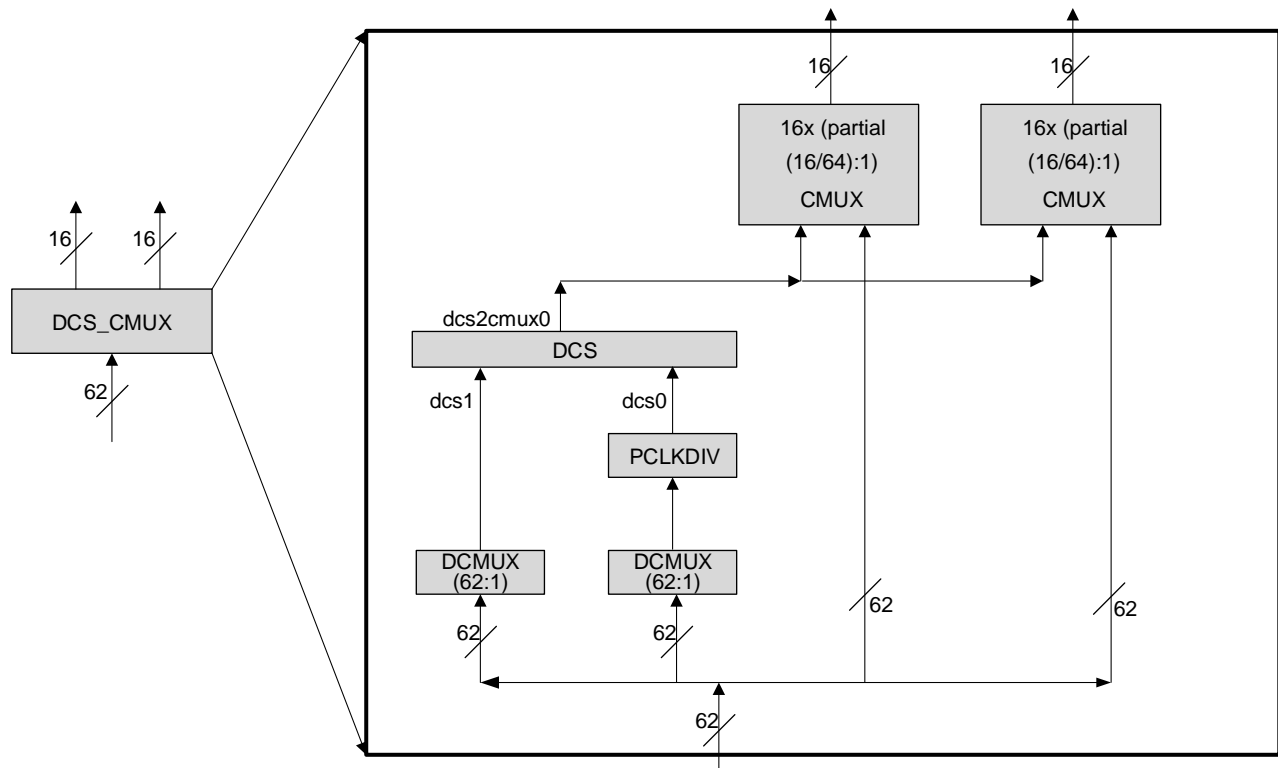


**Figure 2.9. DCS_CMUX Diagram**

### 2.4.7. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operational mode, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve a functioning glitchless DCS output clock, but running clocks are not required when used as a non-glitchless normal clock multiplexer.

There are one (1) or two (2) DCS blocks per device that feed all clock domains. The DCS blocks are located in the DCS_MUX block. The inputs to the DCS blocks come from MIDMUX outputs and user logic clocks via DCC elements. The DCS elements are located at the center of the PLC array core. The output of the DCS is connected to the inputs of Primary Clock Center MUXs (CMUX).

Figure 2.10 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095).
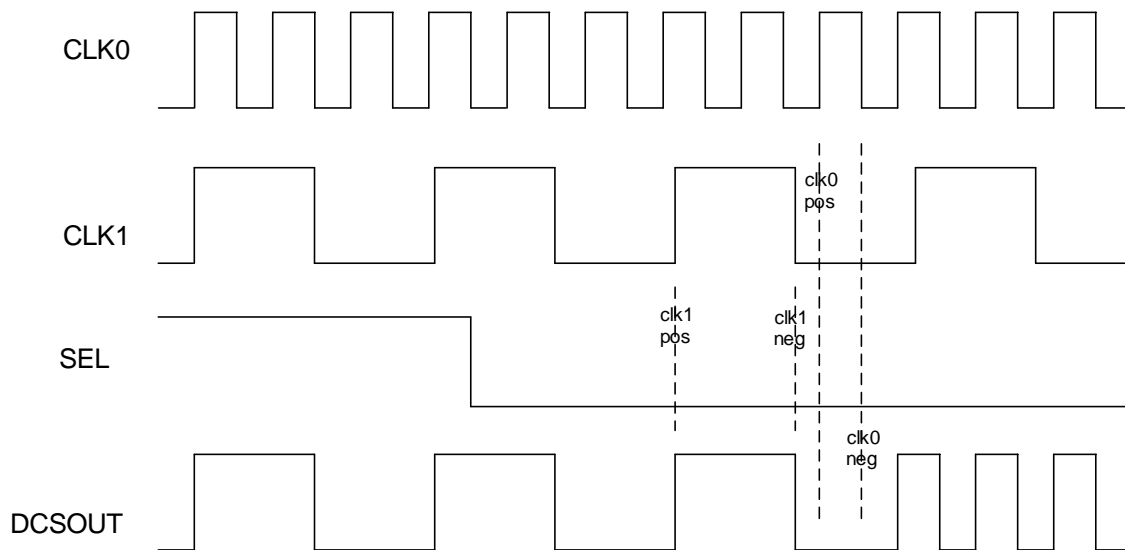
**Figure 2.10. DCS Waveforms**

### 2.4.8. Dynamic Clock Control

The Dynamic Clock Control (DCC), Domain Clock enable/disable feature allows internal logic control of the domain primary clock network. When a clock network is disabled, the clock signal is static and does not toggle. All the logic fed by that clock also does not toggle, reducing the overall power consumption of the device. The disable function is glitchless, and does not increase the clock latency to the primary clock network.

Four additional DCC elements control the clock inputs from the LIFCL-33/33U domain logic to the Center MUX elements (DSC_CMUX).

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the domain clock network. For more information about the DCC, refer to sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095).

### 2.4.9. DDRDLL

LIFCL-33/33U devices have two identical DDRDLL blocks, located in the lower left corner of the device.  Each DDRDLL (master DLL block) can generate a 9-bit phase shift value corresponding to a 90-degree phase shift of the reference clock input and provide this value to every DQS block and DLLDEL slave delay element. The reference clock can be either from a PLL, or an input pin.

- The value is also sent to another slave DLL, DLLDEL, which takes a primary clock input and generates a 90-degree shifted clock output to drive the clocking structure. This is useful in an edge-aligned Generic DDR interface, where 90-degree clocking needs to be created. Not all primary clock inputs have associated DLLDEL control. Figure 2.11 shows DDRDLL connectivity to a DLLDEL block.
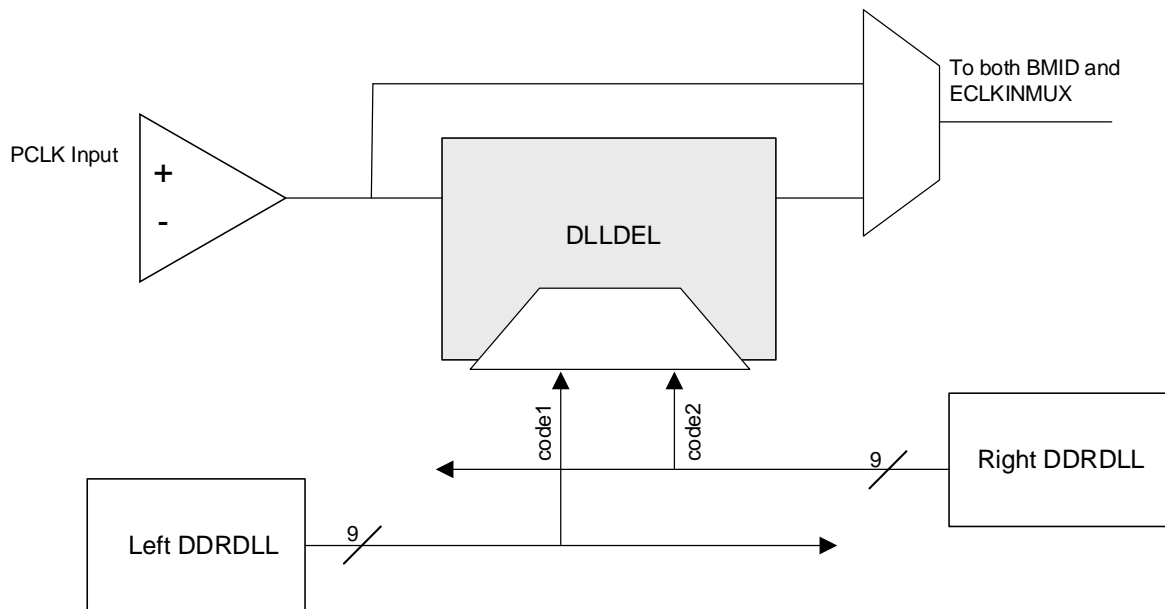
**Figure 2.11. DLLDEL Functional Diagram**

Each DDRDLL can generate a delay value based on the reference clock frequency. The DLLDELs use the value (code) to either create phase shifted inputs from the DDR memory or create a 90-degree shifted clock. Figure 2.12 shows the connections between the DDRDLL and the DLLDELs.
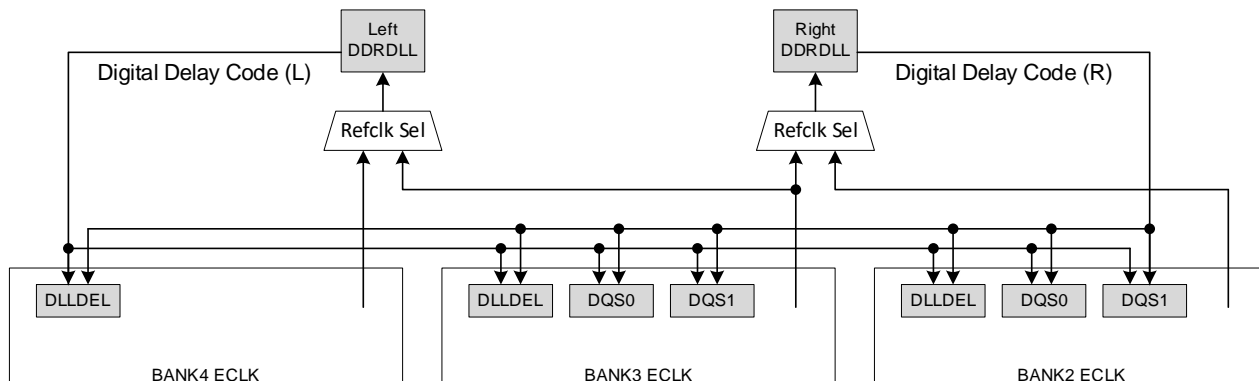


**Figure 2.12. DDRDLL Architecture**

## 2.5. sysMEM Memory

LIFCL-33/33U devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 kb RAM with memory core, dedicated input registers and output registers as well as optional pipeline registers at the outputs. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and built in FIFO.
In LIFCL-33/33U devices, unused EBR blocks is powered down to minimize power consumption.

### 2.5.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.4. FIFOs can be implemented using the built in read and write address counters and programmable full, almost full, empty and almost empty flags. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to Memory User Guide for Nexus Platform (FPGA-TN-02094).

**Table 2.4. sysMEM Block Configurations**

| Memory Mode | Configurations |
|---|---|
| Single Port | 16,384 × 1 |
| | 8,192 × 2 |
| | 4,096 × 4 |
| | 2,048 × 9 |
| | 1,024 × 18 |
| | 512 × 36 |
| True Dual Port | 16,384 × 1 |
| | 8,192 × 2 |
| | 4,096 × 4 |
| | 2,048 × 9 |
| | 1,024 × 18 |
| Pseudo Dual Port | 16,384 × 1 |
| | 8,192 × 2 |
| | 4,096 × 4 |
| | 2,048 × 9 |
| | 1,024 × 18 |
| | 512 × 36 |

### 2.5.2. Bus Size Matching

All the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### 2.5.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

### 2.5.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

### 2.5.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

### 2.5.6. Memory Output Reset

The EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.13. The optional Pipeline Registers at the outputs of both ports are also reset in the same way.
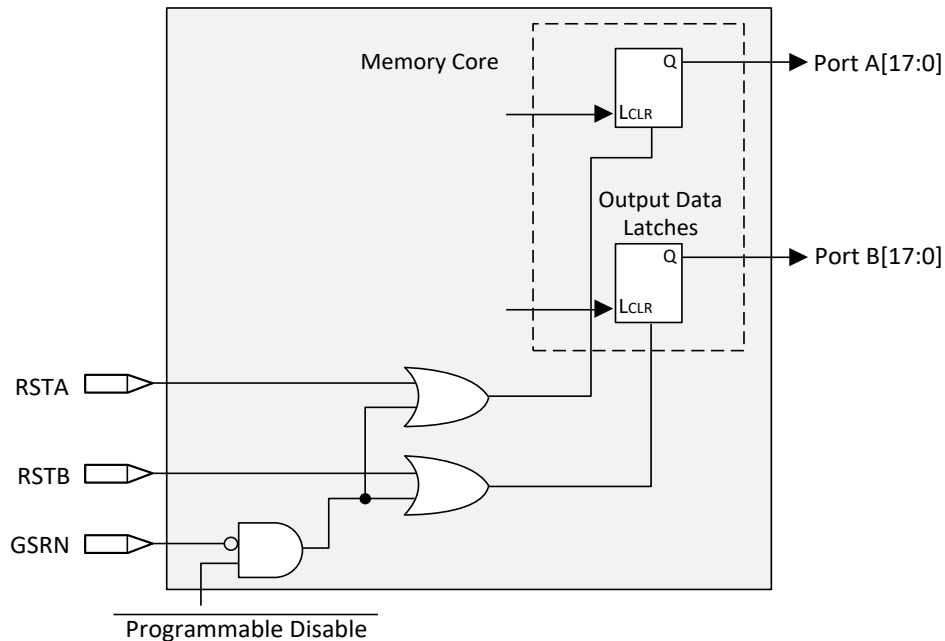


**Figure 2.13. Memory Core Reset**

For further information on the sysMEM EBR block, see the list of technical documentation in References section.

## 2.6. Large RAM

The LIFCL-33/33U devices include additional memory resources in the form of Large Random-Access Memory (LRAM) blocks.

The LRAM is designed to work as Single-Port RAM, Dual-Port RAM, Pseudo Dual-Port RAM, and ROM memories. It is meant to function as additional memory resources for the user beyond what is available in the EBR and PFU.

Each individual Large RAM block contains 0.5 Mbits of memory and has a programmable data width of up to 32 bits. Cascading Large RAM blocks allows data widths of up to 64 bits. Additionally, there is the ability to use either Error Correction Coding (ECC) or byte enable.

## 2.7. sysDSP

LIFCL-33/33U devices provide an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

### 2.7.1. sysDSP Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the LIFCL-33/33U device family, there are many DSP blocks that can be used to support different data widths. This allows the user to use highly parallel implementations of DSP functions. User can optimize DSP performance versus area by choosing appropriate levels of parallelism. Figure 2.14 compares the fully serial implementation to the mixed parallel and serial implementation.
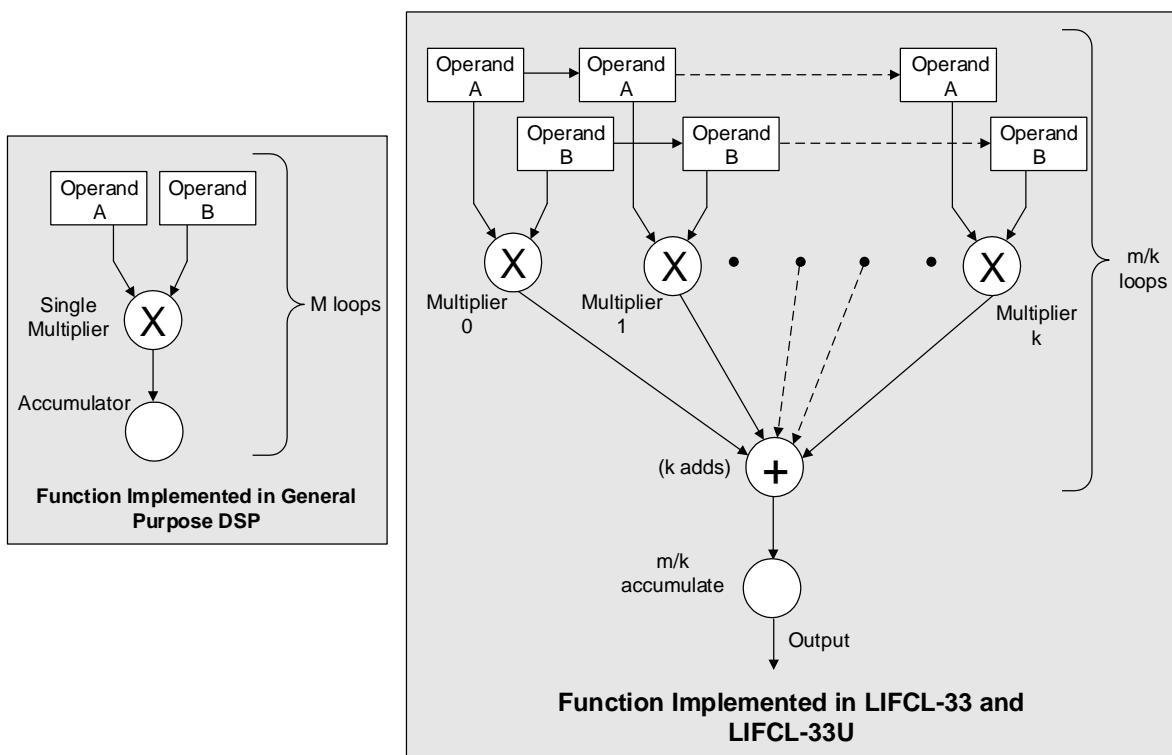


**Figure 2.14. Comparison of General DSP, LIFCL-33, and LIFCL-33U Approaches**

## 2.7.2. sysDSP Architecture Features

The LIFCL-33/33U sysDSP block contains two sysDSP slices. The LIFCL-33/33U sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LIFCL-33/33U sysDSP block (two sysDSP slices) supports many functions that include the following:

- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
    - Odd Mode – Filter with Odd number of taps
    - Even Mode – Filter with Even number of taps
      Two-dimensional (2D) Symmetry Mode – Supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture.
- Fully cascadable DSP across slices. Support for symmetric, asymmetric and non-symmetric filters.
- Multiply (36 × 36, two 18 × 36, four 18 × 18 or eight 9 × 9)
- Multiply Accumulate (supports one 18 × 36 multiplier result accumulation, two 18 × 18 multiplier result accumulation or four 9 × 9 multiplier result accumulation)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 × 18 Multiplies feed into an accumulator that can accumulate up to 54 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
    - Odd Mode – Filter with Odd number of taps
    - Even Mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
    - 3 × 3 and 3 × 5 – Internal DSP Slice support
    - 5 × 5 and larger size 2D blocks – Semi internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading DSP blocks
    - Minimizes fabric use for common DSP functions
      Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
    - Provides matching pipeline registers
      Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users.
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle.

For most cases, as shown in Figure 2.15, the LIFCL-33/33U sysDSP block is backwards-compatible with the LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to LIFCL-33/33U sysDSP. Figure 2.15 shows the diagram of sysDSP block.
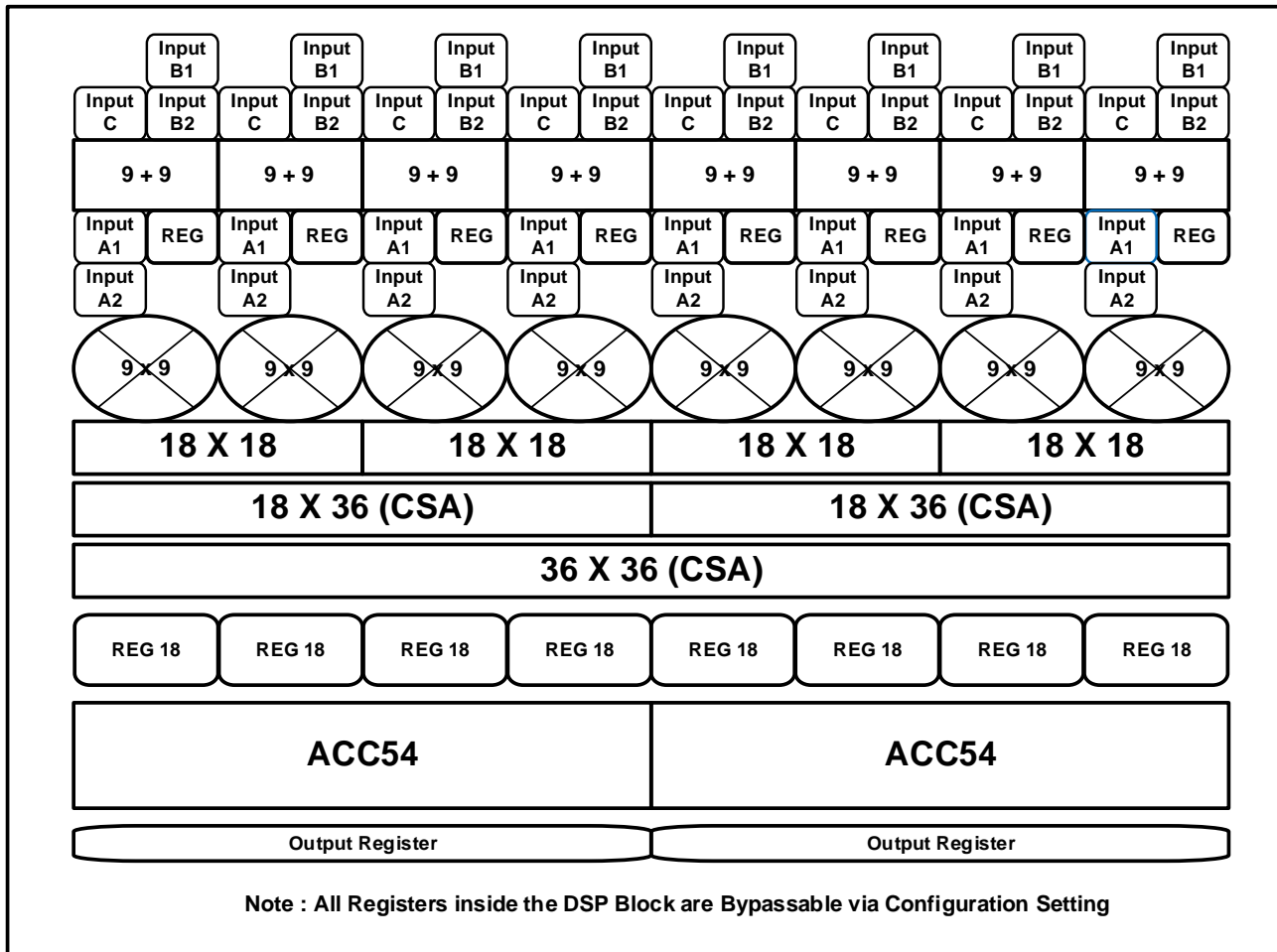
**Figure 2.15. DSP Functional Block Diagram**

The LIFCL-33/33U sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.5 shows the capabilities of LIFCL-33/33U sysDSP block versus the above functions.

**Table 2.5. Maximum Number of Elements in a sysDSP Block**

| Width of Multiply | x9 | x18 | x36 |
|---|---|---|---|
| MULT | 8 | 4 | 1 |
| MAC | 2 | 2 | — |
| MULTADDSUB | 2 | 2 | — |
| MULTADDSUBSUM | 2 | 2 | — |

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting *dynamic operation,* the following operations are possible:

- In the Add/Sub option, the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to sysDSP User Guide for Nexus Platform (FPGA-TN-02096).

## 2.8.    Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads.

On all LIFCL-33/33U devices, two adjacent PIO can be combined to provide a complementary output driver pair.

## 2.9.    Programmable I/O Cell (PIC)

The programmable I/O cells (PIC) provides I/O function and necessary gearing logic associated with PIO. LIFCL-33/33U devices consist of base PIC and gearing PIC.

Base PICs contain three blocks: an input register block, output register block, and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic. Base PICs cover the top bank. Gearing PICs contain gearing logic and edge monitor used for locating the center of data window. Gearing PICs cover the bottom banks to support DDR operation.
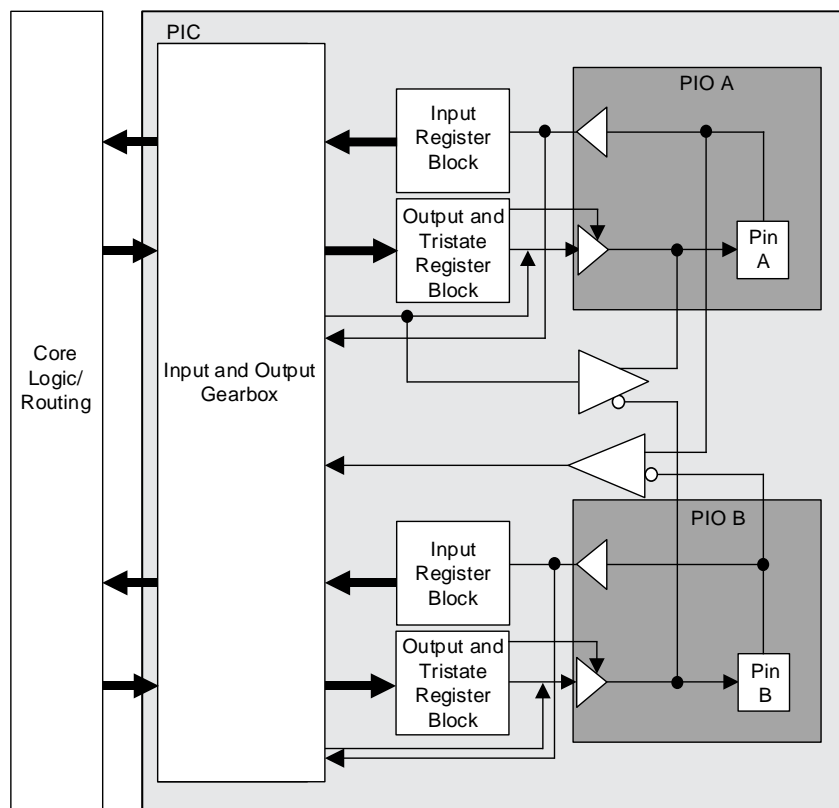


**Figure 2.16. Group of Two High Performance Programmable I/O Cells**
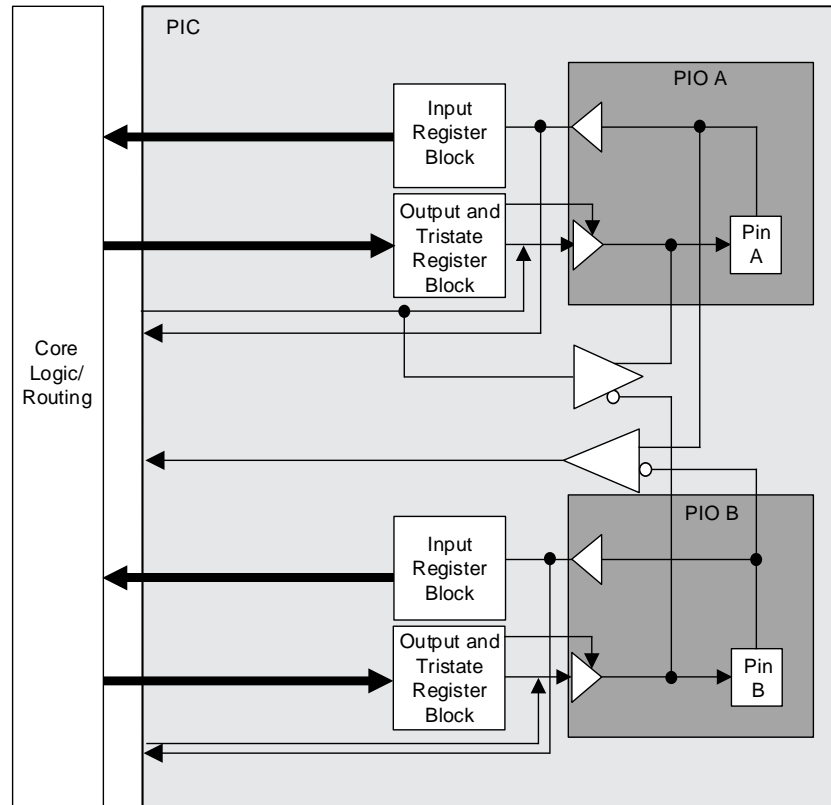
**Figure 2.17. Wide Range Programmable I/O Cells**

### 2.9.1. Input Register Block

The input register blocks for the PIO on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

The Input register block on the bottom side includes gearing logic and registers to implement IDDRX1, IDDRX2, IDDRX4, IDDRX5 gearing functions. With two PICs sharing the DDR register path, it can also implement the IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. For more information on gearing function, refer to CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280).

**Input FIFO**

The LIFCL-33/33U PIO has a dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock, which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high-speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointers to every PIC in same DQS group.

**Table 2.6. Input Block Port Description**

| Name | Type | Description |
|---|---|---|
| D | Input | High Speed Data Input |
| Q[1:0]/Q[3:0]/Q[6:0]/Q[7:0]/Q[9:0] | Output | Low Speed Data to the device core |
| RST | Input | Reset to the Output Block |
| SCLK | Input | Slow Speed System Clock |
| ECLK | Input | High Speed Edge Clock |
| DQS | Input | Clock from DQS control Block used to clock DDR memory data |
| ALIGNWD | Input | Data Alignment signal from device core. |

Figure 2.18 shows the input register block for the PIO on the top edge.
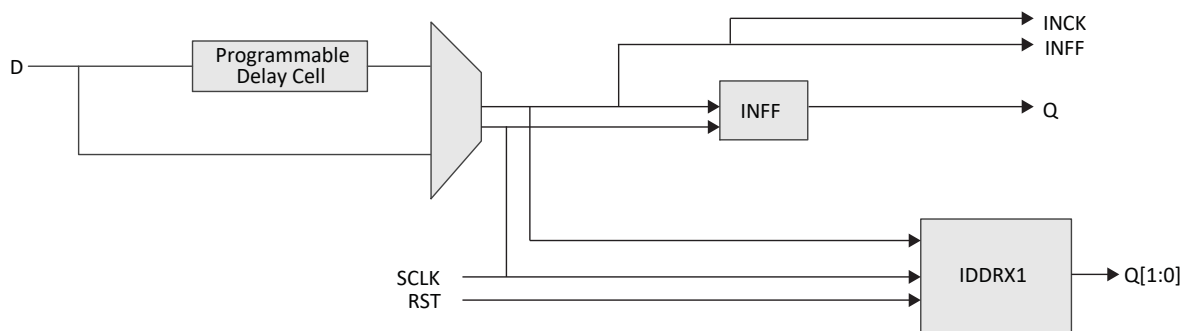


**Figure 2.18. Input Register Block for PIO on Top Side of the Device**

Figure 2.19 shows the input register block for the PIO located on the bottom edge.
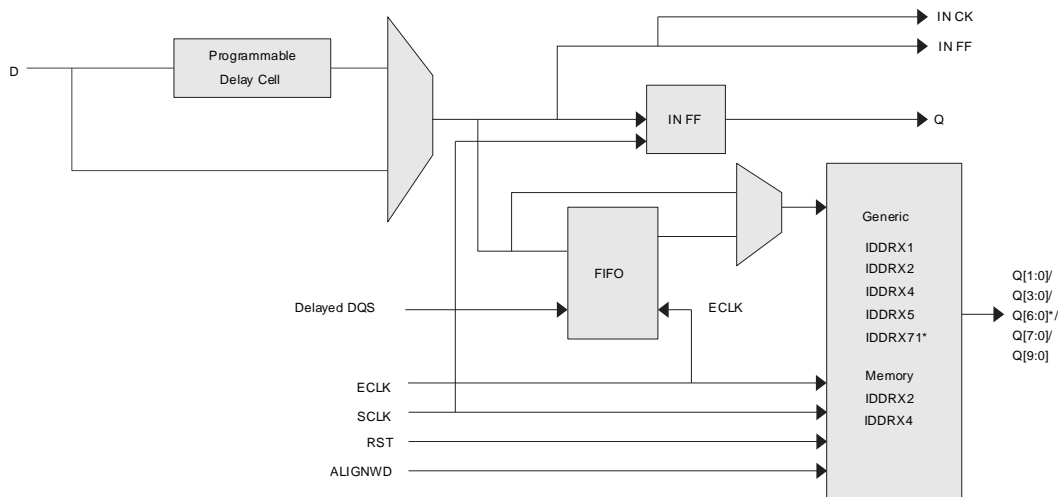


*For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

**Figure 2.19. Input Register Block for PIO on Bottom Side of the Device**

## 2.9.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

The LIFCL-33/33U output data path has programmable registers and output gearing logic. On the bottom side, the output register block can support 1x, 2x, x4, x5, and 7:1 gearing enabling high speed DDR and DDR memory interfaces. On the top side, the banks support 1x gearing. The LIFCL-33/33U output data path diagram is shown in Figure 2.20. The programmable delay cells are also available in the output data path.

For a detailed description of the output register block modes and usage, refer to CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280).
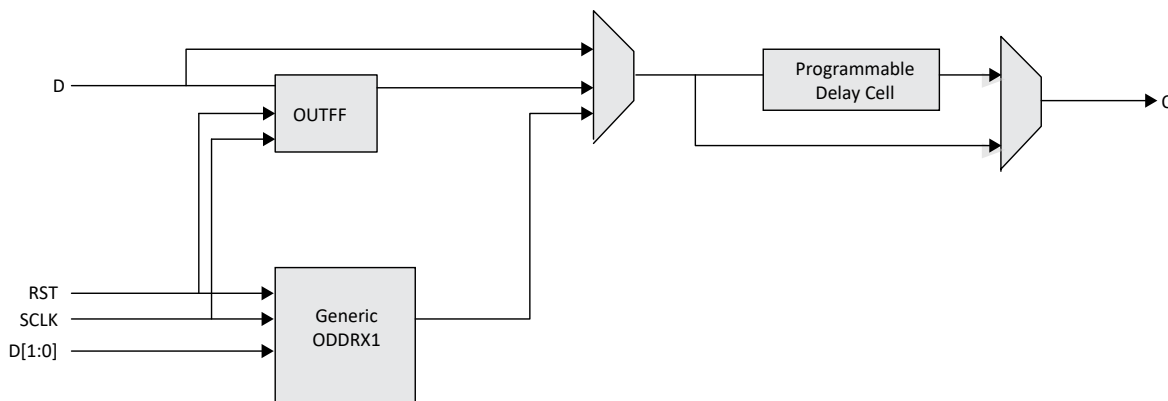


**Figure 2.20. Output Register Block on Top Side**
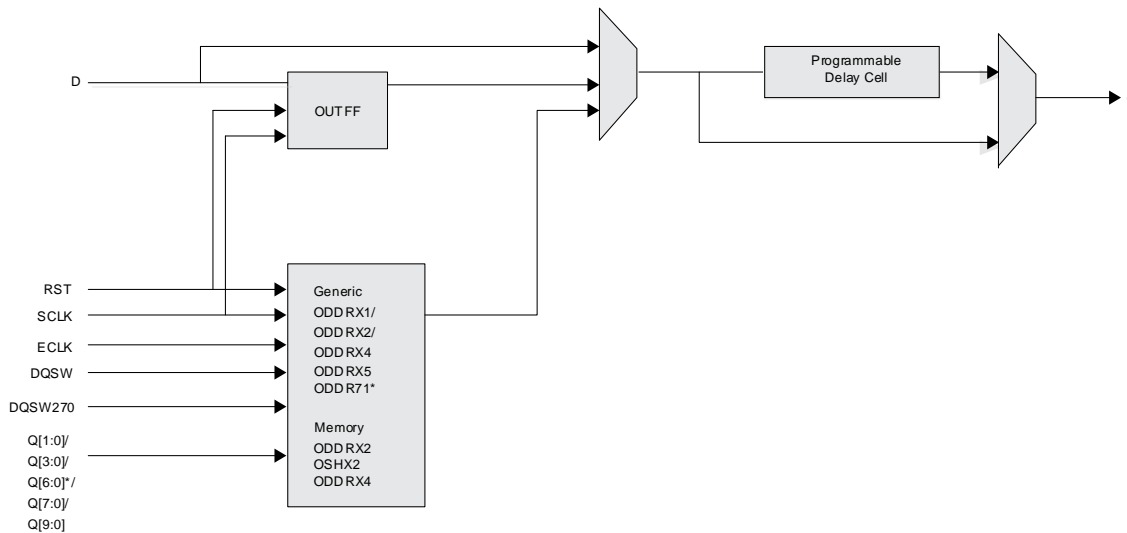


*For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

**Figure 2.21. Output Register Block on Bottom Side**

**Table 2.7. Output Block Port Description**

| Name | Type | Description |
|---|---|---|
| Q | Output | High Speed Data Output |
| D | Input | Data from core to output SDR register |
| Q[1:0]/Q[3:0]/Q[6:0]/Q[7:0]/Q[9:0] | Input | Low Speed Data from device core to output DDR register |
| RST | Input | Reset to the Output Block |
| SCLK | Input | Slow Speed System Clock |
| ECLK | Input | High Speed Edge Clock |
| DQSW | Input | Clock from DQS control Block used to generate DDR memory DQS output |
| DQSW270 | Input | Clock from DQS control Block used to generate DDR memory DQ output |

## 2.10. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, the TD input feeds one of the flip-flops that then feeds the output. In DDR, operations used mainly for DDR memory interfaces can be implemented on the bottom side of the device. Here, two inputs feed the tri-state registers clocked by both ECLK and SCLK.

Figure 2.22 and Figure 2.23 show the Tri-state Register Block functions on the device. For a detailed description of the tri-state register block modes and usage, refer to CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280).
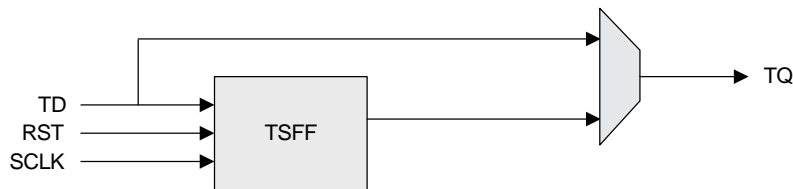


**Figure 2.22. Tri-state Register Block on Top Side**
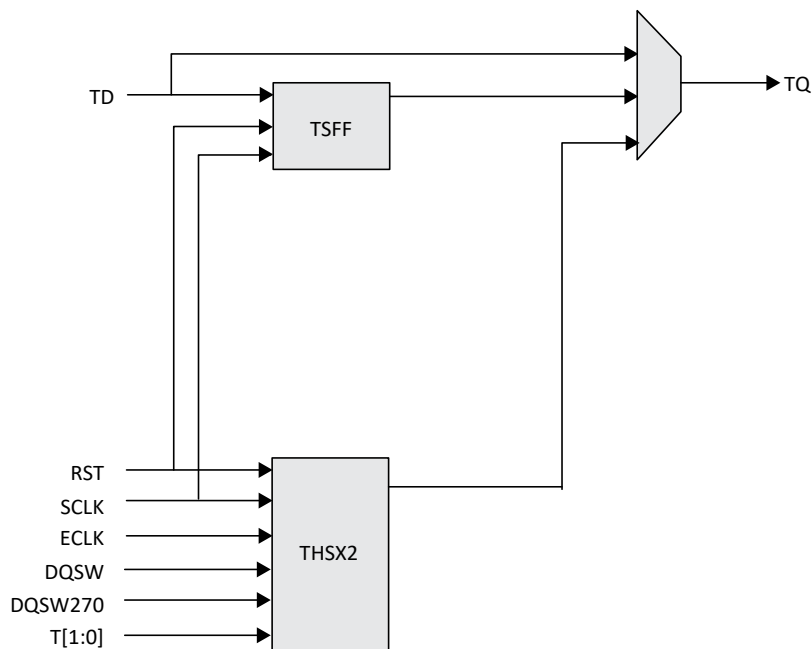


**Figure 2.23. Tri-state Register Block on Bottom Side**

**Table 2.8. Tri-state Block Port Description**

| Name | Type | Description |
|------|------|-------------|
| TD | Input | Tri-state Input to Tri-state SDR Register |
| RST | Input | Reset to the Tri-state Block |
| T[1:0] | Input | Tri-state input to TSHX2 function |
| SCLK | Input | Slow Speed System Clock |
| ECLK | Input | High Speed Edge Clock |
| DQSW | Input | Clock from DQS control Block used to generate DDR memory DQS output |
| DQSW270 | Input | Clock from DQS control Block used to generate DDR memory DQ output |
| TQ | Output | Output of the Tri-state block |

## 2.11. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow you to implement a wide variety of standards that are found in today's systems including LVDS, LVCMOS, LVTTL, and MIPI.

The LIFCL-33/33U family contains multiple Programmable I/O Cell (PIC) blocks. Each PIC contains two Programmable I/O, PIOA and PIOB. Each PIO includes a sysI/O buffer and I/O logic. Two adjacent PIO can be joined to provide a differential I/O pair referred to as True and Comp, where True Pad is associated with the positive side of the differential I/O, and the complement with the negative.

The top side bank support I/O standards from 3.3 V to 1.0 V while the bottom supports I/O standards from 1.8 V to 1.0 V. Every pair of I/O on the bottom bank also have a true LVDS and SLVS Tx Driver. In addition, the bottom bank supports single-ended input termination. Both static and dynamic termination are supported. For more information about DDR implementation in I/O Logic and DDR memory interface support, refer CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280).

### 2.11.1. Supported sysI/O Standards

LIFCL-33/33U sysI/O buffers support both single-ended differential and differential standards. Single-ended standards can be further subdivided into internally ratioed standards such as LVCMOS, LVTTL and externally referenced standards such as HSTL. The buffers support the LVTTL, LVCMOS 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. Differential standards supported include LVDS, SLVS, and differential LVCMOS. For better support of video standards, subLVDS and MIPI_D-PHY are also supported. Table 2.9 and Table 2.10 provide a list of sysI/O standards supported in LIFCL-33/33U devices.

**Table 2.9. Single-Ended I/O Standards**

| Standard | Input | Output | Bi-directional |
|---|---|---|---|
| LVTTL33 | Yes | Yes | Yes |
| LVCMOS33 | Yes | Yes | Yes |
| LVCMOS25 | Yes | Yes | Yes |
| LVCMOS18 | Yes | Yes | Yes |
| LVCMOS15 | Yes | Yes | Yes |
| LVCMOS12 | Yes | Yes | Yes |
| LVCMOS10 | Yes | No | No |
| HTSL15 I | Yes | Yes | Yes |
| LVCMOS18H | Yes | Yes | Yes |
| LVCMOS15H | Yes | Yes | Yes |
| LVCMOS12H | Yes | Yes | Yes |
| LVCMOS10H | Yes | Yes | Yes |
| LVCMOS10R | Yes | — | Yes[1] |

**Note:**
1. Output supported by LVCMOS10H.

**Table 2.10. Differential I/O Standards**

| Standard | Input | Output | Bi-directional |
|---|---|---|---|
| LVDS | Yes | Yes | Yes |
| SUBLVDS | Yes | No | — |
| SLVS | Yes | Yes | — |
| SUBLVDSE | — | Yes | — |
| SUBLVDSEH | — | Yes | — |
| LVDSE | — | Yes | — |
| MIPI_D-PHY | Yes | Yes | Yes |
| HSTL15D_I | Yes | Yes | Yes |
| LVTTL33D | — | Yes | — |
| LVCMOS33D | — | Yes | — |
| LVCMOS25D | — | Yes | — |

### 2.11.2. sysI/O Banking Scheme

The LIFCL-33/33U devices have up to six banks in total. There are three banks on the top, and three at the bottom side of the device. Bank 0, Bank 1, and Bank 5 support up to VCCIO 3.3 V while Bank 2, Bank 3, and Bank 4 support up to VCCIO 1.8 V.

Bank 5 is only supported in LIFCL-33, while AON and USB signals are only available in LIFCL-33U.

**Typical sysI/O Behavior During Power-up**

The internal Power-On-Reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated the FPGA core logic becomes active. It is the responsibility of the user to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LIFCL-33/33U devices, see the list of technical documentation in References section.

$V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas $V_{CCIO}$ supplies power to the I/O buffers. To simplify the system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. For the different power supply voltage levels supported by the I/O banks, refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067) for detailed information.

**VREF1 and VREF2**

Bank 2, Bank 3, and Bank 4 can support two separate VREF input voltages, VREF1, and VREF2. To assign a VREF driver, use IO_Type = VREF1_DRIVER or VREF2_DRIVER. To assign VREF to a buffer, use VREF1_LOAD or VREF2_LOAD.

**sysI/O Standards Supported by I/O Bank**

All banks can support multiple I/O standards under the VCCIO rules discussed above. Table 2.11 and Table 2.12 summarize the I/O standards supported on various sides of the LIFCL-33/33U devices.

**Table 2.11. Single-Ended I/O Standards Supported on Various Sides**

| Standard | Top | Bottom |
|----------|-----|--------|
| LVTTL33 | Yes | — |
| LVCMOS33 | Yes | — |
| LVCMOS25 | Yes | — |
| LVCMOS18 | Yes | — |
| LVCMOS15 | Yes | — |
| LVCMOS12 | Yes | — |
| LVCMOS10 | Yes | — |
| LVCMOS18H | — | Yes |
| LVCMOS15H | — | Yes |
| LVCMOS12H | — | Yes |
| LVCMOS10H | — | Yes |
| LVCMOS10R | — | Yes |
| HTSL15 I | — | Yes |

**Table 2.12. Differential I/O Standards Supported on Various Sides**

| Standard | Top | Bottom |
|---|---|---|
| LVDS | — | Yes |
| SUBLVDS | — | Yes |
| SLVS | — | Yes |
| SUBLVDSE | Yes | — |
| SUBLVDSEH | — | Yes |
| LVDSE | Yes | — |
| MIPI_D-PHY | — | Yes |
| HSTL15D_I | — | Yes |
| LVTTL33D | Yes | — |
| LVCMOS33D | Yes | — |
| LVCMOS25D | Yes | — |

**Hot Socketing**

LIFCL-33/33U devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/O remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Bank 0, Bank 1, and Bank 5 wide range I/O (excluding MCLK/MCSN/MOSI/INITN/DONE) are hot socketable. Bank 2, Bank 3, and Bank 4 do not support hot socketing.

### 2.11.3. sysI/O Buffer Configurations

This section describes the various sysI/O features available on the LIFCL-33/33U devices. Refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067) for detailed information.

## 2.12. IEEE 1149.1-Compliant Boundary Scan Testability

All LIFCL-33/33U devices contain various ports that can be used for configuration, including a Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK, and TMS. The test access port uses VCCIO1 for power supply. The test access port is supported for VCCIO1 = 1.8 V - 3.3 V.

For more information, refer to sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099).

## 2.13. Always On (AON)

The Hardware (HW) AON block in LIFCL-33U is provided to support low power application, where the main FPGA device can be put in the power down state while the AON block continues to operate as a wake-up timer. The auxiliary power (always on power domain) to the AON block is provided by the dedicated $V_{CCAUX\_AON}$ supply rail. This is isolated from the rest of the FPGA power domain that can be turned off for low power applications. The AON_OUT output pin is provided to control the external power switch and AON_INT is provided to interrupt or to override the power down state. Both external signals follow the 1.8 V LVCMOS I/O standard. Figure 2.24 shows the high-level block diagram with internal FPGA internal interface control signals for the AON block. Table 2.13 provides the descriptions of the AON ports.

For more information, refer to Always ON Module IP User Guide (FPGA-IPUG-02216).
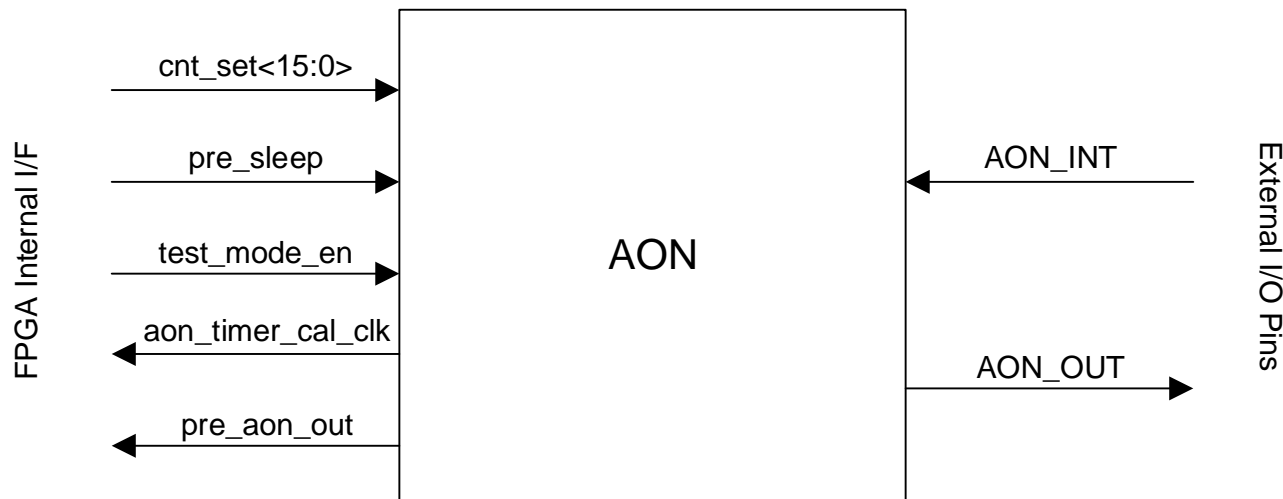
**Figure 2.24. AON Functional Block Diagram**

**Table 2.13. AON Port Description**

| Interface | Port Names | In/Out to AON | Description |
|---|---|---|---|
| FPGA Internal I/F | cnt_set<15:0> | Input | Upon FPGA power up, this 16-bit AON timer counter value is used to set the AON wake up timer output (AON_OUT). Internal timer is running at 1 kHz nominal clock frequency |
| | pre_sleep | Input | This input from the FPGA logic is used to indicate to the AON to drive the AON_OUT low indicating that FPGA can be powered down. |
| | test_mode_en | Input | This input can be used to trigger AON test mode |
| | aon_time_cal_clk | Output | Internal AON timer clock output can be used for calibration. Nominal clock frequency is 16 kHz. |
| | pre_aon_out | Output | Internal test mode output before the AON_OUT external signal. |
| External | AON_INT | Input | Active high (AON_INT = 1) strobe signal to externally switch FPGA from power down state (AON_OUT=0) to power on state (AON_OUT=1) |
| | AON_OUT | Output | Always On output to control power regulator(s). FPGA Power Down=0; FPGA Power Up = 1 |

## 2.14.  USB

The Hardened USB block in CrossLink-NX33U is designed to support device controller applications such as image sensor data transfer through USB 3.2 Gen 1 and $I^2C$, GPIO, SPI control signals through USB 2.0. It can support USB 3.2 Gen 1 (5 Gbps) and USB 2.0 HS (480 Mbps), and FS (12 Mbps) modes. Internal interface consists of PIPE interface to AXI (Main) DMA data transfer for high-speed video applications. For control interface, internal UTMI data is translated to AHB (Secondary) and LMMI interface to FPGA fabric. The high-level block diagram of the USB hard IP is shown in Figure 2.25.
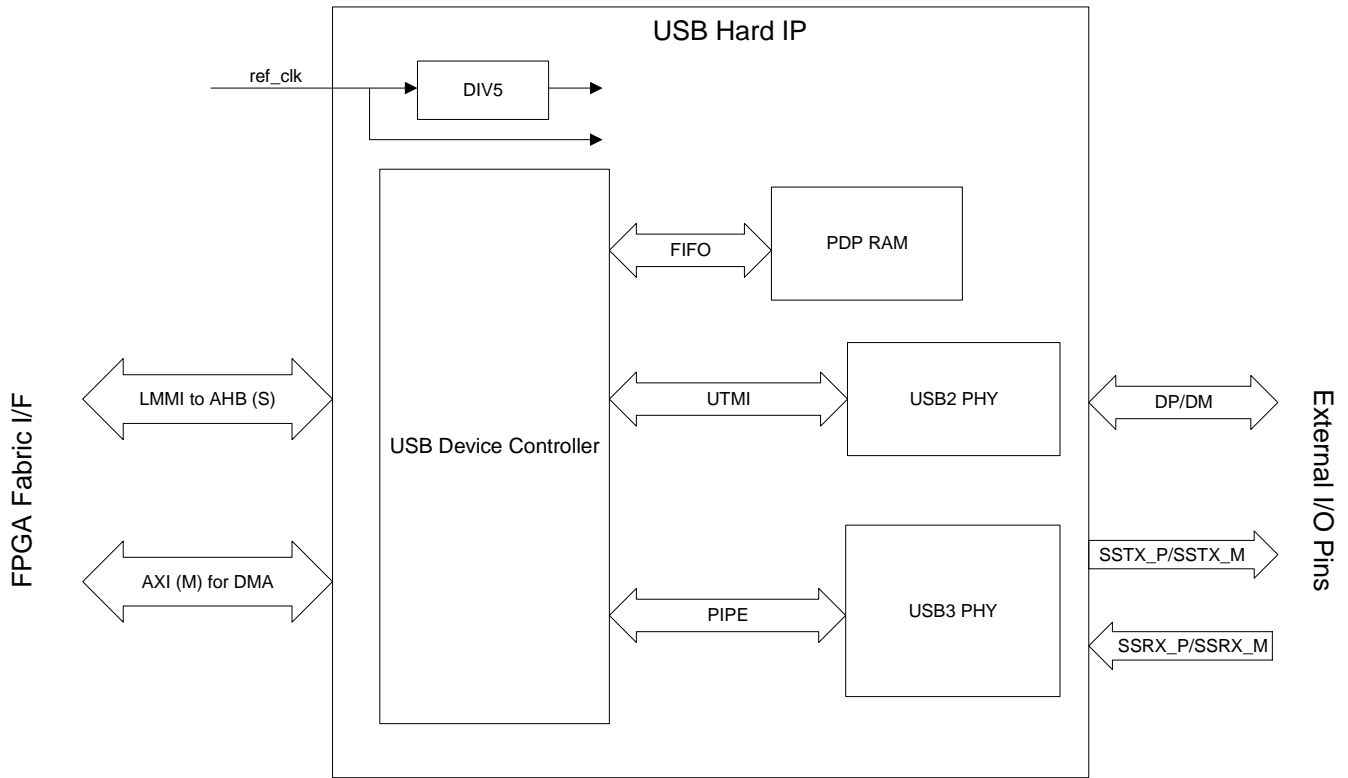
**Figure 2.25. USB Hard IP Functional Block Diagram**

## 2.14.1. USB Hardware Architecture

The typical device applications found in USB 3.2 Gen 1 and LIFCL-33U internal interface are described in this section. The following are the example USB applications:

- USB low speed I/O interface aggregation
- USB video class streaming

Figure 2.26 shows the internal interface block diagram.
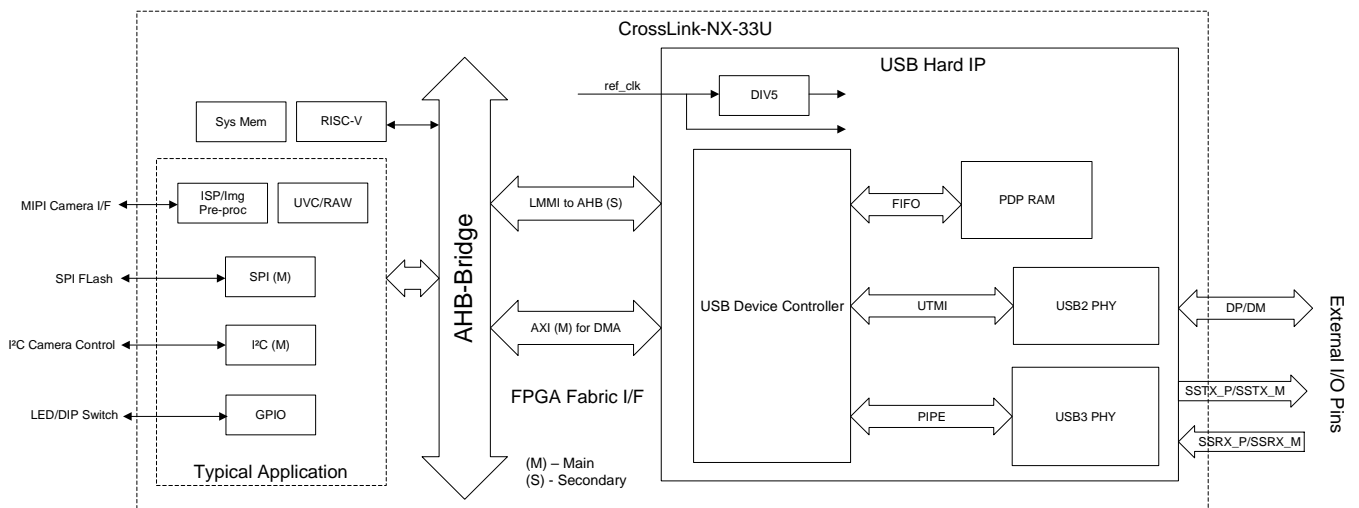


**Figure 2.26. Typical USB Hardware Application Diagram**

### 2.14.1.1. USB Device Controller:

The controller has the following interfaces:

- Application interfaces – AXI and LMMI per hard macro design. The secondary interface is LMMI used as control path for register and RAM debug access. The primary interface is AXI used ad data path for internal DMA accessing external memory. The hard-macro has internal bridge to convert LMMI interface.
- FIFO interface is implemented in PDP RAM and used to access EP RAM per IP definition.
- The PHY interfaces (UTMI and PIPE) are transparent and integrated in Hard Macro.
- Infrastructure connection for clock, reset, debug and power. Refer to Clock, Reset, Debug, and Power section for more details.

### 2.14.1.2. Endpoints

The number of end points and packet sizes are user-configurable. Table 2.14 provides the maximum number and types of EP and maximum packet sizes supported by each end points.

**Table 2.14. USB Endpoint FIFO Size and Burst Size (Maximum Packet Size)**

| EP Type | FIFO Size | | Burst size |
|---|---|---|---|
| Control BiDir | — | | — |
| Bulk | 4 kB | | 4x MPS |
| Bulk | 4 kB | | 4x MPS |
| Isoc | 4 kB | | 4x MPS |
| Isoc | 4 kB | | 4x MPS |
| Interrupt | 4 kB | | 4x MPS |
| Interrupt | 256 B | | — |
| Interrupt | 256 B | | — |
| Interrupt | 256 B | | — |

### 2.14.1.3. Clock, Reset, Debug, and Power

- The following clocks need to be supplied per IP Databook:
    - AHB bus clock and RAM clock can be the same
    - U2MAC clock – same as UTMI clock
    - U3MAC clock – link clock, or same as pipe clock
    - Pipe clock – PHY interface clock
- Clock gating is enabled for low power device application.
- The USB device bus power is managed by the host controller (SoC) for LP PHY modes like P1/2/3 and link states like U1/2/3. The USB 2.0 mode enables LPM-L1 and suspend states to reduce the application power.

### 2.14.1.4. USB PHY

- Reference clock and DIV5 is implemented in hard-macro.
- Based on speed negotiation, only one PHY is active during connect and are mutually exclusive.

### 2.14.1.5. Application Fabric

- The application fabric could be AHB with the appropriate individual bridge (AHB to APB/AXI/LMMI) interface IP.
- Provides main (M) and secondary (S) nodes for all the controller interface with RISC-V.

### 2.14.1.6. RISCV

- The core could be RISC-V MC SIP core with the Lattice Propel™ toolchain.
- The LRAMs are allocated for core system memory and as intermediate buffer to exchange data structures and payload between RISC-V and the controller such as USB, $I^2C$, and SPI.

### 2.14.1.7.  I/O Aggregation and Common Modules

- The standard IP from the library is used for I$^2$C, SPI, and GPIO.
- The SPI (M) controller is mandatory for all USB applications to interface with the flash memory.
- The I$^2$C (M) controller is used for I/O aggregation to interface with platform sensors like temperature sensor.
- The GPIO controller provides access to input (such as DIP switches) and output (LED) wires.

### 2.14.1.8.  Camera streaming Modules

- The image preprocessing block provides the processed image which can be sent to the SoC imaging application. Two possible options are:
    - Typical image preprocessing functions provide downscaling and optionally apply digital gain, gamma, and other functions.
    - Optional standard ISP IP can be used for reference design to improve the image quality.
- There are two options for USB streaming:
    - UVC – This needs the controller IP to convert pixel data to USB video class stream through bulk or isochronous endpoints.
    - RAW streaming – this is custom streaming per Host RAW streaming driver requirement through bulk or isochronous endpoints.
- I$^2$C primary controller is used as camera sensor programming interface.
- GPIO signal provides power and reset signals for camera sensor.

## 2.14.2. USB RISC-V Firmware Stack and Host Software Interface

Figure 2.27 shows the RISCV Firmware (FW) stack and the Host Software (SW) interface with boot loader pointer to SPI Flash. The SPI Flash holds the FPGA bitfile (USB APP) and RISCV FW. The FW stack can be bare metal or RTOS-based, with the module in the figure are applicable for corresponding to typical USB application design.

The USB peripheral driver provides the device application layer based on the application.
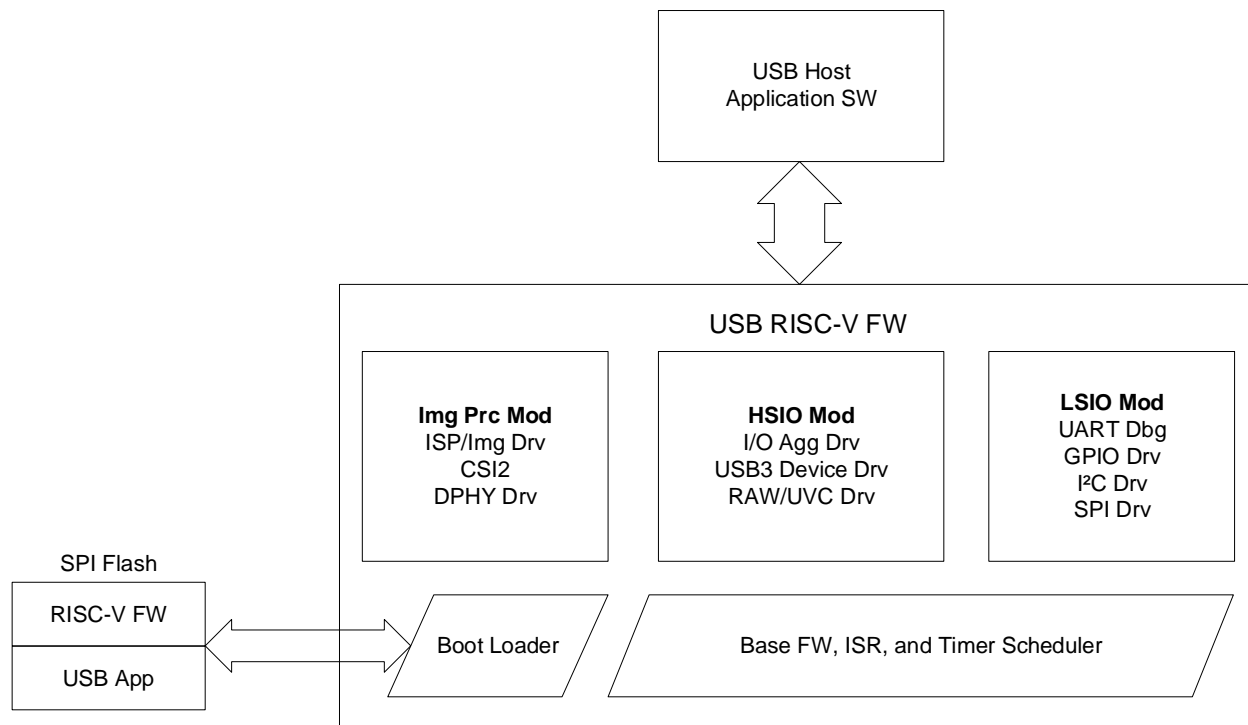


**Figure 2.27. LIFCL-33U USB RISC-V Host FW Stack**

For more information, refer to USB 2.0/3.2 IP Core User Guide (FPGA-IPUG-02237).

## 2.15. Device Configuration

All LIFCL-33/33U devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support serial, quad, and byte configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. JTAG_EN is the only dedicated configuration pin. *PPROGRAMN/INITN/DONE* are enabled by default but can be turned into GPIO. The remaining sysCONFIG pins are used as dual function pins. Refer to sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099) for more information about using the dual-use pins as general purpose I/O.

There are various ways to configure the LIFCL-33/33U devices:

- JTAG (TAP)
- Master Serial Peripheral Interface (SPI) – to load from external SPI flash using x1, x2, or x4 (QSPI) interfaces.
- Inter-Integrated Circuit Bus (I$^2$C)
- Improved Inter-Integrated Circuit Bus (I3C)
- Slave SPI from a system host
- Lattice Memory Mapped Interface (LMMI), refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067) for more details.
- JTAG, SSPI, MSPI, I$^2$C, and I3C are supported for VCCIO = 1.8 V - 3.3 V

On power-up, based on the voltage level (high or low) of the PROGRAMN pin, the FPGA SRAM is configured by the appropriate sysCONFIG port. If PROGRAMN pin is *low*, the FPGA is in Slave configuration mode (Slave SPI, Slave I$^2$C, or Slave I3C) and is waiting for the correct Slave Configuration port activation key. PROGRAMN must be driven high within 50 ns of the end of transmission of the Slave Configuration port activation key, that is, the deassertion of SCSN. If no slave port is declared active before the PROGRAMN pin is sensed HIGH, the FPGA is in Master SPI booting mode. In Master SPI booting mode, the FPGA boots from an external SPI flash. Once a configuration port is activated, it remains active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by enabling the JTAG_EN pin and sending the appropriate command through the TAP port.

### 2.15.1. Enhanced Configuration Options

LIFCL-33/33U devices have enhanced configuration features such as:

- Bitstream Decryption
- Decompression Support
- Watchdog Timer support
- Dual and Multi-boot image support

For more details, refer to sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099).

The Watchdog Timer is a new configuration feature that helps the user to add a programmable timer option for timeout applications.

**Dual-Boot and Multi-Boot Image Support**

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LIFCL-33/33U devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LIFCL-33/33U devices can revert to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099).

## 2.16. Single Event Upset (SEU) Handling

The LIFCL-33/33U devices are unique in that the underlying technology used to build these devices is much more robust and less prone to soft errors.

The LIFCL-33/33U devices have an improved, hardware implemented, Soft Error Detection (SED) circuit which can be used to detect SRAM errors so they can be corrected. There are two layers of SED implemented in LIFCL-33/33U devices, making it more robust and reliable.

The SED hardware in LIFCL-33/33U devices is part of the Configuration block. The SED module in LIFCL-33/33U is an enhanced version as compared to the SED modules implemented in other Lattice devices. The configuration data is divided into frames so that the entire FPGA can be programmed precisely with ease. The SED hardware reads data from the FPGAs configuration memory and performs an Error Correcting Code (ECC) calculation on every frame of configuration data (see Figure 2.2). Once an error is detected, a notification is generated and SED resumes operation. For single bit errors, the corrected value is rewritten to the frame using ECC information. If more than one-bit error is detected within one frame of configuration data, an error message is generated. LIFCL-33/33U devices also have dedicated logic to perform Cycle Redundancy Code (CRC) checks for the entire bitstream, which runs in parallel along with ECC.

After the ECC is calculated on all frames of configuration data, CRC is calculated and checked for the entire bitstream. ECC and CRC checks do not include the contents of RAMs (EBR, Large RAM, and distributed RAM).

For further information on SED support, refer to Soft Error Detection (SED)/Correction (SEC) User Guide for Nexus (FPGA-TN-02076).

## 2.17. On-Chip Oscillator

The LIFCL-33/33U devices feature two on-chip oscillators. Both Oscillators are controlled with internally generated current.

The low frequency oscillator (LFOSC) is tailored for low power operation and runs at a nominal frequency of 128 kHz. The LFOSC always runs and can be used to perform always on functions with the lowest possible power. The high frequency oscillator (HFOSC) runs at a nominal frequency of 450 MHz but can be divided down to a range of 256 MHz to 2 MHz by user attributes.

For more information, refer to OSC Module User Guide (FPGA-IPUG-02065).

## 2.18. User I²C IP

The LIFCL-33/33U devices have one hard I²C interface, which can be configured either as a master (controller) or a slave (target). The pins for the I²C interface are pre-assigned.

The interface core has the option to delay the either the input or the output data (SDA), or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface to any external I²C components. In addition, 50 ns glitch filters are available for both SDA and SCL.

When the IP interface is configured as master (controller), it is able to control other devices on the I²C bus through the pre-assigned pins. When the core is configured as a slave (responder), the device is able to provide, for example, I/O expansion to an I²C master (controller). The I²C core supports the following functionality:

- Master (controller) and Slave (target) operation
- 7-bit and 10-bit addressing
- Multi-master (controller) arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed (Standard-Mode, Fast-Mode, Fast-Mode Plus)
- General Call support
- Optional receive and transmit data FIFOs with programmable sizes
- Optionally 50 ns delay on input or output data (SDA), or both
- Hard-Connection and Programmable I/O Connection Support
- Programmable to a mode compliant with I3C requirements on legacy I²C Slave Devices.
- Fast-Mode and Fast-Mode Plus Support
- Disabled Clock Stretching

- 50 ns SCL and SDA Glitch Filters
- Programmable 7-bit Address

For further information on the User I²C, refer to I²C Hardened IP User Guide for Nexus Platform (FPGA-TN-02142).

## 2.19. Trace ID

Each LIFCL-33/33U devices contain a unique (per device) TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the SPI, I²C, or JTAG interfaces. For further information on TraceID, refer to Using TraceID (FPGA-TN-02084).

## 2.20. Cryptographic Engine

The LIFCL-33/33U family of devices support several cryptographic features that helps customer secure their design. Some of the key cryptographic features include Advanced Encryption Standard (AES), Hashing Algorithms and true random number generator (TRNG). The LIFCL-33/33U devices also feature bitstream encryption (using AES-256), used for protecting confidential FPGA bitstream data, and bitstream authentication (using ECDSA), which maintains bitstream integrity and protects the FPGA design bitstream from copying and tampering.

The Cryptographic Engine (CRE) is the main engine, which is responsible for the bitstream encryption as well as authentication of the LIFCL-33/33U devices. Once the bitstream is authenticated and the device is ready for user functions, the CRE is available for users to implement various cryptographic functions in the FPGA design. To enable specific cryptographic function, the CRE must be configured by setting a few registers.

The Cryptographic Engine supports the below user-mode features:

- True Random Number generator (TRNG)
- Secure Hashing Algorithm (SHA)-256 bit
- Message authentication codes (MACs) – HMAC
- Lattice Memory Mapped Interface (LMMI) interface to user logic
- High Speed Port (HSP) for FIFO-based streaming data transfer
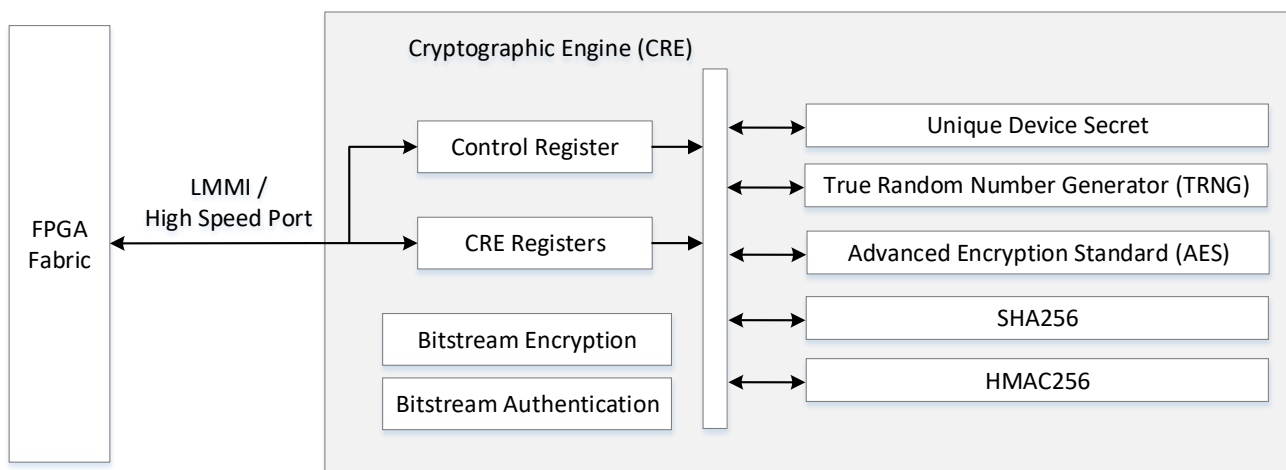


**Figure 2.28. Cryptographic Engine Block Diagram**

# 3. DC and Switching Characteristics for Commercial and Industrial

All specifications in this chapter are characterized within recommended operating conditions unless otherwise specified.

## 3.1. Absolute Maximum Ratings

**Table 3.1. Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$, $V_{CCECLK}$ | Supply Voltage | -0.5 | 1.10 | V |
| $V_{CCAUX}$, $V_{CCAUXA}$, $V_{CCAUXH2}$, $V_{CCAUXH3}$, $V_{CCAUXH4}$, $V_{CCAUX\_AON}$[5] | Supply Voltage | -0.5 | 1.98 | V |
| $V_{CCIO0, 1, 5}$ | I/O Supply Voltage | -0.5 | 3.63 | V |
| $V_{CCIO2, 3, 4}$ | I/O Supply Voltage | -0.5 | 1.98 | V |
| AVDD33[5] | Supply Voltage for Hardened USB[5] | -0.5 | 3.63 | V |
| AVDD18, AVDD18_TX, AVDD18_COM[5] | Supply Voltage for Hardened USB | -0.5 | 1.98 | V |
| AVDD, AVDD_TX[5] | Supply Voltage for Hardened USB | -0.5 | 1.10 | V |
| — | Input or I/O Voltage Applied, Bank 0, Bank 1, Bank 5[6] | -0.5 | 3.63 | V |
| — | Input or I/O Voltage Applied, Bank 2, Bank 3, Bank 4 | -0.5 | 1.98 | V |
| $T_A$ | Storage Temperature (Ambient) | -65 | +150 | °C |
| $T_J$ | Junction Temperature | — | +125 | °C |

**Notes**:
1. Stress above those listed under the *Absolute Maximum Ratings* may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. All $V_{CCAUX}$ should be connected on PCB.
5. $V_{CCAUX\_AON}$ and all AVDD are only supported in LIFCL-33U.
6. Bank 5 is only supported in LIFCL-33.

## 3.2. Recommended Operating Conditions[1, 2, 3]

**Table 3.2. Recommended Operating Conditions**

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$, $V_{CCECLK}$ | Core Supply Voltage | $V_{CC}$ = 1.0 | 0.95 | 1.00 | 1.05 | V |
| $V_{CCAUX}$ | Auxiliary Supply Voltage | Bank 0, Bank 1, Bank 5[6] | 1.71 | 1.80 | 1.89 | V |
| $V_{CCAUXH2/3/4}$ | Auxiliary Supply Voltage | Bank 2, Bank 3, Bank 4 | 1.71 | 1.80 | 1.89 | V |
| $V_{CCAUXA}$, $V_{CCAUX\_AON}$[5] | Auxiliary Supply Voltage for core logic and AON | — | 1.71 | 1.80 | 1.89 | V |
| AVDD33[5] | Supply Voltage for Hardened USB[5] | — | 3.135 | 3.30 | 3.465 | V |
| AVDD18, AVDD18_TX, AVDD18_COM[5] | Supply Voltage for Hardened USB | — | 1.71 | 1.80 | 1.89 | V |
| AVDD, AVDD_TX[5] | Supply Voltage for Hardened USB | — | 0.95 | 1.00 | 1.05 | V |
| $V_{CCIO}$ | I/O Driver Supply Voltage | $V_{CCIO}$ = 3.3 V, Bank 0, Bank 1, Bank 5[6] | 3.135 | 3.30 | 3.465 | V |
| | | $V_{CCIO}$ = 2.5 V, Bank 0, Bank 1, Bank 5[6] | 2.375 | 2.50 | 2.625 | V |
| | | $V_{CCIO}$ = 1.8 V, All Banks | 1.71 | 1.80 | 1.89 | V |
| | | $V_{CCIO}$ = 1.5 V, All Banks[4] | 1.425 | 1.50 | 1.575 | V |
| | | $V_{CCIO}$ = 1.2 V, All Banks[4] | 1.14 | 1.20 | 1.26 | V |
| | | $V_{CCIO}$ = 1.0 V, Bank 2, Bank 3, Bank 4 | 0.95 | 1.00 | 1.05 | V |
| **Operating Temperature** | | | | | | |
| $t_{JCOM}$ | Junction Temperature, Commercial Operation | — | 0 | — | 85 | °C |
| $t_{JIND}$ | Junction Temperature, Industrial Operation | — | -40 | — | 100 | °C |

**Notes**:
1. For correct operation, all supplies must be held in their valid operation voltage range.
2. All supplies with same voltage should be from the same voltage source. Proper isolation filters are needed to properly isolate noise from each other.
3. Common supply rails must be tied together.
4. MSPI (Bank0) and JTAG, SSPI, I2C, and I3C (Bank 1) ports are supported for $V_{CCIO}$ = 1.8 V to 3.3 V.
5. $V_{CCAUX\_AON}$ and all AVDD are only supported in LIFCL-33U.
6. Bank 5 is only supported in LIFCL-33.

## 3.3.    Power Supply Ramp Rates[2]

**Table 3.3. Power Supply Ramp Rates**

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| $t_{RAMP}$ | Power Supply ramp rates for all supplies[1] | 0.1 | — | 50 | V/ms |

**Notes**:
1. Assumes monotonic ramp rates.
2. All supplies need to be in the operating range as defined in Recommended Operating Conditions, when the device has completed configuration and entering User Mode. Supplies that are not in the operating range needs to be adjusted to faster ramp rate, or users must delay configuration or wake up.

## 3.4.    Power up Sequence

Power-On-Reset (POR) puts the LIFCL-33/33U devices into a reset state. There is no power up sequence required for the LIFCL-33/33U devices.

**Table 3.4. Power-On Reset**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|--------|-----------|--|-----|-----|-----|------|
| $V_{PORUP}$ | Power-On-Reset ramp-up trip point (Monitoring $V_{CC}$, $V_{CCAUX}$, $V_{CCIO0}$, and $V_{CCIO1}$) | $V_{CC}$ | 0.73 | — | 0.83 | V |
| | | $V_{CCAUX}$ | 1.34 | — | 1.62 | V |
| | | $V_{CCIO0}$,$V_{CCIO1}$ | 0.89 | — | 1.05 | V |
| $V_{PORDN}$ | Power-On-Reset ramp-up trip point (Monitoring $V_{CC}$ and $V_{CCAUX}$) | $V_{CC}$ | 0.51 | — | 0.81 | V |
| | | $V_{CCAUX}$ | 1.38 | — | 1.59 | V |

## 3.5.    On-Chip Programmable Termination

The LIFCL-33/33U devices support a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40 Ω, 50 Ω, 60 Ω, or 75 Ω.
- Common mode termination of 100 Ω for differential inputs.
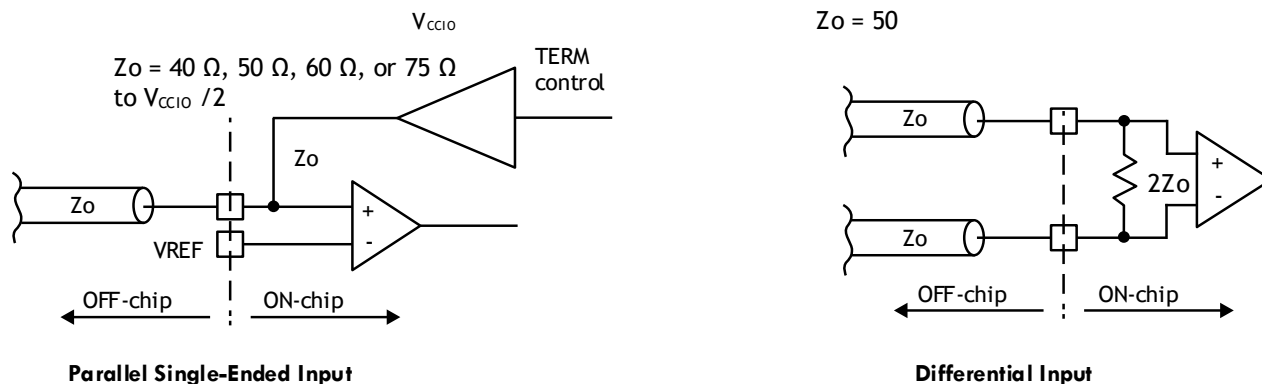


**Figure 3.1. On-Chip Termination**

See Table 3.5 for termination options for input modes.

**Table 3.5. On-Chip Termination Options for Input Modes**

| IO_TYPE | Differential Termination Resistor[1] | Terminate to V$_{CCIO}$/2[1] |
|---|---|---|
| subLVDS | 100, OFF | OFF |
| SLVS | 100, OFF | OFF |
| MIPI_DPHY | 100 | OFF |
| HSTL15D_I | 100, OFF | OFF |
| LVCMOS15H | OFF | OFF |
| LVCMOS12H | OFF | OFF |
| LVCMOS10H | OFF | OFF |
| LVCMOS12H | OFF | OFF |
| LVCMOS10H | OFF | OFF |
| LVCMOS18H | OFF | OFF, 40, 50, 60, 75 |
| HSTL15_I | OFF | 50 |

**Note**:

1. Use of TERMINATE to V$_{CCIO}$/2 and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance –10%/+60%.

Refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067) for on-chip termination usage and value ranges.

## 3.6. Hot Socketing Specifications

**Table 3.6. Hot Socketing Specifications for GPIO**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| I$_{DK}$ | Input or I/O Leakage Current for Wide Range I/O (excluding MCLK/MCSN/MOSI/INITN/DONE) | $0 < V_{IN} < V_{IH}$ (max) $0 < V_{CC} < V_{CC}$ (max) $0 < V_{CCIO} < V_{CCIO}$ (max) $0 < V_{CCAUX} < V_{CCAUX}$ (max) | -1.5 | — | 1.5 | mA |

**Notes**:

- I$_{DK}$ is additive to I$_{PU}$, I$_{PD}$, or I$_{BH}$.
- Hot socketing specs are defined at a device junction temperature of 85 °C or below. When the device junction temperature is above 85 °C, the I$_{DK}$ current can exceed the above spec.
- Going beyond the hot socketing ranges specified here will cause exponentially higher Leakage currents and potential reliability issues. A total of 64 mA per 8 I/O should not be exceeded.

## 3.7. ESD Performance

Refer to the LIFCL-33/33U Product Family Qualification Summary for complete Commercial and Industrial grade qualification data, including ESD performance.

## 3.8. DC Electrical Characteristics

**Table 3.7. DC Electrical Characteristics – Wide Range**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1] | Input or I/O Leakage current (Commercial/Industrial) | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 10 | μA |
| $I_{IH}$[2] | Input or I/O Leakage current | $V_{CCIO} \le V_{IN} \le V_{IH}$ (max) | — | — | 100 | μA |
| $I_{PU}$ | I/O Weak Pull-up Resistor Current | $0 \le V_{IN} \le 0.7 \times V_{CCIO}$ | -30 | — | -150 | μA |
| $I_{PD}$ | I/O Weak Pull-down Resistor Current | $V_{IL}$ (max) $\le V_{IN} \le V_{CCIO}$ | 30 | — | 150 | μA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (max) | 30 | — | | μA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7 \times V_{CCIO}$ | -30 | — | | μA |
| $I_{BHLO}$ | Bus hold low Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 150 | μA |
| $I_{BHHO}$ | Bus hold high Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | -150 | μA |
| $V_{BHT}$ | Bus Hold Trip Points | — | $V_{IL}$ (max) | — | $V_{IH}$ (min) | V |

**Notes**:
1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tristated. Bus Maintenance circuits are disabled.
2. The input leakage current $I_{IH}$ is the worst-case input leakage per GPIO when the pad signal is high and also higher than the bank $V_{CCIO}$. This is considered a mixed mode input.

**Table 3.8. DC Electrical Characteristics – High Speed**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1] | Input or I/O Leakage | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 10 | μA |
| $I_{PU}$ | I/O Weak Pull-up Resistor Current | $0 \le V_{IN} \le 0.7 \times V_{CCIO}$ | -30 | — | -150 | μA |
| $I_{PD}$ | I/O Weak Pull-down Resistor Current | $V_{IL}$ (max) $\le V_{IN} \le V_{CCIO}$ | 30 | — | 150 | μA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (max) | 30 | — | — | μA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7 \times V_{CCIO}$ | -30 | — | — | μA |
| $I_{BHLO}$ | Bus hold low Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 150 | μA |
| $I_{BHHO}$ | Bus hold high Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | -150 | μA |
| $V_{BHT}$ | Bus Hold Trip Points | — | $V_{IL}$ (max) | — | $V_{IH}$ (min) | V |

**Note:**
1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tri-stated. Bus Maintenance circuits are disabled.

**Table 3.9. Capacitors – Wide Range**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_1$[1] | I/O Capacitance[1] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2V | — | 6 | — | pF |
| $C_2$[1] | Dedicated Input Capacitance[1] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2V | — | 6 | — | pF |

**Note**:
1. $T_A$ = 25 °C, f = 1.0 MHz.

**Table 3.10. Capacitors – High Performance**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| $C_1{}^1$ | I/O Capacitance[1] | $V_{CCIO}$ = 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2V | — | 6 | — | pF |
| $C_2{}^1$ | Dedicated Input Capacitance[1] | $V_{CCIO}$ = 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2V | — | 6 | — | pF |
| $C_3{}^1$ | D-PHY I/O Capacitance | $V_{CCA\_D\text{-}PHY}$ = 1.8 V, $V_{CC}$ = typ., $V_{IO}$ = 0 to $V_{CCA\_D\text{-}PHY}$ + 0.2V | — | 5 | — | pF |

**Note:**
1.    $T_A$ = 25 °C, f = 1.0 MHz.

**Table 3.11. Single Ended Input Hysteresis – Wide Range**

| IO_TYPE | VCCIO | TYP Hysteresis |
|---------|-------|----------------|
| LVCMOS33 | 3.3 V | 250 mV |
| LVCMOS25 | 3.3 V | 200 mV |
|  | 2.5 V | 250 mV |
| LVCMOS18 | 1.8 V | 180 mV |
| LVCMOS15 | 1.5 V | 50 mV |
| LVCMOS12 | 1.2 V | 0 |
| LVCMOS10 | 1.2 V | 0 |

**Table 3.12. Single Ended Input Hysteresis – High Performance**

| IO_TYPE | VCCIO | TYP Hysteresis |
|---------|-------|----------------|
| LVCMOS18H | 1.8 V | 180 mV |
| LVCMOS15H | 1.8 V | 50 mV |
|  | 1.5 V | 150 mV |
| LVCMOS12H | 1.2 V | 0 |
| LVCMOS10H | 1.0 V | 0 |
| MIPI-LP-RX | 1.2 V | >25 mV |

## 3.9.    Supply Currents

For estimating and calculating current, use Power Calculator in the Lattice Design software.

This operating and peak current is design dependent and can be calculated in the Lattice Design software. Some blocks can be placed into low current standby modes. Refer to Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075).

## 3.10. sysI/O Recommended Operating Conditions

**Table 3.13. sysI/O Recommended Operating Conditions**

| Standard | Support Banks | $V_{CCIO}$ (Input) Typ. | $V_{CCIO}$ (Output) Typ. |
|---|---|---|---|
| **Single-Ended** | | | |
| LVCMOS33 | 0, 1, 5 | 3.3 | 3.3 |
| LVTTL33 | 0, 1, 5 | 3.3 | 3.3 |
| LVCMOS25[1, 2] | 0, 1, 5 | 2.5, 3.3 | 2.5 |
| LVCMOS18[1, 2] | 0, 1, 5 | 1.2, 1.5, 1.8, 2.5, 3.3 | 1.8 |
| LVCMOS18H | 2, 3, 4 | 1.8 | 1.8 |
| LVCMOS15[1, 2] | 0, 1, 5 | 1.2, 1.5, 1.8, 2.5, 3.3 | 1.5 |
| LVCMOS15H[1] | 2, 3, 4 | 1.5, 1.8 | 1.5 |
| LVCMOS12[1, 2] | 0, 1, 5 | 1.2, 1.5, 1.8, 2.5, 3.3 | 1.2 |
| LVCMOS12H[1] | 2, 3, 4 | 1.2, 1.35, 1.5, 1.8 | 1.2 |
| LVCMOS10[1] | 0, 1, 5 | 1.2, 1.5, 1.8, 2.5, 3.3 | — |
| LVCMOS10H[1] | 2, 3, 4 | 1.0, 1.2, 1.35, 1.5, 1.8 | 1.0 |
| LVCMOS10R[1] | 2, 3, 4 | 1.0, 1.2, 1.35, 1.5, 1.8 | — |
| HSTL15_I[3] | 2, 3, 4 | 1.5[7] | 1.5[7] |
| MIPI D-PHY LP Input[6] | 2, 3, 4 | 1.2 | 1.2 |
| **Differential[6]** | | | |
| LVDS | 2, 3, 4 | 1.2, 1.35, 1.5, 1.8 | 1.8 |
| LVDSE[5] | 0, 1, 5 | — | 2.5 |
| subLVDS | 2, 3, 4 | 1.2, 1.35, 1.5, 1.8 | — |
| subLVDSE[5] | 0, 1, 5 | — | 1.8 |
| subLVDSEH[5] | 2, 3, 4 | — | 1.8 |
| SLVS[6] | 2, 3, 4 | 1.0, 1.2, 1.35, 1.5, 1.8[4] | 1.2, 1.35, 1.5, 1.8 [4] |
| MIPI_DPHY[6] | 2, 3, 4 | 1.2 | 1.2 |
| LVCMOS33D[5] | 0, 1, 5 | — | 3.3 |
| LVTTL33D[5] | 0, 1, 5 | — | 3.3 |
| LVCMOS25D[5] | 0, 1, 5 | — | 2.5 |
| HSTL15D_I[5] | 2, 3, 4 | — | 1.5 |

**Notes**:
1. Single-ended input can mix into I/O Banks with $V_{CCIO}$ different from the standard requires due to some of these input standards use internal supply voltage source ($V_{CC}$, $V_{CCAUX}$) to power the input buffer, which makes them to be independent of $V_{CCIO}$ voltage. For more details, please refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067). The following is a brief guideline to follow:
   a. Weak pull-up on the I/O must be set to OFF.
   b. Bank 2, Bank 3, and Bank 4 I/O can only mix into banks with $V_{CCIO}$ higher than the pin standard, due to clamping diode on the pin in these banks. Bank 0 and Bank 1 does not have this restriction.
   c. LVCMOS25 uses $V_{CCIO}$ supply on input buffer in Bank 0, Bank 1, and Bank 5. It can be supported with $V_{CCIO}$ = 3.3 V to meet the $V_{IH}$ and $V_{IL}$ requirements, but there is additional current drawn on $V_{CCIO}$. Hysteresis has to be disabled when using 3.3 V supply voltage.
   d. LVCMOS15 uses $V_{CCIO}$ supply on input buffer in Bank 2, Bank 3, and Bank 4. It can be supported with $V_{CCIO}$ = 1.8 V to meet the $V_{IH}$ and $V_{IL}$ requirements, but there is additional current drawn on $V_{CCIO}$.
2. Single-ended LVCMOS inputs can mixed into I/O Banks with different $V_{CCIO}$, providing weak pull-up is not used.
   For additional information on Mixed I/O in Bank $V_{CCIO}$, refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067).
3. These inputs use differential input comparator in Bank 2, Bank 3, and Bank 4. The differential input comparator uses $V_{CCAUXH}$ power supply. These inputs require the $V_{REF}$ pin to provide the reference voltage in the Bank. Refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067) for details.
4. All differential inputs use differential input comparator in Bank 2, Bank 3, and Bank 4. The differential input comparator uses $V_{CCAUXH}$ power supply. There is no differential input signaling supported in Bank 0, Bank 1, and Bank 5.

5. These outputs are emulating differential output pair with single-ended output drivers with true and complement outputs driving on each of the corresponding true and complement output pair pins. The common mode voltage, $V_{CM}$, is ½ × $V_{CCIO}$. Refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067) for details.

6. Soft MIPI D-PHY HS using sysI/O is supported with SLVS input and output that can be placed in banks with $V_{CCIO}$ voltage shown in SLVS. D-PHY with HS and LP modes supported needs to be placed in banks with $V_{CCIO}$ voltage = 1.2 V. Soft MIPI D-PHY LP input and output using sysI/O are supported with LVCMOS12.

7. LVCMOS15 input uses $V_{CCIO}$ supply voltage. If $V_{CCIO}$ is 1.8 V, the DC levels for LVCMOS15 are still met, but there could be increase in input buffer current.

## 3.11. sysI/O Single-Ended DC Electrical Characteristics[3]

**Table 3.14. sysI/O DC Electrical Characteristics – Wide Range I/O**

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$(mA) | $I_{OH}$(mA) |
|---|---|---|---|---|---|---|---|---|
| | Min (V) | Max (V) | Min (V) | Max (V) | | | | |
| LVTTL33 LVCMOS33 | — | 0.8 | 2.0 | 3.465[4] | 0.4 | $V_{CCIO}$ − 0.4 | 2, 4, 8, 12, "50RS"[3] | -2, -4, -8, -12, "50RS"[3] |
| | | | | | 0.48 | $V_{CCIO}$ − 0.52 | 16 | -16 |
| LVCMOS25 | — | 0.7 | 1.7 | 3.465[4] | 0.4 | $V_{CCIO}$ − 0.45 | 2, 4, 8, | -2, -4, -8 |
| | | | | | | $V_{CCIO}$ − 0.60 | 10 | -10 |
| | | | | | | $V_{CCIO}$ − 0.64 | "50RS"[3] | "50RS"[3] |
| LVCMOS18 | — | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | 3.465[4] | 0.4 | $V_{CCIO}$ − 0.45 | 2, 4, 8, "50RS"[3] | -2, -4, -8, "50RS"[3] |
| LVCMOS15 | — | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | 3.465[4] | 0.4 | $V_{CCIO}$ − 0.4 | 2, 4 | -2, -4 |
| LVCMOS12 | — | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | 3.465[4] | 0.4 | $V_{CCIO}$ − 0.4 | 2, 4 | -2, -4 |
| LVCMOS10 | — | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | 3.465[4] | No O/P Support | | | |

**Notes**:

1. For electro-migration, the average DC current drawn by the I/O pads within a bank of I/O shall not exceed 10 mA per I/O average.
2. For the types of I/O standard supported in which bank, refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067) for details.
3. Select "50RS" in driver strength is selecting 50 Ω series impedance driver.
4. $V_{IH}$ (MAX) for inputs on these standards (in Bank 0, Bank 1, and Bank 5) can go up to 3.465 V if the input clamp is OFF. Otherwise, the input cannot be higher than VCCIO + 0.3 V.

**Table 3.15. sysI/O DC Electrical Characteristics – High Performance I/O[3]**

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min (V) | Max (V) | Min (V) | Max (V) | | | | |
| LVCMOS18H | — | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | 0.4 | $V_{CCIO} - 0.45$ | 2, 4, 8, 12, "50RS"[3] | -2, -4, -8, -12, "50RS"[3] |
| LVCMOS15H | — | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | 0.4 | $V_{CCIO} - 0.4$ | 2, 4, 8, "50RS"[3] | -2, -4, -8, "50RS"[3] |
| LVCMOS12H | — | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | 0.4 | $V_{CCIO} - 0.4$ | 2, 4, 8, "50RS"[3] | -2, -4, -8, "50RS"[3] |
| LVCMOS10H | — | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.27 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2, 4 | -2, -4 |
| HSTL15_I | — | $V_{REF} - 0.10$ | $V_{REF} + 0.15$ | $V_{CCIO} + 0.3$ | 0.40 | $V_{CCIO} - 0.40$ | 8 | −8 |
| LVCMOS10R | — | $V_{REF} - 0.10$ | $V_{REF} + 0.10$ | $V_{CCIO} + 0.3$ | — | — | — | — |

**Notes**:
1. For electro-migration, the average DC current drawn by the I/O pads within a bank of I/O shall not exceed 10 mA per I/O average.
2. For the types of I/O standard supported in which bank, refer to sysI/O User Guide for Nexus Platform (FPGA-TN-02067) for details.
3. Select "50RS" in driver strength is selecting 50 Ω series impedance driver.

**Table 3.16. I/O Resistance Characteristics**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 50RS | Output Drive Resistance when 50RS Drive Strength Selected | $V_{CCIO}$ = 1.8 V, 2.5 V, or 3.3 V | — | 50 | — | Ω |
| $R_{DIFF}$ | Input Differential Termination Resistance | Bank 2, Bank 3, and Bank 4 for I/O selected to be differential | — | 100 | — | Ω |
| SE Input Termination | Input Single Ended Termination Resistance | Bank 2, Bank 3, and Bank 4 for I/O selected to be Single Ended | 36 | 40 | 64 | Ω |
| | | | 46 | 50 | 80 | |
| | | | 56 | 60 | 96 | |
| | | | 67 | 75 | 120 | |

**Table 3.17. V$_{IN}$ Maximum Overshoot/Undershoot Allowance – Wide Range[1, 2]**

| AC Voltage Overshoot | % of UI at –40 °C to 100 °C | AC Voltage Undershoot | % of UI at –40 °C to 100 °C |
|---|---|---|---|
| V$_{CCIO}$ + 0.4 | 100.0% | -0.4 | 100.0% |
| V$_{CCIO}$ + 0.5 | 100.0% | -0.5 | 44.2% |
| V$_{CCIO}$ + 0.6 | 94.0% | -0.6 | 10.1% |
| V$_{CCIO}$ + 0.7 | 21.0% | -0.7 | 1.3% |
| V$_{CCIO}$ + 0.8 | 10.2% | -0.8 | 0.3% |
| V$_{CCIO}$ + 0.9 | 2.5% | -0.9 | 0.1% |

**Notes:**
1. The peak overshoot or undershoot voltage and the duration above V$_{CCIO}$ + 0.2 V or below GND – 0.2 V must not exceed the values in this table.
2. For UI less than 20 µs.

**Table 3.18. V$_{IN}$ Maximum Overshoot/Undershoot Allowance – High Performance[1, 2]**

| AC Voltage Overshoot | % of UI at –40 °C to 100 °C | AC Voltage Undershoot | % of UI at –40 °C to 100 °C |
|---|---|---|---|
| V$_{CCIO}$ + 0.5 | 100.0% | -0.5 | 100.0% |
| V$_{CCIO}$ + 0.6 | 47.3% | -0.6 | 47.3% |
| V$_{CCIO}$ + 0.7 | 10.9% | -0.7 | 10.9% |
| V$_{CCIO}$ + 0.8 | 2.7% | -0.8 | 2.7% |
| V$_{CCIO}$ + 0.9 | 0.7% | -0.9 | 0.7% |

**Notes:**
1. The peak overshoot or undershoot voltage and the duration above V$_{CCIO}$ + 0.2 V or below GND – 0.2 V must not exceed the values in this table.
2. For UI, less than 20 µs.

# 3.12. sysI/O Differential DC Electrical Characteristics

### 3.12.1. LVDS

LVDS input buffer on LIFCL-33/33U is powered by V$_{CCAUX}$ = 1.8 V, and protected by the bank V$_{CCIO}$. Therefore, the LVDS input voltage cannot exceed the bank V$_{CCIO}$ voltage. LVDS output buffer is powered by the Bank V$_{CCIO}$ at 1.8 V.

LVDS can only be supported in Bank 2, Bank 3, and Bank 4. LVDS25 output can be emulated with LVDS25E in Bank 0, Bank 1, and Bank 5. This is described in LVDS25E (Output Only) section.

**Table 3.19. LVDS DC Electrical Characteristics[1]**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| V$_{INP}$, V$_{INM}$ | Input Voltage | — | 0 | — | 1.60[3] | V |
| V$_{ICM}$ | Input Common Mode Voltage | Half the sum of the two Inputs | 0.05 | — | 1.55 [2] | V |
| V$_{THD}$ | Differential Input Threshold | Difference between the two Inputs | ±100 | — | — | mV |
| I$_{IN}$ | Input Current | Power On or Power Off | — | — | ±10 | µA |
| V$_{OH}$ | Output High Voltage for V$_{OP}$ or V$_{OM}$ | R$_T$ = 100 Ω | — | 1.425 | 1.60 | V |
| V$_{OL}$ | Output Low Voltage for V$_{OP}$ or V$_{OM}$ | R$_T$ = 100 Ω | 0.9 V | 1.075 | — | V |
| V$_{OD}$ | Output Voltage Differential | (V$_{OP}$ - V$_{OM}$), R$_T$ = 100 Ω | 250 | 350 | 450 | mV |
| ΔV$_{OD}$ | Change in V$_{OD}$ Between High and Low | — | — | — | 50 | mV |
| V$_{OCM}$ | Output Common Mode Voltage | (V$_{OP}$ + V$_{OM}$)/2, R$_T$ = 100 Ω | 1.125 | 1.25 | 1.375 | V |
| ΔV$_{OCM}$ | Change in V$_{OCM}$, V$_{OCM(MAX)}$ - V$_{OCM(MIN)}$ | — | — | — | 50 | mV |
| I$_{SAB}$ | Output Short Circuit Current | V$_{OD}$ = 0 V Driver outputs shorted to each other | — | — | 12 | mA |
| ΔV$_{OS}$ | Change in V$_{OS}$ between H and L | — | — | — | 50 | mV |

**Notes**:
1. LVDS input or output are supported in Bank 2, Bank 3, and Bank 4. LVDS input uses $V_{CCAUX}$ on the differential input comparator and can be in any $V_{CCIO}$ voltage bank. LVDS output uses $V_{CCIO}$ on the differential output driver, and can only be in bank with $V_{CCIO} = 1.8$ V.
2. $V_{ICM}$ is depending on VID, input differential voltage, so the voltage on pin cannot exceed $V_{INP/\ INM\ (min/max)}$ requirements. $V_{ICM(min)} = V_{INP/INM(min)} + \frac{1}{2} V_{ID}$, $V_{ICM(max)} = V_{INP/INM\ (max)} - \frac{1}{2} V_{ID}$. Values in the table is based on minimum $V_{ID}$ of +/- 100 mV.
3. $V_{INP}$ and $V_{INM}$ (max) must be less than or equal to $V_{CCIO}$ in all cases.

## 3.12.2. LVDS25E (Output Only)

The top side of the LIFCL-33/33U devices support LVDS25 outputs with emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.2 is one possible solution for point-to-point signals.

**Table 3.20. LVDS25E DC Conditions**

| Parameter | Description | Typical | Unit |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (±5%) | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 20 | Ω |
| $R_S$ | Driver Series Resistor (±1%) | 158 | Ω |
| $R_P$ | Driver Parallel Resistor (±1%) | 140 | Ω |
| $R_T$ | Receiver Termination (±1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage | 1.43 | V |
| $V_{OL}$ | Output Low Voltage | 1.07 | V |
| $V_{OD}$ | Output Differential Voltage | 0.35 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | V |
| $Z_{BACK}$ | Back Impedance | 100.5 | Ω |
| $I_{DC}$ | DC Output Current | 6.03 | mA |
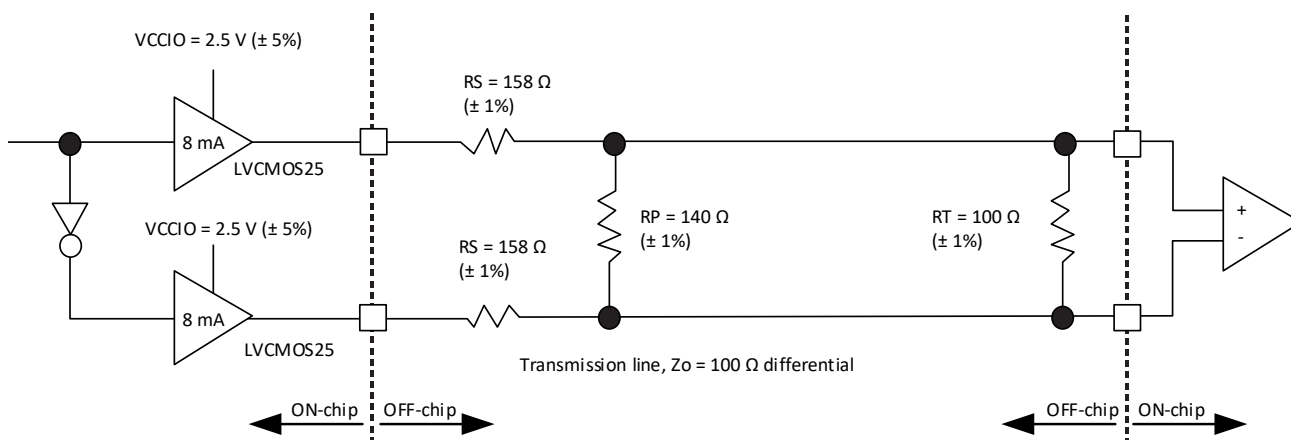


**Figure 3.2. LVDS25E Output Termination Example**

### 3.12.3. SubLVDS (Input Only)

SubLVDS is a reduced-voltage form of LVDS signaling, very similar to LVDS. It is a standard used in many camera types of applications. Being similar to LVDS, the LIFCL-33/33U devices can support the subLVDS input signaling with the same LVDS input buffer. The output for subLVDS is implemented in subLVDSE/subLVDSEH with a pair of LVCMOS18 output drivers (see SubLVDSE/SubLVDSEH (Output Only) section).

**Table 3.21. SubLVDS Input DC Electrical Characteristics (Over Recommended Operating Conditions)**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ID}$ | Input Differential Threshold Voltage | Over $V_{ICM}$ range | 70 | 150 | 200 | mV |
| $V_{ICM}$ | Input Common Mode Voltage | Half the sum of the two Inputs | 0.4 | 0.9 | 1.4[1] | V |

**Note:**

1. $V_{ICM}$ + 1/2 $V_{ID}$ cannot exceed the bank $V_{CCIO}$ in all cases.
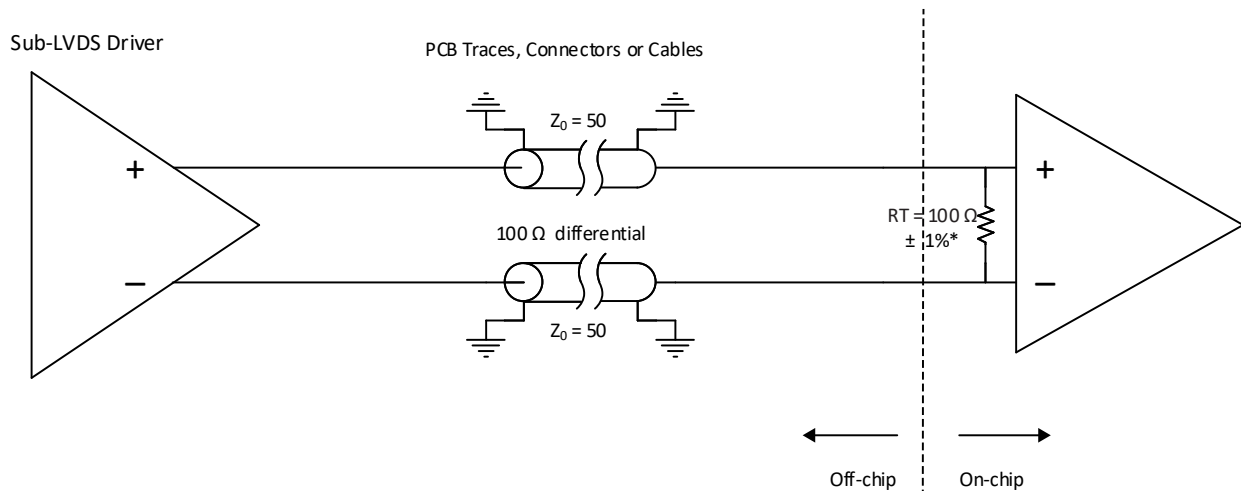


**Figure 3.3. SubLVDS Input Interface**

### 3.12.4. SubLVDSE/SubLVDSEH (Output Only)

SubLVDS output uses a pair of LVCMOS18 drivers with True and Complement outputs. The VCCIO of the bank used for subLVDSE or subLVDSEH needs to be powered by 1.8V. SubLVDSE is for Bank 0, Bank 1, and Bank 5; and subLVDSEH is for Bank 2, Bank 3, and Bank 4.

Performance of the subLVDSE/subLVDSEH driver is limited to the performance of LVCMOS18.

**Table 3.22. SubLVDS Output DC Electrical Characteristics**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Output Differential Voltage Swing | — | — | 150 | — | mV |
| $V_{OCM}$ | Output Common Mode Voltage | Half the sum of the two Outputs | — | 0.9 | — | V |
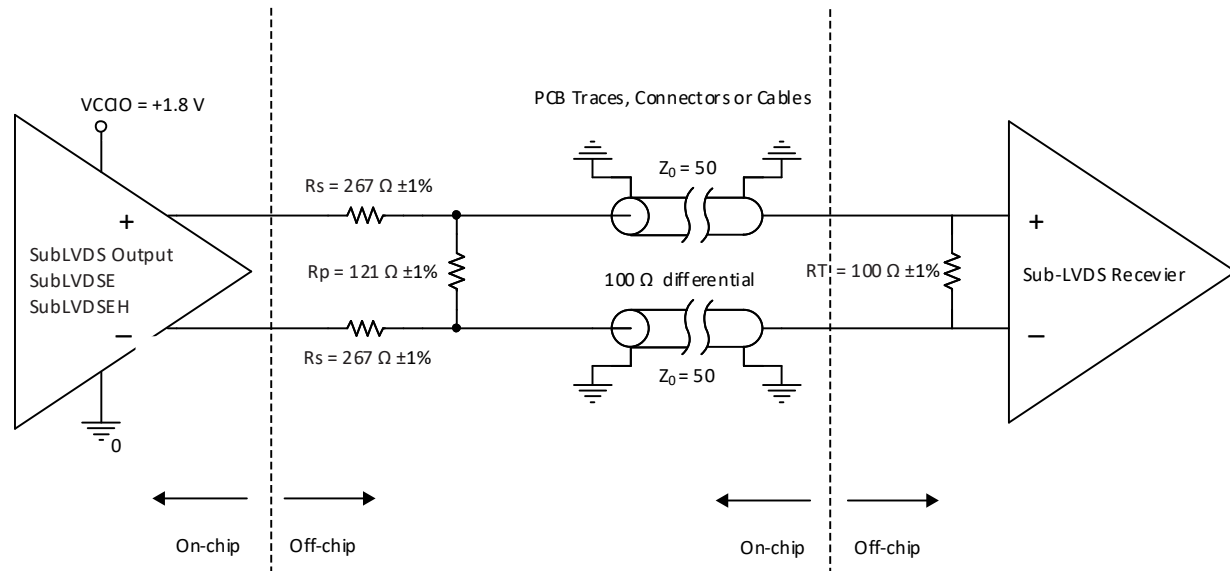
**Figure 3.4. SubLVDS Output Interface**

### 3.12.5. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard with smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The LIFCL-33/33U devices receive SLVS differential input with the LVDS input buffer. This LVDS input buffer is design to cover wide input common mode range that can meet the SLVS input standard specified by the JEDEC standard.

**Table 3.23. SLVS Input DC Characteristics**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ID}$ | Input Differential Threshold Voltage | Over $V_{ICM}$ range | 70 | — | — | mV |
| $V_{ICM}$ | Input Common Mode Voltage | Half the sum of the two Inputs | 70 | 200 | 330 | mV |

The SLVS output on LIFCL-33/33U is supported with the LVDS drivers found in Bank 2, Bank 3, and Bank 4. The LVDS driver on LIFCL-33/33U is a current controlled driver. It can be configured as LVDS driver or configured with the 100 Ω differential termination with center-tap set to $V_{OCM}$ at 200 mV. This means the differential output driver can be placed into bank with $V_{CCIO}$ = 1.2 V, 1.5 V, or 1.8 V, even if it is powered by $V_{CCIO}$.

**Table 3.24. SLVS Output DC Characteristics**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Bank $V_{CCIO}$ | — | -5% | 1.2, 1.5, 1.8 | + 5% | V |
| $V_{OD}$ | Output Differential Voltage Swing | — | 140 | 200 | 270 | mV |
| $V_{OCM}$ | Output Common Mode Voltage | Half the sum of the two Outputs | 150 | 200 | 250 | mV |
| $Z_{OS}$ | Single-Ended Output Impedance | — | 37.5 | 50 | 80 | Ω |
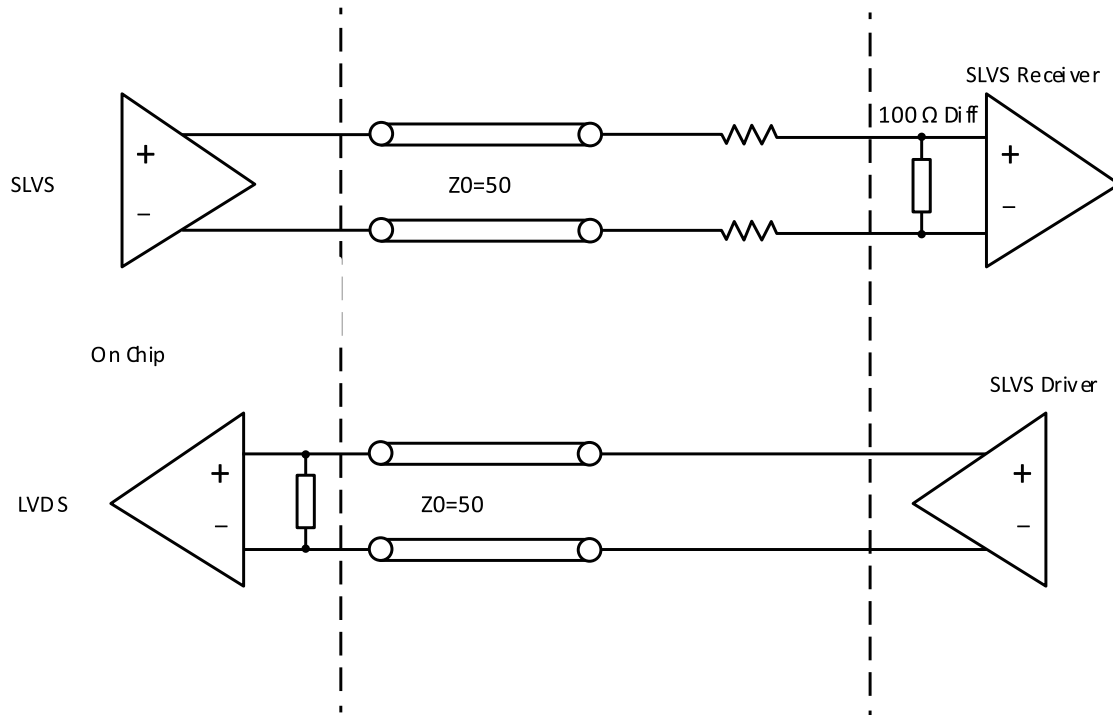
**Figure 3.5. SLVS Interface**

### 3.12.6. Soft MIPI D-PHY

When Soft D-PHY is implemented inside the FPGA logic, the I/O interface needs to use sysI/O buffers to connect to external D-PHY pins.

The LIFCL-33/33U sysI/O provides support for SLVS, as described in SLVS section, plus the LVCMOS12 input / output buffers together to support the High Speed (HS) and Low Power (LP) mode as defined in MIPI Alliance Specification for D-PHY.

To support MIPI D-PHY with SLVS (LVDS) and LVCMOS12, the bank $V_{CCIO}$ cannot be set to 1.5 V or 1.8 V. It has to connect to 1.2 V, or 1.1 V.

All other DC parameters are the same as listed in SLVS section. DC parameters for the LP driver and receiver are the same as listed in LVCMOS12.
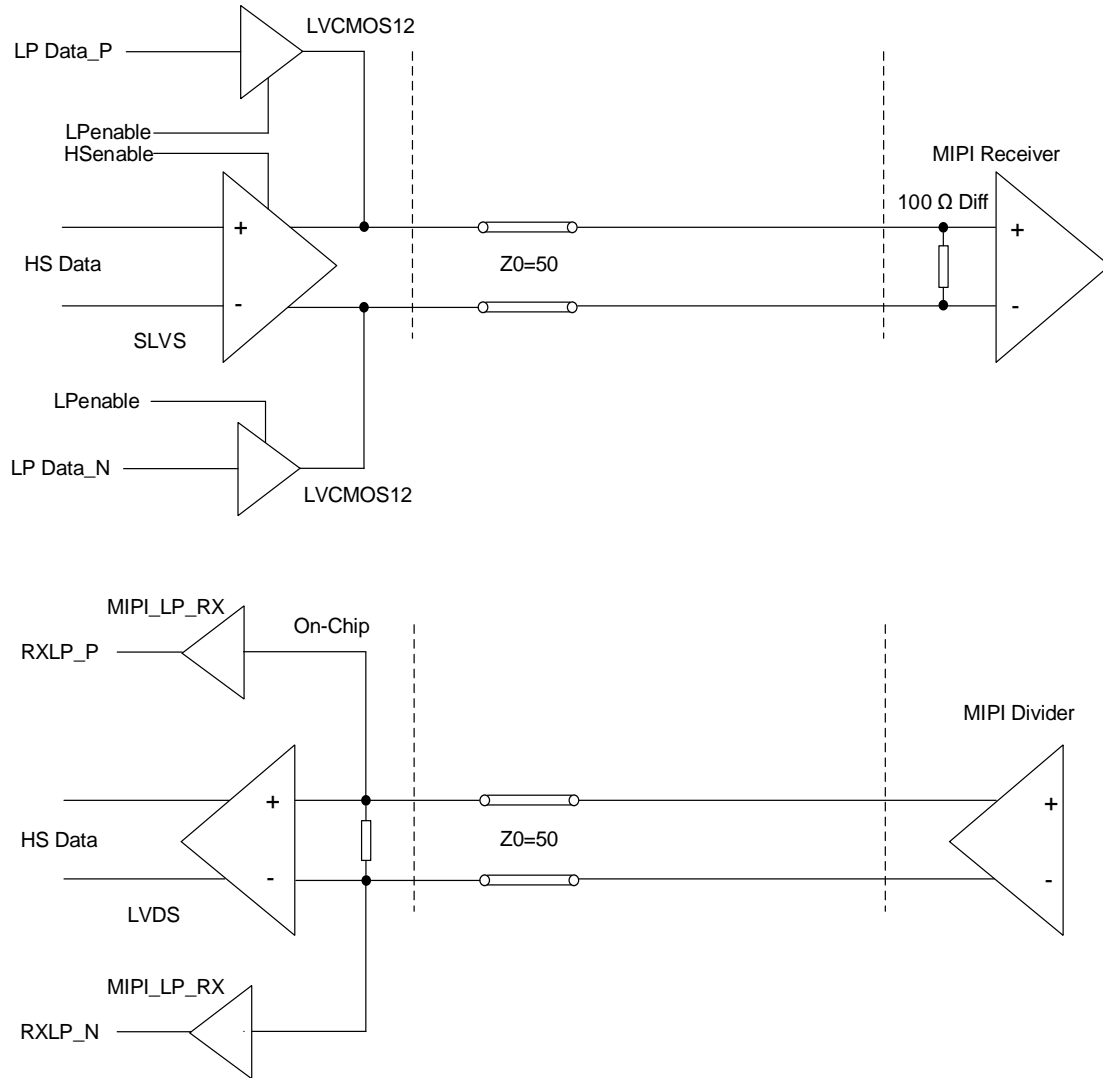
**Figure 3.6. MIPI Interface**

**Table 3.25. Soft D-PHY Input Timing and Levels**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High Speed (Differential) Input DC Specifications | | | | | | |
| $V_{CMRX(DC)}$ | Common-mode Voltage in High-Speed Mode | — | 70 | — | 330 | mV |
| $V_{IDTH}$ | Differential Input HIGH Threshold | — | 70 | — | — | mV |
| $V_{IDTL}$ | Differential Input LOW Threshold | — | — | — | -70 | mV |
| $V_{IHHS}$ | Input HIGH Voltage (for HS mode) | — | — | — | 460 | mV |
| $V_{ILHS}$ | Input LOW Voltage | — | -40 | — | — | mV |
| $V_{TERM-EN}$ | Single-ended voltage for HS Termination Enable[4] | — | — | — | 450 | mV |
| $Z_{ID}$ | Differential Input Impedance | — | 80 | 100 | 125 | Ω |
| High Speed (Differential) Input AC Specifications | | | | | | |
| $\Delta V_{CMRX(HF)}$[1] | Common-mode Interference (>450 MHz) | — | — | — | 100 | mV |
| $\Delta V_{CMRX(LF)}$[2, 3] | Common-mode Interference (50 MHz - 450 MHz) | — | -50 | — | 50 | mV |
| $C_{CM}$ | Common-mode Termination | — | — | — | 60 | pF |
| Low Power (Single-Ended) Input DC Specifications | | | | | | |
| $V_{IH}$ | Low Power Mode Input HIGH Voltage | — | 740 | — | — | mV |
| $V_{IL}$ | Low Power Mode Input LOW Voltage | — | — | — | 480 | mV |
| $V_{IL-ULP}$ | Ultra Low Power Input LOW Voltage | — | — | — | 300 | mV |
| $V_{HYST}$ | Low Power Mode Input Hysteresis | — | 25 | — | — | mV |
| $e_{SPIKE}$ | Input Pulse Rejection | — | — | — | 300 | V·ps |
| $T_{MIN-RX}$ | Minimum Pulse Width Response | — | 20 | — | — | ns |
| $V_{INT}$ | Peak Interference Amplitude | — | — | — | 200 | mV |
| $f_{INT}$ | Interference Frequency | — | 450 | — | — | MHz |

**Notes**:
1. This is peak amplitude of sine wave modulated to the receiver inputs.
2. Input common-mode voltage difference compared to average common-mode voltage on the receiver inputs.
3. Exclude any static ground shift of 50 mV.
4. High Speed Differential $R_{TERM}$ is enabled when both $D_P$ and $D_N$ are below this voltage.

**Table 3.26. Soft D-PHY Output Timing and Levels**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **High Speed (Differential) Output DC Specifications** | | | | | | |
| $V_{CMTX}$ | Common-mode Voltage in High Speed Mode | — | 150 | 200 | 250 | mV |
| $|\Delta V_{CMTX(1,0)}|$ | $V_{CMTX}$ Mismatch Between Differential HIGH and LOW | — | — | — | 5 | mV |
| $|V_{OD}|$ | Output Differential Voltage | $|$D-PHY-P − D-PHY-N$|$ | 140 | 200 | 270 | mV |
| $|\Delta V_{OD}|$ | $V_{OD}$ Mismatch Between Differential HIGH and LOW | — | — | — | 10 | mV |
| $V_{OHHS}$ | Single-Ended Output HIGH Voltage | — | — | — | 360 | mV |
| $Z_{OS}$ | Single Ended Output Impedance | — | 37.5 | 50 | 80 | Ω |
| $\Delta Z_{OS}$ | $Z_{OS}$ mismatch | — | — | — | 20 | % |
| **High Speed (Differential) Output AC Specifications** | | | | | | |
| $\Delta V_{CMTX(LF)}$ | Common-Mode Variation, 50 MHz–450 MHz | — | — | — | 25 | mV$_{RMS}$ |
| $\Delta V_{CMTX(HF)}$ | Common-Mode Variation, above 450 MHz | — | — | — | 15 | mV$_{RMS}$ |
| $t_R$ | Output 20%–80% Rise Time / Output 80%–20% Fall Time | 0.08 Gbps ≤ $t_R$ ≤ 1.00 Gbps | — | — | 0.30 | UI |
| | | 1.00 Gbps < $t_R$ ≤ 1.50 Gbps | — | — | 0.35 | UI |
| $t_F$ | Output Data Valid After CLK Output | 0.08 Gbps ≤ $t_F$ ≤ 1.00 Gbps | — | — | 0.30 | UI |
| | | 1.00 Gbps < $t_F$ ≤ 1.50 Gbps | — | — | 0.35 | UI |
| **Low Power (Single-Ended) Output DC Specifications** | | | | | | |
| $V_{OH}$ | Low Power Mode Output HIGH Voltage | 0.08 Gbps – 1.5 Gbps | 1.07 | 1.2 | 1.3 | V |
| $V_{OL}$ | Low Power Mode Input LOW Voltage | — | -50 | — | 50 | mV |
| $Z_{OLP}$ | Output Impedance in Low Power Mode | — | 110 | — | — | Ω |
| **Low Power (Single-Ended) Output AC Specifications** | | | | | | |
| $t_{RLP}$ | 15%–85% Rise Time | — | — | — | 25 | ns |
| $t_{FLP}$ | 85%–15% Fall Time | — | — | — | 25 | ns |
| $t_{REOT}$ | HS – LP Mode Rise and Fall Time, 30%–85% | — | — | — | 35 | ns |
| $T_{LP-PULSE-TX}$ | Pulse Width of the LP Exclusive-OR Clock | First LP XOR Clock Pulse after STOP State or Last Pulse before STOP State | 40 | — | — | ns |
| | | All Other Pulses | 20 | — | — | ns |
| $T_{LP-PER-TX}$ | Period of the LP Exclusive-OR Clock | — | 90 | — | — | ns |
| $C_{LOAD}$ | Load Capacitance | — | 0 | — | 70 | pF |

**Table 3.27. Soft D-PHY Clock Signal Specification**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Clock Signal Specification** | | | | | | |
| UI Instantaneous | $UI_{INST}$ | — | — | — | 12.5 | ns |
| UI Variation | $\Delta UI$ | — | -10% | — | 10% | UI |
| | | — | -5% | — | 5% | UI |

**Table 3.28. Soft D-PHY Data-Clock Timing Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Data-Clock Timing Specifications** | | | | | | |
| $T_{SKEW[TX]}$ | Data to Clock Skew | 0.08 Gbps ≤ $T_{SKEW[TX]}$ ≤ 1.00 Gbps | -0.15 | — | 0.15 | $UI_{INST}$ |
| | | 1.00 Gbps < $T_{SKEW[TX]}$ ≤ 1.50 Gbps | -0.20 | — | 0.20 | $UI_{INST}$ |
| $T_{SKEW[TLIS]}$ | Data to Clock Skew | 0.08 Gbps ≤ $T_{SKEW[TLIS]}$ ≤ 1.00 Gbps | -0.20 | — | 0.20 | $UI_{INST}$ |
| | | 1.00 Gbps < $T_{SKEW[TLIS]}$ ≤ 1.50 Gbps | -0.10 | — | 0.10 | $UI_{INST}$ |
| $T_{SETUP[RX]}$ | Input Data Setup Before CLK | 0.08 Gbps ≤ $T_{SETUP[RX]}$ ≤ 1.00 Gbps | 0.15 | — | — | UI |
| | | 1.00 Gbps < $T_{SETUP[RX]}$ ≤ 1.50 Gbps | 0.20 | — | — | UI |
| $T_{HOLD[RX]}$ | Input Data Hold After CLK | 0.08 Gbps ≤ $T_{HOLD[RX]}$ ≤ 1.00 Gbps | 0.15 | — | — | UI |
| | | 1.00 Gbps < $T_{HOLD[RX]}$ ≤ 1.50 Gbps | 0.20 | — | — | UI |

### 3.12.7.  Differential HSTL15D (Output Only)

Differential HSTL outputs are implemented as a pair of complementary single-ended HSTL outputs.

### 3.12.8.   Differential LVCMOS25D, LVCMOS33D, LVTTL33D (Output Only)

Differential LVCMOS and LVTTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output drive strengths are supported.

## 3.13. Maximum sysI/O Buffer Speed

Over recommended operating conditions.

**Table 3.29. Maximum I/O Buffer Speed[1, 2, 3, 4, 7]**

| Buffer | Description | Banks | Max | Unit |
|---|---|---|---|---|
| **Maximum sysI/O Input Frequency** | | | | |
| **Single-Ended** | | | | |
| LVCMOS33 | LVCMOS33, $V_{CCIO}$ = 3.3 V | 0, 1, 5 | 200 | MHz |
| LVTTL33 | LVTTL33, $V_{CCIO}$ = 3.3 V | 0, 1, 5 | 200 | MHz |
| LVCMOS25 | LVCMOS25, $V_{CCIO}$ = 2.5 V | 0, 1, 5 | 200 | MHz |
| LVCMOS18 [5] | LVCMOS18, $V_{CCIO}$ = 1.8 V | 0, 1, 5 | 200 | MHz |
| LVCMOS18H | LVCMOS18, $V_{CCIO}$ = 1.8 V | 2, 3, 4 | 200 | MHz |
| LVCMOS15 [5] | LVCMOS15, $V_{CCIO}$ = 1.5 V | 0, 1, 5 | 100 | MHz |
| LVCMOS15H [5] | LVCMOS15, $V_{CCIO}$ = 1.5 V | 2, 3, 4 | 150 | MHz |
| LVCMOS12 [5] | LVCMOS12, $V_{CCIO}$ = 1.2 V | 0, 1, 5 | 50 | MHz |
| LVCMOS12H [5] | LVCMOS12, $V_{CCIO}$ = 1.2 V | 2, 3, 4 | 100 | MHz |
| LVCMOS10 [5] | LVCMOS 1.0, $V_{CCIO}$ = 1.2 V | 0, 1, 5 | 50 | MHz |
| LVCMOS10H [5] | LVCMOS 1.0, $V_{CCIO}$ = 1.0 V | 2, 3, 4 | 50 | MHz |
| LVCMOS10R | LVCMOS 1.0, $V_{CCIO}$ independent | 2, 3, 4 | 50 | MHz |
| HSTL15 | HSTL15, $V_{CCIO}$ = 1.5 V | 2, 3, 4 | 250 | Mbps |
| MIPI D-PHY (LP Mode) | MIPI, Low Power Mode, $V_{CCIO}$ = 1.2 V | 2, 3, 4 | 10 | Mbps |
| **Differential[8]** | | | | |
| LVDS | LVDS, $V_{CCIO}$ independent | 2, 3, 4 | 1250 | Mbps |
| subLVDS | subLVDS, $V_{CCIO}$ independent | 2, 3, 4 | 1250 | Mbps |
| SLVS | SLVS similar to MIPI HS, $V_{CCIO}$ independent | 2, 3, 4 | 1250 | Mbps |
| MIPI D-PHY (HS Mode) | MIPI, High Speed Mode, $V_{CCIO}$ = 1.2 V | 2, 3, 4 | 1250 | Mbps |
| HSTL15D | Differential HSTL15, $V_{CCIO}$ independent | 2, 3, 4 | 250 | Mbps |
| **Maximum sysI/O Output Frequency** | | | | |
| **Single-Ended** | | | | |
| LVCMOS33 (all drive strengths) | LVCMOS33, $V_{CCIO}$ = 3.3 V | 0, 1, 5 | 200 | MHz |
| LVCMOS33 (RS50) | LVCMOS33, $V_{CCIO}$ = 3.3 V, $R_{SERIES}$ = 50 Ω | 0, 1, 5 | 200 | MHz |
| LVTTL33 (all drive strengths) | LVTTL33, $V_{CCIO}$ = 3.3 V | 0, 1, 5 | 200 | MHz |
| LVTTL33 (RS50) | LVTTL33, $V_{CCIO}$ = 3.3 V, $R_{SERIES}$ = 50 Ω | 0, 1, 5 | 200 | MHz |
| LVCMOS25 (all drive strengths) | LVCMOS25, $V_{CCIO}$ = 2.5 V | 0, 1, 5 | 200 | MHz |
| LVCMOS25 (RS50) | LVCMOS25, $V_{CCIO}$ = 2.5 V, $R_{SERIES}$ = 50 Ω | 0, 1, 5 | 200 | MHz |
| LVCMOS18 (all drive strengths) | LVCMOS18, $V_{CCIO}$ = 1.8 V | 0, 1, 5 | 200 | MHz |
| LVCMOS18 (RS50) | LVCMOS18, $V_{CCIO}$ = 1.8 V, $R_{SERIES}$ = 50 Ω | 0, 1, 5 | 200 | MHz |
| LVCMOS18H (all drive strengths) | LVCMOS18, $V_{CCIO}$ = 1.8 V | 2, 3, 4 | 200 | MHz |
| LVCMOS18H (RS50) | LVCMOS18, $V_{CCIO}$ = 1.8 V, $R_{SERIES}$ = 50 Ω | 2, 3, 4 | 200 | MHz |
| LVCMOS15 (all drive strengths) | LVCMOS15, $V_{CCIO}$ = 1.5 V | 0, 1, 5 | 100 | MHz |
| LVCMOS15H (all drive strengths) | LVCMOS15, $V_{CCIO}$ = 1.5 V | 2, 3, 4 | 150 | MHz |
| LVCMOS12 (all drive strengths) | LVCMOS12, $V_{CCIO}$ = 1.2 V | 0, 1, 5 | 50 | MHz |
| LVCMOS12H (all drive strengths) | LVCMOS12, $V_{CCIO}$ = 1.2 V | 2, 3, 4 | 100 | MHz |
| LVCMOS10H (all drive strengths) | LVCMOS12, $V_{CCIO}$ = 1.2 V | 2, 3, 4 | 50 | MHz |
| HSTL15 | HSTL15, $V_{CCIO}$ = 1.5 V | 2, 3, 4 | 250 | Mbps |
| MIPI D-PHY (LP Mode) | MIPI, Low Power Mode, $V_{CCIO}$ = 1.2 V | 2, 3, 4 | 10 | Mbps |

| Buffer | Description | Banks | Max | Unit |
|---|---|---|---|---|
| **Differential[8]** | | | | |
| LVDS | LVDS, $V_{CCIO}$ = 1.8 V USG84 | 2, 3, 4 | 1250 | Mbps |
| | LVDS, $V_{CCIO}$ = 1.8 V CTG104 | 2, 3, 4 | 1500 | Mbps |
| LVDS25E[6] | LVDS25, Emulated, $V_{CCIO}$ = 2.5 V | 0, 1, 5 | 400 | Mbps |
| SubLVDSE[6] | subLVDS, Emulated, $V_{CCIO}$ = 1.8 V | 0, 1, 5 | 400 | Mbps |
| SubLVDSEH[6] | subLVDS, Emulated, $V_{CCIO}$ = 1.8 V | 2, 3, 4 | 800 | Mbps |
| SLVS | SLVS similar to MIPI, $V_{CCIO}$ = 1.2 V USG84 | 2, 3, 4 | 1250 | Mbps |
| | SLVS similar to MIPI, $V_{CCIO}$ = 1.2 V CTG104 | 2, 3, 4 | 1500 | Mbps |
| MIPI D-PHY (HS Mode) | MIPI, High Speed Mode, $V_{CCIO}$ = 1.2 V USG84 | 2, 3, 4 | 1250 | Mbps |
| | MIPI, High Speed Mode, $V_{CCIO}$ = 1.2 V CTG104 | 2, 3, 4 | 1500 | Mbps |
| HSTL15D | Differential HSTL15, $V_{CCIO}$ = 1.5 V | 2, 3, 4 | 250 | Mbps |

**Notes**:
1. Maximum I/O speed is the maximum switching rate of the I/O operating within the guidelines of the defining standard. The actual interface speed performance using the I/O also depends on other factors, such as internal and external timing.
2. These numbers are characterized but not test on every device.
3. Performance is specified in MHz, as defined in clock rate when the sysI/O is used as pin. For data rate performance, this can be converted to Mbps, which equals to 2 times the clock rate.
4. LVCMOS and LVTTL are measured with load specified in Table 3.42.
5. These LVCMOS inputs can be placed in different $V_{CCIO}$ voltage. Performance may vary. Refer to Lattice Design software.
6. These emulated outputs performance is based on externally properly terminated as described in LVDS25E (Output Only) and SubLVDSE/SubLVDSEH (Output Only).
7. All speeds are measured with fast slew.
8. For maximum differential I/O performance only Differential I/O should be placed in the bottom I/O banks. If this is not possible, the following will impact on maximum performance:
   a. If Fast Slew Rate LVCMOS I/O are used, they should be limited to no more than nine I/O (adjacent), four I/O (same bank), 55 I/O to keep degradation below 50%.
   b. If non-Differential I/O (SLOW SLEW) are placed on the bottom but not within the same bank as differential I/O, then the maximum Differential performance is degraded to 70% of original when 21 aggressors are toggling.
   c. If non-Differential I/O (SLOW SLEW) are placed within the same bank as Differential I/O then the maximum performance is degraded to 50% of original when 16 aggressor are toggling.
   d. No performance impact if MIPI D-PHY LP and MIPI D-PHY HS are in the same bank.
   e. If Differential RX/TX I/O are both placed within the same bank, then the maximum performance is degraded to 90%.

## 3.14. Typical Building Block Function Performance

These building block functions can be generated using Lattice Design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

**Table 3.30. Pin-to-Pin Performance**

| Function | Typ. @ VCC = 1.0 V | Unit |
|---|---|---|
| 16-bit Decoder (I/O configured with LVCMOS18, Top Banks) | 5.5 | ns |
| 16-bit Decoder (I/O configured with HSTL15_I, Bottom Banks) | 5.1 | ns |
| 16:1 Mux (I/O configured with LVCMOS18, Top Banks) | 6 | ns |
| 16:1 Mux (I/O configured with HSTL15_I, Bottom Banks) | 6.1 | ns |

**Note**: These functions are generated using Lattice Radiant Design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

**Table 3.31. Register-to-Register Performance[1, 3, 4]**

| Function | Typ. @ VCC = 1.0 V | Unit |
|---|---|---|
| **Basic Functions** | | |
| 16-bit Adder | 500[2] | MHz |
| 32-bit Adder | 496 | MHz |
| 16-bit Counter | 402 | MHz |
| 32-bit Counter | 371 | MHz |
| **Embedded Memory Functions** | | |
| 512 × 36 Single Port RAM, with Output Register | 500[2] | MHz |
| 1024 × 18 True-Dual Port RAM using same clock, with EBR Output Registers | 500[2] | MHz |
| 1024 × 18 True-Dual Port RAM using asynchronous clocks, with EBR Output Registers | 500[2] | MHz |
| **Large Memory Functions** | | |
| 32k × 32 Single Port RAM, with Output Register | 195 | MHz |
| 32k × 32 Single Port RAM with ECC, with Output Register | 170 | MHz |
| 32k × 32 True-Dual Port RAM using same clock, with Output Registers | 115 | MHz |
| **Distributed Memory Functions** | | |
| 16 × 4 Single Port RAM (One PFU) | 500[2] | MHz |
| 16 × 2 Pseudo-Dual Port RAM (One PFU) | 500[2] | MHz |
| 16 × 4 Pseudo-Dual Port (Two PFUs) | 500[2] | MHz |
| **DSP Functions** | | |
| 9 × 9 Multiplier with Input Output Registers | 376 | MHz |
| 18 × 18 Multiplier with Input/Output Registers | 287 | MHz |
| 36 × 36 Multiplier with Input/Output Registers | 200 | MHz |
| MAC 18 × 18 with Input/Output Registers | 203 | MHz |
| MAC 18 × 18 with Input/Pipelined/Output Registers | 287 | MHz |
| MAC 36 × 36 with Input/Output Registers | 119 | MHz |
| MAC 36 × 36 with Input/Pipelined/Output Registers | 155 | MHz |

**Notes**:
1. The Clock port is configured with LVDS I/O type. Performance Grade: 8_High-Performance_1.0V.
2. Limited by the Minimum Pulse Width of the component.
3. These functions are generated using Lattice Radiant Design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
4. For the Pipelined designs, the number of pipeline stages used are 2.

## 3.15. LMMI

Table 3.34 summarizes the performance of the LMMI interface with supported IPs. Additional timing requirement and constraint can be identified through the Lattice Radiance design tools.

**Table 3.32. LMMI F$_{MAX}$ Summary**

| IP | F$_{MAX}$ (MHz) |
|---|---|
| CRE | 54 |
| I$^2$C | 38 |
| PLL_LLC | 55 |

## 3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Lattice Radiant design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Lattice Radiant design tool can provide logic timing numbers at a particular temperature and voltage.

## 3.17. External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.33. External Switching Characteristics (V$_{CC}$ = 1.0 V)

| Parameter | Description | -9 Min | -9 Max | -8 Min | -8 Max | -7 Min | -7 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **Clocks** | | | | | | | | |
| **Primary Clocks** | | | | | | | | |
| f$_{MAX\_PRI}$ | Frequency for Primary Clock | — | 400 | — | 325.2 | — | 276 | MHz |
| t$_{W\_PRI}$ | Clock Pulse Width for Primary | 1.125 | — | 1.384 | — | 1.63 | — | ns |
| t$_{SKEW\_PRI}$[6] | Primary Clock Skew Within a Device | — | 450 | — | 554 | — | 653 | ps |
| **Edge Clock** | | | | | | | | |
| f$_{MAX\_EDGE}$ | Frequency for Edge Clock Tree | — | 800 | — | 650.4 | — | 551.7 | MHz |
| t$_{W\_EDGE}$ | Clock Pulse Width for Edge Clock | 0.537 | — | 0.661 | — | 0.779 | — | ns |
| t$_{SKEW\_EDGE}$[6] | Edge Clock Skew Within a Device | — | 120 | — | 148 | — | 174 | ps |
| **Generic SDR Input** | | | | | | | | |
| **General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL** | | | | | | | | |
| t$_{CO}$ | Clock to Output - PIO Output | — | 8.36 | — | 8.53 | — | 8.67 | ns |
| t$_{SU}$ | Clock to Data Setup - PIO Input | 0 | — | 0 | — | 0 | — | ns |
| t$_{H}$ | Clock to Data Hold - PIO Input | 3.73 | — | 3.83 | — | 3.93 | — | ns |
| t$_{SU\_DEL}$ | Clock to Data Setup - PIO Input | 1.84 | — | 1.84 | — | 1.84 | — | ns |
| t$_{H\_DEL}$ (Top) | Clock to Data Hold - PIO Input | 0.22 | — | 0.22 | — | 0.22 | — | ns |
| t$_{H\_DEL}$ (Bottom) | Clock to Data Hold - PIO Input Register with Data Input Delay | 1.77 | — | 1.77 | — | 1.77 | — | ns |
| **General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL** | | | | | | | | |
| t$_{COPLL}$ | Clock to Output - PIO Output | — | 4.55 | — | 4.67 | — | 5.51 | ns |
| t$_{SUPLL}$ (Top) | Clock to Data Setup - PIO Input | 1.54 | — | 1.54 | — | 1.54 | — | ns |
| t$_{H\_DEL}$ (Bottom) | Clock to Data Setup - PIO Input | 1.33 | — | 1.33 | — | 1.33 | — | ns |
| t$_{HPLL}$ | Clock to Data Hold - PIO Input | 0.98 | — | 1.21 | — | 1.42 | — | ns |
| t$_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input | 4.74 | — | 4.74 | — | 4.74 | — | ns |
| t$_{H\_DELPLL}$ | Clock to Data Hold - PIO Input | 0.00 | — | 0 | — | 0 | — | ns |
| **Generic DDR Input/Output** | | | | | | | | |
| **Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using PCLK Clock Input –** | | | | | | | | |
| t$_{SU\_GDDR1}$ | Input Data Setup Before CLK | 0.917 | — | 0.917 | — | 0.917 | — | ns |
| | | 0.275 | — | 0.275 | — | 0.275 | — | UI |
| t$_{HO\_GDDR1}$ | Input Data Hold After CLK | 0.917 | — | 0.917 | — | 0.917 | — | ns |
| t$_{DVB\_GDDR1}$ | Output Data Valid After CLK Output | 1.134 | — | 1.113 | — | 1.014 | — | ns |
| | | -0.533 | — | -0.554 | — | -0.653 | — | ns + 1/2 UI |
| t$_{DQVA\_GDDR1}$ | Output Data Valid After CLK Output | 1.217 | — | 1.113 | — | 1.014 | — | ns |
| | | -0.45 | — | -0.554 | — | -0.653 | — | ns + 1/2 UI |

| Parameter | Description | -9 | | -8 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{DATA\_GDDRX1}$ | Input/Output Data Rate | — | 300 | — | 300 | — | 300 | Mbps |
| $f_{MAX\_GDDRX1}$ | Frequency of PCLK | — | 150 | — | 150 | — | 150 | MHz |
| ½ UI | Half of Data Bit Time, or 90 | 1.667 | — | 1.667 | — | 1.667 | — | ns |
| Output TX to Input RX Margin per Edge | | 0.3 | — | 0.197 | — | 0.097 | — | ns |
| **Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using PCLK Clock Input – Bank 0, Bank 1 and Bank 5 – Figure 3.8 and Figure 3.10** | | | | | | | | |
| $t_{DVA\_GDDR1}$ | Input Data Valid After CLK | — | -0.917 | — | -0.917 | — | -0.917 | ns + 1/2 UI |
| | | — | 0.75 | — | 0.75 | — | 0.75 | ns |
| | | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVE\_GDDR1}$ | Input Data Hold After CLK | 0.917 | — | 0.917 | — | 0.917 | — | ns + 1/2 UI |
| | | 2.583 | — | 2.583 | — | 2.583 | — | ns |
| | | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $t_{DIA\_GDDR1}$ | Output Data Invalid After CLK | — | 0.554 | — | 0.554 | — | 0.653 | ns |
| $t_{DIB\_GDDR1}$ | Output Data Invalid Before CLK | — | 0.45 | — | 0.554 | — | 0.653 | ns |
| $f_{DATA\_GDDRX1}$ | Input/Output Data Rate | — | 300 | — | 300 | — | 300 | Mbps |
| $f_{MAX\_GDDRX1}$ | Frequency for PCLK | — | 150 | — | 150 | — | 150 | MHz |
| ½ UI | Half of Data Bit Time, or 90 degree | 1.667 | — | 1.667 | — | 1.667 | — | ns |
| Output TX to Input RX Margin per Edge | | 0.3 | — | 0.197 | — | 0.097 | — | ns |
| **Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using PCLK Clock Input – Bank 2, Bank 3, and Bank 4 – Figure 3.7 and Figure 3.9** | | | | | | | | |
| $t_{SU\_GDDR1}$ | Input Data Setup Before CLK | 0.917 | — | 0.917 | — | 0.917 | — | ns |
| | | 0.275 | — | 0.275 | — | 0.275 | — | UI |
| $t_{HO\_GDDR1}$ | Input Data Hold After CLK | 0.917 | — | 0.917 | — | 0.917 | — | ns |
| $f_{DATA\_IN\_GDDRX1}$ | Input Data Rate | — | 300 | — | 300 | — | 300 | Mbps |
| $t_{DVB\_GDDR1}$ | Output Data Valid After CLK Output | 0.670 | | 0.631 | — | 0.744 | — | ns |
| | | -0.330 | — | -0.369 | — | -0.435 | — | ns + 1/2 UI |
| $t_{DQVA\_GDDR1}$ | Output Data Valid After CLK Output | 0.7 | — | 0.631 | — | 0.744 | — | ns |
| | | -0.300 | — | -0.369 | — | -0.435 | — | ns + 1/2 UI |
| $f_{DATA\_OUT\_GDDRX1}$ | Output Data Rate | — | 500 | — | 500 | — | 424 | Mbps |
| $f_{MAX\_GDDRX1}$ | Frequency of PCLK | — | 250 | — | 250 | — | 212 | MHz |
| ½ UI | Half of Data Bit Time, or 90 degree | 1 | — | 1 | — | 1.179 | — | ns |
| Output TX to Input RX Margin per Edge | | 0.15 | — | 0.081 | — | 0.095 | — | ns |
| **Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using PCLK Clock Input – Bank 2, Bank 3, and Bank 4 – Figure 3.8 and Figure 3.10** | | | | | | | | |
| $t_{DVA\_GDDR1}$ | Input Data Valid After CLK | — | -0.917 | — | -0.917 | — | -0.917 | ns + 1/2 UI |
| | | — | 0.75 | — | 0.75 | — | 0.75 | ns |
| | | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVE\_GDDR1}$ | Input Data Hold After CLK | 0.917 | — | 0.917 | — | 0.917 | — | ns + 1/2 UI |
| | | 2.583 | — | 2.583 | — | 2.583 | — | ns |
| | | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{DATA\_IN\_GDDRX1}$ | Input Data Rate | — | 300 | — | 300 | — | 300 | Mbps |
| $t_{DIA\_GDDR1}$ | Output Data Invalid After CLK Output | — | 0.3 | — | 0.369 | — | 0.435 | ns |
| $t_{DIB\_GDDR1}$ | Output Data Invalid Before CLK Output | — | 0.3 | — | 0.369 | — | 0.435 | ns |

| Parameter | Description | -9 Min | -9 Max | -8 Min | -8 Max | -7 Min | -7 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| f<sub>DATA_OUT_GDDRX1</sub> | Output Data Rate | — | 500 | — | 500 | — | 424 | Mbps |
| f<sub>MAX_GDDRX1</sub> | Frequency for PCLK | — | 250 | — | 250 | — | 212 | MHz |
| ½ UI | Half of Data Bit Time, or 90 degree | 1 | — | 1 | — | 1.179 | — | ns |
| Output TX to Input RX Margin per Edge | | 0.15 | — | 0.081 | — | 0.095 | — | ns |
| **Generic DDRX2 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX2_RX/TX.ECLK.Centered) using PCLK Clock Input - Figure 3.7 and Figure 3.9** | | | | | | | | |
| t<sub>SU_GDDRX2</sub> | Data Setup before CLK Input | 0.209 | — | 0.209 | — | 0.206 | — | ns |
| | | 0.209 | — | 0.209 | — | 0.175 | — | UI |
| t<sub>HO_GDDRX2</sub> | Data Hold after CLK Input | 0.213 | — | 0.213 | — | 0.206 | — | ns |
| t<sub>DVB_GDDRX2</sub> | Output Data Valid Before CLK Output | 0.360 | — | 0.352 | — | 0.415 | — | ns |
| | | -0.140 | — | -0.148 | — | -0.174 | — | ns + 1/2 UI |
| t<sub>DQVA_GDDRX2</sub> | Output Data Valid After CLK Output | 0.38 | — | 0.352 | — | 0.415 | — | ns |
| | | -0.12 | — | -0.148 | — | -0.174 | — | ns + 1/2 UI |
| f<sub>DATA_GDDRX2</sub> | Input/Output Data Rate | — | 1000 | — | 1000 | — | 848 | Mbps |
| f<sub>MAX_GDDRX2</sub> | Frequency for ECLK | — | 500 | — | 500 | — | 424 | MHz |
| ½ UI | Half of Data Bit Time, or 90 degree | 0.5 | — | 0.5 | — | 0.589 | — | ns |
| f<sub>PCLK</sub> | PCLK frequency | — | 250 | — | 250 | — | 212.1 | MHz |
| Output TX to Input RX Margin per Edge | | 0.23 | — | 0.202 | — | 0.239 | — | ns |
| **Generic DDRX2 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX2_RX/TX.ECLK.Aligned) using PCLK Clock Input - Figure 3.8 and Figure 3.10** | | | | | | | | |
| t<sub>DVA_GDDRX2</sub> | Input Data Valid After CLK | — | -0.275 | — | -0.275 | — | -0.324 | ns + 1/2 UI |
| | | — | 0.225 | — | 0.225 | — | 0.265 | ns |
| | | — | 0.225 | — | 0.225 | — | 0.265 | UI |
| t<sub>DVE_GDDRX2</sub> | Input Data Hold After CLK | 0.275 | — | 0.275 | — | 0.324 | — | ns + 1/2 UI |
| | | 0.775 | — | 0.775 | — | 0.914 | — | ns |
| | | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| t<sub>DIA_GDDRX2</sub> | Output Data Invalid After CLK | — | 0.12 | — | 0.148 | — | 0.174 | ns |
| t<sub>DIB_GDDRX2</sub> | Output Data Invalid Before CLK | — | 0.12 | — | 0.148 | — | 0.174 | ns |
| f<sub>DATA_GDDRX2</sub> | Input/Output Data Rate | — | 1000 | — | 1000 | — | 848 | Mbps |
| f<sub>MAX_GDDRX2</sub> | Frequency for ECLK | — | 500 | — | 500 | — | 424 | MHz |
| ½ UI | Half of Data Bit Time, or 90 degree | 0.5 | — | 0.5 | — | 0.589 | — | ns |
| f<sub>PCLK</sub> | PCLK frequency | — | 250 | — | 250 | — | 212.1 | MHz |
| Output TX to Input RX Margin per Edge | | 0.105 | — | 0.077 | — | 0.091 | — | ns |
| **Generic DDRX4 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX4_RX/TX.ECLK.Centered) using PCLK Clock Input - Figure 3.7 and Figure 3.9** | | | | | | | | |
| t<sub>SU_GDDRX4</sub> | Input Data Set-Up Before CLK | 0.210 | — | 0.210 | — | 0.244 | — | ns |
| | | 0.315 | — | 0.252 | — | 0.252 | — | UI |
| t<sub>HO_GDDRX4</sub> | Input Data Hold After CLK | 0.254 | — | 0.254 | — | 0.244 | — | ns |
| t<sub>DVB_GDDRX4</sub> | Output Data Valid Before CLK Output | 0.193 | — | 0.269 | — | 0.309 | — | ns |
| | | -0.140 | — | –0.148 | — | -0.174 | — | ns + 1/2 UI |
| t<sub>DQVA_GDDRX4</sub> | Output Data Valid After CLK Output | 0.213 | — | 0.269 | — | 0.309 | — | ns |
| | | -0.12 | — | –0.148 | — | -0.174 | — | ns + 1/2 UI |
| f<sub>DATA_GDDRX4</sub> | Input/Output Data Rate | — | 1500 | — | 1200 | — | 1034 | Mbps |
| f<sub>MAX_GDDRX4</sub> | Frequency for ECLK | — | 750 | — | 600 | — | 517 | MHz |

| Parameter | Description | -9 Min | -9 Max | -8 Min | -8 Max | -7 Min | -7 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| ½ UI | Half of Data Bit Time, or 90 degrees | 0.333 | — | 0.417 | — | 0.483 | — | ns |
| $f_{PCLK}$ | PCLK frequency | — | 187.5 | — | 150 | — | 129.3 | MHz |
| Output TX to Input RX Margin per Edge | | 0.08 | — | 0.102 | — | 0.116 | — | ns |
| **Generic DDRX4 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX4_RX/TX.ECLK.Aligned) using PCLK Clock Input - Figure 3.8 and Figure 3.10** | | | | | | | | |
| $t_{DVA\_GDDRX4}$ | Input Data Valid After CLK | — | -0.216 | — | -0.229 | — | -0.266 | ns + 1/2 UI |
| | | — | 0.117 | — | 0.188 | — | 0.218 | ns |
| | | — | 0.176 | — | 0.225 | — | 0.225 | UI |
| $t_{DVE\_GDDRX4}$ | Input Data Hold After CLK | 0.227 | — | 0.229 | — | 0.266 | — | ns + 1/2 UI |
| | | 0.560 | — | 0.646 | — | 0.749 | — | ns |
| | | 0.840 | — | 0.775 | — | 0.775 | — | UI |
| $t_{DIA\_GDDRX4}$ | Output Data Invalid After CLK Output | — | 0.12 | — | 0.148 | — | 0.174 | ns |
| $t_{DIB\_GDDRX4}$ | Output Data Invalid Before CLK Output | — | 0.12 | — | 0.148 | — | 0.174 | ns |
| $f_{DATA\_GDDRX4}$ | Input/Output Data Rate | — | 1500 | — | 1200 | — | 1034 | Mbps |
| $f_{MAX\_GDDRX4}$ | Frequency for ECLK | — | 750 | — | 600 | — | 517 | MHz |
| ½ UI | Half of Data Bit Time, or 90 degree | 0.333 | — | 0.417 | — | 0.483 | — | ns |
| $f_{PCLK}$ | PCLK frequency | — | 187.5 | — | 150 | — | 129.3 | MHz |
| Output TX to Input RX Margin per Edge | | 0.03 | — | 0.040 | — | 0.044 | — | ns |
| **Generic DDRX5 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX5_RX/TX.ECLK.Centered) using PCLK Clock Input - Figure 3.7 and Figure 3.9** | | | | | | | | |
| $t_{SU\_GDDRX5}$ | Input Data Set-Up Before CLK | 0.231 | — | 0.231 | — | 0.224 | — | ns |
| | | 0.289 | — | 0.277 | — | 0.224 | — | UI |
| $t_{HO\_GDDRX5}$ | Input Data Hold After CLK | 0.229 | — | 0.229 | — | 0.224 | — | ns |
| $t_{WINDOW\_GDDRX5C}$ | Input Data Valid Window | — | — | — | — | — | — | ns |
| $t_{DVB\_GDDRX5}$ | Output Data Valid Before CLK Output | 0.249 | — | 0.269 | — | 0.326 | — | ns |
| | | -0.151 | — | -0.148 | — | -0.174 | — | ns+1/2UI |
| $t_{DQVA\_GDDRX5}$ | Output Data Valid After CLK Output | 0.249 | — | 0.269 | — | 0.326 | — | ns |
| | | -0.151 | — | -0.148 | — | -0.174 | — | ns+1/2UI |
| $f_{DATA\_GDDRX5}$ | Input/Output Data Rate | — | 1250 | — | 1200 | — | 1000 | Mbps |
| $f_{MAX\_GDDRX5}$ | Frequency for ECLK | — | 625 | — | 600 | — | 500 | MHz |
| ½ UI | Half of Data Bit Time, or 90 degree | 0.4 | — | 0.417 | — | 0.500 | — | ns |
| $f_{PCLK}$ | PCLK frequency | — | 125 | — | 120 | — | 100.0 | MHz |
| Output TX to Input RX Margin per Edge | | 0.12 | — | 0.102 | — | 0.126 | — | ns |

| Parameter | Description | -9 | | -8 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| **Generic DDRX5 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX5_RX/TX.ECLK.Aligned) using PCLK Clock Input - Figure 3.8 and Figure 3.10** | | | | | | | | |
| $t_{DVA\_GDDRX5}$ | Input Data Valid After CLK | — | -0.220 | — | -0.229 | — | -0.275 | ns + 1/2 UI |
| | | — | 0.18 | — | 0.188 | — | 0.225 | ns |
| | | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVE\_GDDRX5}$ | Input Data Hold After CLK | 0.22 | — | 0.229 | — | 0.275 | — | ns + 1/2 UI |
| | | 0.62 | — | 0.646 | — | 0.775 | — | ns |
| | | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $t_{WINDOW\_GDDRX5A}$ | Input Data Valid Window | — | — | — | — | — | — | ns |
| $t_{DIA\_GDDRX5}$ | Output Data Invalid After CLK Output | — | 0.12 | — | 0.148 | — | 0.174 | ns |
| $t_{DIB\_GDDRX5}$ | Output Data Invalid Before CLK Output | — | 0.12 | — | 0.148 | — | 0.174 | ns |
| $f_{DATA\_GDDRX5}$ | Input/Output Data Rate | — | 1250 | — | 1200 | — | 1000 | Mbps |
| $f_{MAX\_GDDRX5}$ | Frequency for ECLK | — | 625 | — | 600 | — | 500 | MHz |
| ½ UI | Half of Data Bit Time or 90 degrees | 0.4 | — | 0.417 | — | 0.500 | — | ns |
| $f_{PCLK}$ | PCLK frequency | — | 125 | — | 120 | — | 100.0 | MHz |
| Output TX to Input RX Margin per Edge | | 0.06 | — | 0.051 | — | ns | 0.04 | — |
| **Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input** | | | | | | | | |
| $t_{SU\_GDDRX4\_MP}$ | Input Data Set-Up Before CLK | 0.133 | — | 0.167 | — | 0.193 | — | ns |
| | | 0.2 | — | 0.2 | — | 0.2 | — | UI |
| $t_{HO\_GDDRX4\_MP}$ | Input Data Hold After CLK | 0.133 | — | 0.167 | — | 0.193 | — | ns |
| $t_{DVB\_GDDRX4\_MP}$ | Output Data Valid Before CLK Output | 0.133 | — | 0.167 | — | 0.193 | — | ns |
| | | 0.2 | — | 0.2 | — | 0.2 | — | UI |
| $t_{DQVA\_GDDRX4\_MP}$ | Output Data Valid After CLK Output | 0.133 | — | 0.167 | — | 0.193 | — | ns |
| | | 0.2 | — | 0.2 | — | 0.2 | — | UI |
| $f_{DATA\_GDDRX4\_MP}$ | Input Data Bit Rate for MIPI PHY (USG84) | — | 1250 | — | 1000 | — | — | Mbps |
| | Input Data Bit Rate for MIPI PHY (CTG104) | — | 1500 | — | 1200 | — | 1034 | Mbps |
| ½ UI | Half of Data Bit Time or 90 | 0.333 | — | 0.417 | — | 0.483 | — | ns |
| $f_{PCLK}$ | PCLK frequency | — | 187.5 | — | 150 | — | 129.3 | MHz |
| Output TX to Input RX Margin per Edge | | 0.067 | — | 0.083 | — | 0.097 | — | ns |
| **Video DDRX71 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) using PLL Clock Input - Figure 3.12 and Figure 3.13** | | | | | | | | |
| $t_{RPBi\_DVA}$ | Input Valid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK) | — | 0.264 | — | 0.264 | — | 0.3 | UI |
| | | — | -0.250 | — | -0.250 | — | -0.249 | ns+(1/2+i) × UI |
| $t_{RPBi\_DVE}$ | Input Hold Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK) | 0.761 | — | 0.761 | — | 0.7 | — | UI |
| | | 0.276 | — | 0.276 | — | 0.249 | — | ns+(1/2+i) × UI |
| $t_{TPBi\_DOV}$ | Data Output Valid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK) | — | 0.159 | — | 0.159 | — | 0.187 | ns+I × UI |

| Parameter | Description | -9 | | -8 | | -7 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{TPBi\_DOI}$ | Data Output Invalid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK) | -0.159 | — | -0.159 | — | -0.187 | — | ns+(i+ 1) × UI |
| $t_{TPBi\_skew\_UI}$ | TX skew in UI | — | 0.15 | — | 0.15 | — | 0.150 | UI |
| $t_B$ | Serial Data Bit Time, = 1 UI | 1.058 | — | 1.058 | — | 1.247 | — | ns |
| $f_{DATA\_TX71}$ | DDR71 Serial Data Rate | — | 945 | — | 945 | — | 802 | Mbps |
| $f_{MAX\_TX71}$ | DDR71 ECLK Frequency | — | 473 | — | 473 | — | 401 | MHz |
| $f_{CLKIN}$ | 7:1 Clock (PCLK) Frequency | — | 135 | — | 135 | — | 114.5 | MHz |
| Output TX to Input RX Margin per Edge | | 0.159 | — | 0.159 | — | 0.187 | — | ns |

**Notes**:
1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Lattice Radiant software.
2. General I/O timing numbers are based on LVCMOS 1.8, 8 mA, Fast Slew Rate, 0 pF load.
   Generic DDR timing are numbers based on LVDS I/O.
3. Uses LVDS I/O standard for measurements.
4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
5. All numbers are generated with the Lattice Radiant software.
6. This clock skew is not the internal clock network skew. The Nexus family devices have very low internal clock network skew that can be approximated to 0 ps. These $t_{SKEW}$ values measured externally at system level includes additional skew added by the I/O, wire bonding and package ball.
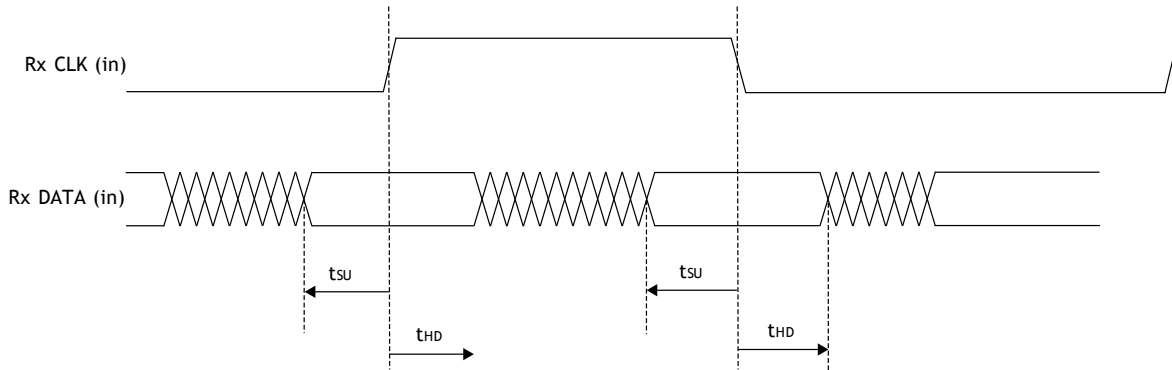


**Figure 3.7. Receiver RX.CLK.Centered Waveforms**
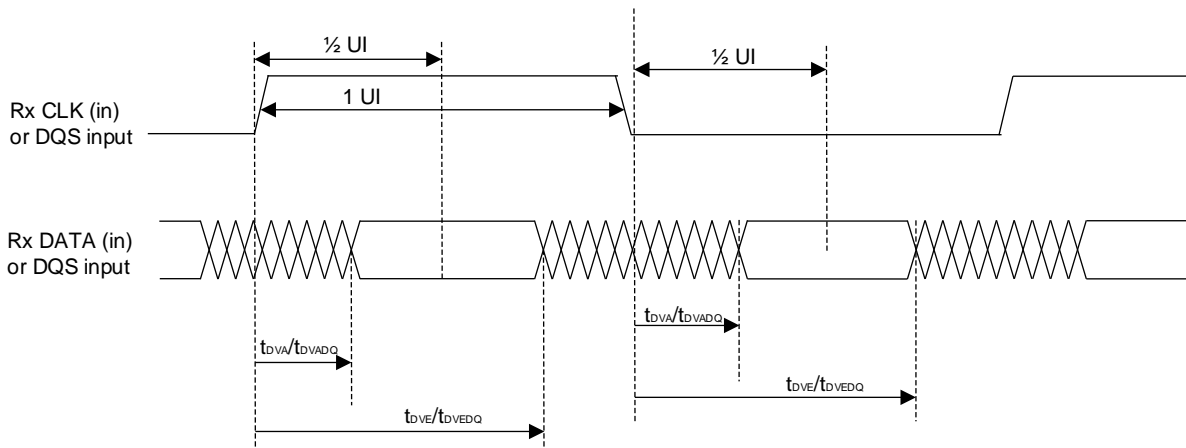


**Figure 3.8. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms**
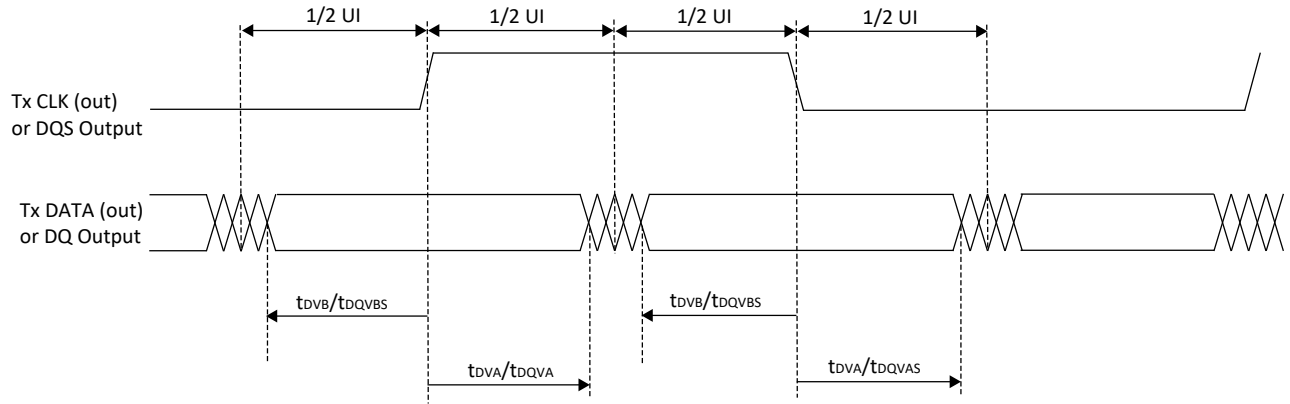
**Figure 3.9. Transmit TX.CLK.Centered and DDR Memory Output Waveforms**
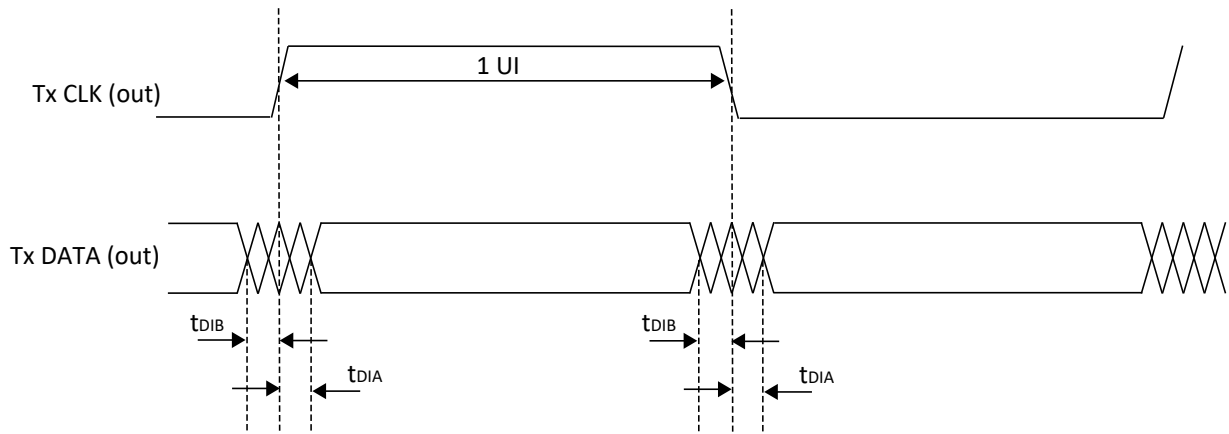
**Figure 3.10. Transmit TX.CLK.Aligned Waveforms**

**Receiver – Shown for one LVDS Channel**
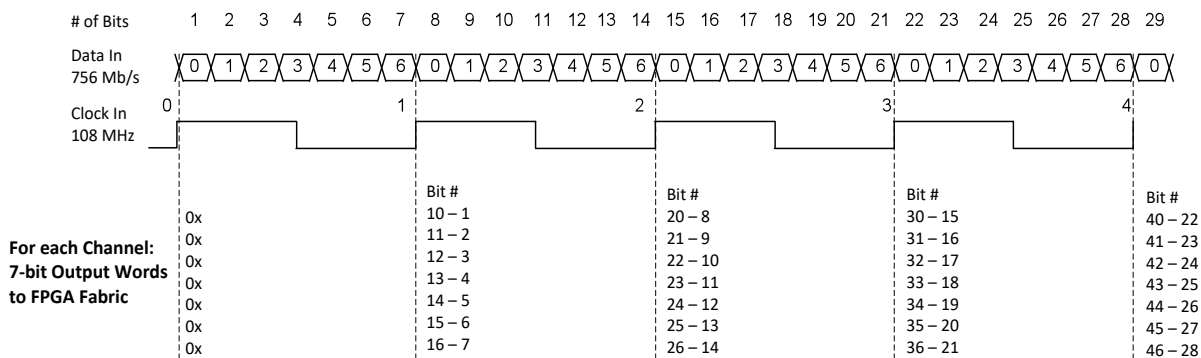


**Transmitter – Shown for one LVDS Channel**
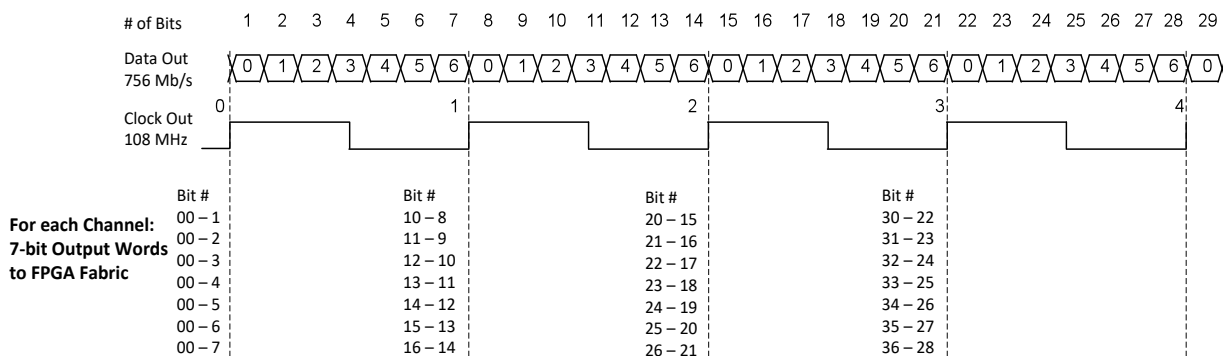


**Figure 3.11. DDRX71 Video Timing Waveforms**
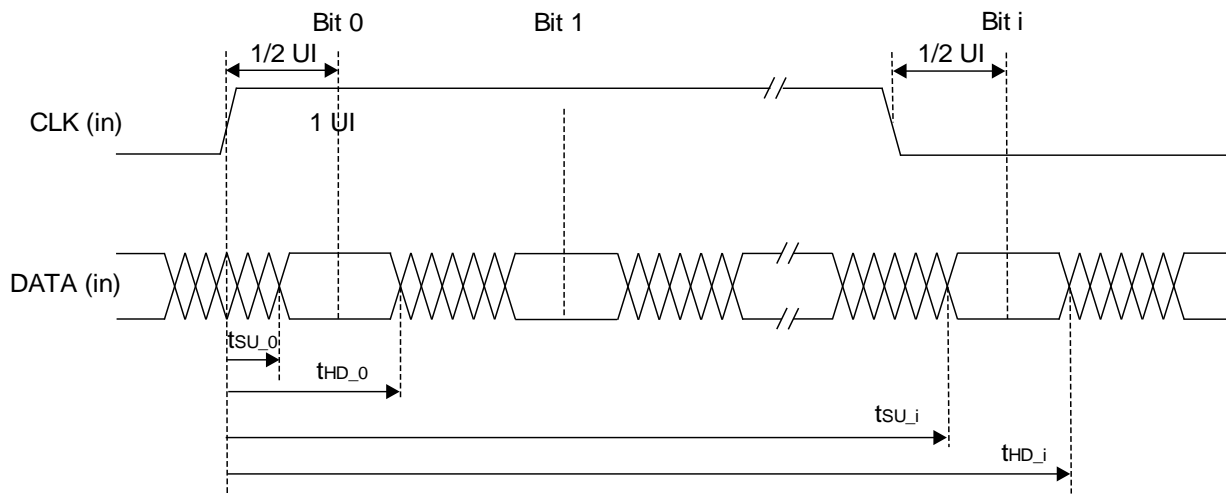


**Figure 3.12. Receiver DDRX71_RX Waveforms**
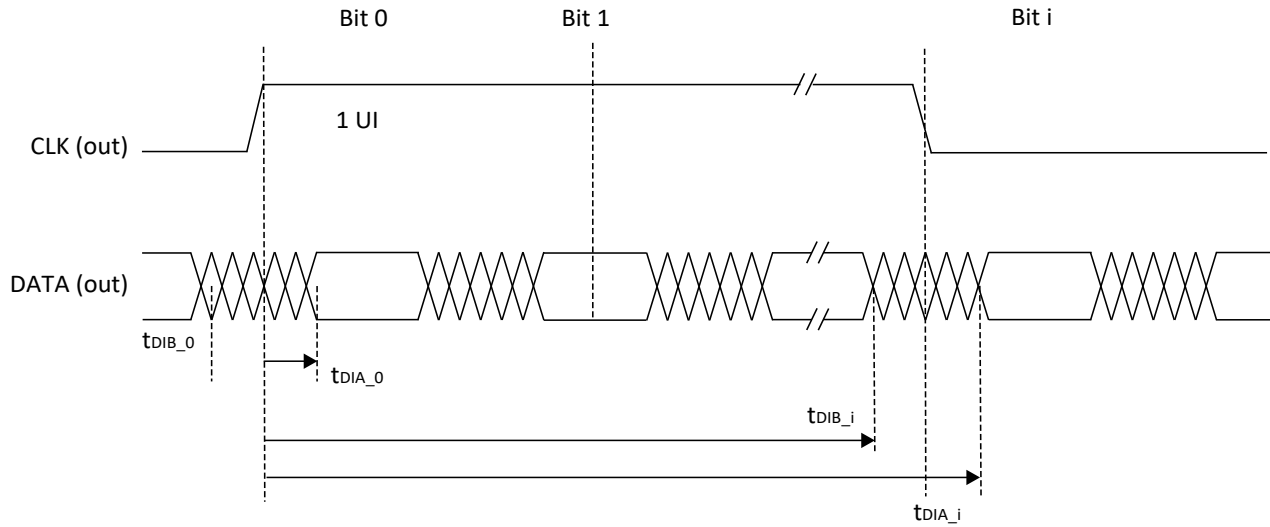
**Figure 3.13. Transmitter DDRX71_TX Waveforms**

# 3.18. sysCLOCK PLL Timing ($V_{CC}$ = 1.0 V)

Over recommended operating conditions.

**Table 3.34. sysCLOCK PLL Timing ($V_{CC}$ = 1.0 V)**

| Parameter | Descriptions | Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | — | 18 | — | 500 | MHz |
| $f_{OUT}$ | Output Clock Frequency | — | 6.25 | — | 800 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | — | 800 | — | 1600 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | Without Fractional-N Enabled | 18 | — | 500 | MHz |
| | | With Fractional-N Enabled | 18 | — | 100 | MHz |
| **AC Characteristics** | | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | — | 45 | — | 55 | % |
| $t_{PH}$[4] | Output Phase Accuracy | — | -5 | — | 5 | % |

| Parameter | Descriptions | Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{OPJIT}$[1] | Output Clock Period Jitter | $f_{OUT} \geq 200$ MHz | — | — | 250 | ps p-p |
| | | $f_{OUT} < 200$ MHz | — | — | 0.05 | UIPP |
| | Output Clock Cycle-to-Cycle Jitter | $f_{OUT} \geq 200$ MHz | — | — | 250 | ps p-p |
| | | $f_{OUT} < 200$ MHz | — | — | 0.05 | UIPP |
| | Output Clock Phase Jitter | $f_{PFD} \geq 200$ MHz | — | — | 250 | ps p-p |
| | | 60 MHz $\leq f_{PFD} < 200$ | — | — | 350 | ps p-p |
| | | 30 MHz $\leq f_{PFD} < 60$ | — | — | 450 | ps p-p |
| | | 18 MHz $\leq f_{PFD} < 30$ | — | — | 650 | ps p-p |
| | Output Clock Period Jitter (Fractional-N) | $f_{OUT} \geq 200$ MHz | — | — | 350 | ps p-p |
| | | $f_{OUT} < 200$ MHz | — | — | 0.07 | UIPP |
| | Output Clock Cycle-to-Cycle Jitter (Fractional-N) | $f_{OUT} \geq 200$ MHz | — | — | 400 | ps p-p |
| | | $f_{OUT} < 200$ MHz | — | — | 0.08 | UIPP |
| $f_{BW}$[3] | PLL Loop Bandwidth | — | 0.45 | — | 13 | MHz |
| $t_{LOCK}$[2] | PLL Lock-in Time | — | — | — | 10 | ms |
| $t_{UNLOCK}$ | PLL Unlock Time (from RESET goes HIGH) | — | — | — | 50 | ns |
| $t_{IPJIT}$ | Input Clock Period Jitter | $f_{PFD} \geq 20$ MHz | — | — | 500 | ps p-p |
| | | $f_{PFD} < 20$ MHz | — | — | 0.01 | UIPP |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | — | ns |
| $t_{RST}$ | RST/ Pulse Width | — | 1 | — | — | ms |
| $f_{SSC\_MOD}$ | Spread Spectrum Clock Modulation Frequency | — | 20 | — | 200 | kHz |
| $f_{SSC\_MOD\_AMP}$ | Spread Spectrum Clock Modulation Amplitude Range | — | 0.25 | — | 2.00 | % |
| $f_{SSC\_MOD\_STEP}$ | Spread Spectrum Clock Modulation Amplitude Step Size | — | — | 0.25 | — | % |

**Notes**:
1. Jitter sample is taken over 10,000 samples for Period jitter, and 1,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Result from Lattice Radiant software.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency.

## 3.19. Internal Oscillators Characteristics

**Table 3.35. Internal Oscillators (V$_{CC}$ = 1.0 V)**

| Symbol | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| f$_{CLKHF}$ | HFOSC CLKK Clock Frequency | 418.5 | 450 | 481.5 | MHz |
| f$_{CLKLF}$ | LFOSC CLKK Clock Frequency | 25.6 | 32 | 38.4 | kHz |
| DCH$_{CLKHF}$ | HFOSC Duty Cycle (Clock High Period) | 45 | 50 | 55 | % |
| DCH$_{CLKLF}$ | LFOSC Duty Cycle (Clock High Period) | 45 | 50 | 55 | % |

## 3.20. User I$^2$C Characteristics

**Table 3.36. User I$^2$C Specifications (V$_{CC}$ = 1.0 V)**

| Symbol | Parameter Description | STD Mode | | | FAST Mode | | | FAST Mode Plus[2] | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f$_{scl}$ | SCL Clock Frequency | — | — | 100 | — | — | 400 | — | — | 1000 | kHz |
| T$_{DELAY}$[1] | Optional delay through delay block | — | — | 62 | — | — | 62 | — | — | 62 | ns |

**Notes**:

1. Refer to the I$^2$C Specification for timing requirements. User design should set constraints in Lattice Design software to meet this industrial I$^2$C Specification.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I$^2$C bus. Internal pull up may not be sufficient to support the maximum speed.

## 3.21. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

**Table 3.37. sysCONFIG Port Timing Specifications**

| Symbol | Parameter | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| **Master SPI POR/REFRESH Timing** | | | | | |
| t$_{ICFG}$ | REFRESH command executed, to the rising edge of INITN (bulk-erase off) | — | — | 30 | µs |
| t$_{VMC}$ | Time from rising edge of INITN to the valid Master MCLK | — | — | 5 | µs |
| f$_{MCLK\_DEF}$ | Default MCLK frequency (Before MCLK frequency selection in bitstream) | — | 3.5 | — | MHz |
| t$_{ICFG\_POR}$ | Time during POR, from VCC, VCCAUX, VCCIO0, or VCCIO1 (whichever is the last) pass POR trip voltage, to the rising edge if INITN | — | — | 5 | ms |

| Symbol | Parameter | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| **Slave SPI/I²C/I3C POR** | | | | | |
| $t_{MSPI\_INH}$ | Time during POR, from $V_{CC}$, $V_{CCAUX}$, $V_{CCIO0}$ or $V_{CCIO1}$ (whichever is the last) pass POR trip voltage, to pull PROGRAMN LOW to prevent entering MSPI mode | — | — | 1 | µs |
| $t_{ACT\_PROGRAMN\_H}$ | Minimum time driving PROGRAMN HIGH after last activation clock | 50 | — | — | ns |
| $t_{CONFIG\_CCLK}$ | Minimum time to start driving CCLK (SSPI) after PROGRAMN HIGH | 50 | — | — | ns |
| $t_{CONFIG\_SCL}$ | Minimum time to start driving SCL (I²C/I3C) after PROGRAMN HIGH | 50 | — | — | ns |
| **PROGRAMN Configuration Timing** | | | | | |
| $t_{PROGRAMN\_L}$ | PROGRAMN LOW pulse accepted | 50 | — | — | ns |
| $t_{PROGRAMN\_H}$ | PROGRAMN HIGH pulse accepted | 60 | — | — | ns |
| $t_{PROGRAMN\_RJ}$ | PROGRAMN LOW pulse rejected | — | — | 25 | ns |
| $t_{INIT\_LOW}$ | PROGRAMN LOW to INITN LOW | — | — | 100 | ns |
| $t_{INIT\_HIGH}$ | PROGRAMN LOW to INITN HIGH (bulk-erase off) | — | 30 | — | µs |
| $t_{DONE\_LOW}$ | PROGRAMN LOW to DONE LOW | — | — | 55 | µs |
| $t_{DONE\_HIGH}$[2] | PROGRAMN HIGH to DONE HIGH | — | — | 2 | s |
| $t_{IODISS}$ | PROGRAMN LOW to I/O Disabled | — | — | 125 | ns |
| **Master SPI** | | | | | |
| $f_{MCLK}$[1] | Max selected MCLK output frequency | — | 150 | 165 | MHz |
| $f_{MCLK\_DC}$ | MCLK output clock duty cycle | 40 | — | 60 | % |
| $t_{MCLKH}$ | MCLK output clock pulse width HIGH | 3 | — | — | ns |
| $t_{MCLKL}$ | MCLK output clock pulse width LOW | 3 | — | — | ns |
| $t_{SU\_MSI}$ | MSI to MCLK setup time | 3 | — | — | ns |
| $t_{HD\_MSI}$ | MSI to MCLK hold time | 0.5 | — | — | ns |
| $t_{CO\_MSO}$[2] | MCLK to MSO delay | — | — | 12 | ns |
| **Slave SPI** | | | | | |
| $f_{CCLK}$ | CCLK input clock frequency | — | — | 135 | MHz |
| $t_{CCLKH}$ | CCLK input clock pulse width HIGH | 3.5 | — | — | ns |
| $t_{CCLKL}$ | CCLK input clock pulse width LOW | 3.5 | — | — | ns |
| $t_{VMC\_SLAVE}$ | Time from rising edge of INITN to Slave CCLK driven | 50 | — | — | ns |
| $t_{VMC\_MASTER}$ | CCLK input clock duty cycle | 40 | — | 60 | % |
| $t_{SU\_SSI}$ | SSI to CCLK setup time | 3.2 | — | — | ns |
| $t_{HD\_SSI}$ | SSI to CCLK hold time | 1.9 | — | — | ns |
| $t_{CO\_SSO}$ | CCLK falling edge to valid SSO output | — | — | 30 | ns |
| $t_{EN\_SSO}$ | CCLK falling edge to SSO output enabled | — | — | 30 | ns |
| $t_{DIS\_SSO}$ | CCLK falling edge to SSO output disabled | — | — | 30 | ns |
| $t_{HIGH\_SCSN}$ | SCSN HIGH time | 74 | — | — | ns |
| $t_{SU\_SCSN}$ | SCSN to CCLK setup time | 3.5 | — | — | ns |
| $t_{HD\_SCSN}$ | SCSN to CCLK hold time | 1.6 | — | — | ns |
| **I²C/I3C** | | | | | |
| $f_{SCL\_I2C}$ | SCL input clock frequency for I²C | — | — | 1 | MHz |
| $f_{SCL\_I3C}$ | SCL input clock frequency for I3C | — | — | 12 | MHz |
| $t_{SCLH\_I2C}$ | SCL input clock pulse width HIGH for I²C | 400 | — | — | ns |
| $t_{SCLL\_I2C}$ | SCL input clock pulse width LOW for I²C | 400 | — | — | ns |

| Symbol | Parameter | Min | Typ. | Max | Unit |
|--------|-----------|-----|------|-----|------|
| $t_{SU\_SDA\_I2C}$ | SDA to SCL setup time for I²C | 250 | — | — | ns |
| $t_{HD\_SDA\_I2C}$ | SDA to SCL hold time for I²C | 50 | — | — | ns |
| $t_{SU\_SDA\_I3C}$ | SDA to SCL setup time for I3C | 30 | — | — | ns |
| $t_{HD\_SDA\_I3C}$ | SDA to SCL hold time for I3C | 30 | — | — | ns |
| $t_{CO\_SDA}$ | SCL falling edge to valid SDA output | — | — | 200 | ns |
| $t_{EN\_SDA}$ | SCL falling edge to SDA output enabled | — | — | 200 | ns |
| $t_{DIS\_SDA}$ | SCL falling edge to SDA output disabled | — | — | 200 | ns |
| **Wake-Up Timing** | | | | | |
| $t_{WAKEUP\_DONE\_HIGH}$[2] | Last configuration clock cycle to DONE going HIGH | — | — | 60 | µs |
| $t_{FIO\_EN}$[2] | User I/O enabled in Early I/O Mode | — | | 31184 | cycles |
| $t_{IOEN}$[2] | Config clock to user I/O enabled | 130 | — | — | ns |
| $t_{MCLKZ}$[2, 3] | Master MCLK to Hi-Z | — | — | 2.5 | µs |

**Notes**:

1.  $f_{MCLK}$ has a dependency on HFOSC and is 1/3 of $f_{CLKHF}$.
2.  Based on 30k uncompressed/unauthenticated/default MCLK timing (3.5 MHz)/x1. Other permutations result in different values.
3.  Measure using LVCMOS18, default MCLK frequency, slow slew rate.
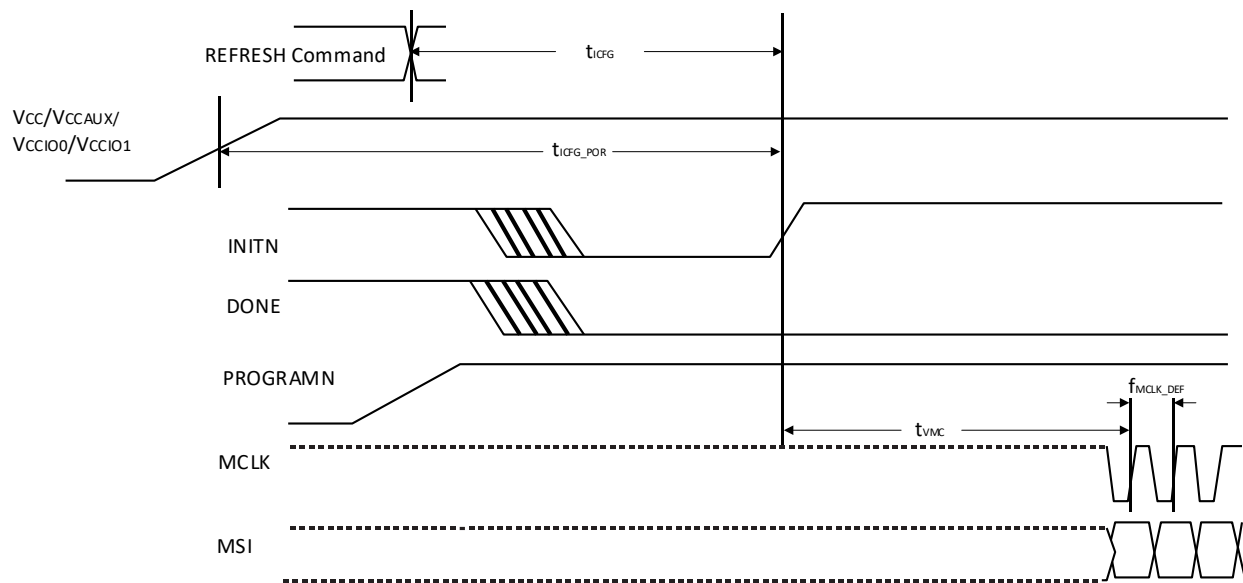


**Figure 3.14. Master SPI POR/REFRESH Timing**
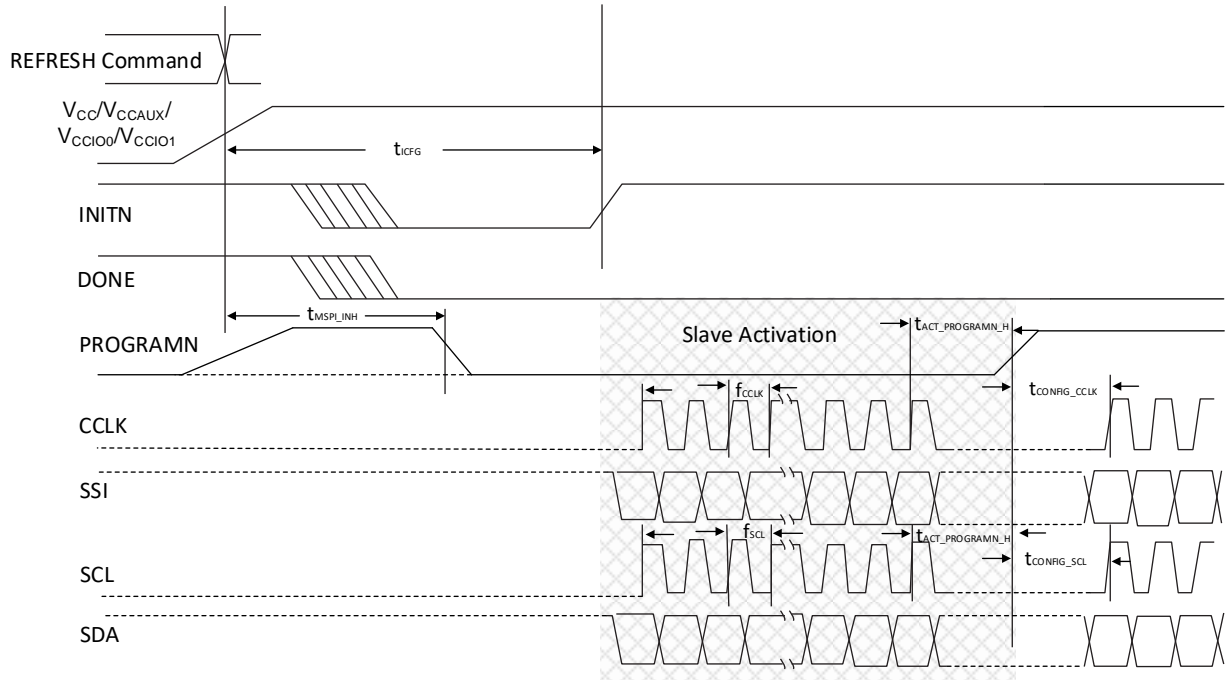
Figure 3.15. Slave SPI/I²C/I3C POR/REFRESH Timing
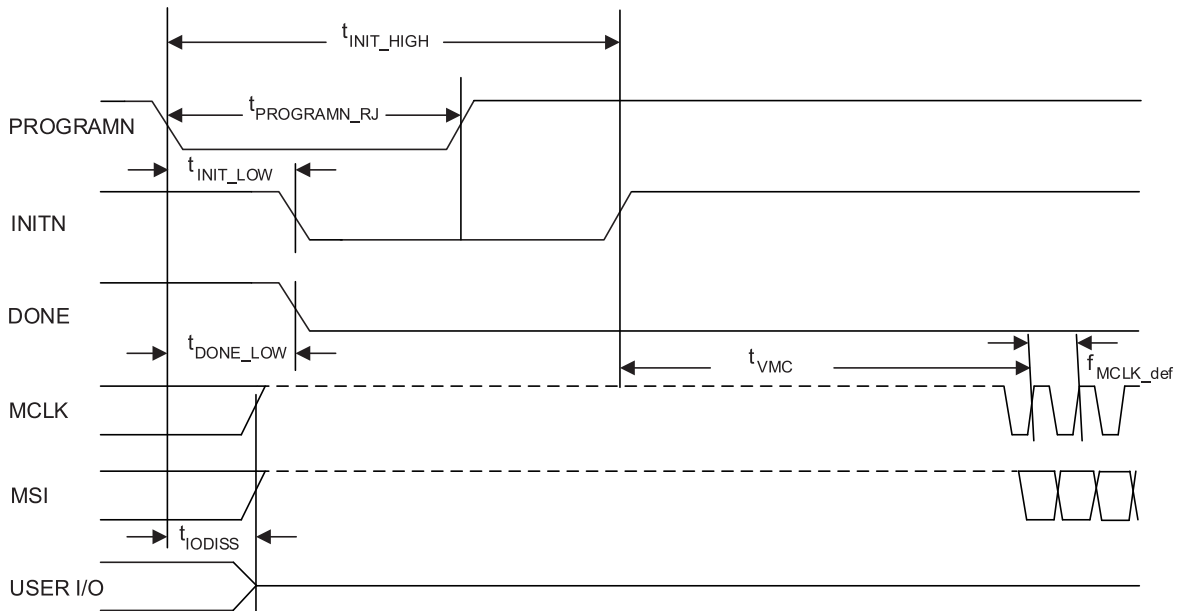


Figure 3.16. Master SPI PROGRAMN Timing
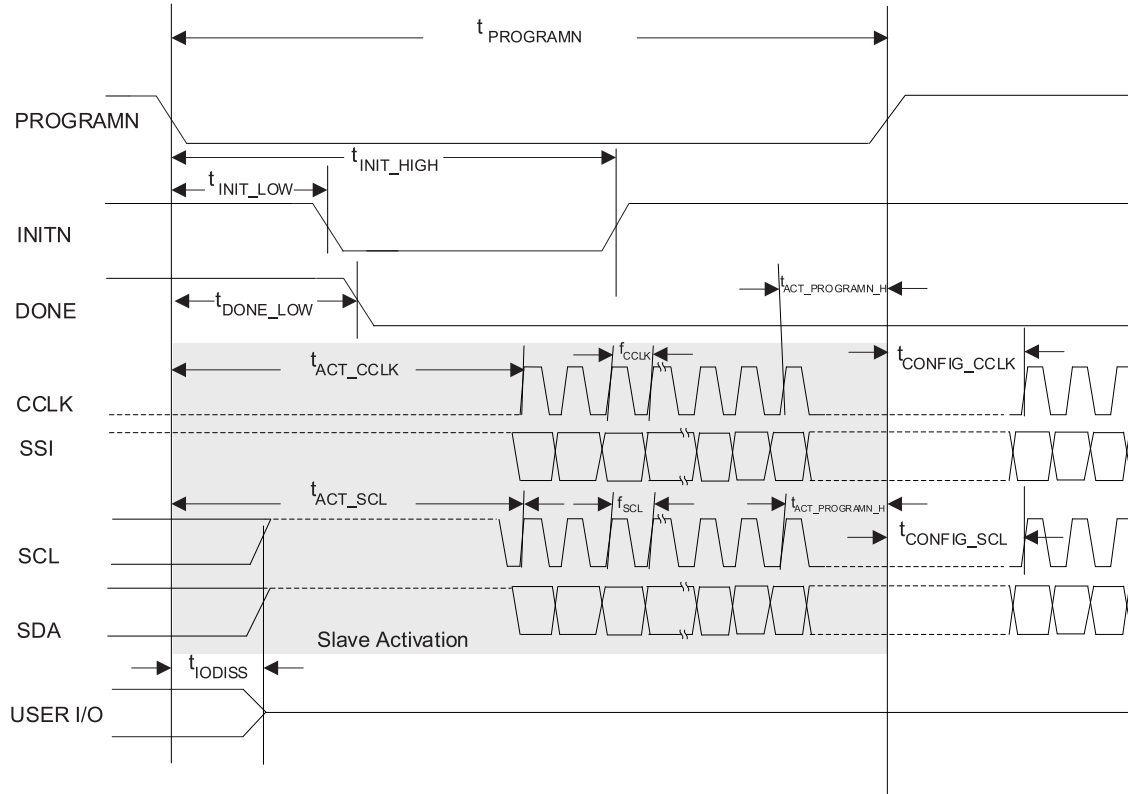
**Figure 3.17. Slave SPI/I$^2$C/I3C PROGRAMN Timing**
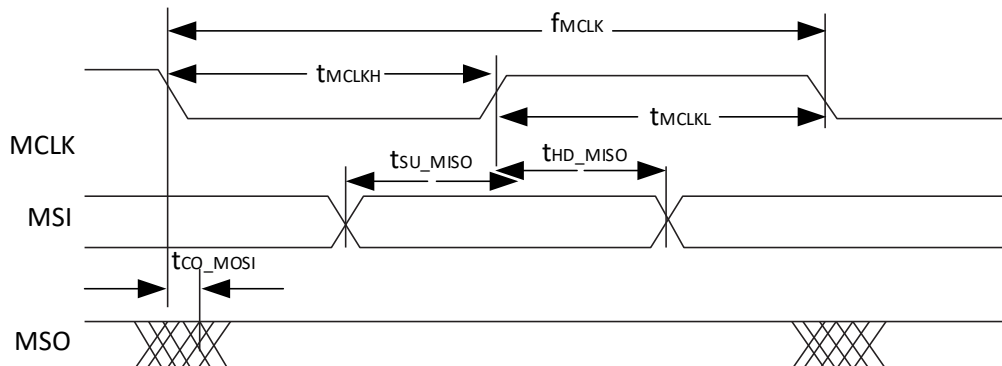


**Figure 3.18. Master SPI Configuration Timing**
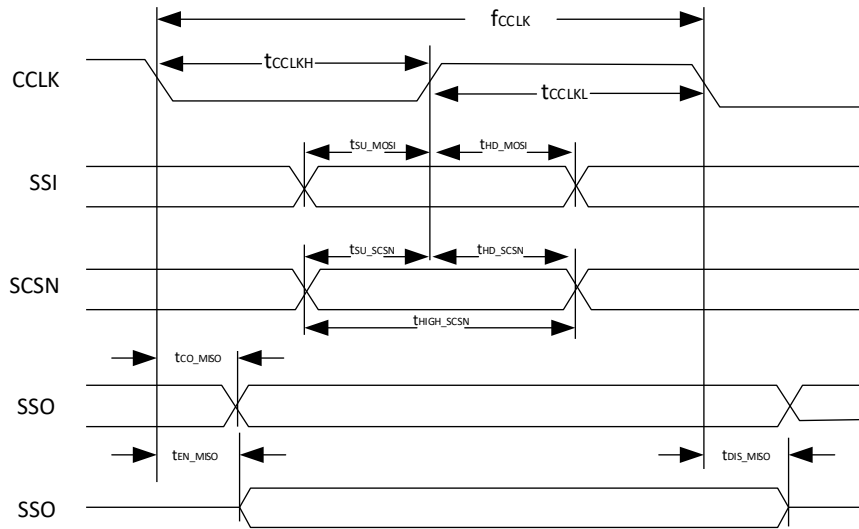
**Figure 3.19. Slave SPI Configuration Timing**
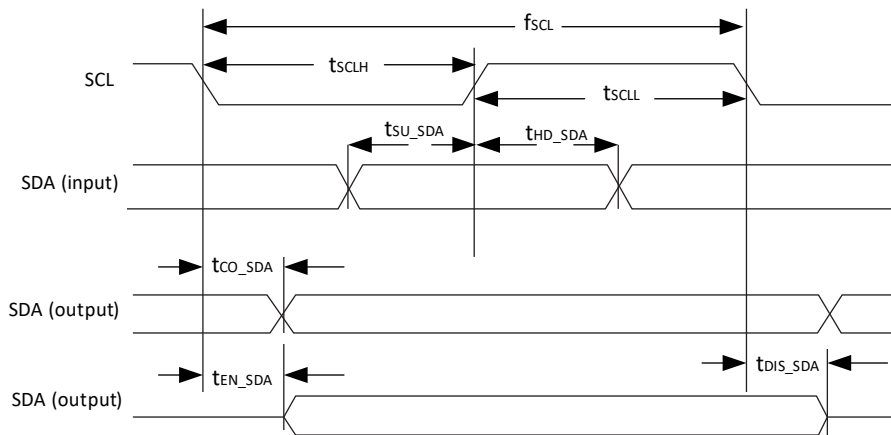


**Figure 3.20. I²C /I3C Configuration Timing**
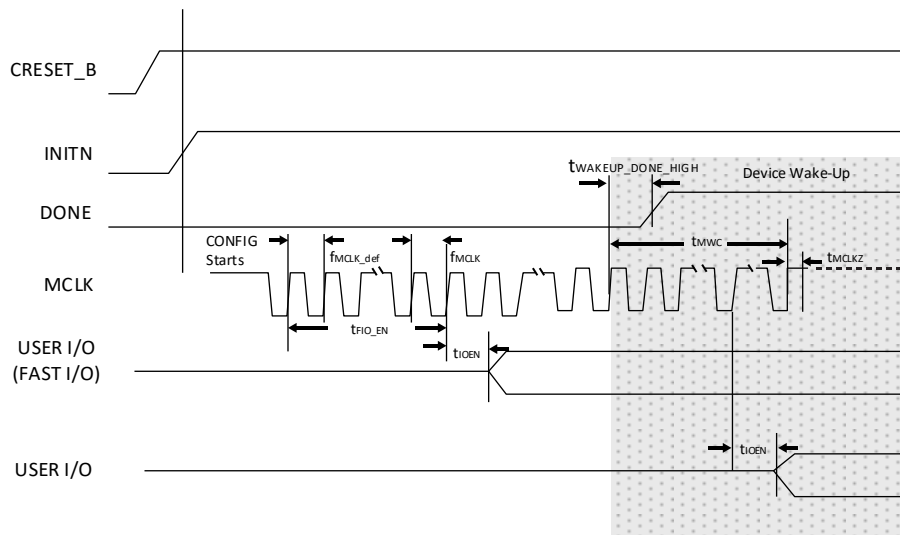


**Figure 3.21. Master SPI Wake-Up Timing**
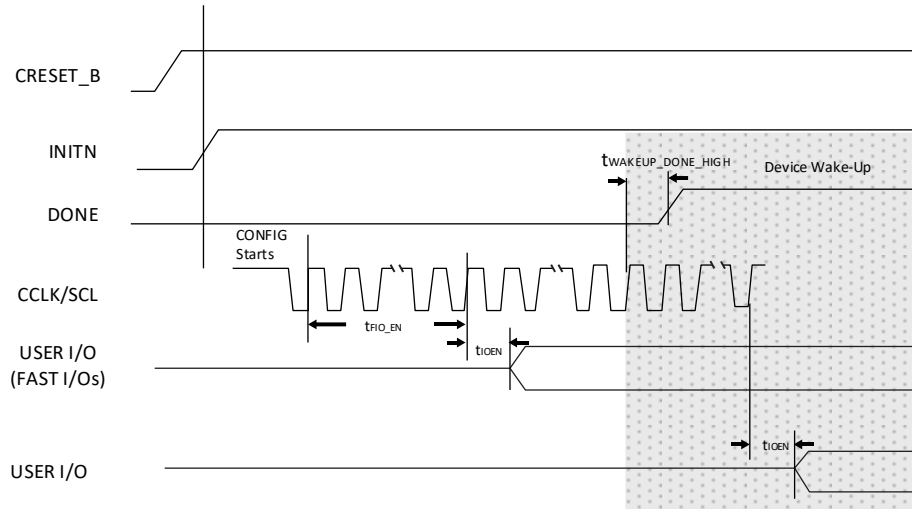
**Figure 3.22. Slave SPI/I²C/I3C Wake-Up Timing**
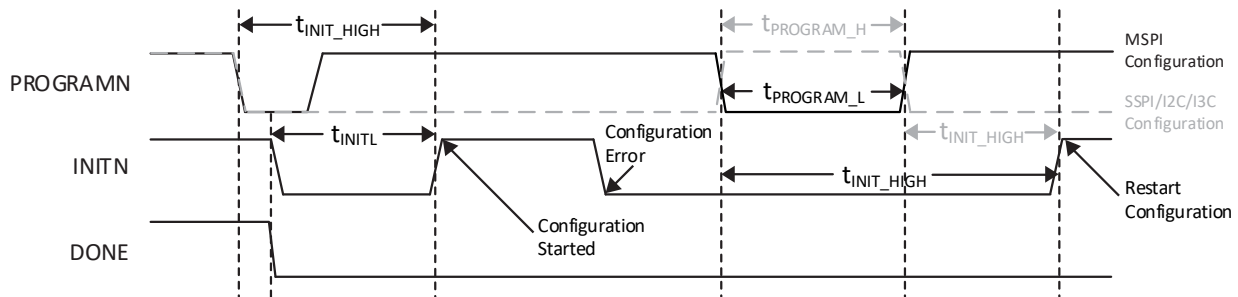


Note: $t_{INTL}$ = SRAM Memory Initialization Period

**Figure 3.23. Configuration Error Notification**

## 3.22. AON Block Specifications ($V_{CCAUX\_AON}$ = 1.8V)

Over recommended operating conditions.

**Table 3.38. AON Block Specification ($V_{CCAUX\_AON}$ = 1.8 V)**

| Symbol | Description | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CCAUX\_AON}$ | AON Supply Current | — | — | 70 | — | uA |
| $f_{OSC\_AON\_TIMER\_CAL}$ | Internal timer calibration frequency | — | — | 11 | — | kHz |
| $t_{PWRDN}$ | Power down time | — | — | — | 90 | sec |
| $t_{PWRDN}$ | Power down time | — | 2.5 | — | — | ms |

**Note:** AON is only supported in LIFCL-33U.

## 3.23. Hardened USB Specifications

Over recommended operating conditions.

**Table 3.39. Hardened USB2 Specifications**

| Symbol | Description | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{REF\_CLK}$ | Reference Clock Frequency | — | | 12/24/60 | | MHz |
| $t_{OFFSET}$ | Clock offset | — | -300 | — | 300 | ppm |
| $t_{DUTY}$ | Clock duty cycle | — | 40 | — | 60 | % |
| $t_{RAN\_JIT}$ | Random Jitter | — | — | — | $3^2$ | ps |
| $t_{P2P\_JIT}$ | Period to Period Jitter | — | -100 | — | $100^3$ | ps |

**Notes:**
1. USB 2.0 is only supported in LIFCL-33U.
2. $t_{RAN\_JIT}$ 1.5M to Nyquist frequency (Clock frequency/2).
3. $t_{P2P\_JIT}$ is less than 10 MHz.

**Table 3.40. Hardened USB3 Specifications**

| Symbol | Description | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{REF\_CLK}$ | Reference Clock Frequency | — | | 25/50/60 | | MHz |
| $t_{OFFSET}$ | Clock offset | — | -150 | — | 150 | ppm |
| $t_{DUTY}$ | Clock duty cycle | — | 40 | — | 60 | % |
| $t_{RAN\_JIT}$ | Random Jitter | — | — | — | $3^2$ | ps |
| $t_{SKEW}$ | Clock Skew | — | — | — | 200 | ps |
| $t_{P2P\_JIT}$ | Period to Period Jitter | — | -75 | — | $75^3$ | ps |
| $v_{COMM}$ | Input Common Mode Level | — | 0 | — | AVDD--0.5 * Peak-Peak Differential swing[4] | V |

**Notes:**
1. USB 3.2 Gen 1 is only supported in LIFCL-33U -9 speed grade.
2. $t_{RAN\_JIT}$ 1.5M to Nyquist frequency (Clock frequency/2).
3. $t_{P2P\_JIT}$ is less than 10 MHz.
4. $V_{COMM}$ is only for external REFCLK:REFIN_CLK_EXT_P/N.

## 3.24. JTAG Port Timing Specifications

Over recommended operating conditions.

**Table 3.41. JTAG Port Timing Specifications**

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | TCK clock frequency | — | — | 25 | MHz |
| $t_{BTCPH}$ | TCK clock pulse width high | 20 | — | — | ns |
| $t_{BTCPL}$ | TCK clock pulse width low | 20 | — | — | ns |
| $t_{BTS}$ | TCK TAP setup time | 5 | — | — | ns |
| $t_{BTH}$ | TCK TAP hold time | 5 | — | — | ns |
| $t_{BTRF}$ | TAP controller TDO rise/fall time[1] | 100 | — | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | — | 14 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | — | 14 | ns |

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | — | 14 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | — | 25 | ns |

**Note:**

1. Based on default I/O setting of slow slew rate.
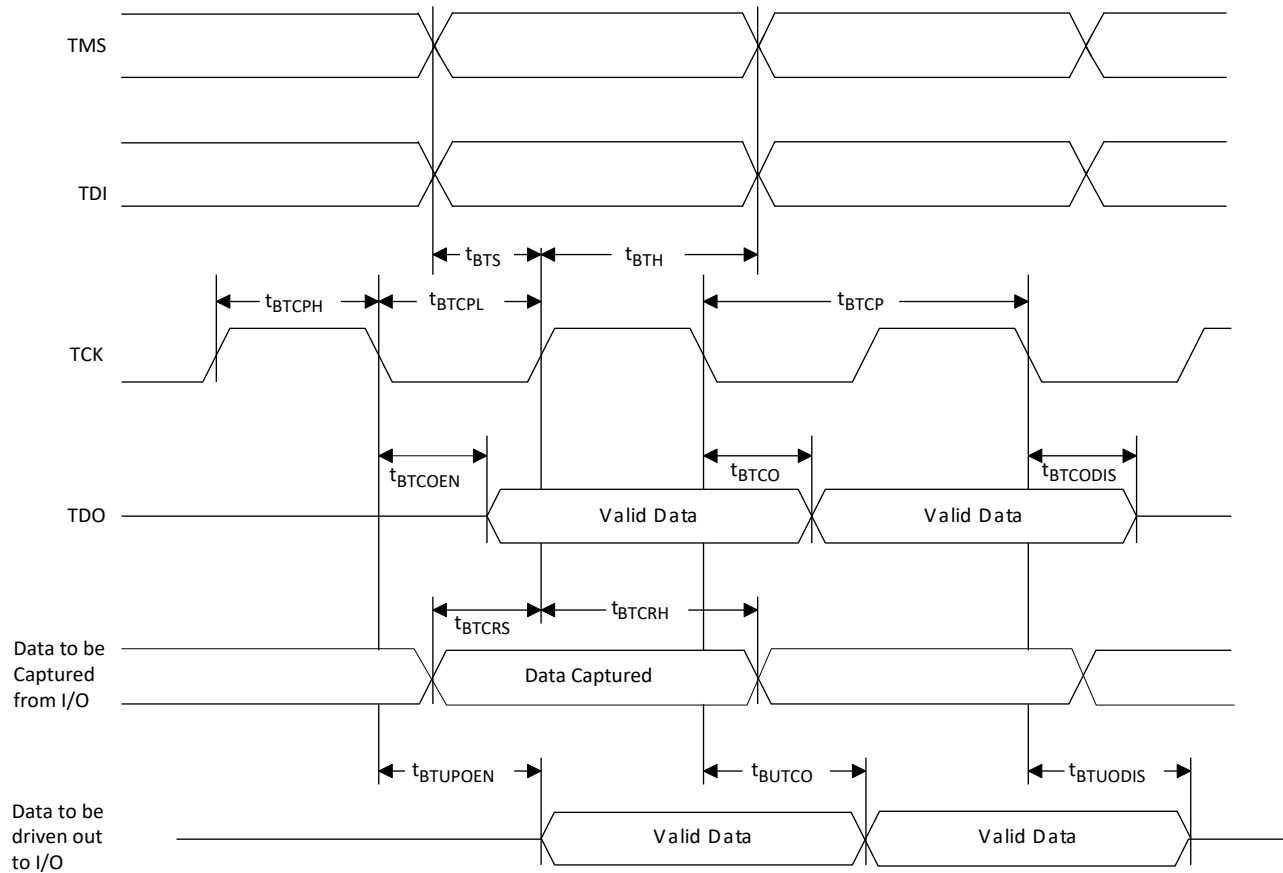


**Figure 3.24. JTAG Port Timing Waveforms**

## 3.25. Switching Test Conditions

Figure 3.25 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.42.
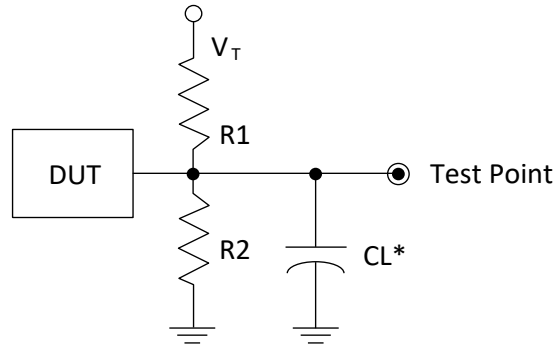
*CL Includes Test Fixture and Probe Capacitance

**Figure 3.25. Output Test Load, LVTTL, and LVCMOS Standards**

**Table 3.42. Test Fixture Required Components, Non-Terminated Interfaces**

| Test Condition | $R_1$ | $R_2$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|---|
| LVTTL and other LVCMOS settings (L ≥ H, H ≥ L) | ∞ | ∞ | 0 pF | LVCMOS 3.3 = 1.5 V | — |
| | | | | LVCMOS 2.5 = $V_{CCIO}$/2 | — |
| | | | | LVCMOS 1.8 = $V_{CCIO}$/2 | — |
| | | | | LVCMOS 1.5 = $V_{CCIO}$/2 | — |
| | | | | LVCMOS 1.2 = $V_{CCIO}$/2 | — |
| LVCMOS 2.5 I/O (Z ≥ H) | ∞ | 1 MΩ | 0 pF | $V_{CCIO}$/2 | — |
| LVCMOS 2.5 I/O (Z ≥ L) | 1 MΩ | ∞ | 0 pF | $V_{CCIO}$/2 | $V_{CCIO}$ |
| LVCMOS 2.5 I/O (H ≥ Z) | ∞ | 100 | 0 pF | $V_{OH} - 0.10$ | — |
| LVCMOS 2.5 I/O (L ≥ Z) | 100 | ∞ | 0 pF | $V_{OL} + 0.10$ | $V_{CCIO}$ |

**Note**: Output test conditions for all other interfaces are determined by the respective standards.

# 4. Pinout Information

## 4.1. Signal Descriptions

| Signal Name | Bank | Type | Description |
|---|---|---|---|
| **Power and GND** | | | |
| Vss, AVSSx, VSS_AON[1] | — | GND | Ground for internal FPGA logic, USB logic, Always ON (AON), and I/O |
| $V_{CC}$ | — | Power | Power supply pins for core logic. $V_{CC}$ is connected to 1.0 V (nom.) supply voltage. Power On Reset (POR) monitors this supply voltage. |
| $V_{CCAUXA}$ | — | Power | Auxiliary power supply pin for internal analog circuitry. This supply is connected to 1.8 V (nom.) supply voltage. POR monitors this supply voltage. |
| $V_{CCAUX}$ | — | Power | Auxiliary power supply pin for I/O Bank 0, Bank 1, and Bank 5. This supply is connected to 1.8 V (nom.) supply voltage, and is used for generating stable drive current for the I/O. |
| $V_{CCAUXHx}$ | — | Power | Auxiliary power supply pin for I/O Bank 2, Bank 3, and Bank 4. This supply is connected to 1.8 V (nom.) supply voltage and is used for generating stable current for the differential input comparators. |
| $V_{CCAUX\_AON}$[1] | 81 | Power | Auxiliary power for Always ON (AON) functional block |
| AVDD33[1] | 80 | Power | 3.3 V power for Hardened USB Block |
| AVDD18, AVDD18_TX, AVDD18_COM[1] | 80 | Power | 1.8 V power for Hardened USB Block |
| AVDD, AVDD_TX[1] | 80 | Power | 1.0 V power for Hardened USB Block |
| $V_{CCIOx}$ | 0-4[2]<br>0-5[3] | Power | Power supply pins for I/O bank x.<br>For x = 0, 1, and 5, VCCIO can be connected to (nom.) 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V.<br>For x = 2, 3, and 4, VCCIO can be connected to (nom.) 1.0 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.<br>There are dedicated and shared configuration pins in banks 0 and 1. POR monitors these banks supply voltages. |
| **Dedicated Pins** | | | |
| **Dedicated Configuration I/O Pin** | | | |
| JTAG_EN | 1 | Input | LVCMOS input pin. This input selects the JTAG shared GPIO to be used for JTAG<br>0 = GPIO<br>1 = JTAG |
| **Misc Pins** | | | |
| NC | — | — | No connect. |
| RESERVED | — | — | This pin is reserved and should not be connected to anything on the board. |
| **Always ON (AON) I/O Pins** | | | |
| AON_xxx[1] | 81 | Input, Output | Dedicated input and output pin for AON function |
| **USB I/O Pins** | | | |
| DP/DM, TX_M/P, RX_M/P | — | Input, Output | USB Data pins |
| REFIN_CLK_EXT_P/N | — | Input | USB Clock Pins |
| VBUS, REXT23 | — | Input, Output | USB Control pins |

| Signal Name | Bank | Type | Description |
|---|---|---|---|
| **General Purpose I/O Pins** | | | |
| P[T/B] [Number]_[A/B] | T = 0, 1, 5<br>B = 2, 3, 4 | Input,<br>Output,<br>Bi-Dir | Programmable User I/O:<br>[T/B/L/R] indicates the package pin/ball is in T (Top), B (Bottom) of the device.<br>[Number] identifies the PIO [A/B] pair.<br>[A/B] shows the package pin/ball is A or B signal in the pair. PIO A and PIO B are grouped as a pair.<br>Each A/B pair in the bottom banks supports true differential input and output buffers. When configured as differential input, differential termination of 100 Ω can be selected.<br>Each A/B pair in the top bank does not support true differential input or output buffer. It supports all single-ended inputs and outputs, and can be used for emulated differential output buffer.<br>Some of these user-programmable I/O are used during configuration, depending on the configuration mode. User needs to make appropriate connection on the board to isolate the two different functions before/after configuration.<br>Some of these user-programmable I/O are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/O for user logic.<br>During configuration the user-programmable I/O are tri-stated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tri-stated and default to have weak pull-down enabled after configuration. |
| **Shared Configuration Pins**<br>1. **These pins can be used for configuration during configuration mode. When configuration is completed, these pins can be used as GPIO, or shared function in GPIO. When these pins are used in dual function, the users need to isolate the signal paths for the dual functions on the board.**<br>2. **The pins used are defined by the configuration modes detected. Slave SPI or I$^2$C/I3C modes are detected during slave activation. Pins that are not used in the configuration mode selected are tri-stated during configuration, and can connect directly as GPIO in user's function.** | | | |
| PTxxx/SDA/USER_SDA | 1 | Input,<br>Output,<br>Bi-Dir | Configuration:<br>I$^2$C/I3C Mode: SDA signal<br>User Mode:<br>PTxxx: GPIO<br>User_SDA: SDA signal for I$^2$C/I3C interface |
| PTxxx/SCL/USER_SCL | 1 | Input,<br>Output,<br>Bi-Dir | Configuration:<br>I$^2$C/I3C Mode: SCL signal<br>User Mode:<br>PTxxx: GPIO<br>User_SDA: SCL signal for I$^2$C/I3C interface |
| PTxxx/TDO/SSO | 1 | Input,<br>Output,<br>Bi-Dir | Configuration:<br>Slave SPI Mode: Slave Serial Output<br>User Mode:<br>PTxxx: GPIO<br>TDO: When JTAG_EN = 1, used as TDO signal for JTAG |
| PTxxx/TDI/SSI | 1 | Input,<br>Output,<br>Bi-Dir | Configuration:<br>Slave SPI Mode: Slave Serial Input<br>User Mode:<br>PTxxx: GPIO<br>TDI: When JTAG_EN = 1, used as TDI signal for JTAG |

| Signal Name | Bank | Type | Description |
|---|---|---|---|
| PTxxx/TMS/SCSN | 1 | Input, Output, Bi-Dir | Configuration:<br>Slave SPI Mode: Slave Chip Select<br>User Mode:<br>PTxxx: GPIO<br>TMS: When JTAG_EN = 1, used as TMS signal for JTAG |
| PTxxx/TCK/SCLK | 1 | Input, Output, Bi-Dir | Configuration:<br>Slave SPI Mode: Slave Clock Input<br>User Mode:<br>PTxxx: GPIO<br>TCK: When JTAG_EN = 1, used as TCK signal for JTAG |
| PTxxx/MCSNO | 0 | Input, Output, Bi-Dir | Configuration:<br>Flow-through Daisy Chain Mode: Chip Select Output<br>User Mode:<br>PTxxx: GPIO |
| PTxxx/MD3 | 0 | Input, Output, Bi-Dir | Configuration:<br>Master Quad SPI Mode: I/O3<br>User Mode:<br>PTxxx: GPIO |
| PTxxx/MD2 | 0 | Input, Output, Bi-Dir | Configuration:<br>Master Quad SPI Mode: I/O2<br>User Mode:<br>PTxxx: GPIO |
| PTxxx/MSI/MD1 | 0 | Input, Output, Bi-Dir | Configuration:<br>Master SPI Mode: Master Serial Input<br>Master Quad SPI Mode: I/O1<br>User Mode:<br>PTxxx: GPIO |
| PTxxx/MSO/MD0 | 0 | Input, Output, Bi-Dir | Configuration:<br>Master SPI Mode: Master Serial Output<br>Master Quad SPI Mode: I/O0<br>User Mode:<br>PTxxx: GPIO |
| PTxxx/MCSN/PCLKT0_1 | 0 | Input, Output, Bi-Dir | Configuration:<br>Master SPI Mode: Master Chip Select Output<br>User Mode:<br>PTxxx: GPIO<br>PCLKT0_0: Top PCLK Input |
| PTxxx/MCLK/PCLKT0_0 | 0 | Input, Output, Bi-Dir | Configuration:<br>Master SPI Mode: Master Clock Output<br>User Mode:<br>PTxxx: GPIO<br>PCLKT0_1: Top PCLK Input |
| PTxxx/PROGRAMN | 0 | Input, Output, Bi-Dir | Configuration:<br>PROGRAMN: Initiate configuration sequence when asserted LOW.<br>User Mode:<br>PTxxx: GPIO |

| Signal Name | Bank | Type | Description |
|---|---|---|---|
| PTxxx/INITN | 0 | Input, Output, Bi-Dir | Configuration:<br>INITN: Open Drain I/O pin. This signal is driven to LOW when configuration sequence is started, to indicate the device is in initialization state. This signal is released after initialization is completed, and the configuration download can start. User can keep drive this signal LOW to delay configuration download to start.<br>User Mode:<br>PTxxx: GPIO |
| PTxxx/DONE | 0 | Input, Output, Bi-Dir | Configuration:<br>DONE: Open Drain I/O pin. This signal is driven to LOW during configuration time. It is released to indicate the device has completed configuration. User can keep drive this signal LOW to delay the device to wake up from configuration.<br>User Mode:<br>PTxxx: GPIO |
| **Shared User GPIO Pins** | | | |
| 1. **Shared User GPIO pins are pins that can be used as GPIO, or functional pins that connect directly to specific functional blocks, when device enters into User Mode.**<br>2. **Declaring on assigning the pin as GPIO or specific functional pin is done by configuration bitstream, except JTAG pins.**<br>3. **JTAG pins are controlled by JTAG_EN signal. When JTAG_EN = 1, the pins are used for JTAG interface. When JTAG = 0, the pins are used as GPIO or specific functional pin defined by configuration bitstream.**<br>4. **Refer to package pin file.** | | | |
| **Shared JTAG Pins** | | | |
| PTxxx/TDO/yyyy | 1 | Input, Output, Bi-Dir | User Mode:<br>PTxxx: GPIO<br>TDO: When JTAG_EN = 1, used as TDO signal for JTAG<br>yyyy: Other possible selectable specific functional |
| PTxxx/TDI/yyyy | 1 | Input, Output, Bi-Dir | User Mode:<br>PTxxx: GPIO<br>TDI: When JTAG_EN = 1, used as TDI signal for JTAG<br>yyyy: Other possible selectable specific functional |
| PTxxx/TMS/yyyy | 1 | Input, Output, Bi-Dir | User Mode:<br>PTxxx: GPIO<br>TMS: When JTAG_EN = 1, used as TMS signal for JTAG<br>yyyy: Other possible selectable specific functional |
| PTxxx/TCK/ yyy | 1 | Input, Output, Bi-Dir | User Mode:<br>PTxxx: GPIO<br>TCK: When JTAG_EN = 1, used as TCK signal for JTAG<br>Yyyy: Other possible selectable specific functional |

| Signal Name | Bank | Type | Description |
|---|---|---|---|
| **Shared CLOCK Pins** | | | |
| 1. Some PCLK pins can also be used as GPLL reference clock input pin. Refer to **sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095).** | | | |
| PBxxx/PCLK[T,C][2,3,4]_[0-3]/yyyy | 2, 3, 4 | Input, Output, Bi-Dir | User Mode: <br> PBxxx: GPIO <br> PCLK: Primary Clock or GPLL Refclk signal <br>   [T,C] = True/Complement when using differential signaling <br>   [2,3,4] = Bank <br>   [0-3] Up to 4 signals in the bank <br> yyyy: Other possible selectable specific functional |
| PTxxx/PCLKT0_[0-1]/yyyy | 0 | Input, Output, Bi-Dir | User Mode: <br> PTxxx: GPIO <br> PCLKT: Primary Clock or GPLL Refclk signal (Only Single Ended) <br>   [0-1] Up to 2 signals in the bank <br> yyyy: Other possible selectable specific functional |
| PTxxx/PCLKT1_[0-3]/yyyy | 1 | Input, Output, Bi-Dir | User Mode: <br> PTxxx: GPIO <br> PCLKT: Primary Clock or GPLL Refclk signal (Only Single Ended) <br>   [0-2] Up to 3 signals in the bank <br> yyyy: Other possible selectable specific functional |
| PBxxx/PCLK2_[0-3]/yyyy | 2 | Input, Output, Bi-Dir | User Mode: <br> PBxxx: GPIO <br> yyyy: Other possible selectable specific functional |
| PBxxx/LLC_GPLL[T,C]_IN/yyyy | 4 | Input, Output, Bi-Dir | User Mode: <br> PBxxx: GPIO <br> LLC_GPLL: Lower Left GPLL Refclk signal (PLLCK) <br>   [T,C] = True/Complement when using differential signaling <br> yyyy: Other possible selectable specific functional |
| **Shared VREF Pins** | | | |
| PBxxx/VREF[2,3,4]_[1-2]/yyyy | 2, 3, 4 | Input, Output, Bi-Dir | User Mode: <br> PBxxx: GPIO <br> VREF: Reference Voltage for DDR memory function <br>   [2,3,4] = Bank <br>   [1-2] Up to VREFs for each bank <br> yyyy: Other possible selectable specific functional |

**Notes:**
1. AON and all AVDD signals are only supported in LIFCL-33U.
2. Bank 0 to Bank 4 are supported in LIFCL-33U only.
3. Bank 0 to Bank 5 are supported in LIFCL-33 only.

## 4.2. Pin Information Summary

| Pin Information Summary | | NX33-84WLCSP | NX33U-84WLCSP | NX33U-104FCCSP |
|---|---|---|---|---|
| **User I/O Pins** | | | | |
| General Purpose I/O per Bank | Bank 0 | 7 | 7 | 8 |
| | Bank 1 | 11 | 9 | 11 |
| | Bank 2 | 14 | 14 | 16 |
| | Bank 3 | 10 | 11 | 12 |
| | Bank 4 | 2 | 2 | 4 |
| | Bank 5 | 15 | 0 | 0 |
| Total Single-Ended User I/O | | 59 | 43 | 51 |
| Differential I/O Pairs | Bank 0 | 3 | 3 | 4 |
| | Bank 1 | 5 | 4 | 5 |
| | Bank 2 | 7 | 7 | 8 |
| | Bank 3 | 5 | 5 | 6 |
| | Bank 4 | 1 | 1 | 2 |
| | Bank 5 | 7 | 0 | 0 |
| Total Differential I/O Pairs | | 28 | 20 | 25 |
| **Power Pins** | | | | |
| VCC | | 5 | 5 | 7 |
| VCCAUX | | 5 | 5 | 5 |
| VCCIO | Bank 0 | 1 | 1 | 1 |
| | Bank 1 | 1 | 1 | 1 |
| | Bank 2 | 1 | 1 | 1 |
| | Bank 3 | 1 | 1 | 1 |
| | Bank 4 | 1 | 1 | 1 |
| | Bank 5 | 1 | 0 | 0 |
| Total Power Pins | | 16 | 15 | 17 |
| **GND Pins** | | | | |
| VSS | | 8 | 8 | 11 |
| Total GND Pins | | 8 | 8 | 11 |
| **USB Hardened Block Pins** | | | | |
| Hardened USB Pairs | | 0 | 3 | 4 |
| REXT23 | | 0 | 1 | 1 |
| VBUS | | 0 | 1 | 1 |
| AVDD | | 0 | 4 | 6 |
| AVSS | | 0 | 2 | 4 |
| **Always ON Block Pins** | | | | |
| Always ON I/O | | 0 | 2 | 2 |
| VCCAUX | | 0 | 1 | 1 |
| VSS | | 0 | 0 | 1 |

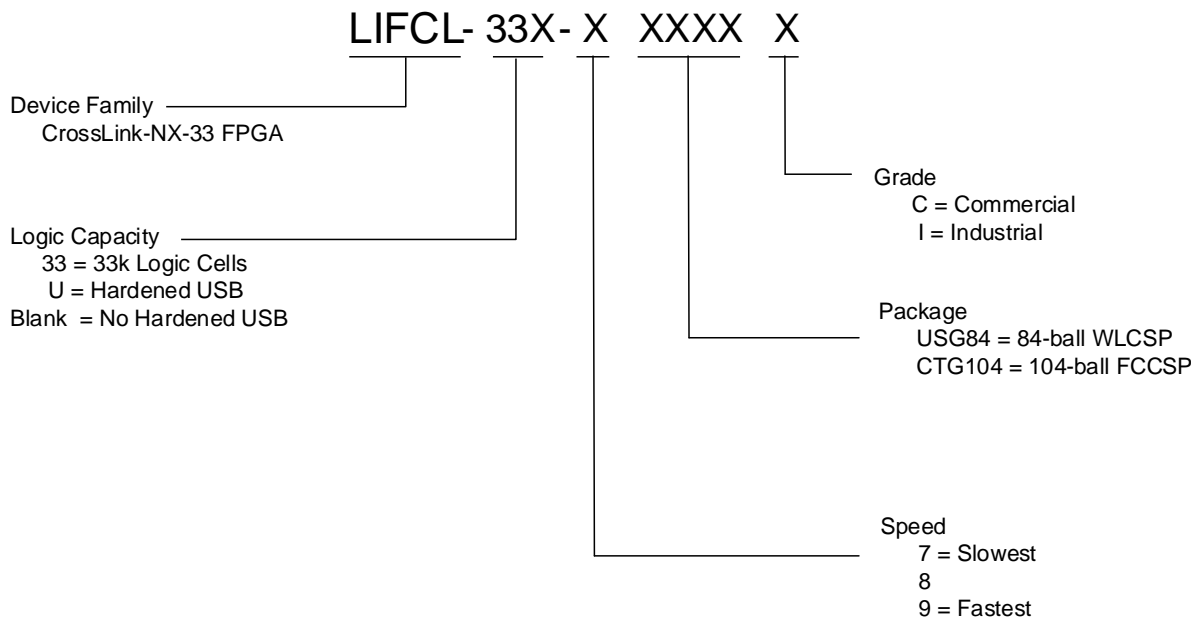| Pin Information Summary | | NX33-84WLCSP | NX33U-84WLCSP | NX33U-104FCCSP |
|---|---|:---:|:---:|:---:|
| **Dedicated Miscellaneous Pins** | | | | |
| JTAGEN | | 1 | 1 | 1 |
| **Shared Pins** | | | | |
| Shared Configuration Pins | Bank 0 | 7 | 7 | 7 |
| | Bank 1 | 9 | 8 | 9 |
| | Bank 2 | 0 | 0 | 0 |
| | Bank 3 | 0 | 0 | 0 |
| | Bank 4 | 0 | 0 | 0 |
| | Bank 5 | 0 | 0 | 0 |
| Shared JTAG Pins | Bank 0 | 0 | 0 | 0 |
| | Bank 1 | 4 | 4 | 4 |
| | Bank 2 | 0 | 0 | 0 |
| | Bank 3 | 0 | 0 | 0 |
| | Bank 4 | 0 | 0 | 0 |
| | Bank 5 | 0 | 0 | 0 |
| Shared PCLK Pins | Bank 0 | 0 | 0 | 0 |
| | Bank 1 | 4 | 4 | 4 |
| | Bank 2 | 8 | 8 | 8 |
| | Bank 3 | 8 | 8 | 8 |
| | Bank 4 | 2 | 2 | 2 |
| | Bank 5 | 0 | 0 | 0 |
| Shared GPLL Pins | Bank 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 |
| | Bank 2 | 0 | 0 | 0 |
| | Bank 3 | 0 | 0 | 0 |
| | Bank 4 | 0 | 0 | 2[1] |
| | Bank 5 | 0 | 0 | 0 |
| Shared VREF Pins | Bank 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 |
| | Bank 2 | 2 | 2 | 2 |
| | Bank 3 | 2 | 2 | 2 |
| | Bank 4 | 1 | 1 | 2 |
| | Bank 5 | 0 | 0 | 0 |

**Note:**

1.  GPLL is only supported in 104 package of LIFCL-33U.

# 5. Ordering Information

Lattice provides a wide variety of services for its products including custom marking, factory programming, known good die, and application specific testing. Contact the local sales representatives for more details.

## 5.1. Part Number Description

LIFCL- 33X- X  XXXX  X

Device Family
CrossLink-NX-33 FPGA

Logic Capacity
33 = 33k Logic Cells
U = Hardened USB
Blank = No Hardened USB

Speed
7 = Slowest
8
9 = Fastest

Package
USG84 = 84-ball WLCSP
CTG104 = 104-ball FCCSP

Grade
C = Commercial
I = Industrial

**Note:** ECC is only available on CTG104 -8 and -9 speed grade devices. USB 3.2 Gen 1 is only supported in LIFCL-33U -9 speed grade.

## 5.2. Ordering Part Numbers

### 5.2.1. Commercial

| Part Number | Speed | Package | Pins | Grade | Logic Cells (k) |
|---|---|---|---|---|---|
| LIFCL-33-8USG84C | −8 | Lead free WLCSP | 84 | Commercial | 33 |
| LIFCL-33U-7CTG104C | −7 | Lead free FCCSP | 104 | Commercial | 33 |
| LIFCL-33U-8USG84C | −8 | Lead free WLCSP | 84 | Commercial | 33 |
| LIFCL-33U-8CTG104C | −8 | Lead free FCCSP | 104 | Commercial | 33 |
| LIFCL-33U-9CTG104C | −9 | Lead free FCCSP | 104 | Commercial | 33 |

### 5.2.2. Industrial

| Part Number | Speed | Package | Pins | Grade | Logic Cells (k) |
|---|---|---|---|---|---|
| LIFCL-33-8USG84I | −8 | Lead free WLCSP | 84 | Industrial | 33 |
| LIFCL-33U-7CTG104I | −7 | Lead free FCCSP | 104 | Industrial | 33 |
| LIFCL-33U-8USG84I | −8 | Lead free WLCSP | 84 | Industrial | 33 |
| LIFCL-33U-8CTG104I | −8 | Lead free FCCSP | 104 | Industrial | 33 |
| LIFCL-33U-9CTG104I | −9 | Lead free FCCSP | 104 | Industrial | 33 |

# References

- CrossLink-NX web page

A variety of technical notes for LIFCL-33/33U devices are available.

- CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280)
- CrossLink-NX Single Event Upset (SEU) Report (FPGA-TN-02174)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- $I^2$C Hardened IP User Guide for Nexus Platform (FPGA-TN-02142)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- Multi-Boot User Guide for Nexus Platform (FPGA-TN-02145)
- Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075)
- Soft Error Detection (SED)/Correction (SEC) User Guide for Nexus Platform (FPGA-TN-02076)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysDSP User Guide for Nexus Platform (FPGA-TN-02096)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- Thermal Management (FPGA-TN-02044)
- Using TraceID (FPGA-TN-02084)

For more information on the LIFCL-33/33U-related IP, reference designs, and board documents, refer to the following pages:

- IP and Reference Designs for CrossLink-NX
- Development Kits and Boards for CrossLink-NX

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL) – www.jedec.org

Other references:

- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Radiant FPGA design software

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

# Revision History

**Revision 1.0, July 2024**

| Section | Change Summary |
|---|---|
| All | Moved document status to *Production Release*. |
| Acronyms in This Document | Added row for PIPE. |
| General Desciption | • Updated Table 1.1. LIFCL-33/33U Key Features to change AXI4-Streaming to *AXI protocol* and added speed grade limitations in USB2.0/USB3.2 section.<br>• Updated the following in Table 1.2. LIFCL-33/33U Commercial/Industrial Family Selection Guide:<br>  • Added table note and reference to table note for GPLL.<br>  • Added table note and reference to table note for USB2.0/USB3.2.<br>  • Removed Soft D-PHY table note. |
| Architecture | • Added document reference to AON IP User Guide in Always On (AON) section.<br>• Removed LS (1.5 Mbps) mode in USB section.<br>• Added document reference to USB 2.0/3.2 IPUG in USB RISC-V Firmware Stack and Host Software Interface section.<br>• Changed on board to *on-chip* and added document reference to OSC IPUG in On-Chip Oscillator.<br>• Changed Responder to *Target* in User I²C IP. |
| DC and Switching Characteristics for Commercial and Industrial | • Updated Table 3.1. Absolute Maximum Ratings:<br>  • Added $V_{CCAUXH2}$ and removed $V_{CCAUXH5}$.<br>  • Changed $V_{CCIO0, 1, 2, 6, 7}$ to $V_{CCIO0, 1, 5}$.<br>  • Changed $V_{CCIO3, 4, 5}$ to $V_{CCIO2, 3, 4}$.<br>  • Added reference to footnote 5 in AVDD33.<br>  • Changed to *All AVDD* in footnote 5.<br>• Updated the following in Table 3.2. Recommended Operating Conditions:<br>  • Changed $V_{CCAUXH2/3/4/5}$ to $V_{CCAUXH2/3/4}$.<br>  • Added reference to footnote 5 in AVDD33.<br>  • Changed to *All AVDD* in footnote 5.<br>• Added reference to footnote 2 in Power Supply Ramp Rates2 section.<br>• Fixed Differential typo in footnote of Table 3.5. On-Chip Termination Options for Input Modes.<br>• Fixed typo from $T_A$ 25 to $T_A = 25$ in Table 3.9. Capacitors – Wide Range and Table 3.10. Capacitors – High Performance.<br>• Updated MIPI D-PHY to *MIPI_DPHY* in Table 3.13. sysI/O Recommended Operating Conditions.<br>• Updated the following in Table 3.29. Maximum I/O Buffer Speed:<br>  • Updated LVDS, SLVS, and MIPI D-PHY in Maximum sysI/O Output Frequency Differential section to collapse rows and updated values for USG84 and CTG104 packages.<br>  • Changed MIPI LP and MIPI HS table note to *MIPI D-PHY LP and MIPI D-PHY HS*.<br>• Updated the following in Table 3.33. External Switching Characteristics (VCC = 1.0 V):<br>  • Added -9 device column and values.<br>  • Updated -8 and -7 Min values for $t_{SU}$ and $t_{H\_DELPLL}$ to *0*.<br>  • Updated -8 Max value for Generic DDRX2 I/O with Clock and Data Centered ½ UI from 500 to —.<br>  • Updated $f_{DATA\_GDDRX4}$ to keep it in one row and Max values for -8 and 7 at 1200 and 1034, respectively; updated Description to *Input/Output Data Rate*.<br>• Updated Table 3.37. sysCONFIG Port Timing Specifications to change $t_{PROGRAMN}$ to $t_{PROGRAMN\_L}$ and added row for $t_{PROGRAMN\_H}$.<br>• Added Figure 3.23. Configuration Error Notification.<br>• Added footnote in Table 3.38. AON Block Specification (VCCAUX_AON = 1.8 V). |

| Section | Change Summary |
|---------|----------------|
| | • Updated the following in Hardened USB Specifications:<br>  • Updated table name to Table 3.39. Hardened USB2 Specifications, removed t$_{SKEW}$ row, updated f$_{REF\_CLK}$ row values to merge Min, Typ, and Max cells, updated max value of t$_{RAN\_JIT}$, updated row of t$_{P2P\_JIT}$ including symbol name, and added footnotes and reference to footnotes.<br>  • Added Table 3.40. Hardened USB3 Specifications. |
| Pinout Information | • Updated to *All AVDD* for footnote 1 in Signal Descriptions.<br>• Updated Pin Information Summary table to add table note and reference to table note for GPLL Bank 4 (NX33U-104FCCSP). |
| Ordering Information | • Updated Part Number Description to add 9 speed grade and updated note for ECC (including adding support information for USB 3.2 Gen 1).<br>• Updated Ordering Part Numbers tables to add OPN for 9 CTG104 . |

### Revision 0.94, February 2024

| Section | Change Summary |
|---------|----------------|
| Architecture | • Updated DDRDLL and Input Register Block section to remove DQSBUF information.<br>• Updated Edge Clock and sysI/O Buffer to remove DDR information.<br>• Removed DLL Calibrated DQS Delay and Control Block section. |
| DC and Switching Characteristics for Commercial and Industrial | • Updated SubLVDS (Input Only) section to remove SMIA information.<br>• Updated Figure 3.15. Slave SPI/I2C/I3C POR/REFRESH Timing to remove tICFG_POR, tACT_CCLK, tACT_SCL and adjusted VCC/VCCAUX/VCCIO0/VCCIO1, REFRESH Command, CCLK, SSI, SCL, and SDA signals, adjusted rising edge of PROGRAMN, and changed tACT_CRESETB_N to tACT_PROGRAMN_H in the timing diagram.<br>• Updated Table 3.29. Maximum I/O Buffer Speed to remove DDR3/3L footnote.<br>• Updated GDDRX4 Inputs/Outputs with Clocks and Data Centered values in Table 3.33. External Switching Characteristics (VCC = 1.0 V). |

### Revision 0.93, December 2023

| Section | Change Summary |
|---------|----------------|
| All | • Updated document title to *CrossLink-NX-33 and CrossLinkU-NX*.<br>• Used *LIFCL-33/33U* to refer to the CrossLink-NX-33 and CrossLinkU-NX devices across the document. |
| Disclaimers | Updated this section. |
| General Description | Updated Table 1.2. LIFCL-33/33U Commercial/Industrial Family Selection Guide to change device name to *LIFCL-33* and *LIFCL-33U*. |
| Architecture | • Updated Figure 2.7. Clocking to remove LMID and RMID and update number of PCLK pin for top and bottom I/O banks.<br>• Updated Figure 2.14. Comparison of General DSP, LIFCL-33, and LIFCL-33U Approaches to change to Function Implemented in *LIFCL-33* and *LIFCL-33U*. |
| DC and Switching Characteristics for Commercial and Industrial | Updated Table 3.31. Register-to-Register Performance to change Large Memory Function values to 195, 170, and 115, add table note reference to 1, 2, and 3, and change performance grade in table note 1 to *8*. |
| References | Changed section name from Supplemental Information to *References*. |
| Technical Support Assistance | Added this section. |

**Revision 0.92, September 2023**

| Section | Change Summary |
|---|---|
| All | • Added CrossLink-NX-33U support, including AON and USB, across the document.<br>• Changed document title from CrossLink-NX-33 to *CrossLink-NX-33 and CrossLink-NX-33U*. |
| Acronyms in This Document | • Added AON, GPIO, MPS, and USB definition.<br>• Removed PCS from the acronym list. |
| General Description | • Added USB 2.0, USB 3.2 Gen 1, and AON information for CrossLink-NX-33U only.<br>• Restructured the Features section by adding Table 1.1. CrossLink-NX-33 and CrossLink-NX-33U Key Features and updating the following in the table:<br>  • Changed programmable sysI/O from 68 to *60*.<br>  • Updated support from 1.5 Gbps to *1.2 Gbps*.<br>  • Removed *SEU Mitigation Support* and its sub-items from the Cryptographic Engine section and added it as another main section.<br>  • Removed AXI4-Streaming as main section and moved it under *Internal Bus Interface Support* section.<br>  • Added AON and USB 2.0/USB 3.2 Gen 1 sections.<br>• Updated the following in Table 1.2. CrossLink-NX-33 and CrossLink-NX-33U Commercial/Industrial Family Selection Guide:<br>  • Changed table name to add CrossLink-NX-33U.<br>  • Added column for CrossLink-NX-33U.<br>  • Added USB 2.0/USB 3.2 Gen 1 and AON support.<br>  • Added 104 FCCSP package.<br>  • Changed cell title to *Total I/O (Wide Range, High Performance)* and adjusted format.<br>  • Updated support from 1.5 Gbps to *1.2 Gbps*. |
| Architecture | • Added Figure 2.2. CrossLink-NX-33U Simplified Block Diagram.<br>• Updated Figure 2.14. Comparison of General DSP, CrossLink-NX-33, and CrossLink-NX-33U Approaches to add CrossLink-NX-33U.<br>• Added text in sysI/O Banking Scheme specifying Bank 5 is supported in CrossLink-NX-33 and AON and USB signals in CrossLink-NX-33U only.<br>• Added Always On (AON) and USB sections.<br>• Updated Figure 2.29. Cryptographic Engine Block Diagram to change Unique ID to *Unique Device Secret* and HMAC SHA256 to *HMAC256*. |

| Section | Change Summary |
|---|---|
| DC and Switching Characteristics for Commercial and Industrial | • Updated the following in Table 3.1. Absolute Maximum Ratings:<br>  • Added $V_{CCAUX\_AON}$ and AVDD, AVDD_TX.<br>  • Changed $V_{CCA\_DPHY0, 1}$ to AVDD33 and updated Max value to 3.63.<br>  • Changed $V_{CC\_DPHY0, 1}$ to AVDD18, AVDD18_TX, AVDD18_COM and updated Max value to 1.98.<br>• Added VCCAUX_AON and rows for AVDD33, AVDD, AVDD_TX, AVDD18, AVDD18_TX, AVDD18_COM, and and AVDD, AVDD_TX in Table 3.2. Recommended Operating Conditions.<br>• Updated Table 3.14. sysI/O DC Electrical Characteristics – Wide Range I/O to change LVCMOS10 VIL Min value to 0.35 x VCCIO.<br>• Updated the following in Table 3.33. External Switching Characteristics (VCC = 1.0 V):<br>  • Added column and values for -7 speed grade.<br>  • Updated unit for $t_{H\_DEL}$ (Bottom).<br>  • Changed -8 speed grade value of $f_{MAX\_GDDR2}$ to blank.<br>  • Updated $f_{DATA\_GDDRX4\_MP}$ to add rows per package.<br>• Added AON Block Specifications (VCCAUX_AON = 1.8V) and Hardened USB Specifications sections. |
| Pinout Information | • Updated the following in Signal Descriptions:<br>  • Added AVSSx and $V_{SS\_AON}$ in $V_{SS}$ signal and updated description to add USB logic and AON.<br>  • Added rows for AVDD33, AVDD, AVDD_TX, AVDD18, AVDD18_TX, AVDD18_COM, and REFIN_CLK_EXT_P/N.<br>  • Added table notes and reference to table notes to specify that AON and AVDD signals are supported in CrossLink-NX-33U as well as Bank 0-4, and Bank 0-5 are supported in CrossLink-NX-33.<br>• Added Pin Information Summary. |
| Ordering Information | • Added new package option CTG104, -7 speed grade, and note for -8 speed grade in Part Number Description, as well as updated Logic Capacity to add Hardened USB.<br>• Added CrossLink-NX-33U part numbers in Ordering Part Numbers.<br>• Updated Commercial and Industrial tables to change column name from Temp to *Grade*. |
| Supplemental Information | • Updated document links, rearranged list in alphabetical order, and updated document name for High-Speed I/O Interface and Hardware Checklist documents.<br>• Added references to the CrossLink-NX, Lattice Insights, and Lattice Radiant Web Page, IP Core, Reference Design, and Evaluation Board documents. |

## Revision 0.91, March 2023

| Section | Change Summary |
|---|---|
| Acronyms in This Document | Removed MLVDS in the table. |
| Architecture | Adjustment in formatting to move Clocking Structure as sub-section under the Architecture section. |
| Supplemental Information | Added link for High Speed PCB Design Considerations (FPGA-TN-02178). |
| Technical Support Assistance | Added this section. |

**Revision 0.90, November 2022**

| Section | Change Summary |
|---|---|
| All | Removed EBR-ECC references across the document. |
| Architecture | • Removed HSUL and SSTL references in the following sections and tables:<br>  • sysI/O Buffer<br>  • Supported sysI/O Standards<br>  • Table 2.10. Single-Ended I/O Standards<br>  • Table 2.11. Differential I/O Standards<br>  • Table 2.12. Single-Ended I/O Standards Supported on Various Sides<br>  • Table 2.13. Differential I/O Standards Supported on Various Sides |
| DC and Switching Characteristics for Commercial and Industrial | • Removed Differential SSTL135D/SSTL15D and HSUL12D sections.<br>• Added row for tJIND and removed VCCIO DDR3L in Table 3.2. Recommended Operating Conditions.<br>• Updated max value of VCCAUX for VPORUP and VPORDN in Table 3.4. Power-On Reset.<br>• Removed HSUL and SSTL references in Table 3.5. On-Chip Termination Options for Input Modes and Table 3.29. Maximum I/O Buffer Speed.<br>• Removed table note referring to DDR3L and HSUL/SSTL references in Table 3.13. sysI/O Recommended Operating Conditions.<br>• Updated VOL (max), VOH (min), IOL and IOH for LVTTL33/LVCMOS33 and LVCMOS25 in Table 3.14. sysI/O DC Electrical Characteristics – Wide Range I/O.<br>• Updated VIH (min) in HSTL15_I and removed SSTL and HSUL standards in Table 3.15. sysI/O DC Electrical Characteristics – High Performance I/O.<br>• Updated SE Input Termination min value from 71 to 67 in Table 3.16. I/O Resistance Characteristics.<br>• Updated Large Memory Function values in Table 3.31. Register-to-Register Performance.<br>• Updated the following in Table 3.33. External Switching Characteristics (VCC = 1.0 V):<br>  • Updated max values of fMAX_PRI and tSKEW_PRI, and min value of tW_PRI in Primary Clock.<br>  • Updated max values of fMAX_EDGE and tSKEW_EDGE, and min value of tW_EDGE in Edge Clock.<br>  • Updated tCO max value, min value of tSU, tH, tSU_DEL, tH_DEL (top), and added tH_DEL (bottom) in General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL.<br>  • Updated max value of tCO_PLL, min value of tSU_PLL (top), tH_PLL, tSU_DELPLL, tH_DELPLL, and added tSU_PLL (bottom) in General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL.<br>  • Updated Generic DDR Input/Output group to reflect correct values.<br>  • Removed SSTL and HSUL references in footnote 2.<br>  • Added footnote and reference to footnote 6.<br>• Updated entire content of Table 3.37. sysCONFIG Port Timing Specifications to reflect correct values. |
| Ordering Information | Updated section content, Including diagram, to remove -7 speed grade. |

**Revision 0.81, September 2022**

| Section | Change Summary |
|---|---|
| All | Minor changes in formatting, including removing product name from heading, figure, and table names. |
| DC and Switching Characteristics for Commercial and Industrial | • Added Table 3.17. VIN Maximum Overshoot/Undershoot Allowance – Wide Range and Table 3.18. VIN Maximum Overshoot/Undershoot Allowance – High Performance.<br>• Updated footnote reference in the Differential groups in Table 3.29. Maximum I/O Buffer Speed.<br>• Updated DSP functions in Table 3.31. Register-to-Register Performance.<br>• Updated the following in Table 3.34. sysCLOCK PLL Timing (VCC = 1.0 V) – Commercial/Industrial:<br>  • Raised minimum input clock frequency from 10 to 18 MHz.<br>  • Raised minimum phase detector input frequency from 10 to 18 MHz; removed table note and table note reference.<br>  • Corrected $t_{PH}$ footnote.<br>  • Removed and Added conditions for the $t_{OPJIT}$ parameter to accurately reflect PLL jitter performance. |

**Revision 0.80, June 2022**

| Section | Change Summary |
|---|---|
| All | • Changed document status to Preliminary.<br>• Minor adjustments in formatting across the document. |
| Acronyms in This Document | • Removed definition for ADC and DTR. |
| Introduction | • Added note for ECC in Flexible Memory Resources bullet point.<br>• Updated Table 1.1. CrossLink-NX-33 Commercial/Industrial Family Selection Guide to change I/O count for 84 WLCSP to 34/26. |
| CrossLink-NX-33 Architecture | • Updated Figure 2.1. CrossLink-NX-33 Simplified Block Diagram.<br>• Added information on select speed grades in sysMEM Memory Block.<br>• Updated TD[1:0] parameter name to T[1:0] in Table 2.8. Tri-state Block Port Description.<br>• Updated DELAY CODE to DELAYCODE_I and DELAYCODE_O in Figure 2.23. DQS Control and Delay Block (DQSBUF). |
| DC and Switching Characteristics for Commercial and Industrial | • Added Commercial and Industrial grade information in ESD Performance.<br>• Updated Figure 3.21. Master SPI Wake-Up Timing and Figure 3.22. Slave SPI/I2C/I3C Wake-Up Timing to change $t_{DONE\_HIGH}$ to $t_{WAKEUP\_DONE\_HIGH}$.<br>• Updated LVDS and subLVDS $V_{CCIO}$ (Input) value; Updated table note 1b and d to change bank 3, bank 4, and bank 5 to bank 2, bank 3, and bank 4 in Table 3.13. sysI/O Recommended Operating Conditions.<br>• Updated information for $V_{CCAUX}$ in LVDS.<br>• Updated $V_{IH}$, $V_{IL}$, $I_{OL}$, $I_{OH}$ values and table notes in Table 3.14. sysI/O DC Electrical Characteristics – Wide Range I/O and Table 3.15. sysI/O DC Electrical Characteristics – High Performance I/O.<br>• Changed $V_{INN}$ to $V_{INM}$ in table note 2 and added table note 3 in Table 3.17. LVDS DC Electrical Characteristics.<br>• Added table note for $V_{ICM}$ in Table 3.19. SubLVDS Input DC Electrical Characteristics (Over Recommended Operating Conditions).<br>• Updated max value of $Z_{OS}$ in Table 3.22. SLVS Output DC Characteristics.<br>• Updated max value of $Z_{OS}$ in Table 3.24. Soft D-PHY Output Timing and Levels.<br>• Updated max value of HSTL15 in Table 3.27. CrossLink-NX-33 Maximum I/O Buffer Speed.<br>• Updated Generic DDRX1 group to add WRIO and HPIO in Table 3.31. CrossLink-NX-33 External Switching Characteristics (VCC = 1.0 V). |

| Section | Change Summary |
|---|---|
| CrossLink-NX-33 Pinout Information | Adjustment in formatting to remove superscripts for Shared Configuration Pins, Shared User GPIO Pins, and Shared CLOCK Pins; Updated signal names and description, specifically for Bank 1, for Shared JTAG Pins, Shared Configuration Pins, and Shared CLOCK Pins in Signal Descriptions. |
| CrossLink-NX-33 Ordering Information | • Added note regarding availability of Input Comparator, ADC, EBR, ECC, and DTR in select speed grades.<br>• Added Ordering Part Numbers section. |

**Revision 0.70, November 2021**

| Section | Change Summary |
|---|---|
| All | Advance release |