Evaluating the AD5683R (SPI) and the AD5693R (I^2C) Single-Channel, 16-Bit, Serial, Voltage Output DACs

FEATURES

- Full-featured evaluation boards for the AD5683R (SPI) and AD5693R (I^2C)
- On-board reference
- Various link options
- PC control in conjunction with the Analog Devices, Inc., EVAL-SDP-CK1Z (SDP-K1) controller board

EVALUATION KIT CONTENTS

- EVAL-AD5683RARDZ (SPI) or EVAL-AD5693RARDZ (I^2C) evaluation board
- AD5683R (SPI) or AD5693R (I^2C) device

HARDWARE REQUIRED

- EVAL-SDP-CK1Z (SDP-K1) controller board, which must be purchased separately

SOFTWARE REQUIRED

- Analysis | Control | Evaluation (ACE) Software, which is available for download from the EVAL-AD5683RARDZ (SPI) or EVAL-AD5693RARDZ (I^2C) product page

TYPICAL EVALUATION BOARD SETUP

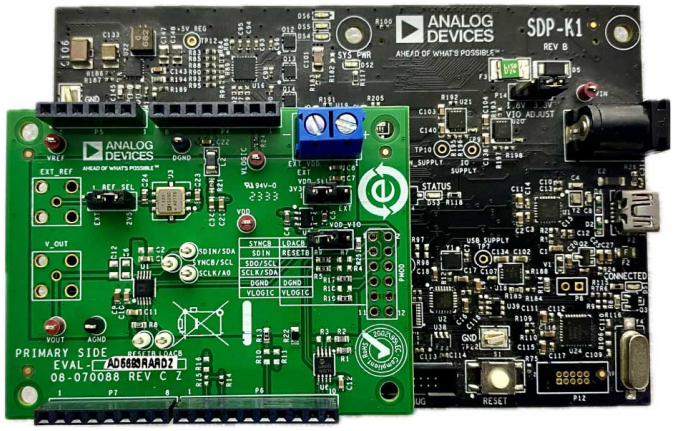

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Figure 1. Evaluation Board Connected to the SDP-K1 Controller Board (EVAL-AD5683RARDZ or EVAL-AD5693RARDZ Version)

GENERAL DESCRIPTION

This user guide details the operation of the EVAL-AD5683RARDZ (serial peripheral interface (SPI)) evaluation board and the EVAL-AD5693RARDZ (I^2C) evaluation board for the AD5683R (SPI) and the AD5693R (I^2C), respectively, which are both single-channel, serial voltage output digital-to-analog converters (DACs).

The EVAL-AD5683RARDZ and the EVAL-AD5693RARDZ are designed to facilitate quick prototyping of the AD5683R and AD5693R circuits, thereby reducing design time. Both devices operate from a single 2.7 V to 5.5 V supply. Additionally, these devices also incorporate an internal 2.5 V on-board reference. A different reference voltage can be applied via the EXT_REF SMB connector, if required. While sharing common features, the two DACs differ in their digital interface protocols. The AD5683R employs SPI, while the AD5693R employs I^2C.

The EVAL-AD5683RARDZ and the EVAL-AD5693RARDZ interface with the USB port of a PC via the System Demonstration Platform (SDP) controller board (EVAL-SDP-CK1Z (SDP-K1)). The Analysis | Control | Evaluation (ACE) software is available for download from both the EVAL-AD5683RARDZ product page and the EVAL-AD5693RARDZ product page. This software can be used with either evaluation board to allow the user to program the AD5683R and AD5693R, respectively. A PMOD connection is also available to allow the connection of a microcontroller to either evaluation board. Note that when a microcontroller is used through the PMOD connection, the EVAL-SDP-CK1Z (SDP-K1) must be disconnected, and the user cannot use the ACE software.

The EVAL-AD5683RARDZ and the EVAL-AD5693RARDZ both require the EVAL-SDP-CK1Z (SDP-K1) controller board, which is available for purchase from Analog Devices.

For full details on the AD5683R and the AD5693R, see the AD5683R and AD5693R data sheets, which must be consulted in conjunction with this user guide when using either of the EVAL-AD5683RARDZ or the EVAL-AD5693RARDZ evaluation boards.

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REVISION HISTORY

1/2024—Revision 0: Initial Version

GETTING STARTED

INSTALLING THE SOFTWARE

The EVAL-AD5683RARDZ and EVAL-AD5693RARDZ evaluation boards use the **Analysis | Control | Evaluation (ACE)** software, a desktop software application that allows the evaluation and control of multiple evaluation systems.

The ACE software is available for download on the EVAL-AD5683RARDZ or EVAL-AD5693RARDZ evaluation board page and must be installed before connecting the EVAL-SDP-CK1Z (SDP-K1) controller board to the USB port of the PC to ensure that the EVAL-SDP-CK1Z (SDP-K1) is recognized when it connects to the PC. Note that the ACE software installs all the necessary SDP drivers and the Microsoft® .NET Framework 4 by default. For full instructions on how to install and use this software, see the ACE software page on the Analog Devices website.

After the ACE software installation completes and the software is opened, the EVAL-AD5683RARDZ or EVAL-AD5693RARDZ evaluation board plugin appears.

INITIAL SETUP

To set up the EVAL-AD5683RARDZ or EVAL-AD5693RARDZ evaluation board, take the following steps:

1. Connect the EVAL-AD5683RARDZ or EVAL-AD5693RARDZ to the EVAL-SDP-CK1Z (SDP-K1) controller board and then connect a USB cable between the SDP-K1 and the PC.
2. Run the ACE software, and the main window appears as shown in Figure 2. The EVAL-AD5683RARDZ or EVAL-AD5693RARDZ board plugins appear in the **Attached Hardware** section of the **Start** tab.
3. Double-click the board plugin to open the board view shown in Figure 3.
4. Double-click the **AD5683R** or **AD5693R** chip to access the chip view as shown in Figure 4. This view provides a basic representation of the functionality of the board. See Figure 5 and Table 1 for the details on the main function blocks of the board.

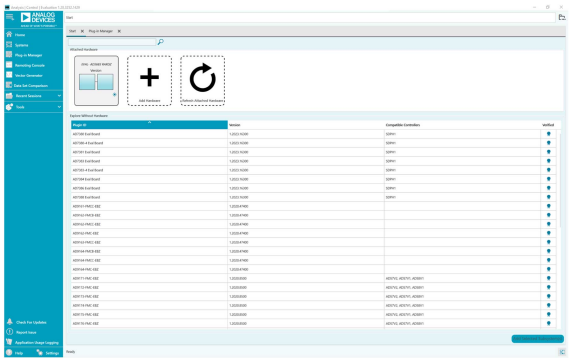

Figure 2. ACE Software Main Window

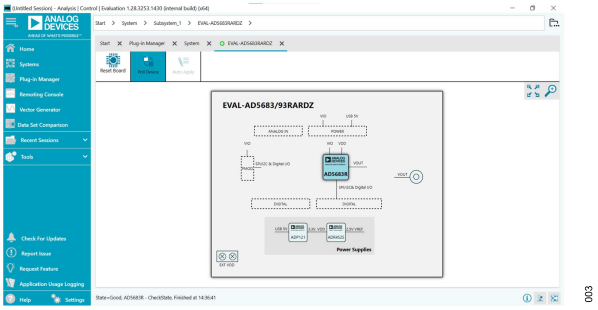

Figure 3. Board View of the EVAL-AD5683RARDZ or EVAL-AD5693RARDZ

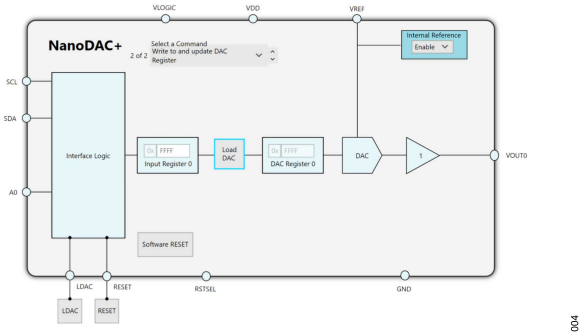

Figure 4. Chip Block Diagram View of the AD5683R or AD5693R

BLOCK DIAGRAM AND DESCRIPTION

The EVAL-AD5683RARDZ or EVAL-AD5693RARDZ software is organized so that it appears similar to the functional block diagram shown in the data sheets. In this way, it is easy to correlate the functions on the board with the descriptions in the data sheets. A full description of each block, register, and its settings is given in the AD5683R or AD5693R data sheets.

Some of the blocks and their functions are described in this section as they pertain to the EVAL-AD5683RARDZ or EVAL-AD5693RARDZ. The block diagram is shown in Figure 5, and Table 1 describes the functionality of each block.

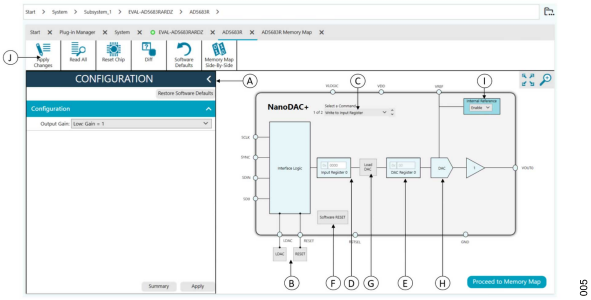

Figure 5. Block Diagram with Labels

Table 1. Block Diagram Functions

Label	Button/Function Name	Function
A	**CONFIGURATION**	This function is used to set the initial configuration for the evaluation board. Select the reference gain case from the **Output Gain** dropdown menu. A gain of 1 is the default. For a gain of 2, an external supply is needed (V_{DD} = V_{REF} + 1.5 V). After setting up the initial configuration, click **Apply Changes** (J) to apply the values. These settings can be modified at any stage while evaluating the board.
B	**LDAC** and **RESET** (GPIO buttons)	The **LDAC** and **RESET** buttons act as external GPIO pulses to the $\overline{LDAC}$ and $\overline{RESET}$ pins. The **LDAC** button transfers data from the input registers (D) to the DAC registers (E). The **RESET** button clears all data from input registers and DAC registers. These buttons are live; therefore, there is no need to click **Apply Changes** (J).
C	**Select a Command**	The **Select a Command** dropdown menu controls how the data transfer to the device affects the input and DAC registers. When a data value is entered in an input register (D), it can be transferred to one or both of the internal DAC registers. The data transfer can be either to the DAC input register only or to both the DAC input register and the DAC register simultaneously. If both registers are updated, the channel DAC register (E) shows the new value.
D	Input register	This function is used to select the 16-bit data-word to transfer to the device. Then, click **Apply Changes** (J) to transfer the selected 16-bit data-word to the device.
E	DAC register	This box displays the value that is currently present in the DAC register on the device. Selecting the appropriate command option or toggle **LDAC** (B) to update the DAC register.
F	**Software RESET**	Click **Software RESET** to return the evaluation board and software to their default values. This button is live; therefore, there is no need to click **Apply Changes** (J).
G	**Load DAC**	Click **Load DAC** to individually control which channel loads the values from the input register to the DAC register.
H	**DAC**	The DAC configuration options provide access to individual channel configuration options, such as power-down options and hardware $\overline{LDAC}$ mask enable and disable settings.
I	**Internal Reference**	In the **Internal Reference** area, select **Enable** from the dropdown menu to enable the on-chip reference for the evaluation board. If **Disable** is selected, an external reference must be applied.
J	**Apply Changes**	Click **Apply Changes** to update the device with all the modified values. However, if there is no evaluation board connected, the input register value is not transferred to the DAC register.

BLOCK DIAGRAM AND DESCRIPTION

MEMORY MAP

All registers are fully accessible from the memory map tab. The memory map allows registers to be edited at a bit level. The bits shaded in dark gray are read only bits and cannot be accessed from ACE. All other bits are toggled. Click **Apply Changes** to transfer data to the device. All changes here correspond to the block diagram; for example, if the internal register bit is enabled, it shows as enabled on the block diagram. Any bits or registers that are in bold are modified values that have not been transferred to the evaluation board. After clicking **Apply Changes**, data is transferred to the evaluation board.

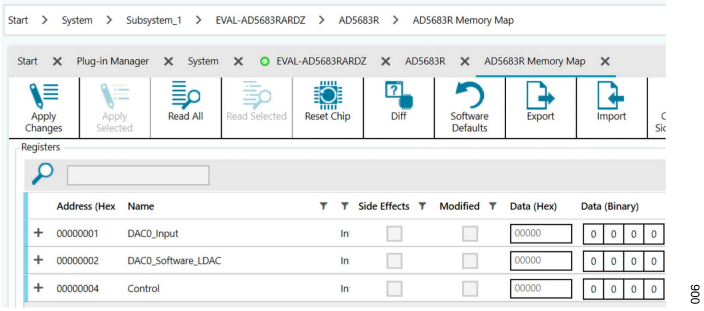

Figure 6. AD5683R or AD5693R Memory Map Tab

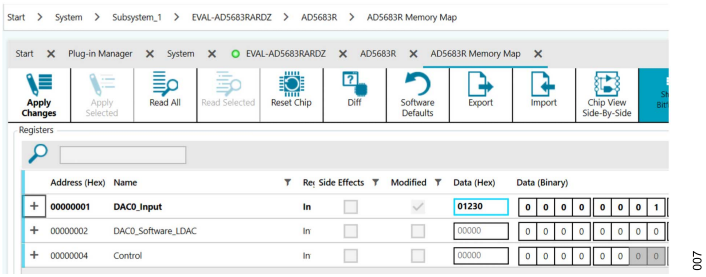

Figure 7. Memory Map of AD5683R or AD5693R with Pending Changes in the DAC0_Input Register

EVALUATION BOARD HARDWARE

Before applying power and signals to the EVAL-AD5683RARDZ or EVAL-AD5693RARDZ, ensure that all link positions are as required by the operating mode. The two modes available for operating the evaluation board are SDP control mode, which must be used with the EVAL-SDP-CK1Z (SDP-K1), or standalone mode where an external supply must be provided.

POWER SUPPLIES

The EVAL-AD5683RARDZ and EVAL-AD5693RARDZ evaluation boards provide an on-board, 3.3 V regulator powered through the USB supply. If the evaluation board is controlled through a PMOD, or a gain of 2 is required, an external supply must be provided via the EXT_VDD connectors. See Table 2 and the power requirements specifications in the AD5683R or AD5693R data sheets for additional details.

Both the AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location close to the AD5683R or AD5693R. To avoid ground loop problems, it is recommended that AGND and DGND not be connected elsewhere in the system.

All supplies are decoupled to ground with 10 µF and 0.1 µF capacitors.

Table 2. Power Supply Connectors

Connector	Label	External Voltage Supplies Description
EXT_VDD, Pin 1	EXT_VDD	External analog power supply from 2.7 V to 5.5 V, V_{DD}.
EXT_VDD, Pin 2	EXT_VDD	Analog ground.
EXT_REF, SMB Connector	EXT_REF	External voltage reference supply.

EVALUATION BOARD HARDWARE

LINK CONFIGURATION OPTIONS

A number of link and switch options are incorporated on the EVAL-AD5683RARDZ or EVAL-AD5693RARDZ evaluation board and must be set for the required operating conditions before using the board. The link function options are described in Table 4.

Table 3 lists the positions of the different links controlled by the PC via the USB port, and an SDP controller board operating in single-supply mode is required.

Table 3. Link Options Setup for SDP-K1 Control (Default)

Link	Options
VDD_SEL	Position A (1-2)
REF_SEL	Position A (1-2)
VDD_VIO	Disconnected

Table 4. Link Functions

Link	Function Options
VDD_SEL	This link selects the DAC analog voltage source.
	Position A (1-2): the 3V3 option selects the on-board voltage source (SDP-K1, ADP121).
	Position B (2-3): the VDD_EXT option selects an external supply voltage (EXT_VDD connector).
REF_SEL	This link selects the DAC voltage reference source.
	Position A (1-2): the VREF_EXToption selects an external reference source (EXT_REF connector). If no external supply is present, it defaults to the internal on-chip reference.
	Position B (2-3) the VREF_2V5 option selects the on-board reference from the ADR4525.
VDD_VIO	The VDD_VIO link selects the DAC digital voltage source. The following two options are available:
	Connected: shorts V_{DD} and V_{LOGIC}. Only use this option when the SDP-K1 controller board is not connected.
	Disconnected: opens the connection of V_{DD} and V_{LOGIC}. Only use this option when using the SDP-K1 controller board.

EVALUATION BOARD SCHEMATICS AND ARTWORK

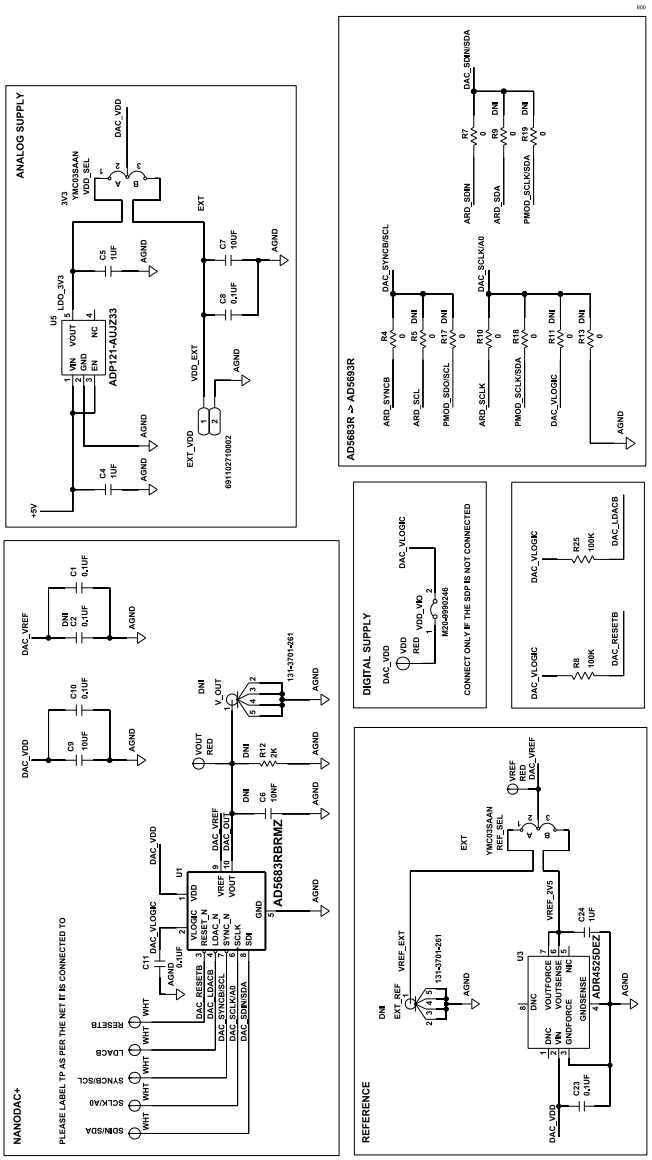

Figure 8. NanoDAC+ Evaluation Board Schematic Diagram, Power Supply and Signal Routes

EVALUATION BOARD SCHEMATICS AND ARTWORK

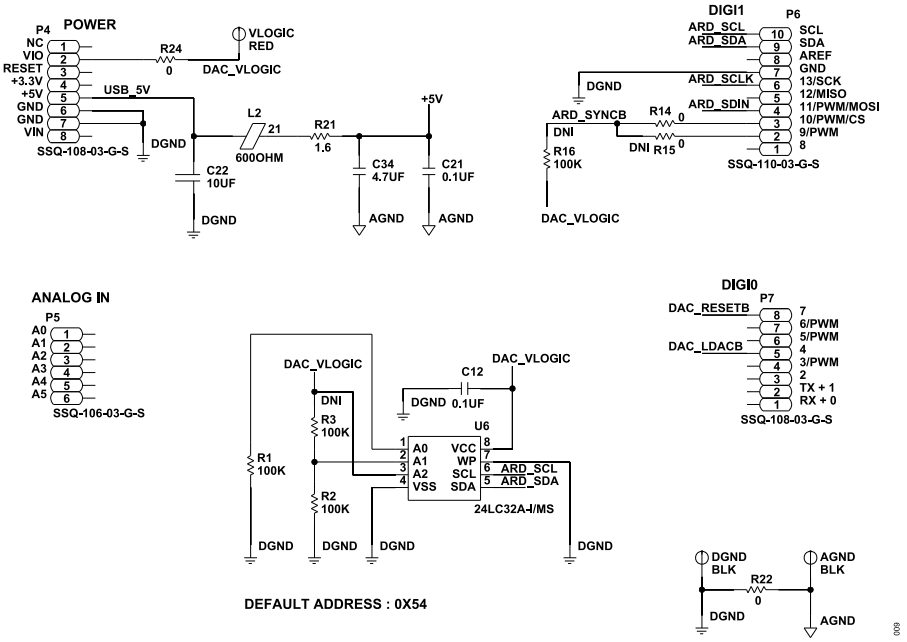

Figure 9. NanoDAC+ Evaluation Board Schematic Diagram, SDP Connector

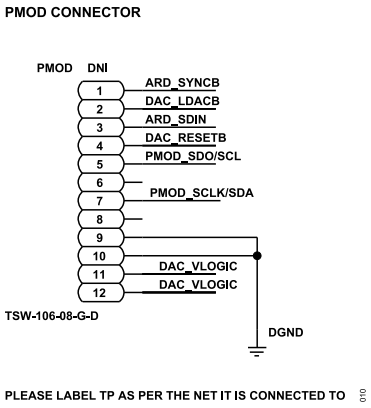

Figure 10. NanoDAC+ Evaluation Board Schematic Diagram, PMOD Connector

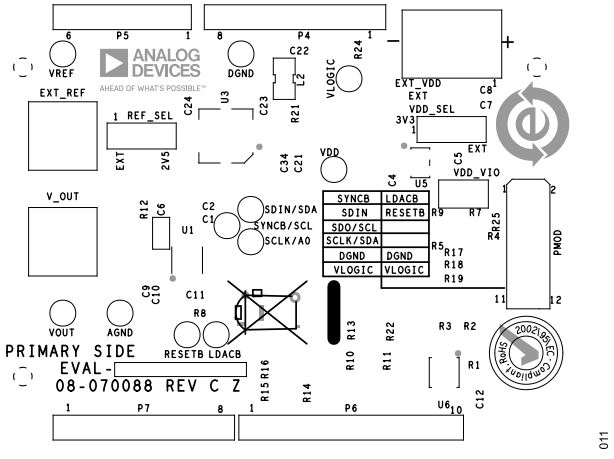

Figure 11. NanoDAC+ Evaluation Board, Component Placement

EVALUATION BOARD SCHEMATICS AND ARTWORK

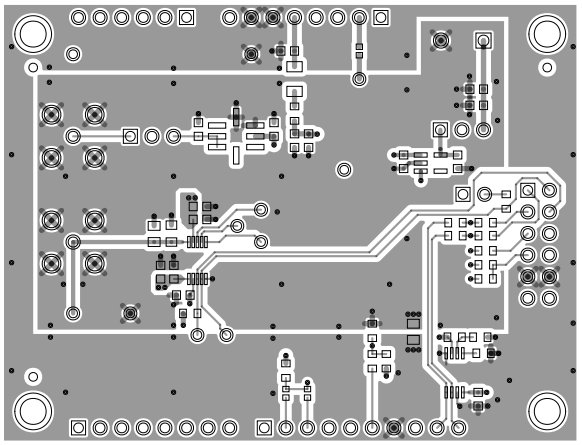

Figure 12. NanoDAC+ Evaluation Board, Top Side Routing

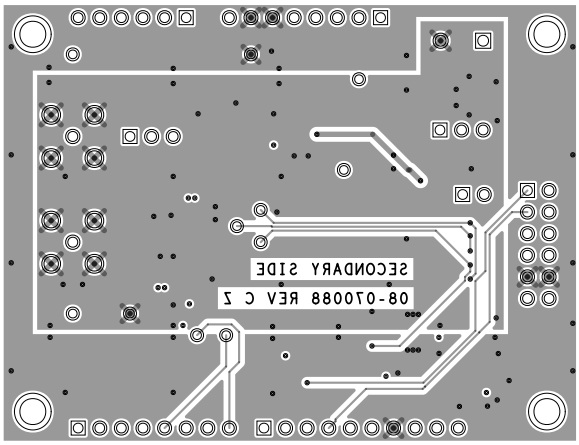

Figure 13. NanoDAC+ Evaluation Board, Bottom Side Routing

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. Bill of Materials

Quantity	Reference Designator	Description	Supplier, Part Number[1]
1	U1	Tiny 16-bit SPI nanoDAC+, with ±2 (16-bit) LSB INL and 2 ppm/°C reference	Analog Devices, AD5683R or AD5693R
1	U3	Ultra-low noise, high accuracy 2.5 V voltage reference	Analog Devices, ADR4542DEZ
1	U5	150 mA, low quiescent current, complementary metal-oxide semiconductor (CMOS) linear regulator in 5-lead TSOT or 4-ball WLCSP	Analog Devices, ADP121-AUJZ33
1	U6	IC, 32 KBIT serial, electrically erasable programmable read-only memory (EEPROM)	Generic
2	AGND, DGND	Connector, printed circuit board (PCB), black test points	Generic
4	C1, C8, C10, C11	0.1 µF ceramic capacitors, 16 V, 10%, X7R, 0603	Generic
3	C12, C21, C23	0.1 µF ceramic capacitors, 50 V, 10%, X7R, 0603	Generic
1	C22	10 µF ceramic capacitor, 6.3 V, 20%, X5R, 0603	Generic
3	C4, C5, C24	1 µF ceramic capacitors, 16 V, 10%, X7R, 0603	Generic
1	C34	4.7 µF ceramic capacitor, 10 V, 20%, X5R, 0603	Generic
2	C7, C9	10 µF ceramic capacitors, 10 V, 20%, X5R, 0603	Generic
1	EXT_VDD	Connector-PCB, 2-position terminal block, side entry, 5 mm pitch	Generic
1	L2	Inductor, ferrite bead, 600 Ω, 25%, 100 MHz, 2.9 A, 0.038 Ω, 1206, AEC-Q200	Generic
5	LDACB, RESETB, SCLK/A0, SDIN/SDA, SYNCB/SCL	Connector-PCB, white test points	Generic
2	P4, P7	Connector-PCB, receptacles, 25 mil square post, 2.54 mm pitch	Generic
1	P5	Connector-PCB, receptacle, 25 mil square post, 2.54 mm pitch	Generic
1	P6	Connector-PCB, receptacle, 25 mil square post, 2.54 mm pitch	Generic
4	R1, R2, R8, R25	100 kΩ resistors, surface-mounted device (SMD), 1%, 1/10 W, 0603	Generic
2	R14, R24	0 Ω resistors, SMD, jumper, 1/16 W, 0402	Generic
1	R21	1.6 Ω resistor, SMD, 1%, 1/5 W, 0603, AEC-Q200	Generic
1	R22	0 Ω resistor, SMD, jumper, ½ W, 0805, AEC-Q200, pulse proof	Generic
2	REF_SEL, VDD_SEL	Connector-PCB, high temperature, 3-position, male headers, unshrouded, single row, straight, 2.54 mm pitch, 3.05 mm solder tail	Generic
4	VDD, VLOGIC, VOUT, VREF	Connector-PCB, red test points	Generic
1	VDD_VIO	Connector-PCB, header, 1 row, 2 way	Generic
4	R4, R7, R10, R18	0 Ω resistors, SMD, jumper, 1/10 W, 0603	Generic- Pref/install for EVAL-AD5683RARDZ
5	R5, R9, R13, R17, R19	0 Ω resistors, SMD, jumper, 1/10 W, 0603	Generic- Pref/install for EVAL-AD5693RARDZ
4	R4, R7, R10, R18	0 Ω resistors, SMD, jumper, 1/10 W, 0603, Do not insert (DNI) or do not populate (DNP) for EVAL-AD5693RARDZ	Not applicable
6	R5, R9, R11, R13, R17, R19	0 Ω resistors, SMD, jumper, 1/10 W, 0603, DNI or DNP for EVAL-AD5683RARDZ	Not applicable
1	C2	0.1 µF ceramic capacitor, 16 V, 10%, X7R, 0603, DNI or DNP for both boards	Not applicable
1	C6	10 nF ceramic capacitor, 200 V, 10%, X7R, 0805, FLEXITERM®, DNI or DNP for both boards	Not applicable
2	EXT_REF, V_OUT	Connector-PCB, coax, SMB, jacks, RF vertical, PC mount gold, DNI or DNP for both boards	Not applicable
1	PMOD	Connector-PCB, BERG, header, straight, male, 12 position, DNI or DNP for both boards	Not applicable

ORDERING INFORMATION

Table 5. Bill of Materials (Continued)

Quantity	Reference Designator	Description	Supplier, Part Number[1]
1	R12	2 kΩ resistor, SMD, 1%, 1/8 W, 0805, AEC-Q200, DNI or DNP for both boards	Not applicable
1	R15	0 Ω resistor, SMD, jumper, 1/16 W, 0402, DNI or DNP for both boards	Not applicable
1	R16	100 kΩ resistor, SMD, 1%, 1/10 W, 0603, AEC-Q200, DNI or DNP for both boards	Not applicable
1	R3	100 kΩ resistor, SMD, 1%, 1/10 W, 0603, DNI or DNP for both boards	Not applicable

[1] Generic indicates that any part with the specified value, size, and rating can be used.

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.