AccuCharge + ModelGauge 1-Cell Fuel Gauge and 3A Charger with Integrated USB Type-C Detection

MAX77972

General Description

The MAX77972 is an autonomous integrated FET charger with integrated fuel gauge, Universal Serial Bus (USB) Type-C and BC1.2 detection. The MAX77972 supports 4.5V to 13.7V inputs and up to 3.15A of charging current. Charge current and voltage are I²C and pin-configurable using resistors. The IC supports USB On-The-Go (OTG) reverse boost and includes a Smart Power Selector™ (SPS), which is best for using limited adapter and battery power.

The fuel gauge uses the ModelGauge™ m5 algorithm, which provides industry-leading accuracy by combining the short-term accuracy and linearity of a coulomb counter with the long-term stability of a voltage-based fuel gauge. ModelGauge m5 automatically compensates for cell aging, temperature, and discharge rate and provides accurate state-of-charge (SOC) over a wide range of operating conditions.

Charging is coordinated with the fuel gauge to provide 9-temperature-region JEITA charge control as well as step-charging. Other protection features include junction thermal regulation, over/under voltage protection, and short circuit protection.

The USB Type-C Configuration Channel (CC) detection pins on the MAX77972 enable automatic USB Type-C power source detection and input current limit configuration. To support a variety of legacy USB types as well as proprietary adapters, the IC also integrates BC1.2 detection using the D+ and D- pins. The IC runs the CC pin and BC1.2 detection automatically as soon as a USB plug is inserted without any software control.

The IC is available in a lead-free 3.208mm x 3.258mm 36-bump 0.5mm pitch Wafer-level packaging (WLP) package.

Applications

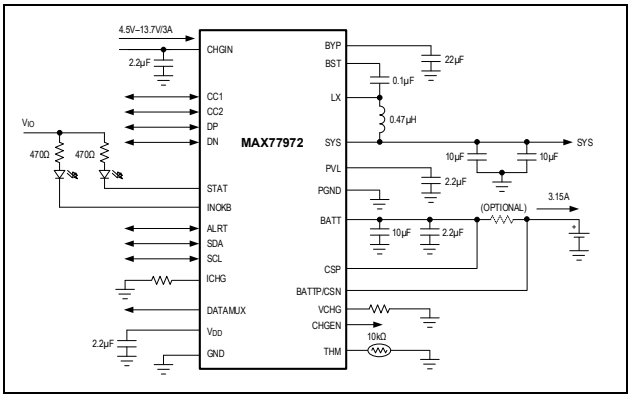
- Mobile Point-of-Sale Devices
- Portable speakers
- Wireless Headset Charging Cases
- Power Banks
- Mobile Hotspots
- AR/VR Devices
- E-Readers and Tablets

Benefits and Features

- Stand-Alone AccuCharge™ Buck Charger
  - 13.7V Input Operating Voltage, up to 16V protection
  - I²C or Resistor Configured Fast Charge Current 100mA to 3150mA
  - I²C or Resistor Configured Charge Termination Voltage 3.4V to 4.66V
  - I²C Programmable JEITA zones – 9 Automatic Temperature Charge Control Region
  - Prequal and Step-Charging Options
  - Fuel Gauge-Assisted Charge Termination
  - 6A Peak Discharge Current
  - OTG/Reverse Boost up to 5.1V, 1.5A
  - Adaptive Input Current Limit (AICL)
- ModelGauge m5 EZ Algorithm
  - Percent, Capacity, Age
  - Cycle+™ Age Forecast
- Precision Measurement Without Calibration
  - Current, Voltage, Time, Cycles
  - Die Temperature and Thermistors
- Integrated USB Detection
  - CC Detection for USB Type-C
  - BC1.2 Detection for Legacy SDP, DCP, and CDP
  - Automatic Input Current Limit Configuration
- OCV Keep-Out Region for Special Chemistry Cell

Ordering Information **appears at end of data sheet.**

Simplified Block Diagram



Analog Devices is in the process of updating documentation to provide culturally appropriate terminology and language. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

19-101877; Rev 0; 4/24

TABLE OF CONTENTS

Absolute Maximum Ratings

CHGIN to GND ..... -0.3V to +16V

BYP, LX to PGND ..... -0.3V to +16V

BATSP to GND ..... -0.3V to BATT + 0.3V

BST to PVL ..... -0.3V to +16V

BST to LX ..... -0.3V to +2.2V

PVL to GND ..... -0.3V to +2.2V

BATSN, PGND to GND ..... -0.3V to +0.3V

LX, PGND Continuous Current ..... $4.5A_{RMS}$

SYS, BATT Continuous Current ..... $7.5A_{RMS}$

SYS, BATT Continuous Current (Continuous current at 10% utilization across 10 years at ≤ 120°C) 4.5A

CHGIN, BYP Continuous Current ..... $3.2A_{RMS}$

Continuous Sink Current for SDA, ALRT 20mA

Operating Temperature Range ..... -40°C to +85°C

Storage Temperature Range ..... -55°C to +125°C

Soldering Temperature (reflow) ..... +260°C

Lead Temperature (soldering 10s) ..... +300°C

BATT, SYS to GND ..... -0.3V to +6V

ALRT to GND ..... -0.3V to +16V

TH to GND ..... -0.3V to BATT + 0.3V

REG to GND ..... -0.3V to +2.2V

CSN to BATT ..... - 0.3V to + 0.3V

CSP to BATT ..... - 0.3V to + 0.3V

SDA, SCL, VCHG, ICHG, STAT, CHGEN, INOKB, DATAMUX to GND ..... -0.3V to +6V

USBC DN, DP to GND ..... -0.3V to +6.0V

USBC CC1, CC2 to GND ..... -0.3V to +6.0V

Thermal Absolute Maximum Rating Operating Temperature Range ..... -40°C to +85°C

Thermal Absolute Maximum Rating Storage Temperature Range ..... -65°C to +150°C

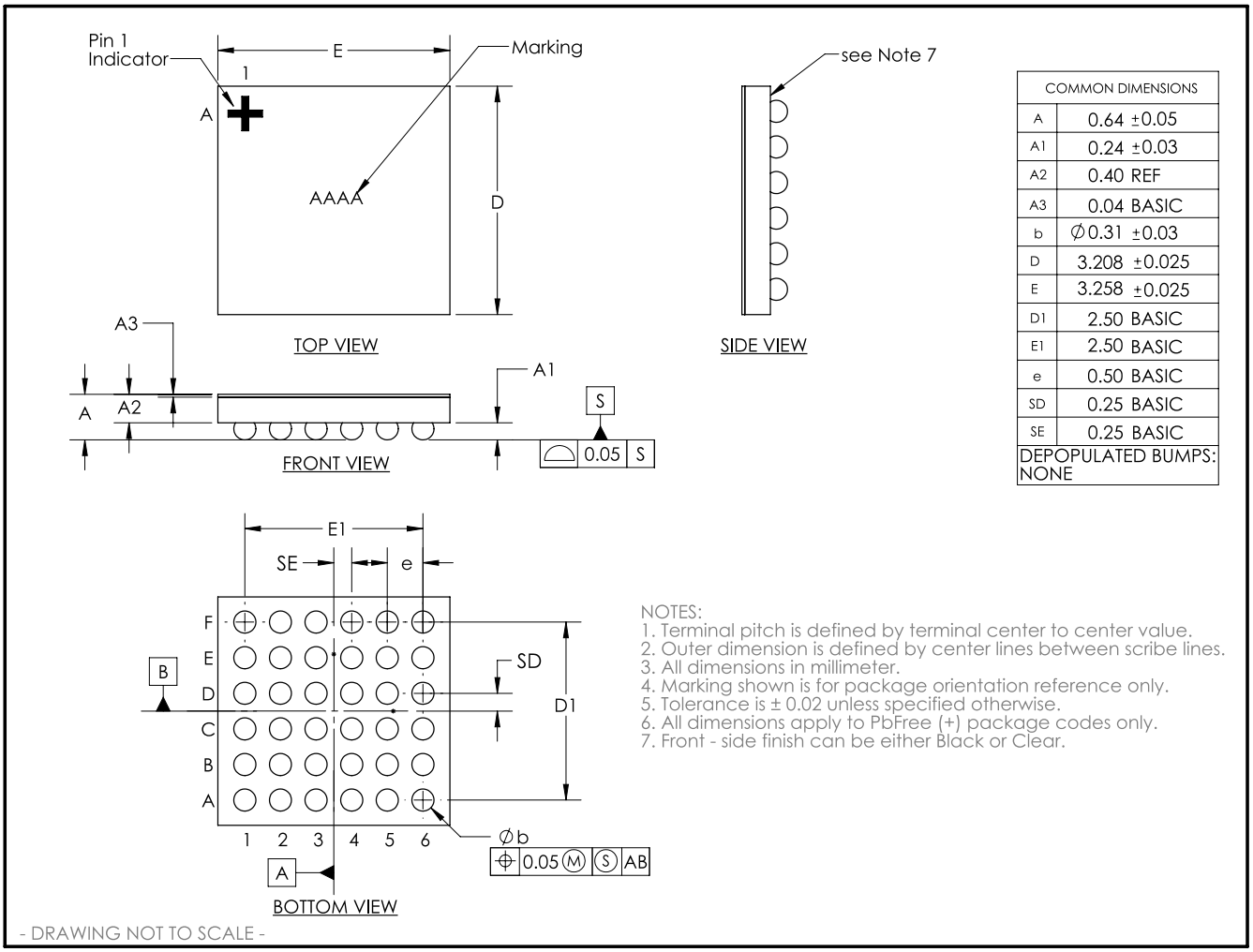
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	W363B3+1
Outline Number	*21-100517*
Land Pattern Number	*Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	37.68°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to Packaging Index. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to Thermal Characterization of IC Packages.



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.24 ±0.03
A2	0.40 REF
A3	0.04 BASIC
b	Ø0.31 ±0.03
D	3.208 ±0.025
E	3.258 ±0.025
D1	2.50 BASIC
E1	2.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

Electrical Characteristics

(V_{BATT} = 2.3V to 4.9V, typical value at 3.6V, T_A = -40°C to +85°C, typical values are T_A = +25°C, see for more details. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Battery Voltage Range	V_{BATT}		2.3		4.9	V
Ship Mode Supply Current	I_{DD1}	T_A ≤ +50°C, typical at +25°C		3.2	7.2	µA
Hibernate Supply Current	I_{DD2}	DpShpEn = 0, T_A ≤ +50°C, typical at +25°C		30	60	µA
Battery-Only Gauge Active Supply Current	I_{DD4}	USB unplugged. T_A ≤ +50°C, typical at +25°C, average current, not including thermistor measurement current.		50	90	µA
V_{DD} Regulation Voltage	V_{REG}			1.8		V
DeepShip Mode	$I_{DEEPSHIP}$	Shutdown command. Charger to wakeup.		1.2	2.5	µA
INPUT/OUTPUT						
Output Drive Low, ALRT, SDA, DATAMUX	V_{OL}	I_{OL} = 4mA, V_{BATT} = 2.3V	0.01		0.4	V
Input Logic High, SCL, SDA, CHGEN, DATAMUX	V_{IH}		1.5			V
Input Logic Low, SCL, SDA, CHGEN, DATAMUX	V_{IL}				0.5	V
External Thermistance Resistance	R_{EXT10}	nADCCFG.R100 = 0		10		kΩ
	R_{EXT100}	nADCCFG.R100 = 1		100		
INPUT/OUTPUT / INOKB, STAT						
Logic Input Leakage Current				0.1	1	µA
Output Low Voltage INOKB, STAT		I_{SOURCE} = 5mA, T_A = 25°C			0.4	V
Output High Leakage INOKB, STAT		V_{SYS} = 5.5V, T_A = +25°C	-1	0	1	µA
		V_{SYS} = 5.5V, T_A = 85°C		0.1		
2-WIRE INTERFACE						
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL Clock	T_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		1.2	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 1)	5		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 1)	5		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Width Suppressed by Input Filter	t_{SP}				50	ns
Capacitive Load for Each Bus Line	C_B				400	pF
SCL, SDA Input Capacitance	C_{BIN}	(Note 1)		6		pF
CHARGER/GENERAL ELECTRICAL CHARACTERISTICS						
Battery Only Quiescent Current	I_{BATT_Q}	USBC as UFP and BATT = SYS = 3.6V		30	50	µA
CHARGER/SWITCHING MODE CHARGER						
CHGIN Voltage Range	V_{CHGIN}	Operating Voltage (Note 2)	V_{CHGIN_UVLO}		V_{CHGIN_OVLO}	
CHGIN Overvoltage Threshold	V_{CHGIN_OVLO}	V_{CHGIN} Rising	13.4	13.7	14	V
CHGIN Overvoltage Threshold Hysteresis	V_{CHGINH_OVLO}	V_{CHGIN} Falling		300		mV
CHGIN to GND Minimum Turn-On Threshold Accuracy	V_{CHGIN_REG}	V_{CHGIN} rising, 4.7V setting	4.6	4.7	4.8	
CHGIN to SYS Minimum Turn-On Threshold	$V_{CHGIN2SYS}$	V_{CHGIN} rising, 50mV hysteresis	V_{SYS} + 0.12	V_{SYS} + 0.20	V_{SYS} + 0.28	V
CHGIN Adaptive Voltage Regulation Threshold Accuracy	V_{CHGIN_REG}	4.5V setting	4.4	4.5	4.6	V
CHGIN Supply Current	I_{IN}	V_{CHGIN} = 5.0V, Charger enabled, V_{SYS} = V_{BATT} = 4.5V, (No switching, battery charged).		2.7	4	mA
CHGIN Input Current Limit	$I_{INLIMIT}$	Charger enabled, 500mA Input Current Setting, T_A = 25°C.	423	460	510	mA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Charger enabled, 1500mA Input Current Setting, T_A = 25°C.	1300	1400	1500	
		Charger enabled, 3000mA Input Current Setting, T_A = +25°C.	2600	2800	3000	
CHGIN Self-Discharge Down to UVLO Time	t_{INSD}	Time required for the charger input to cause the CHGIN capacitor to decay from 6.0V to 4.3V.		100		ms
CHGIN Input Self Discharge Resistance	R_{INSD}			37		kΩ
CHGIN to BYP Resistance	$R_{CHGIN2BYP}$	Bidirectional		21		mΩ
LX High-Side Resistance	R_{HS}			41		mΩ
LX Low-Side Resistance	R_{LS}			42		mΩ
BATT to SYS Dropout Resistance	$R_{BAT2SYS}$			12		mΩ
CHGIN to BATT Dropout Resistance	$R_{CHGIN2BAT}$	Calculation estimates a 0.04Ω inductor resistance (R_L). $R_{CHGIN2BAT}$ = $R_{CHGIN2BYP}$ + R_{HS} + R_L+ $R_{BAT2SYS}$.		165		mΩ
LX Leakage Current		LX = PGND or BYP, T_A = +25°C		0.01	10	µA
		LX = PGND or BYP, T_A = +85°C		1		
BST Leakage Current		BST – LX = 1.8V, T_A = +25°C		0.01	10	µA
		BST – LX = 1.8V, T_A = +85°C		1		
BYP Leakage Current		V_{BYP} = 5.5V, V_{CHGIN} = 0V, LX = 0V, Charger Disabled, T_A = +25°C.		0.01	10	µA
		V_{BYP} = 5.5V, V_{CHGIN} = 0V, LX = 0V, Charger Disabled, T_A = +85°C.		1		
SYS Leakage Current		V_{SYS} = 0V, V_{BATT} = 4.2V, Charger Disabled, T_A = +25°C.		0.01	10	µA
		V_{SYS} = 0V, V_{BATT} = 4.2V, Charger Disabled, T_A = +85°C.		1		
Minimum ON Time	t_{ON-MIN}			75		ns
Minimum OFF Time	$t_{OFF-MIN}$			75		ns
Buck Current Limit	I_{LIM}		5.16	6.0	6.84	A
Reverse Boost Quiescent Current		Not Switching: Output forced 200mV above its target regulation voltage.		2000		µA
Reverse Boost BYP Voltage	$V_{BYP.OTG}$	5.1V setting, 3.4V < V_{BATT} < 4.5V	4.94	5.1	5.26	V
CHGIN Output Current Limit	$I_{CHGIN.OTG.LIM}$	3.4V < V_{BATT} < 4.5V, T_A = 25°C	1500		1725	mA
Reverse Boost Output Voltage Ripple		Discontinuous inductor current (i.e. skip mode).		±150		mV

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Continuous inductor current.		±150		
BATT Voltage Setting Regulation Range		See the register map for step size.	3.4		4.64	V
BATT Voltage Setting Regulation Accuracy		T_A = +25°C, Battery regulation voltage 4.2V	4.175	4.200	4.210	V
		T_A = +25°C, Battery regulation voltage 4.35V	4.325	4.350	4.360	
		T_A = +25°C, Battery regulation voltage 4.4V	4.375	4.400	4.410	
		T_A = +25°C, Battery regulation voltage 4.45V	4.424	4.450	4.461	
		T_A = 0°C to +85°C, Battery regulation voltage.	-1	-0.3	+0.5	%
Fast-Charge Currents	I_{FC}	T_A = +25°C, V_{BATT} > V_{SYSMIN}, Programmed for 3.0A	2850	3000	3150	mA
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, Programmed for 2.0A	1900	2000	2100	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, Programmed for 0.5A	465	500	535	
Trickle Charge Threshold	$V_{TRICKLE}$	V_{BATT} Rising	3.0	3.1	3.2	V
Precharge Threshold	V_{PRECHG}	V_{BATT} Rising	2.4	2.5	2.6	V
Prequalification Threshold Hysteresis	V_{PQ-H}	Applies to both $V_{TRICKLE}$ and V_{PRECHG}		100		mV
Trickle Charge Current	$I_{TRICKLE}$	Default setting = Disabled.	270	300	340	mA
Precharge Charge Current	I_{PRECHG}		40	55	80	mA
Charger Restart Threshold	V_{RSTRT}		50	100	150	mV
Charger Restart Deglitch Time		10mV overdrive, 100ns rise time.		130		ms
Charge Termination Deglitch Time	t_{TERM}	2mV overdrive, 100ns rise/fall time.		30		ms
Charger Soft Start Time	t_{SS}			1.5		ms
BATT to SYS Reverse Regulation Voltage	V_{BSREG}	I_{BATT} = 20mA		70		mV
		Load regulation during the reverse regulation mode.		1		mV/A
Minimum SYS Voltage Accuracy	V_{SYSMIN}	V_{BATT} = 3.5V default	-3		3	%
Prequalification Time	t_{PQ}	Applies to both low-battery precharge and trickle modes.		30		min

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fast-Charge Constant Current + Fast-Charge Constant Voltage Time	t_{FC}			6		hr
Timer Accuracy			-20		20	%
Junction Temperature Thermal Regulation Loop Setpoint Program Range	T_{REG}	Junction temperature when the charge current is reduced. nChgConfig2.REGTEMP = 0x9.		130		°C
Thermal Regulation Gain	ATJ_{REG}	The charge current is decreased by 5% of the fast charge current setting for every degree the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 3.15A is reduced to 0A by the time the junction temperature is 20°C above the programmed loop set point. For lower programmed charge currents such as 480mA, this slope is valid for charge current reductions down to 80mA; below 100mA, the slope becomes shallower, but the charge current is still reduced to 0A if the junction temperature is 20°C above the programmed loop set point.		-157.5		mA/°C
Battery Overcurrent Discharge Range	$I_{BOVCRDRNG}$	Programmable with 15 steps between minimum and maximum.	3		6.2	A
Battery Overcurrent Discharge Accuracy	$I_{BOVCRDTH}$	B_{2SOVRC} = 3A, T_A = 0°C to +85°C, Battery Only mode, Boost mode.	2.8	3	3.2	A
Battery Overcurrent Debounce Time	t_{BOVRC}		6			ms
Battery Overcurrent Discharge Retry	t_{OCP_RETRY}			0.15		sec
Battery Overcurrent Discharge Protection Quiescent Current	I_{BOVRC}	Battery Only Mode		3 + I_{BATT} /22000		µA
System Power-Up Current	I_{SYSPU}		35	50	80	mA
System Power-Up Voltage	V_{SYSPU}	V_{SYS} Rising, 100mV hysteresis	1.9	2.0	2.1	V
Watchdog Timer	t_{WD}		80			s
CHARGER/CHARGER DETECTION						
BC1.2 State Timeout	t_{TMO}		180	200	220	ms
Data Contact Detect time-out	t_{DCDTMO}		700	800	900	ms
Primary to Secondary Timer	$t_{PDSDWait}$		27	35	39	ms

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charger Detection Debounce	t_{CDDeb}		45	50	55	ms
V_{BUS64} Threshold	V_{BUS64}	DP and DN pins. The threshold in percent of V_{BUS} voltage 3V < V_{BUS} < 5.5V.	57	64	71	%
V_{BUS64} hysteresis	V_{BUS64_H}			0.015		V
V_{BUS47} Threshold	V_{BUS47}	DP and DN pins. The threshold in percent of V_{BUS} voltage 3V < V_{BUS} < 5.5V.	43.3	47	51.7	%
V_{BUS47} hysteresis				0.015		V
V_{BUS31} Threshold	V_{BUS31}	DP and DN pins. The threshold in percent of V_{BUS} voltage 3V < V_{BUS} < 5.5V.	26	31	36	%
V_{BUS31} hysteresis				0.015		V
I_{WEAK} Current	I_{WEAK}		0.01	0.1	0.5	µA
RDM_DWN Resistor	R_{DM_DWN}		14.25	20	24.8	kΩ
IDP_SRC Current	I_{DP_SRC} /I_{DCD}	Accurate over 0V to 2.5V.	7	10	13	µA
V_{LGC} threshold	V_{LGC}		1.62	1.7	1.9	V
V_{LGC} hysteresis	V_{LGC_H}			0.015		V
V_{DAT_REF} threshold	V_{DAT_REF}		0.25	0.32	0.4	V
V_{DAT_REF} hysteresis	$V_{DAT\_REF\_H}$			0.015		V
V_{DN_SRC} Voltage	V_{DN_SRC}/ V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
V_{DP_SRC} Voltage	V_{DP_SRC}/ V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
COMP2 Load Resistor	R_{USB}	Load Resistor on DP/DN.	3	6.1	12	MΩ
CHARGER/CC DETECTION						
CC pin voltage, in Downstream-Facing Port (DFP) 1.5A mode	V_{CC_PIN}	Measured at CC pins with 126KΩ load. IDFP1.5_CC enable and V_{AVL} ≥ 2.5V.	1.85			V
CC pin clamp Voltage	V_{CC_CLAMP}	60µA ≤ $I_{CC\_}$ ≤ 600µA		1.1	1.32	V
CC pin clamp Voltage (5.5V)		$I_{CC\_}$ < 2mA		5.25	5.5	V
CC UFP pull-down resistance	R_{PD_UFP}		-10%	5.1	10%	kΩ
CC RA RD threshold	$V_{RA\_RD0.5}$		0.15	0.2	0.25	V
CC UFP 0.5A RD threshold	$V_{UFP\_RD0.5}$		0.61	0.66	0.7	V
CC UFP 0.5A RD hysteresis	$V_{UFP\_RD0.5\_H}$			0.015		V
CC UFP 1.5A RD threshold	$V_{UFP\_RD1.5}$		1.16	1.23	1.31	V
CC UFP 1.5A RD hysteresis	$V_{UFP\_RD1.5\_H}$			0.15		V

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CC pin Power uptime	$t_{ClampSwap}$	Maximum time allowed from the removal of voltage clamp till 5.1kΩ resistor attached.				15	ms
CC Detection Debounce	t_{CCDeb}			100	119	200	ms
Type-C Debounce	t_{PDDeb}			10	15	20	ms
Type-C Quick Debounce	t_{QDeb}			0.9	1	1.1	ms
GAUGE/ANALOG-TO-DIGITAL CONVERSION							
BATT Voltage Measurement Error	V_{GERR}	T_A = +25°C		-7.5		+7.5	mV
		-40°C ≤ T_A ≤ +85°C		-20		+20	
Voltage Measurement Resolution	V_{LSB}				78.125		µV
Voltage Measurement Range	V_{FS}			2.3		4.9	V
CURRENT CHANNEL							
Current Measurement Resolution	I_{LSB}				0.15625		mA
Current Measurement Range	I_{RANGE}				±3.6		A
Current Measurement Offset	I_{OERR}	Long-term average at zero input current.			±0.25		mA
Current Measurement Symmetrical Error	I_{SERR}				2		%
Current Measurement Asymmetrical Error	I_{AERR}	±3150mA	V_{BATT} = 3.8V	-150		150	mA
		±1000mA	V_{BATT} = 3.8V	-20		20	
		±300mA	V_{BATT} = 3.8V	-10		10	
		+50mA	V_{BATT} = 3.8V	-10		10	
Linear Regulator Mode Current Measurement Error	I_{LRERR}	+1500mA		-75		75	mA
		+100mA		-25		25	
Current Measurement Offset Error	I_{OERR}	CSN = 0V, long-term average.			±1.5		µV
Current Measurement Gain Error	I_{GERR}	CSP between -50mV and +50mV		-1		+1	% of Reading
Current Measurement Resolution	I_{LSB}				1.5625		µV
Internal Temperature Measurement Error	TI_{GERR}	T_A = +25°C			±1		°C
Internal Temperature Measurement Resolution	TI_{LSB}	T_H			0.00391		°C
T_H, I_{CHG}, V_{CHG} Ratiometric Measurement Error	TE_{GERR}			-0.5		+0.5	% of Reading
T_H, I_{CHG}, V_{CHG} Ratiometric	TE_{LSB}				0.001526		%

(V_{BATT} = 2.3V to 4.9V, typical value at 3.6V, T_A = -40°C to +85°C, typical values are T_A = +25°C, see for more details. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Measurement Resolution						
GAUGE/CHGIN CURRENT CHANNEL						
CHGIN Current Measurement Resolution	I_{LSB}			0.15625		mA
CHGIN Current Measurement Range	I_{RANGE}		0		3	A
CHGIN Current Measurement Error	I_{AERR}	+3000mA	-150		150	mA
		+1000mA	-20		20	
		+300mA	-12.5		12.5	
BYP CHANNEL						
BYP Voltage Measurement Error	V_{GERR}		-100		+100	mV
BYP Voltage Measurement Resolution	V_{LSB}			625		µV
BYP Voltage Measurement Range	V_{FS}	(Digital full-scale is 20.48V)	4.5		13.4	V
GAUGE/TIMING						
TH Precharge Time	t_{PRE}	Time between turning on the TH bias and analog-to-digital conversions.	8.48			ms
Power-on-Reset Time	t_{POR}				10	ms
Task Period	t_T			175.8		ms
Time-base Accuracy	t_{ERR}	V_{SYS} = 3.8V at T_A = -40°C to +85°C	-5		5	%
		V_{SYS} = 3.8V at T_A = +25°C		±1		
GAUGE/RESISTANCE AND LEAKAGE						
Leakage Current, CSN, CSP ALRT, TH	I_{LEAK}		-1		+1	µA

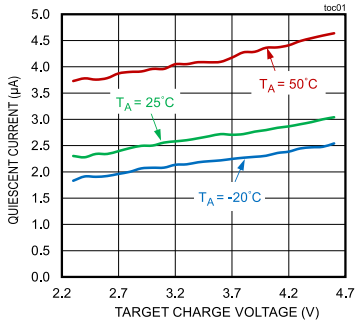
Note 1: Specification is guaranteed by design (GBD), and not production tested.

Note 2: The CHGIN input must be less than V_{CHGIN_OVLO} and greater than both V_{CHGIN_UVLO} and $V_{CHGIN2SYS}$ for the charger to turn on.

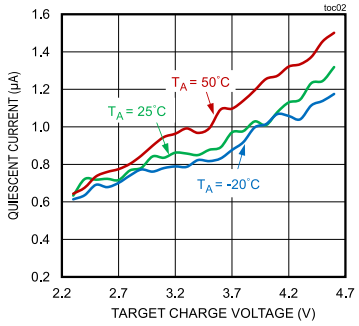
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

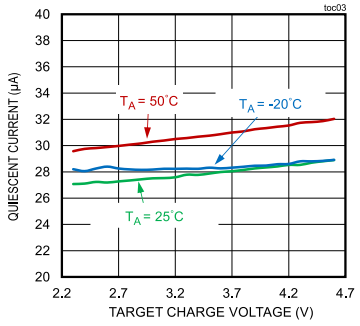
BATTERY QUIESCENT CURRENT SHIP MODE



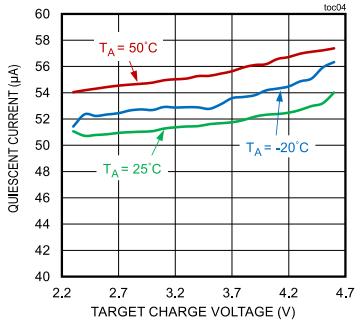
BATTERY QUIESCENT CURRENT DEEPSHIP MODE



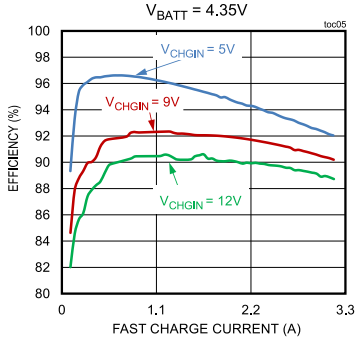
BATTERY QUIESCENT CURRENT HIBERNATE MODE



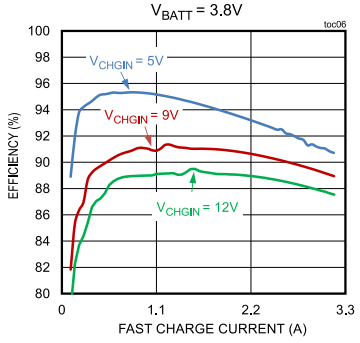
BATTERY QUIESCENT CURRENT ACTIVE MODE



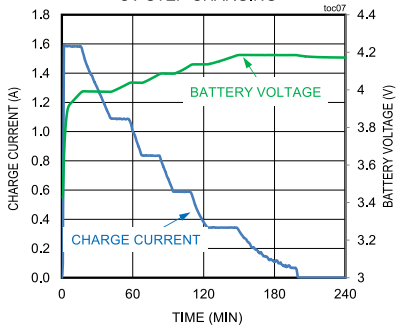
EFFICIENCY vs. FAST CHARGE CURRENT V_{BATT} = 4.35V



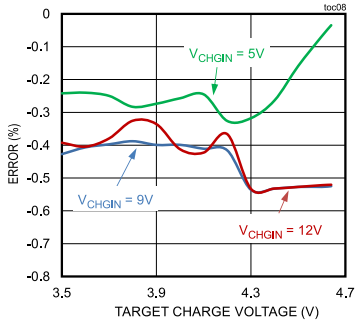
EFFICIENCY vs. FAST CHARGE CURRENT V_{BATT} = 3.8V



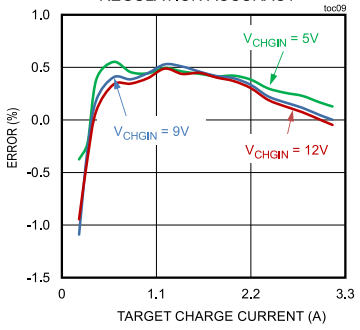
CHARGING PROFILE V_{CHGIN} = 5V, IChgTerm = 50mA, CV STEP CHARGING



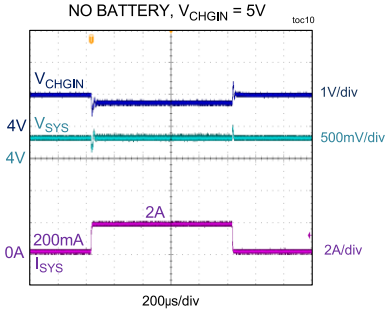
CHARGE VOLTAGE REGULATION ACCURACY



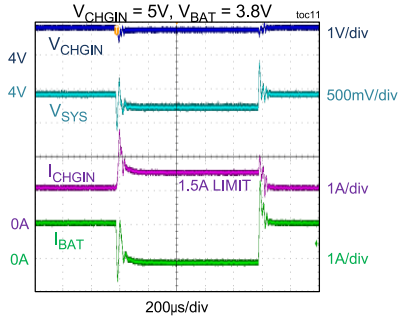
CHARGE CURRENT REGULATION ACCURACY



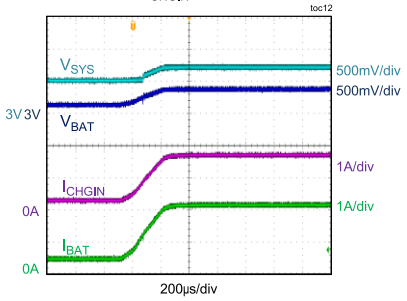
SYS LOAD TRANSIENT
CHGEN LOW, CV TO CV,
NO BATTERY, V_{CHGIN} = 5V



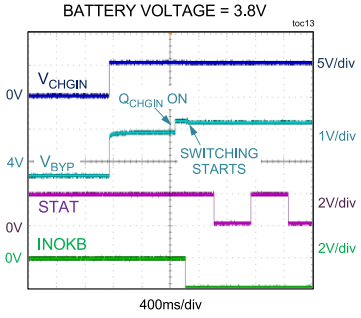
SYS LOAD TRANSIENT
CC to INPUT CURRENT, I_{SYS} = 0.2 to 2A
V_{CHGIN} = 5V, V_{BAT} = 3.8V



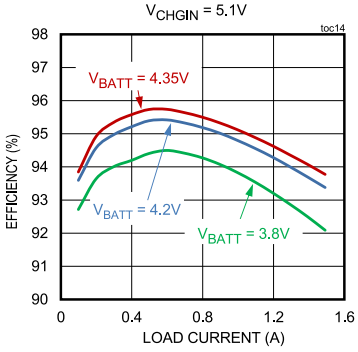
TRICKLE CHARGE TO FAST CHARGE
V_{CHGIN} = 5V



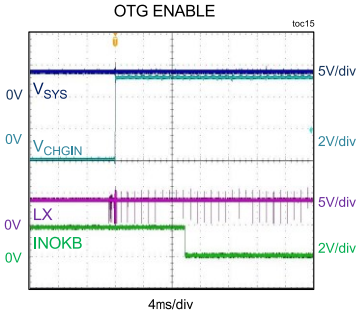
INPUT INSERTION
BATTERY VOLTAGE = 3.8V



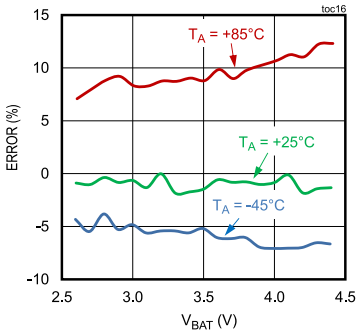
OTG EFFICIENCY vs. LOAD CURRENT
V_{CHGIN} = 5.1V



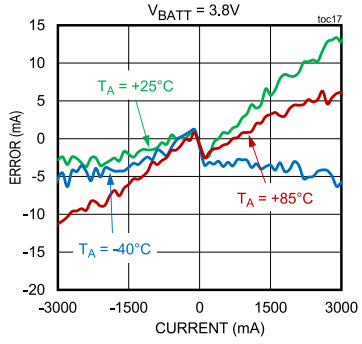
OTG ENABLE



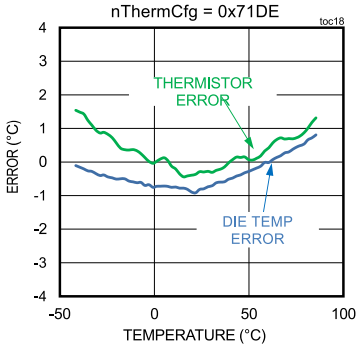
VCELL MEASUREMENT ERROR



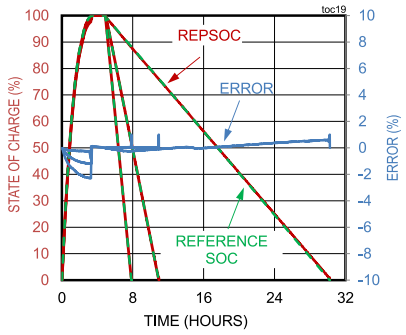
CURRENT MEASUREMENT ACCURACY
V_{BATT} = 3.8V



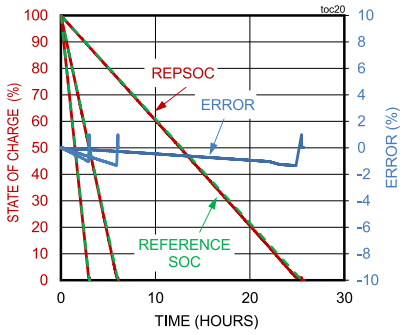
DIE TEMP AND THERMISTOR MEASUREMENT ERROR
nThermCfg = 0x71DE



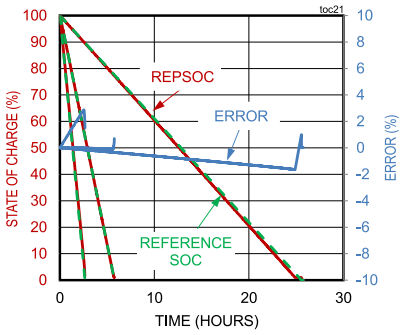
CHARGE AND DISCHARGE AT 20°C



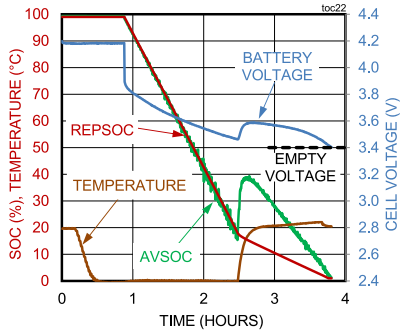
HOT DISCHARGE AT 40°C



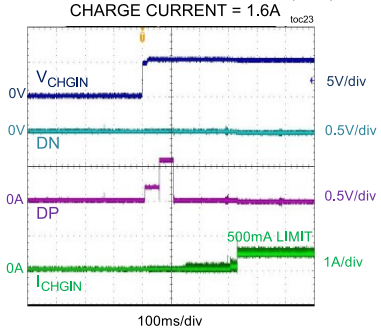
COLD DISCHARGE AT 0°C



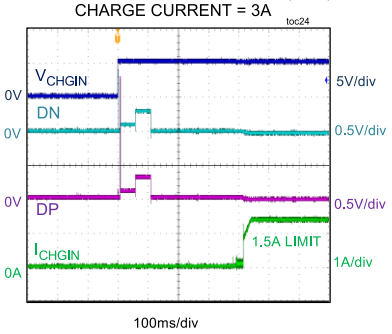
RESPONSE TO TEMPERATURE TRANSIENT AT CONSTANT-CURRENT LOAD



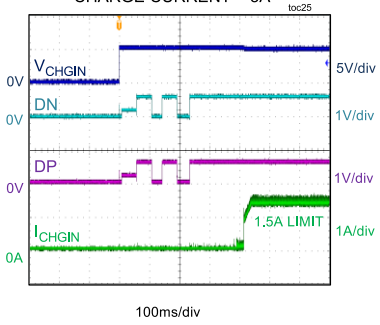
CHARGER DETECTION STANDARD DOWNSTREAM PORT (SDP) CHARGE CURRENT = 1.6A



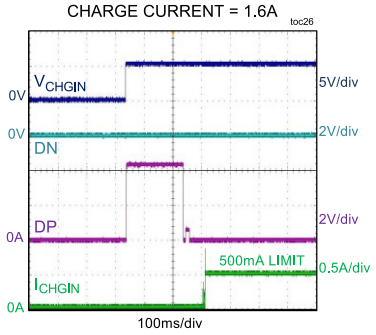
CHARGER DETECTION CHARGING DOWNSTREAM PORT (CDP) CHARGE CURRENT = 3A



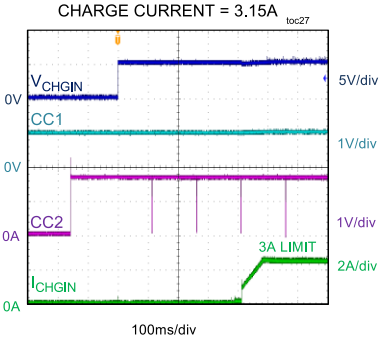
CHARGER DETECTION DEDICATED CHARGING PORT (DCP) CHARGE CURRENT = 3A



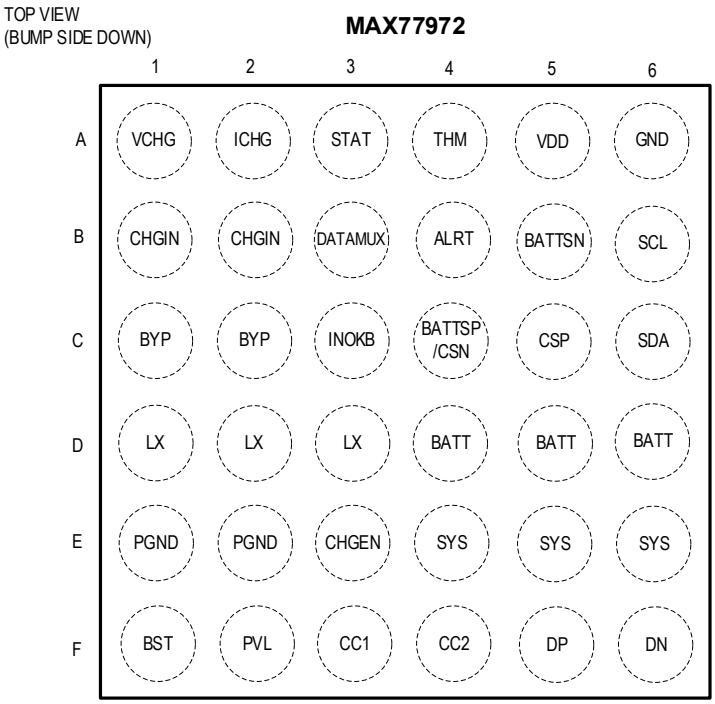
CHARGER DETECTION DATA CONTACT DETECT TIMEOUT CHARGE CURRENT = 1.6A



USB TYPE-C DETECTION CHARGE CURRENT = 3.15A



Pin Configurations



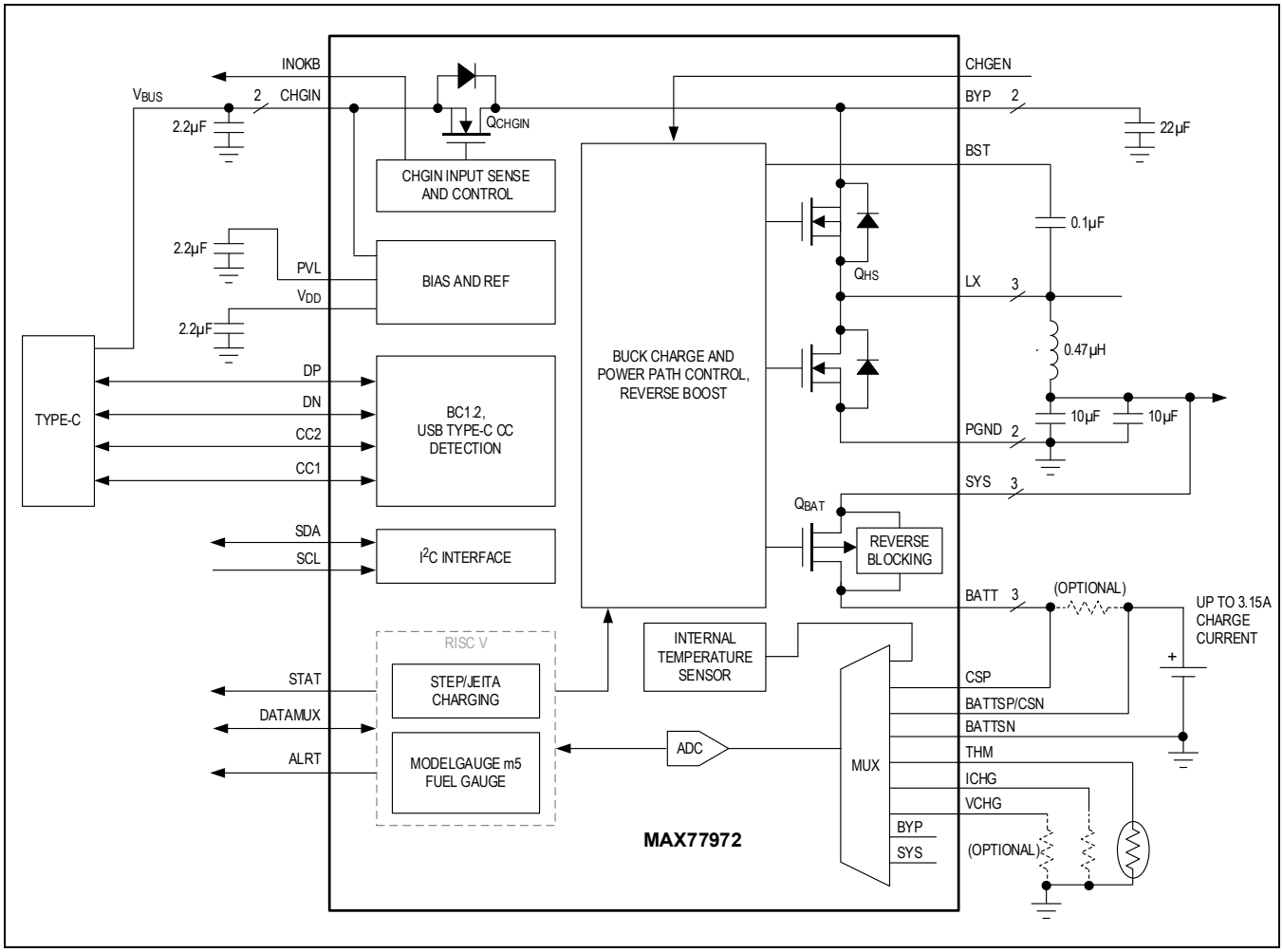
36-BUMP WLP
(3.208mm x 3.258mm, 0.5mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION
F1	BST	Provides Drive to High-Side Internal nMOS. Connect a 100nF/6.3V bootstrap capacitor between this pin and the LX node.
C3	INOKB	Charger Input Valid. Active low logic output flag. The open-drain output indicates when a valid voltage is present at CHGIN.
A3	STAT	Open Drain Charge Status Indication Output. STAT is toggling Low and High impedance during charge. STAT becomes low in the CHARGE DONE state. STAT becomes High impedance when charge faults happen, or no adapter is found.
F4	CC2	USB Type-C CC2 connection.
F3	CC1	USB-Type-C CC1 connection.
F5	DP	Common Positive Output. Connect to D+ on a Type-C or micro-USB connector.
F6	DN	Common Negative Output. Connect to D- on a Type-C or micro-USB connector.
A6	GND	Analog Ground. Short to ground plane.
A5	VDD	1.8V Always-On Regulator Powers the IC. Bypass with a 2.2µF/10V ceramic capacitor to GND.
D4, D5, D6	BATT	Battery Power Connection. Connect to the positive terminal of a single-cell (or parallel cell) Li-ion battery. Bypass BATT to PGND ground plane with 10µF + 2.2µF ceramic capacitor.
E4, E5, E6	SYS	System Power Node. Bypass SYS to PGND with 2 × 10µF/10V ceramic capacitors.

F2	PVL	Output of On-Chip LDO. Noisy rail due to bootstrap operation. Bypass with a 2.2µF/10V ceramic capacitor to PGND. Powering external loads from PVL is not recommended.
E1, E2	PGND	Power Ground. Connect the return of the Buck output capacitor close to these pins.
D1, D2, D3	LX	Switching Node. Connect an inductor between LX and SYS. When the Buck converter is enabled, LX switches between BYP and PGND to control the input current, battery current, battery voltage, and die temperature.
C1, C2	BYP	System Power Connection. Output of OVP adapter input block and input to switching charger. Bypass with 22µF/16V ceramic capacitor from BYP to PGND.
B1, B2	CHGIN	Charger Input. It operates up to 13.7V, and the 16V DC withstands the input pin connected to the adapter or USB power source. Connect a 2.2µF/16V ceramic capacitor from CHGIN to GND.
B6	SCL	I^2C Clock
C6	SDA	I^2C Data
C4	BATTSP/ CSN	High-side Current Sense Negative. When using internal Q_{BAT} FET sensing, short CSP, CSN, and BATT. When using an external sense resistor, Kelvin connect CSP and CSN to the external current sense resistor.
C5	CSP	Current Sense Positive and BATT Sense. Connect to BATT.
B4	ALRT	Alert Open Drain Output. Connect a 10kΩ pullup.
A4	THM	10kΩ/100kΩ Thermistor Input. Internally biased to BATT for 12ms each 1.4s. It indicates ±1°C battery temperature (-40°C to 85°C) for gauging and charging (JEITA). It can also be used as battery ID/presence detection if NTC is not needed.
A2	ICHG	Current Configuration. Resistor input that configures parameters in *Table 2*.
B5	BATTSN	Battery Negative Differential Sense Connection. Connect to the negative or ground terminal close to the battery.
B3	DATAMUX	External USB Data Mux Select. Allows IC to borrow DP/DN data lines for USB detection in case they are shared with an external device. It can also be used to cycle SYS power with a >6s pull down, or ship mode with a >12s pull down when the USB data mux feature is disabled. See the *Reset Modes* section for a detailed description.
A1	VCHG	Voltage Configuration. Resistor input that configures parameters in *Table 3*.
E3	CHGEN	Charge Enable. Connect CHGEN high to enable charging. Pull CHGEN low to disable charging. Note that the CHGEN needs to be high to enter OTG mode.

Functional Diagram



Detailed Description

The MAX77972 is a highly integrated USB Type-C autonomous charger and ultra-low power fuel gauge for a 1-cell lithium-ion (Li+) or lithium polymer (LiPoly) battery. The fuel gauge offers OCV keep-out region for special chemistry battery such as lithium iron phosphate (LiFePo4) battery. The MAX77972 can operate with input range from 4.5V to 13.7V to support 5V, 9V, and 12V AC adapter and USB input. The fast charge current, charge termination current, and charge termination voltage are both I2C and resistor configurable. The MAX77972 controls charging current, voltage, temperature, and power limit modes. With the aid of the ModelGauge m5 EZ fuel gauge, MAX77972 provides appropriate charging voltage and charging current to safely charge the battery depending on the state of the battery and the temperature. The MAX77972 offers 9-zone JEITA temperature settings and 5-zone step-charging where fast charging current and charge termination voltage are automatically adjusted according to temperature change. That ensures fast charging speed under the condition of battery safety.

The MAX77972 contains an ultra-low power fuel gauge which implements the Analog Devices' ModelGauge m5 EZ algorithm. The IC accurately measures voltage, current, and temperature to produce fuel gauge results. The ModelGauge m5 EZ robust algorithm provides tolerance against battery diversity. This additional robustness enables simpler implementation for most applications and batteries by avoiding time-consuming battery characterization. The ModelGauge m5 algorithm combines the short-term accuracy and linearity of a coulomb counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation, to provide industry-leading fuel gauge accuracy. The IC automatically compensates for battery age, temperature, and discharge rate and provides an accurate state of charge (SOC) in % and remaining capacity in mAh over a wide range of operating conditions. Additionally, fuel gauge error always converges to 0% as the cell approaches empty.

The MAX77972 runs BC1.2 and USB Type-C CC detection upon input insertion and configure input source to max power option and charger input current limit to max power. The fast charge current, charge termination current, and battery regulation voltage can be programmed with external resistors. The input voltage regulation with adaptive input current limit feature (AICL) allows charging to continue even with a weak adapter by preventing it from collapsing or folding back. The power path design provides system power even when the battery is fully discharged, and the charger supplements current from the battery and charges input automatically when the system demands a higher current. Reverse boost from the battery can be enabled through the I2C interface to allow 5.1V/1.5A OTG to CHGIN pin.

Buck Charger

Charging Control

Lithium-ion/polymer batteries are very common in various portable electronic devices because they have a very high energy density, minimal memory effect, and low self-discharge. However, care must be taken to avoid overheating or overcharging these batteries to prevent damage, potentially resulting in dangerous outcomes/explosive results. By operating in safe temperature ranges, at safe voltages and under safe current levels, the overall safety of the lithium-ion/polymer batteries can be assured throughout the life of the battery. Using AccuCharge technology, the MAX77972 controls the charging voltage and current dynamically based on the JEITA charge profile, step-charging and battery temperature. The charge current is reduced at low battery voltage (prequel), low and high temperature, or when the battery voltage reaches the battery regulation voltage. *Figure 1* shows an example of the charge profile without step charging and JEITA profile changing the target charge current and charge voltage. Real time target charging current and charging voltage are available at ChargingVoltage and ChargingCurrent registers, automatically modulated by temperature and step-charging. See nIChgCfg1/2, nVChgCfg1/2, nStepVolt, nStepCurr, and nTPrtTh1, nTPrtTh2 for configuration details in *Fast Charge - Step Charging* and *FAST CHARGE - JEITA* sections.

PRECHARGE: The battery is charged with I_{PRECHG} 55mA (typ) to check if it is safe to charge until it reaches V_{PRECHG} 2.5V (typ). MAX77972 can support battery down to 0V in this state.

TRICKLE CHARGE: The battery is charged with $I_{TRICKLE}$ 300mA (typ) until it reaches trickle charge threshold 3.1V (typ). Charger enters Fast Charge CC stage when battery voltage is above trickle charge threshold. This state can be disabled by setting ChgConfig0.PQEN = 0. When disabled, the charger moves from the precharge state directly to the Fast Charge CC state.

FAST CHARGE/STEP CHARGING: The battery is charged to this terminal voltage in Fast Charge stage. Charging profile shown in *Figure 1* has disabled step charging for simplicity. See *Step Charging* section for detailed configurations.

- ChargingVoltage: Register indicating battery regulation voltage in the fast charge stage. ChargingVoltage register changes with nStepVolt, nVChgCfg1 and nVChgCfg2 registers at each step charging stage under different temperature conditions.
- ChargingCurrent: Register indicating charging current in the fast charge stage. The ChargingCurrent register changes with nStepCurr, nIChgCfg1 and nIChgCfg2 registers at each step charging stage under different temperature conditions from 100mA to 3.15A.
  The charging profile shown in *Figure 1* has step charging disabled for simplicity. See *Step Charging* section for detailed configurations.

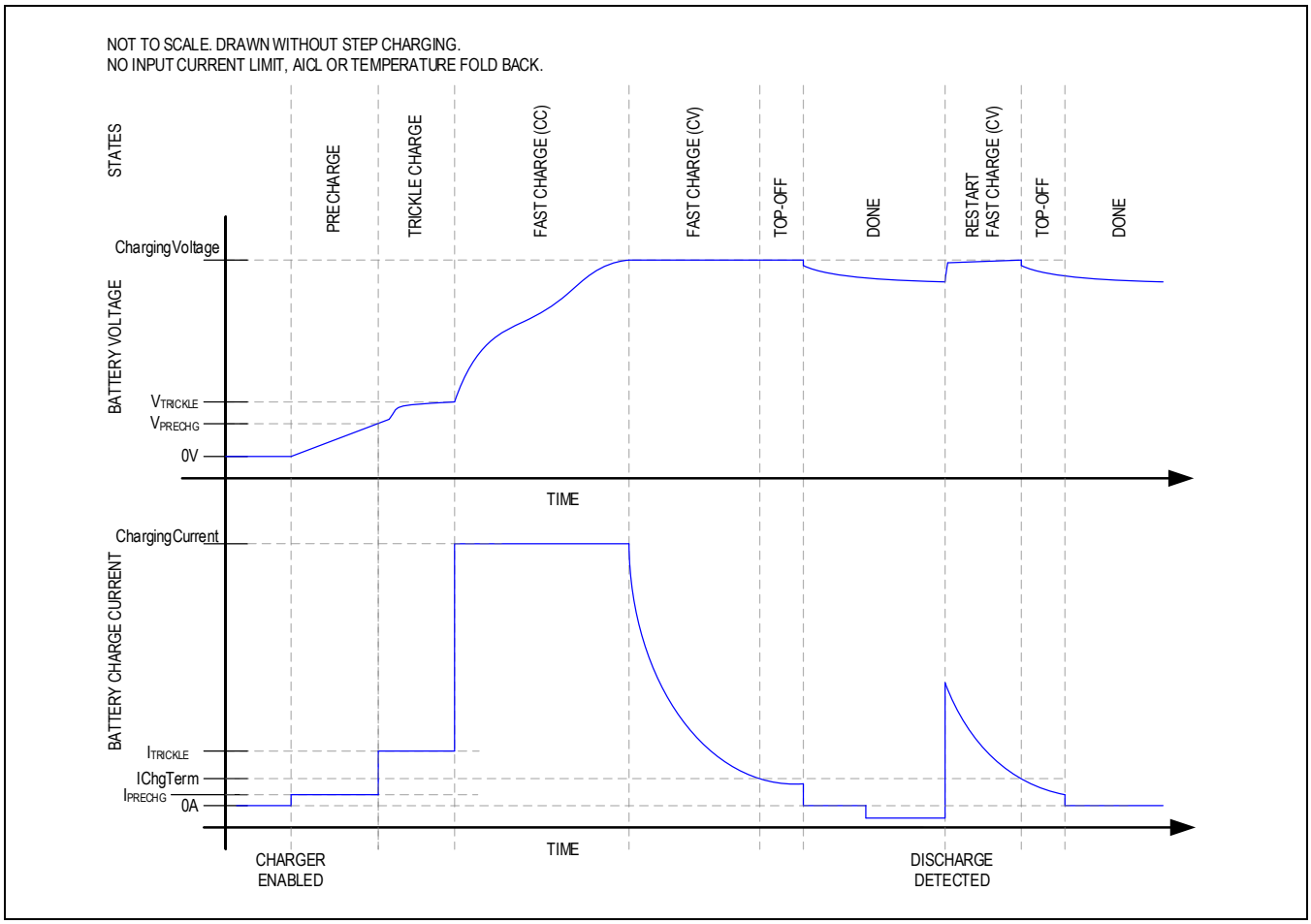


Figure 1. Li+/Li-Poly Charge Profile

CHARGE TERMINATION: The charger goes into top off mode after IChgTerm (from 20mA to 500mA) register setting is reached. Top off ends based on an I^2C programmable timer.

CHARGE RESTART: Once the charger stops charging after Full detected, if the discharge is detected, the charger restarts.

INIT State

From any non-fault state shown in *Figure 2*, MAX77972 enters INIT state whenever the charger inputs CHGIN is invalid. While in the INIT state, charging is disabled, the charge timer is forced to 0, Q_{BAT} is fully on, and power to the system is provided by the battery. To exit the INIT state, the charger input must be valid.

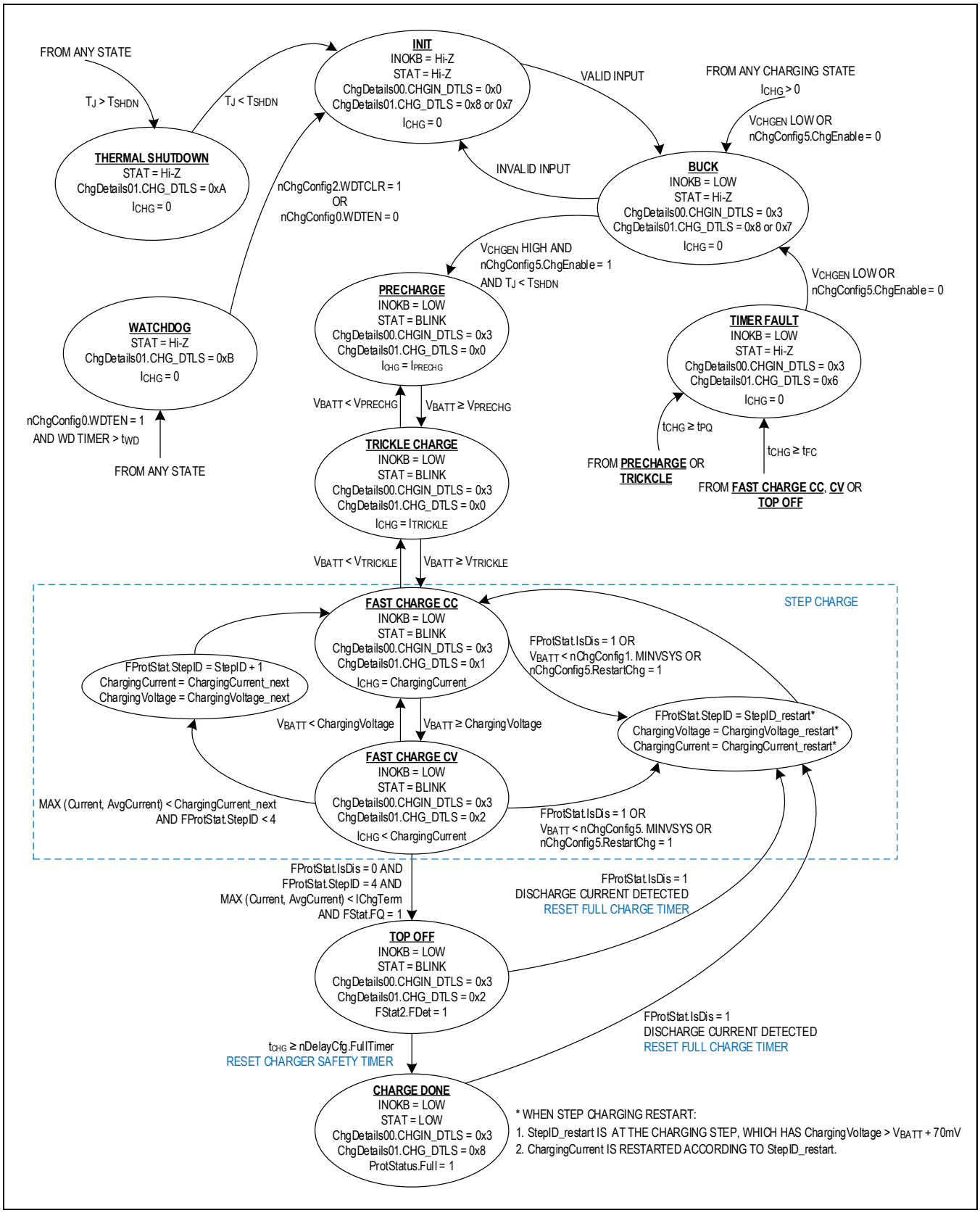

FROM ANY STATE
TJ > TSHDN
THERMAL SHUTDOWN
STAT = Hi-Z
ChgDetails01.CHG_DTLS = 0xA
ICHG = 0
TJ < TSHDN
INIT
INOKB = Hi-Z
STAT = Hi-Z
ChgDetails00.CHGIN_DTLS = 0x0
ChgDetails01.CHG_DTLS = 0x8 or 0x7
ICHG = 0
VALID INPUT
FROM ANY CHARGING STATE
ICHG > 0
VCHGEN LOW OR
nChgConfig5.ChgEnable = 0
INVALID INPUT
BUCK
INOKB = LOW
STAT = Hi-Z
ChgDetails00.CHGIN_DTLS = 0x3
ChgDetails01.CHG_DTLS = 0x8 or 0x7
ICHG = 0
nChgConfig2.WDTCLR = 1
OR
nChgConfig0.WDTEN = 0
VCHGEN HIGH AND
nChgConfig5.ChgEnable = 1
AND TJ < TSHDN
PRECHARGE
INOKB = LOW
STAT = BLINK
ChgDetails00.CHGIN_DTLS = 0x3
ChgDetails01.CHG_DTLS = 0x0
ICHG = IPRECHG
VCHGEN LOW OR
nChgConfig5.ChgEnable = 0
TIMER FAULT
INOKB = LOW
STAT = Hi-Z
ChgDetails00.CHGIN_DTLS = 0x3
ChgDetails01.CHG_DTLS = 0x6
ICHG = 0
WATCHDOG
STAT = Hi-Z
ChgDetails01.CHG_DTLS = 0xB
ICHG = 0
VBATT < VPRECHG
VBATT ≥ VPRECHG
nChgConfig0.WDTEN = 1
AND WD TIMER > tWD
FROM ANY STATE
TRICKLE CHARGE
INOKB = LOW
STAT = BLINK
ChgDetails00.CHGIN_DTLS = 0x3
ChgDetails01.CHG_DTLS = 0x0
ICHG = ITRICKLE
tCHG ≥ tPQ
tCHG ≥ tFC
FROM PRECHARGE OR
TRICKCLE
FROM FAST CHARGE CC, CV OR
TOP OFF
VBATT < VTRICKLE
VBATT ≥ VTRICKLE
STEP CHARGE
FAST CHARGE CC
INOKB = LOW
STAT = BLINK
ChgDetails00.CHGIN_DTLS = 0x3
ChgDetails01.CHG_DTLS = 0x1
ICHG = ChargingCurrent
FProtStat.StepID = StepID + 1
ChargingCurrent = ChargingCurrent_next
ChargingVoltage = ChargingVoltage_next
FProtStat.IsDis = 1 OR
VBATT < nChgConfig1. MINVSYS OR
nChgConfig5.RestartChg = 1
FProtStat.StepID = StepID_restart*
ChargingVoltage = ChargingVoltage_restart*
ChargingCurrent = ChargingCurrent_restart*
VBATT < ChargingVoltage
VBATT ≥ ChargingVoltage
FAST CHARGE CV
INOKB = LOW
STAT = BLINK
ChgDetails00.CHGIN_DTLS = 0x3
ChgDetails01.CHG_DTLS = 0x2
ICHG < ChargingCurrent
MAX (Current, AvgCurrent) < ChargingCurrent_next
AND FProtStat.StepID < 4
FProtStat.IsDis = 1 OR
VBATT < nChgConfig5. MINVSYS OR
nChgConfig5.RestartChg = 1
FProtStat.IsDis = 0 AND
FProtStat.StepID = 4 AND
MAX (Current, AvgCurrent) < IChgTerm
AND FStat.FQ = 1
FProtStat.IsDis = 1
DISCHARGE CURRENT DETECTED
RESET FULL CHARGE TIMER
TOP OFF
INOKB = LOW
STAT = BLINK
ChgDetails00.CHGIN_DTLS = 0x3
ChgDetails01.CHG_DTLS = 0x2
FStat2.FDet = 1
tCHG ≥ nDelayCfg.FullTimer
RESET CHARGER SAFETY TIMER
FProtStat.IsDis = 1
DISCHARGE CURRENT DETECTED
RESET FULL CHARGE TIMER
CHARGE DONE
INOKB = LOW
STAT = LOW
ChgDetails00.CHGIN_DTLS = 0x3
ChgDetails01.CHG_DTLS = 0x8
ProtStatus.Full = 1
* WHEN STEP CHARGING RESTART:
1. StepID_restart IS AT THE CHARGING STEP, WHICH HAS ChargingVoltage > VBATT + 70mV
2. ChargingCurrent IS RESTARTED ACCORDING TO StepID_restart.

Figure 2. Charger State Diagram

BUCK State

Once a valid input is applied to CHGIN, MAX77972 enters the BUCK state. The charger input is compared with several voltage thresholds to determine if it is valid. A valid charger input must meet the following three conditions:

- CHGIN must be above V_{CHGIN_UVLO} 4.7V. Once CHGIN is above the UVLO threshold, the information is latched and can only be reset when VCHGIN drops below AICL (adaptive input current loop) threshold V_{CHGIN_REG} 4.5V and the input current is lower than 60mA. The CHGIN UVLO and AICL thresholds are I^2C programmable through nChgConfig4.VCHGIN_REG.
- CHGIN must be below its overvoltage lockout threshold VCHGIN_OVLO 13.7V (typ).
- CHGIN must be above V_{SYS} by 200mV (typ).

The buck converter turns on, and power is delivered to SYS in the BUCK state. Charger exits BUCK state if charging is enabled: CHGEN pin is pulled high. It should be noted that there is an internal pulldown resistor connected to the CHGEN pin to ensure it is low when left floating. When it is pulled high, there is a microampere level of current going into CHGEN. To save power, it is recommended to tie CHGEN low or leave it floating in the battery-only mode when a switcher is not needed. ChgDetails00.CHGEN indicates inverse of CHGEN pin voltage when CHGIN voltage is valid. If CHGIN voltage is invalid, ChgDetails00.CHGEN stays 0, ignoring CHGEN pin voltage. Charger exits charging states and goes back to BUCK state if nChgConfig5.ChgEnable is set to 0 (default 1, enable charging).

PRECHARGE State

As shown in *Figure 2*, the PRECHARGE state occurs when the main battery voltage is less than V_{PRECHG} 2.5V. In this state, the charge current into the battery is I_{PRECHG} 55mA.

The following events cause the state machine to exit this state:

- The battery voltage rises above V_{PRECHG} 2.5V (typ), and the charger enters the TRICKLE CHARGE state.
- If the battery charger remains in this state for longer than t_{PQ} 30min, the charger moves to the TIMER FAULT state. ChgDetails01.CHG_DTLS indicates the timer fault status.

Note that the PRECHARGE state works with battery voltages down to 0V. The low 0V operation typically allows this battery charger to recover batteries that have an “open” internal pack protector. Typically, a pack internal protection circuit opens if the battery has seen an overcurrent, undervoltage or overvoltage. When a battery with an “open” internal pack protector is used with this charger, the precharge current flows into the 0V battery – this current raises the pack’s terminal voltage to the point where the internal pack protection switch closes.

A normal battery typically stays in the PRECHARGE state for several minutes or less. Therefore, a battery that stays in the PRECHARGE state for longer than 30 minutes may be experiencing a problem.

TRICKLE CHARGE State

As shown in *Figure 2*, the TRICKLE CHARGE state occurs when $V_{BATT} > V_{PRECHG}$ 2.5V (typ) and $V_{BATT} < V_{TRICKLE}$ 3.1V (typ). When the MAX77972 is in the TRICKLE CHARGE state, the charge current in the battery is less than or equal to $I_{TRICKLE}$ 300mA (typ). Charge current can be less than the setting value due to various reasons. See the *Reduced Charge Current* section for more details.

The following events cause the state machine to exit this state:

- When the battery voltage rises above $V_{TRICKLE}$ 3.1V, the charger enters the FAST CHARGE state.
- If the battery charger remains in this state for longer than the prequel timer t_{PQ} 30min (typ), the charger moves to the TIMER FAULT state. ChgDetails01.CHG_DTLS indicates the TIMER FAULT status.

Note that a normal battery typically stays in the TRICKLE CHARGE state for several minutes or less. Therefore, a battery that stays in TRICKLE CHARGE for longer than t_{PQ} may be experiencing a problem. The prequel timer runs through both PRECHARGE and TRICKLE CHARGE states. The TRICKLE CHARGE state can be disabled through nChgConfig0.PQEN. If it is disabled, the charger enters the FAST CHARGE state directly from the PRECHARGE state.

FAST CHARGE - STEP CHARGING

As shown in *Figure 2*, the charger enters the fast charge stage after the battery voltage rises above the trickle charge threshold. In the fast charge stage, MAX77972 offers a step charging profile, which sets five charge voltages/currents and manages a state-machine to transit through the stages, as shown in *Figure 3*. There are two step-charging schemes: Constant Voltage Step-Charging (CV Step-Charging) and Constant Current Step-Charging (CC Step-Charging). For simplicity, this section shows room temperature only. See the *FAST CHARGE - JEITA* section for JEITA operations.

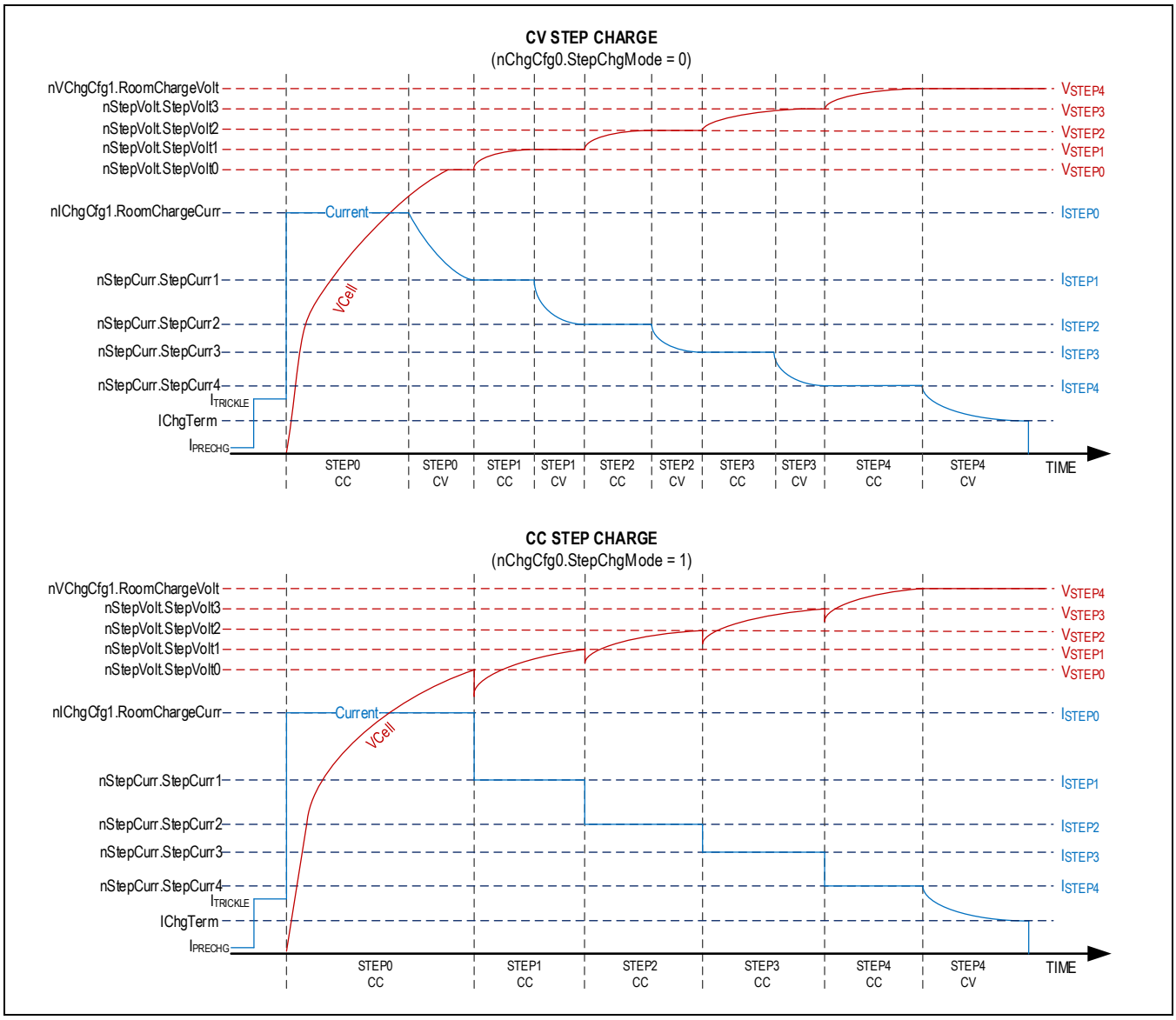


Figure 3. Step-Charging State Machine

The step-charging algorithm divides charging into five stages. In each step, the charge current and battery regulation voltage are updated in the ChargingCurrent and ChargingVoltage registers. ChargingCurrent decreases from step 0 to step 4, and ChargingVoltage increases from step 0 to step 4.

1. Step 0. Highest charging current, lowest charging voltage.

- $I_{CHG[Step0][Room]}$ = (nIChgCfg1.RoomChargeCurr + 1) × 50mA
- $V_{CHG[Step0][Room]}$ = $V_{CHG[Step1][Room]}$ - nStepVolt.StepVolt0 × 10mV

2. Step 1
   - $I_{CHG[Step1][Room]} = I_{CHG[Step0][Room]}$ - nStepCurr.StepCurr1 × 2 × 50mA
   - $V_{CHG[Step1][Room]} = V_{CHG[Step2][Room]}$ - nStepVolt.StepVolt1 × 10mV
3. Step 2
   - $I_{CHG[Step2][Room]} = I_{CHG[Step1][Room]}$ - nStepCurr.StepCurr2 × 50mA
   - $V_{CHG[Step2][Room]} = V_{CHG[Step3][Room]}$ - nStepVolt.StepVolt2 × 10mV
4. Step 3
   - $I_{CHG[Step3][Room]} = I_{CHG[Step2][Room]}$ - nStepCurr.StepCurr3 × 50mA
   - $V_{CHG[Step3][Room]} = V_{CHG[Step4][Room]}$ - nStepVolt.StepVolt3 × 10mV
5. Step 4. Lowest current, highest voltage.
   - $I_{CHG[Step4][Room]} = I_{CHG[Step3][Room]}$ - nStepCurr.StepCurr4 × 50mA
   - $V_{CHG[Step4][Room]}$ = 3.4V + (nVChgCfg1.RoomChargeVolt × 10mV)

MAX77972 offers two step-charging schemes: constant voltage step-charging and constant current step-charging. The main difference between the two control schemes is the way to move from one step to the next step.

- Constant Voltage Step-Charging (nChgCfg0.StepChgMode = 0, default). The charger moves to the next step when both of the below conditions are met:
  - Battery voltage reaches the ChargingVoltage register setting, and charger enters the CV state
    - ChgDetails01.CHG_DTLS is 0x2
  - Charge current drops below next step ChargingCurrent register setting
    - MAX(Current, AvgCurrent) < ChargingCurrent_next
- Constant Current Step-Charging (nChgCfg0.StepChgMode = 1). The charger moves to the next step when the below condition is met:
  - Battery voltage reaches the ChargingVoltage register setting.

As shown in *Figure 3.* CV step-charging allows battery voltage to increase smoothly, while CC step-charging may cause battery voltage to drop during transition due to cable/PCB parasitic and sharp reduced charge current. Step-charging can be disabled by setting nStepVolt or nStepCurr to 0. Charge current can be less than the ChargingCurrent setting value for various reasons; see the *Reduced Charge Current* section for more details.

In the step charging stage, the charger is not allowed to go from the higher step to the lower step unless under any of the following conditions:

- Discharge current detected.
  - FProtStat.IsDis = 1.
- Battery voltage drops below minimum system voltage.
  - V_{BATT} < nChgConfig1.MINVSYS
- Write charger restart bit to 1.
  - nChgConfig5.RestartChg = 1. This bit is auto-cleared to 0 after the restart is completed.

Once MAX77972 detects the restart event, it compares battery voltage with the lower step's ChargingVoltage. The charger is reset to a charging step, which has restarted ChargingVoltage 70mV higher than the battery voltage. ChargingCurrent is also restarted to the corresponding step.

The following events cause the state machine to exit the FAST CHARGE state:

- The charger enters TOP-OFF state when all the below conditions are met:
  - Charger is in step 4.
    - FProtStat.StepID is 0x4.
  - Battery voltage reaches ChargingVoltage[Step4] and charger enters CV state.
    - ChgDetails01.CHG_DTLS is 0x2
  - Charge current drops below the IChgTerm register setting.
    - MAX(Current, AvgCurrent) < IChgTerm

- If the battery charger remains in this state for longer than the fast charge timer, the charger moves to the TIMER FAULT state. ChgDetails01.CHG_DTLS indicates the TIMER FAULT status. The fast charge timer is I2C programmable through nChgConfig0.FCHGTIME.

The battery charger dissipates the most power in the FAST CHARGE state. This power dissipation causes the temperature to rise. There are 2 layers of charging control/protection: one through an external thermistor and the other through a die temperature sensor. See the *FAST CHARGE - JEITA* and *Thermal Foldback* section for more information.

FAST CHARGE - JEITA

The MAX77972 offers automatic charging control after the charger enters the FAST CHARGE stage with 9 JEITA temperature zones. There are three potential sources of JEITA temperature: thermistor from THM pin (default), internal die temperature sensor, or external overwrite through I2C. See the *Temperature Measurement* section for a detailed description.

As shown in *Figure 4*, all the JEITA thresholds are I2C programmable through nTPrtTh1 and nTPrtTh2. When the temperature changes from the room zone to other JEITA zones, the thresholds are set by the nTPrtTh1/2 corresponding setting. When the temperature changes from other JEITA zones back to the room zone, a 2.5°C hysteresis is applied to avoid instability at JEITA boundaries.

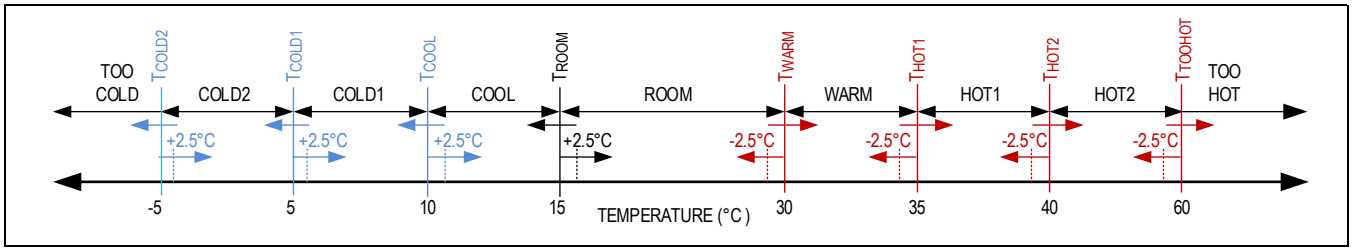
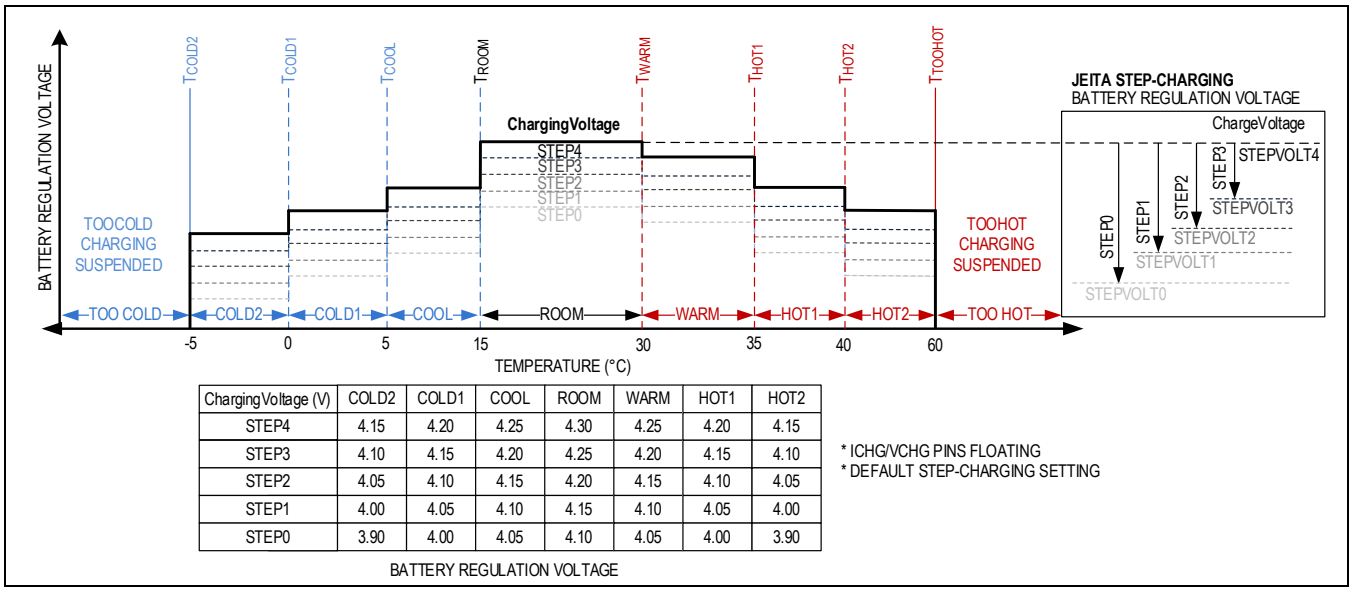


Figure 4. JEITA Temperature Regions

The room threshold is calculated as shown below:

- Room temperature threshold: T_{ROOM} = nTPrtTh1.Troom × 2.5°C + 10°C. For non-zero temperature settings of other JEITA temperature thresholds:
- Cool temperature threshold: $T_{COOL} = T_{ROOM}$ - (nTPrtTh1.Tcool + 1) × 2.5°C
- Cold1 temperature threshold: $T_{COLD1} = T_{COOL}$ - (nTPrtTh1.Tcold1 + 1) × 2.5°C
- Cold2 temperature threshold: $T_{COLD2} = T_{COLD1}$ - (nTPrtTh1.Tcold2 + 1) × 2.5°C
- Warm temperature threshold: $T_{WARM} = T_{ROOM}$ + (nTPrtTh2.Twarm + 1) × 2.5°C
- Hot1 temperature threshold: $T_{HOT1} = T_{WARM}$ + (nTPrtTh2.Thot1 + 1) × 2.5°C
- Hot2 temperature threshold: $T_{HOT2} = T_{HOT1}$ + (nTPrtTh2.Thot2 + 1) × 2.5°C
- TooHot temperature threshold: $T_{TOOHOT} = T_{HOT2}$ + (nTPrtTh2.Ttoohot + 1) × 2.5°C

Note that the corresponding temperature region is skipped if one JEITA field is set to 0. It is highly recommended to set nTPrtTh2.Twarm to be non-zero to maintain the minimum charging region for room temperature. In each JEITA temperature zone, ChargingCurrent and ChargingVoltage are updated to set charge current and battery regulation voltage at each charging step according to JEITA settings, as shown in *Figure 5* and *Figure 6*.

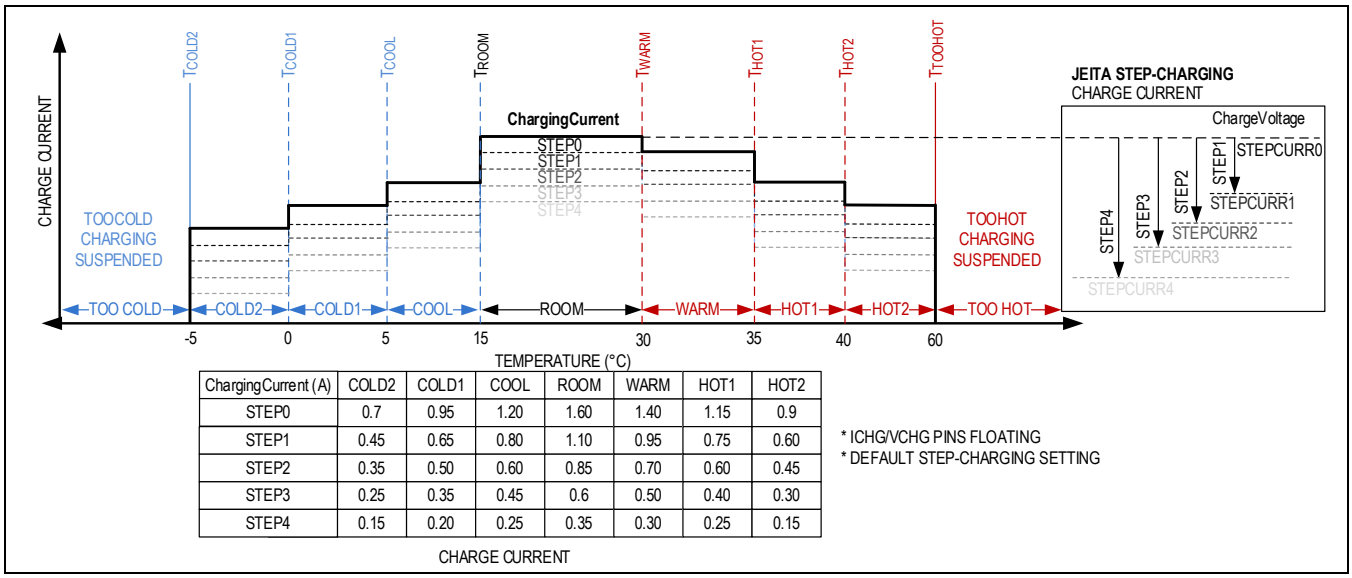


ChargingVoltage (V)	COLD2	COLD1	COOL	ROOM	WARM	HOT1	HOT2
STEP4	4.15	4.20	4.25	4.30	4.25	4.20	4.15
STEP3	4.10	4.15	4.20	4.25	4.20	4.15	4.10
STEP2	4.05	4.10	4.15	4.20	4.15	4.10	4.05
STEP1	4.00	4.05	4.10	4.15	4.10	4.05	4.00
STEP0	3.90	4.00	4.05	4.10	4.05	4.00	3.90

BATTERY REGULATION VOLTAGE

* ICHG/VCHG PINS FLOATING
* DEFAULT STEP-CHARGING SETTING

Figure 5. JEITA Step Voltage



ChargingCurrent (A)	COLD2	COLD1	COOL	ROOM	WARM	HOT1	HOT2
STEP0	0.7	0.95	1.20	1.60	1.40	1.15	0.9
STEP1	0.45	0.65	0.80	1.10	0.95	0.75	0.60
STEP2	0.35	0.50	0.60	0.85	0.70	0.60	0.45
STEP3	0.25	0.35	0.45	0.6	0.50	0.40	0.30
STEP4	0.15	0.20	0.25	0.35	0.30	0.25	0.15

CHARGE CURRENT

* ICHG/VCHG PINS FLOATING
* DEFAULT STEP-CHARGING SETTING

Figure 6. JEITA Step Current

The ChargingVoltage at step 4 (highest battery regulation voltage) for each temperature region is calculated as follows:

- $V_{CHG[Step4][Room]}$ = 3.4V + (nVChgCfg1.RoomChargeVolt × 10mV)
- $V_{CHG[Step4][Warm]}$ = $V_{CHG[Step4][Room]}$ - nVChgCfg1.WarmChargeVolt × 10mV
- $V_{CHG[Step4][Hot1]}$ = $V_{CHG[Step4][Warm]}$ - nVChgCfg2.Hot1ChargeVolt × 10mV
- $V_{CHG[Step4][Hot2]}$ = $V_{CHG[Step4][Hot1]}$ - nVChgCfg2.Hot2ChargeVolt × 10mV
- $V_{CHG[Step4][Cool]}$ = $V_{CHG[Step4][Room]}$ - nVChgCfg1.CoolChargeVolt × 10mV
- $V_{CHG[Step4][Cold1]}$ = $V_{CHG[Step4][Cool]}$ - nVChgCfg2.Cold1ChargeVolt × 10mV
- $V_{CHG[Step4][Cold2]}$ = $V_{CHG[Step4][Cold1]}$ - nVChgCfg2.Cold2ChargeVolt × 10mV

The ChargingCurrent at step 0 (highest charge current) for each temperature region is calculated as follows:

- $I_{CHG[Step0][Room]}$ = (nIChgCfg1.RoomChargeCurr +1) × 50mA
- $I_{CHG[Step0][Warm]}$ = $I_{CHG[Step0][Room]}$ – nIChgCfg1.WarmChargeCurr × 50mA
- $I_{CHG[Step0][Hot1]}$ = $I_{CHG[Step0][Warm]}$ – nIChgCfg2.Hot1ChargeCurr × 50mA
- $I_{CHG[Step0][Hot2]}$ = $I_{CHG[Step0][Hot1]}$ – nIChgCfg2.Hot2ChargeCurr × 50mA
- $I_{CHG[Step0][Cool]}$ = $I_{CHG[Step0][Room]}$ – nIChgCfg1.CoolChargeCurr × 50mA
- $I_{CHG[Step0][Cold1]}$ = $I_{CHG[Step0][Cool]}$ – nIChgCfg2.Cold1ChargeCurr × 50mA
- $I_{CHG[Step0][Cold2]}$ = $I_{CHG[Step0][Cold1]}$ – nIChgCfg2.Cold2ChargeCurr × 50mA

Battery regulation voltage in each step under the corresponding JEITA zone is calculated as follows:

- $V_{CHG[StepX][JEITA]}$ = $V_{CHG[StepX][Room]}$ / $V_{CHG[Step4][Room]}$ × $V_{CHG[Step4][JEITA]}$

Note that the ChargingVoltage has a 10mV resolution above 4V and a 100mV resolution below 4V. The actual regulation voltage is rounded down to the closest available value. The default value of the JEITA step voltage table is shown in *Figure 5*. Charge current in each step under the corresponding JEITA zone is calculated as follows:

- $I_{CHG[StepX][JEITA]}$ = $I_{CHG[StepX][Room]}$ / $I_{CHG[Step0][Room]}$ × $I_{CHG[Step0][JEITA]}$

Note that the ChargingCurrent has a 50mA resolution with 100mA as a minimum. The actual regulation current is rounded down to the closest available value and clamped to 100mA. The default value of the JEITA step current table is shown in *Figure 6*. In the TooCold and TooHot zone, charging is suspended:

- $I_{CHG[StepX][TooHot]}$ = 0. Charging is suspended. ProtStat.TooHot is set to 1.
- $I_{CHG[StepX][TooCold]}$ = 0. Charging is suspended. ProtStat.TooCold is set to 1.

The charger goes back to the BUCK state when it is under TooHot/TooCold protection. To disable the temperature dependence and create a flat charging voltage/current across the temperature range, set nVChgCfg1.RoomChargeVolt or nIChgCfg.RoomChargeCurr as desired and configure the other settings with a value of 0x0.

TOP-OFF State

As shown in *Figure 2*, the charger enters a TOP-OFF state when all the following conditions are met:

- Charger is in step 4.
  - FProtStat.StepID is 0x4.
- Battery voltage reaches ChargingVoltage[Step4] and charger enters CV state.
  - ChgDetails01.CHG_DTLS is 0x2
- Charge current drops below the IChgTerm register setting.
  - MAX(Current, AvgCurrent) < IChgTerm

The MAX77972 starts full-timer once the above conditions are met. In the top-off state, the battery charger tries to maintain the battery voltage at the regulation target, and typically, the charge current is less than or equal to IChgTerm.

The following events cause the state machine to exit this state:

- After nDelayCfg.FullTimer timeout, the charger enters the FULL state.
- If discharge current is detected FProtStat.IsDis = 1, the charger goes back to the FAST CHARGE CC state. MAX77972 sends the charger back to step charging with the following process:
  - Reset the Charging Voltage to be at least 70mV higher than the MAX(VCell, AvgVCell) from the step charging table.
  - Reset FProtStat.StepID and ChargingCurrent accordingly with selected CharingVoltage.

CHARGE DONE/FULL State

As shown in *Figure 2*, the battery charger enters the CHARGE DONE/FULL state after the charger has been in the TOPOFF state for nDelayCfg.FullTimer. The following events cause the state machine to exit this state:

- If discharge current is detected FProtStat.IsDis = 1, the charger goes back to the FAST CHARGE CC state. MAX77972 sends the charger back to step charging with the following process:
  - Reset ChargingVoltage to be at least 70mV higher than MAX(VCell, AvgVCell) from the step charging table.
  - Reset FProtStat.StepID and ChargingCurrent accordingly with selected CharingVoltage.

Charging Indicators Input Status (INOKB)

INOKB is an open-drain and active low output that indicates charger input status. When a valid input source is inserted, the buck converter starts switching, and subsequently, INOKB is pulled low. When the reverse boost is enabled, INOKB pulls low to indicate 5V output from CHGIN. INOKB can be used as an LED indicator driver by adding a current limit resistor and LED to SYS. Alternatively, INOKB can be used as a logic output for the system processor by adding a 200kΩ pull-up resistor to the system IO voltage.

Charge Status Output (STAT)

STAT is an open-drain and active low output that indicates charging status. The various STAT pin states are listed below. STAT can be used as a logic output for system processor by adding a 200kΩ pull-up resistor to system IO voltage and a rectifier (a diode and a capacitor). STAT also can be used as a LED indicator driver by adding a current limit resistor and a LED to SYS.

Table 1. STAT Output Per Charging Status

CHARGE STATUS	STAT PIN BEHAVIOR	PIN EQUIVALENT LOGIC STATE	CHARGE STATUS LED
No Input	High Impedance	High	OFF
Trickle, Precharge, Fast Charge	Repeat Low and High Impedance with 1Hz, 50% duty cycle	After an external diode and a capacitor rectifier, High.	Blinking with 1Hz, 50% duty cycle.
Done	Low	Low	Solid ON
Faults	High Impedance	High	OFF

Charger Interrupt (ALRT)

The MAX77972 allow interrupts to be generated by detecting various charging events. Interrupts are generated on the ALRT pin open-drain output driver. An external pullup resistor is required to generate a logic-high signal. When any of the charger interrupt mask in ChgMaskSts is unmasked, the corresponding interrupt shows on the ALRT pin. Write 0 to the interrupt bit to clear it from ALRT. Note that the charger and fuel gauge interrupts share the ALRT pin. Charger interrupts have a higher priority to toggle the pin. See the *Fuel Gauge Alert* section for fuel gauge alerts.

ICHG/VCHG Resistor Configured Charging

On MAX77972, ICHG and VCHG pins can be populated with 1% resistors to achieve the desired configuration of various charging and fuel gauge settings. See *Table 2* and *Table 3* for the series resistor and selected output value. The ICHG pin is biased and checked to determine nIChgCfg1.RoomChargeCurr, IChgTerm and DesignCap. The VCHG pin is biased and checked to determine nVChgCfg1.RoomChargeVolt, Vempty, ModelCFG.ModelID and ModelCFG.VCHG. MAX77972 launches ICHG/VCHG detection under the following two circumstances:

- After POR, ICHG/VCHG pin are biased and checked automatically.
- Write Config.PinConfig to 1 to manually launch ICHG/VCHG detection and reset the corresponding registers. Config.PinConfig is auto cleared after ICHG/VCHG detection is completed.

After the ICHG/VCHG detection is completed, MAX77972 clears FOTPStat.PinDraft to 0. VCHG Selection does not support some chemistries such as lithium-iron-phosphate (LiFePO4) and Panasonic NCR/NCA series cells; for those cells, I²C configuration is required.

Table 2. ICHG Pin Resistor Configuration

ICHG 1% resistor (kΩ)	PinID.ICHG	nIChgCfg1.RoomChargeCurr (mA)	IChgTerm (mA)	DesignCap (mAh)
0.075	0x0	3150	350	1575
0.232	0x1	3000	300	1500
0.402	0x2	2750	300	1375
0.576	0x3	2500	300	1250
0.768	0x4	2250	300	1125
0.976	0x5	2000	200	1000
1.21	0x6	1900	200	950
1.43	0x7	1800	200	900
1.69	0x8	1700	200	850
1.96	0x9	1600	200	800
2.26	0xA	1500	150	750
2.61	0xB	1400	150	700
3.01	0xC	1300	150	650
3.4	0xD	1200	150	600
3.83	0xE	1100	150	550
4.42	0xF	1000	100	500
4.99	0x10	900	100	450
5.62	0x11	800	100	400
6.34	0x12	700	100	350
7.32	0x13	650	100	325
8.25	0x14	600	100	300
9.53	0x15	550	100	275
11	0x16	500	100	250
13	0x17	450	100	225
15.4	0x18	400	100	200
18.2	0x19	350	100	175
22.6	0x1A	300	100	150
28.7	0x1B	250	100	125
38.3	0x1C	200	100	100
54.9	0x1D	150	100	75
95.3	0x1E	100	100	50
> 294	0x1F	1600	100	1500

Table 3. VCHG Pin Resistor Configuration

VCHG 1% resistor (kΩ)	PinID.VCHG	nVChgCfg1.RoomChargeVolt (V)	Vempty.VE (V)	Vempty.VR (V)	ModelCFG. ModelID	ModelCFG. VCHG
0.075	0x0	4.5	3.4	3.96	0	1
0.232	0x1	4.47	3.4	3.96	0	1
0.402	0x2	4.45	3.4	3.96	0	1
0.576	0x3	4.44	3.4	3.96	0	1
0.768	0x4	4.43	3.4	3.96	0	1
0.976	0x5	4.42	3.4	3.96	0	1
1.21	0x6	4.4	3.4	3.96	0	1
1.43	0x7	4.39	3.35	3.92	0	1
1.69	0x8	4.38	3.35	3.92	0	1
1.96	0x9	4.37	3.35	3.92	0	1
2.26	0xA	4.36	3.35	3.92	0	1
2.61	0xB	4.35	3.35	3.92	0	1
3.01	0xC	4.34	3.3	3.88	0	1
3.4	0xD	4.32	3.3	3.88	0	1
3.83	0xE	4.3	3.3	3.88	0	1
4.42	0xF	4.27	3.3	3.88	0	1
4.99	0x10	4.25	3.3	3.88	0	1
5.62	0x11	4.22	3.3	3.88	0	0
6.34	0x12	4.2	3.3	3.88	0	0
7.32	0x13	4.17	3.3	3.88	0	0
8.25	0x14	4.15	3.3	3.88	0	0
9.53	0x15	4.12	3.3	3.88	0	0
11	0x16	4.1	3.3	3.76	0	0
13	0x17	4	3.3	3.68	0	0
15.4	0x18	3.9	3.2	3.56	0	0
18.2	0x19	3.8	3.1	3.48	0	0
22.6	0x1A	3.7	3	3.36	6	0
28.7	0x1B	3.6	2.9	3.32	6	0
38.3	0x1C	3.55	2.85	3.32	6	0
54.9	0x1D	3.5	2.8	3.28	6	0
95.3	0x1E	3.45	2.7	3.2	6	0
> 294	0x1F	4.3	3.3	3.88	0	1

Charger Operation Modes

The MAX77972 includes a full-featured switch-mode charger for a one-cell lithium-ion (Li+) or lithium polymer (Li-polymer) battery. The current limit for CHGIN input is automatically configured allowing flexibility for connection to either an AC-to-DC wall adapter or a USB port. The synchronous switch-mode DC-DC converter utilizes 1.5MHz switching frequency, which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The charger can operate in buck mode, OTG mode and reverse boost mode as needed.

ADI's Smart Power Selector architecture always makes the best use of the limited adapter power and the battery's power to supply up-to-buck mode CHGIN current limit from the adapter to the system. Additionally, supplement mode provides additional current from the battery to the system up to BATT to SYS overcurrent threshold. Adapter power that is not used for the system goes to charging the battery. All power switches for charging and switching the system load between battery and adapter power are integrated on the chip – no external MOSFET required.

ADI's proprietary process technology allows for low-$R_{DS(on)}$ devices in a small solution size. The total dropout resistance from the adapter power input to the battery is 165mΩ (typ), assuming the inductor has 0.04Ω of ESR. This 165mΩ typical dropout resistance allows for charging a battery up to 3.15A. The resistance from the BATT to the SYS node is 20mΩ, allowing for low power dissipation and long battery life. A multitude of safety features ensures reliable charging. Features include a charge timer, junction thermal regulation, over/under voltage protection, short circuit protection, and BATT to SYS overcurrent protection (see the *Charger Protections* section for more information).

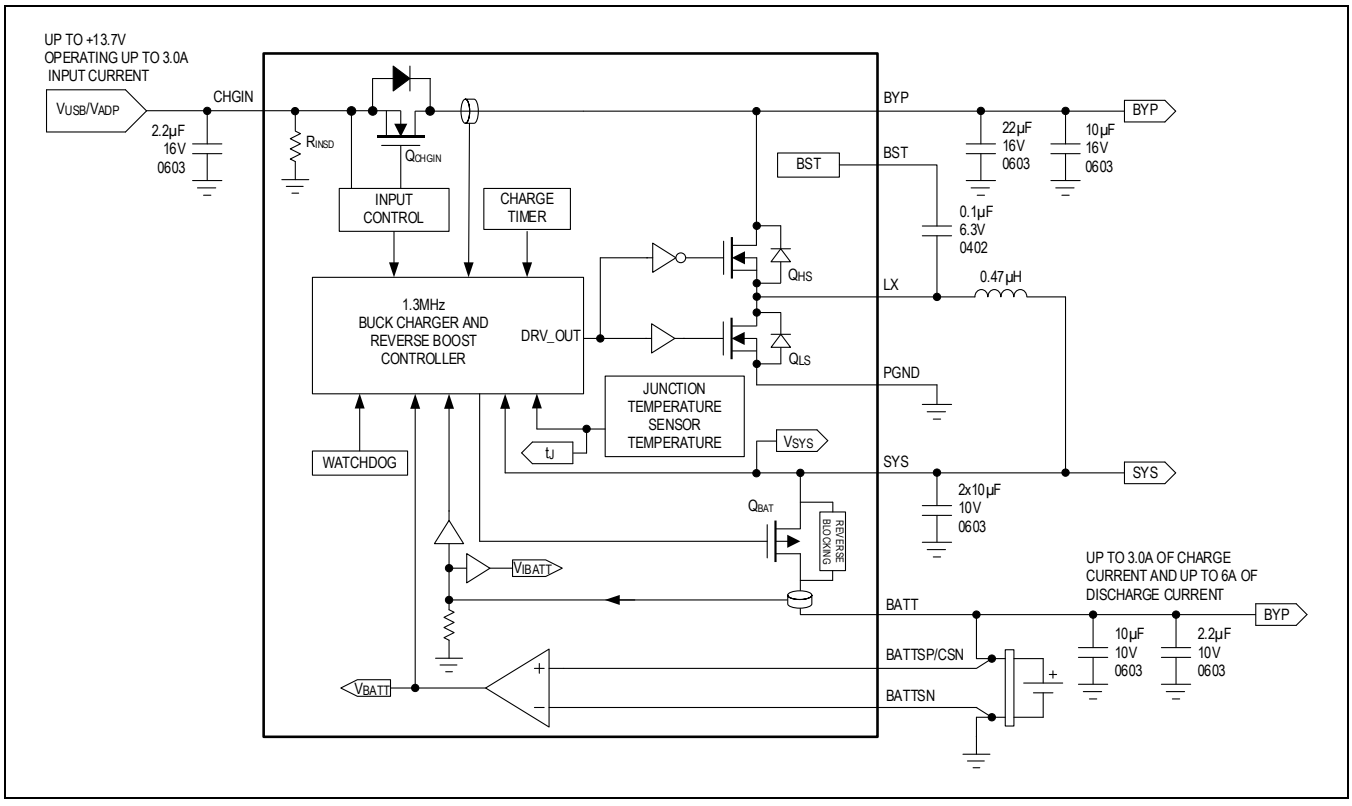


Figure 7. Battery Charger Detailed Functional Diagram

Smart Power Selector

The Smart Power Selector architecture is a network of internal switches and control loops that distributes energy among CHGIN, BYP, SYS and BATT. The principle of the energy delivery is:

- Both V_{CHGIN} and V_{BAT} are valid
  - CHGIN is the primary source of energy.
  - The battery is the secondary source of energy.
  - Energy delivery to SYS is the highest priority.
  - Any energy that is not required by SYS is available to the battery.
- Battery only mode
  - Energy delivery to SYS is the highest priority.
  - Any energy not required by SYS is available for BYP or CHGIN when reverse boost or OTG is enabled.

The charger switches among a couple of modes during operation to achieve the above goals. *Figure 7* shows a detailed functional diagram of this architecture. The charger operation is summarized in *Table 4*.

Table 4. Charger Operation Mode

	BUCK REGULATION TARGET	Q_{CHGIN}	Q_{HS}/Q_{LS}	Q_{BAT}	SYS VOLTAGE
Buck No Charging	V_{SYS} (ChargingVoltage)	On	Switching	Off	ChargingVoltage
Precharge	V_{SYS} (ChargingVoltage) I_{CHG} (Fixed 55mA) from internal current source	On	Off	Off	ChargingVoltage
Trickle Charge	V_{SYS} (nChgConfig1.MINVSYS) I_{CHG} (Fixed 300mA)	On	Switching	Linear	nChgConfig1.MINVSYS
Fast Charge	I_{BATT} (ChargingCurrent)	On	Switching	On	$V_{BATT} + I_{BATT} \times R_{BAT2SYS}$
Input Current	I_{CHGIN} (USB detection or nChgConfig3.CHGIN_ILIM)	On	Switching	On	$V_{BATT} - V_{BSREG}$ (Trickle) $V_{BATT} - I_{BATT} \times R_{BAT2SYS}$ (Fast Charge)
Input Voltage (AICL)	V_{CHGIN} (nChgConfig4.VCHGIN_REG)	On	Switching	On	$V_{BATT} - V_{BSREG}$ (Trickle) $V_{BATT} - I_{BATT} \times R_{BAT2SYS}$ (Fast Charge)
Thermal Foldback	T_J (nChgConfig2.REGTEMP)	On	Switching	On	$V_{BATT} - V_{BSREG}$ (Trickle) $V_{BATT} - I_{BATT} \times R_{BAT2SYS}$ (Fast Charge)
OTG	V_{BYP} (Fixed 5.1V)	On	Switching	On	$V_{BATT} - I_{BATT} \times R_{BAT2SYS}$
Reverse Boost	V_{BYP} (nChgConfig3.VBYPSET)	Off	Switching	On	$V_{BATT} - I_{BATT} \times R_{BAT2SYS}$
Battery Only	N/A	Off	Off	On	$V_{BATT} - I_{BATT} \times R_{BAT2SYS}$

Input Current Limit

The input current limit loop allows the battery to provide a supplement current when the combined load (BYP and SYS) exceeds the input current limit. MAX77972 offers two ways to set the input current limit.

- Through integrated USB detection. Once the USB device is plugged in, after the charger type detection is done, MAX77972 automatically configuresthe input current limit to the highest settings that the source can provide. See the *USB Detection* section for details. By default, the automatic USB detection for the input current limit is enabled.
- Manually set the input current limit through I^2C. Write nChgConfig4.NO_AUTOISET to 1 to enable manual input current setting. Then set nChgConfig3.CHGIN_ILIM to the desired input current limit.

Adaptive Input Current Limiting Loop (AICL)

An adaptive input current limiting loop (AICL) allows the charger to be well-behaved when attached to a poor-quality charge source. The loop improves performance with relatively high resistance charge sources that exist when long cables

are used, or devices are charged with non-compliant USB hub configurations. The AICL loop automatically reduces the input current to keep the input voltage at V_{CHGIN_REG} 4.5V (default). The CHGIN regulation voltage is I^2C programmable through nChgConfig4.VCHGIN_REG. If the input current limit is reduced to 60mA and the charger is in the AICL loop, then the charger is turned off.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the junction temperature of MAX77972. As shown in *Figure 8*, when the die temperature exceeds the nChgConfig2.REGTEMP, a thermal limiting circuit reduces the battery charger's target current by 5%/°C (ATJ_{REG}). The target charge current reduction is achieved with an analog control loop (i.e. not a digital reduction in the input current).

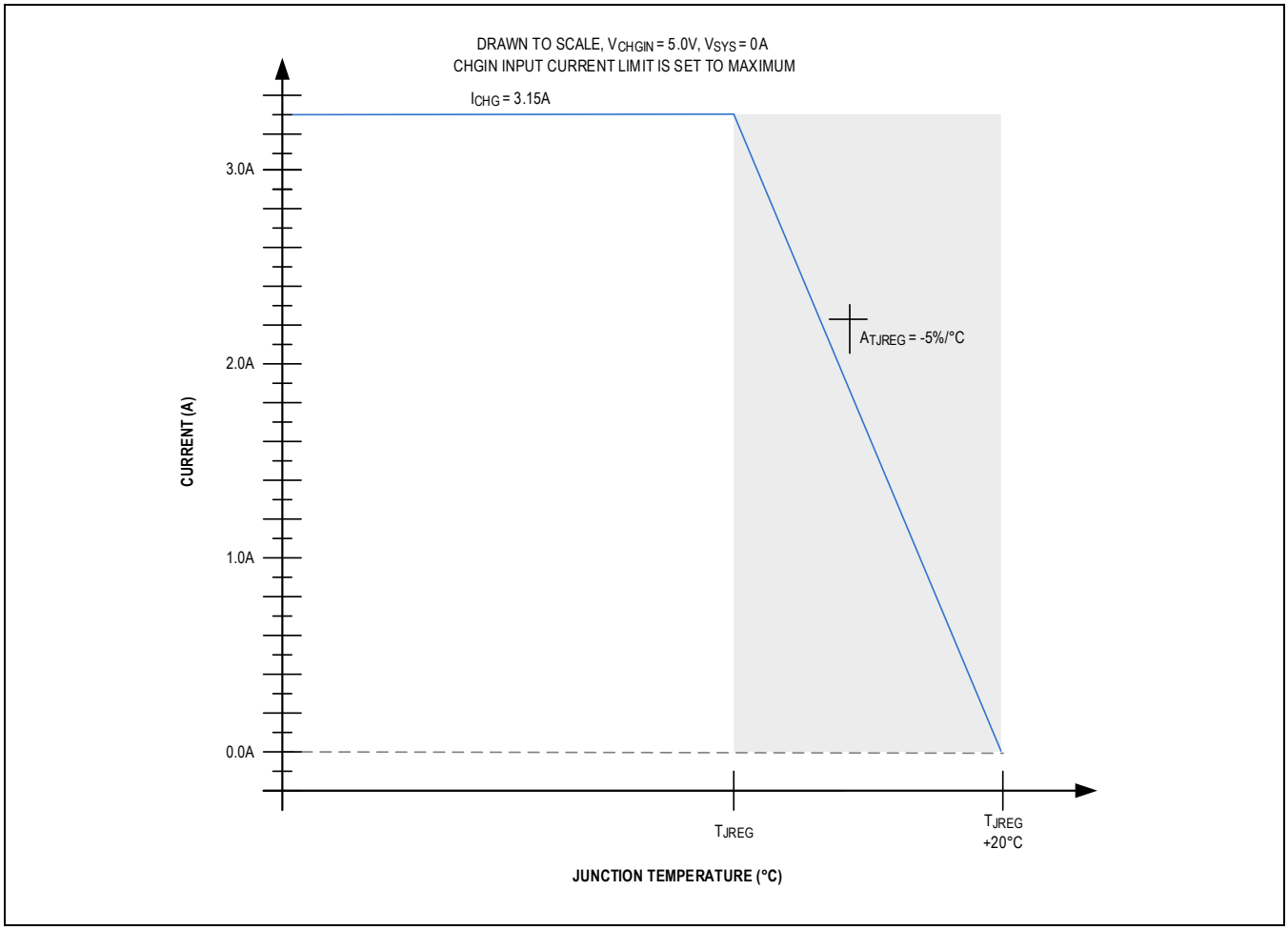


Figure 8. Charge Currents vs. Junction Temperature

Reduced Charge Current

In all the charging state (I_{CHG} > 0) other than PRECHARGE in *Figure 2*, the charge current may be lower than the setting value, $I_{TRICKLE}$, or ChargingCurrent register for various of reasons:

- The charger is in fast charge CV mode.
- The charger input is in the input current limit loop.
- The charger is in the AICL loop.
- The charger is in thermal foldback.

OTG and Reverse Boost Mode

The DC-DC converter topology of the MAX77972 allows it to operate as a buck converter or reverse boost converter. There are two reverse modes: OTG and reverse boost.

- Set nChgConfig0.MODE = 0xA or 0xB to enter OTG mode. In the OTG mode, the DC-DC converter operates in reverse boost mode, and Q_{CHGIN} is fully on. OTG mode allows the charger to source current to BYP and CHGIN. The BYP and CHGIN voltage is maintained at a fixed 5.1V. OTG current limit at CHGIN is I²C configurable through nChgConfig1.OTG_ILIM. The Q_{CHGIN} automatically tries to retry after 300ms if CHGIN loading exceeds nChgConfig1.OTG_ILIM. If the overload at CHGIN persists, then the CHGIN switch toggles ON and OFF with ~60ms ON and ~300ms OFF. It is recommended to follow the steps below to enable OTG:
  - Wait until ChgDetails00.CHGIN_OK is 0. CHGIN voltage is below CHGIN UVLO threshold 4.5V (default)
  - Pull the CHGEN pin high. Note that the CHGEN needs to be high to enable OTG mode
  - Write nChgConfig0.MODE to 0xA or 0xB to enable OTG
- Set nChgConfig0.MODE = 0x8 or 0x9 to enter reverse boost mode. The DC-DC converter operates in reverse boost mode and Q_{CHGIN} is fully off. Reverse boost mode allows charger to source current to only BYP pin. V_{BYP} is I²C programmable through nChgConfig.VBYPSET up to 5.5V. There is no current limit at BYP pin, but if the battery discharge current exceeds nChgConfig1.B2SOVRC, Q_{BAT} is turned off. See the *Battery Discharge Overcurrent Protection* section for detailed description.

Charger operation modes are set through nChgConfig0.MODE as shown in *Table 5*. Note that turning on/off the charger is also controlled by MAX77972's internal logic according to the charging profile described in the *Charging Control* section. If it is desired to force the charger to turn off, set nChgConfig5.ChgEnable to 0 instead of directly setting nChgConfig9.MODE to 0x4.

Table 5. Charger Modes

nChgConfig0.MODE	CHARGER MODES
0x0, 0x1	**Battery Only:** charger = off, OTG = off, buck = off, boost = off
0x4 (Do not set through I²C)	**Charger Off:** charger = off, OTG = off, buck = on, boost = off
0x5	**Charger On:** charger = on, OTG = off, buck = on, boost = off
0x8, 0x9	**Reverse Boost to BYP:** charger = off, OTG = off, buck = off, boost = on
0xA, 0xB	**OTG to CHGIN:** charger = off, OTG = on, buck = off, boost = on
0x2, 0x3, 0x6, 0x7, 0xC, 0xD, 0xE, 0xF	N/A. No change.

Input Self Discharge

To ensure that a rapid removal and re-insertion of a charge source always results in a charger input interrupt, the charger input presents loading to the input capacitor to ensure that when the charge source is removed, the input voltage decays below the UVLO threshold in a reasonable time. The input self-discharge is implemented with a 70kΩ resistor from CHGIN input to ground.

Charger Protections

Charge Timer Fault

The battery charger provides a prequal timer and a fast charge timer to ensure safe charging. The charge timer prevents the battery from charging indefinitely.

- The time that the charger is allowed to remain in precharge and trickle charge states is t_{PQ}, fixed at 30 minutes.
- The time that the charger is allowed to remain in the fast charge CC, CV and top-off states is nChgConfig0.FCHGTIME.

The charger is suspended upon charger timeout. ChgDetails01.CHG_DTLS moves to 0x6. STAT becomes Hi-Z. As shown in *Figure 2*, the charger exit timer fault state by suspending charging and restart:

- Plug out and re-insert the charger input from CHGIN
- Toggle the CHGEN pin low and back to high
- Write nChgConfig5.ChgEnable bit to 0 and restart by setting it to 1

Watchdog Timer

In addition to charger safety timers, the MAX77972 also provides a watchdog timer to ensure safe charging. As shown in *Figure 2*, the watchdog timer protects the battery from charging indefinitely if the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with nChgConfig0.WDTEN = 0. Enable the watchdog timer feature by setting nChgConfig0.WDTEN to 1. While enabled, the system controller must reset the watchdog timer within the timer period t_{WD} 80s (min) for the charger to operate normally. Reset the watchdog timer by programming nChgConfig2.WDTCLR = 0x01.

If the watchdog is not serviced on time, the battery charger can be configured to perform different operations:

- nChgConfig2.WD_QBATOFF bit is set to 0 (default). Charger suspended charging when the watchdog timer expires. The buck converter is still active to support the SYS load. If the charger was previously in any charging state (precharge, trickle charge, fast charge CC, fast charge CV, and top-off) before watchdog timeout, ChgDetails00.CHG_OK is cleared to 0, and a ChgMaskSts.CHG_I interrupt is generated upon timer expiration. ChgDetails00.CHG_DTLS = 0x0B, which indicates that the charger is off because the watchdog timer has expired. Once the watchdog timer has expired, the charger may be restarted by programming nChgConfig2.WDTCLR=0x01. The SYS node can be supported by the battery and/or the adapter through the DC-DC buck while the watchdog timer is expired.
- nChgConfig2.WD_QBATOFF bit is set to 1. and the watchdog timer expires, MAX77972 turns off the buck, charger Q_{BAT} switch and cycle SYS power for 150ms.

Battery Discharge Overcurrent Protection

The MAX77972 protects itself, the battery, and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current may occur for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit.

When the BATT to SYS discharge current exceeds nChgConfig1.B2SOVRC for at least t_{BOVRC} 6ms, MAX77972 turns off Q_{BAT} to disable the BATT to SYS discharge path. Under discharge overcurrent fault condition, when SYS is low (V_{SYS} < V_{SYSUP}) for 150ms, MAX77972 restarts on its own and attempts to pull up SYS again. If the fault condition remains, the whole cycle is repeated until this fault condition is removed.

When MAX77972 is in battery discharge overcurrent protection state, the internal current sense circuit is not under regular operation condition. If the MAX77972 is under this condition for a while, it may affect fuel gauge accuracy. It is recommended to follow the software implementation guide to reload the model if the MAX77972 is found in this fault state. Check ChgDetails01.BAT_dis_OC to see if the fault happened. This indicator bit retains its value until it is written to 0 from the application processor.

Inrush Current Control during System Power-Up

This feature limits the main battery to system current to I_{SYSPU} 50mA (typ) as long as V_{SYS} is less than V_{SYSPU} 2V (typ) during battery-only startup. This feature limits the surge current that typically flows from the main battery to the device's low-impedance system bypass capacitors during a system power-up. A system power-up happens anytime that current from the battery is supplied to SYS when V_{SYS} < V_{SYSPU}. For V_{SYS} < V_{SYSPU}, the systems designer should review how much is the current draw on V_{SYS} since a load exceeding I_{SYSPU} prevents a successful power-up. This "system power-up" condition typically occurs when a battery is hot-inserted into an otherwise unpowered device. When "system power-up" occurs due to hot insertion, a slight delay is required for inrush control circuits to activate. A current spike over I_{SYSPU} may occur during this time.

USB Detection

The MAX77972 provides USB BC1.2 charger detection and Type-C detection. The key features of USB detection are:

- USB BC1.2 charger detection:
  - D+/D- charging signature detector
  - USB BC1.2 Compliant with SDP, DCP and CDP detection
  - Detect proprietary charger types
    - Apple 500mA, 1A, 2A, 12W
    - Samsung 2A
- USB Type-C detection:
  - CC source detection. Automatically set the input current limit according to the source capability.

USB BC1.2 Charger Detection

The USB charger detection is USB BC1.2 compliant and can automatically detect some common proprietary charger types. The MAX77972 USB detection follows USB BC1.2 requirements and detects SDP, CDP and DCP types. In addition to USB BC1.2 State Machine, the IC also detects a limited number of proprietary charger types (Apple, Samsung and generic 500mA). The BC1.2 detected charger type is reported at UsbDetails.CHGTYP and proprietary charger types are reported at UsbDetails.PRCHGTYP. If D+/D- is found as open, UsbDetails.ChgTyp is indicated as SDP by BC1.2 requirements. The MAX77972 automatically sets the CHGIN input current limiting based on the charger type detection results. UsbDetails.USB_INLIM indicates the input current limit set by USB detection. If the charger type detection result is unknown charger type, the input current limit is set to 500mA.

Table 6. USB BC1.2 DETECTED CHARGER TYPE (UsbDetails.CHGTYP)

Input Current Limit	Charger detected
500mA	No adapter found
500mA	SDP
1.5A	CDP
1.5A	DCP

Table 7. Detected Proprietary Charger Type (UsbDetails.PRCHGTYP)

Input Current Limit	Charger detected
500mA	Apple
1A	Apple
2A	Apple
2.4A	Apple 12W
2A	Samsung
3A	All others

After the charger type detection is done, MAX77972 automatically configures the input current limit to the highest settings that the source can provide. If the input source is not a standard power source described by BC1.2 or USB Type-C or a proprietary charger type that MAX77972 can detect, the MAX77972 sets the input current limit to 500mA. Disable USB BC1.2 detection by setting nChgConfig4.CHGDETEN to 0.

USB Type-C Detection

The MAX77972 works as a sink compliant with USB Type-C rev1.2 specifications. The USB Type-C functions are controlled by a logic state machine which follows the Type-C requirements. The MAX77972 sets the CHGIN input current limit based on the current advertised on the CC wires. When a source is detected, the type-C state machine auto-detects the active CC line. The state machine auto-detects the source advertised current (500mA, 1.5A and 3.0A). Upon detection of a change in the advertised current, the chip automatically sets the input current limit. The setting input current is reported at UsbDetails.CC_CURR. USB Type-C detection can be disabled by setting nChgConfig5.CCDetEn to 0.

The MAX77972 executes D+/D- detection and CC detection in parallel and takes the higher of the two input current limit values determined by D+/D- detection and by CC detection.

ModelGauge m5 EZ Fuel Gauge

The MAX77972 incorporate the ModelGauge m5 algorithm that combines the excellent short-term accuracy and linearity of a coulomb counter with the excellent long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. ModelGauge m5 cancels offset accumulation error in the coulomb counter, while providing better short-term accuracy than any purely voltage-based fuel gauge. Additionally, the ModelGauge m5 algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time. The device automatically compensates for aging, temperature, and discharge rate and provides accurate state-of-charge (SOC) in mAh or % over a wide range of operating conditions.

The device provides two methods for reporting the age of the battery: reduction in capacity and cycle odometer. The device provides precision measurements of current, voltage, and temperature. The temperature of the battery pack is measured using an external thermistor supported by ratiometric measurements on an auxiliary input. An I2C interface provides access to data and control registers.

ModelGauge m5 Algorithm

Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated. It causes the reported capacity error to increase over time and requires periodic corrections. Corrections are traditionally performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the true state-of-charge (SOC) based on the battery voltage after a long time of no current flow. Both have the same limitation: if the correction condition is not observed over time in the actual application, the error in the system is boundless. The accuracy of such corrections dominates the performance of classic coulomb counters. Voltage measurement-based SOC estimation has accuracy limitations due to imperfect cell modeling but does not accumulate offset error over time.

The IC includes an advanced voltage fuel gauge (V_{FG}) that estimates open-circuit voltage (OCV), even during current flow, and simulates the nonlinear internal dynamics of a Li+ battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC. This SOC estimation does not accumulate offset error over time. The IC performs a smart empty compensation algorithm that automatically compensates for the effect of temperature conditions and load conditions to provide accurate state-of-charge information. The converge-to-empty function eliminates error toward an empty state. The IC learns battery capacity over time automatically to improve long-term performance. The age information of the battery is available in the output registers.

The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a V_{FG}. See *Figure 9*. The complementary combined result eliminates the weaknesses of both the coulomb counter and the V_{FG} while providing the strengths of both. A mixing algorithm weighs and combines the V_{FG} capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the V_{FG} capacity result is used to continuously make small adjustments to the battery state, cancelling the coulomb-counter drift.

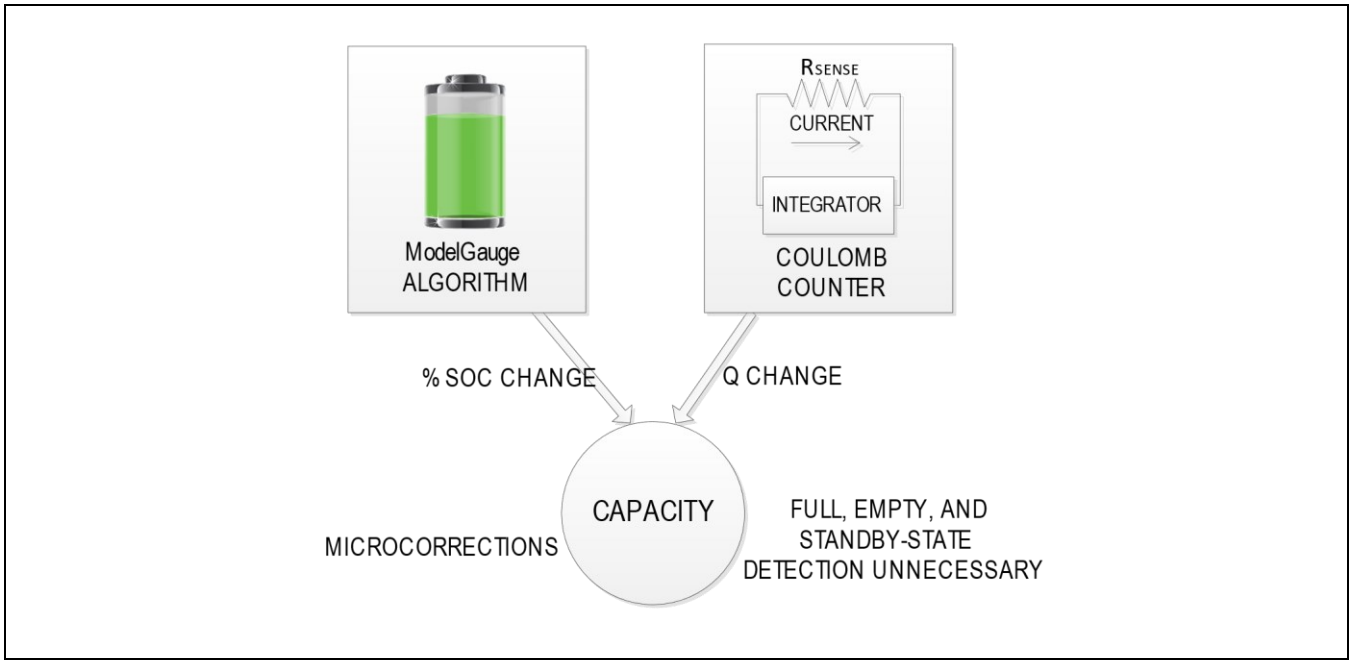


Figure 9. ModelGauge m5 Algorithm

The ModelGauge m5 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. As the battery approaches the critical region near empty, the ModelGauge m5 algorithm invokes a special error correction mechanism that eliminates any error.

The ModelGauge m5 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the voltage-fuel-gauge dynamics adapt based on cell-voltage behavior in the application.

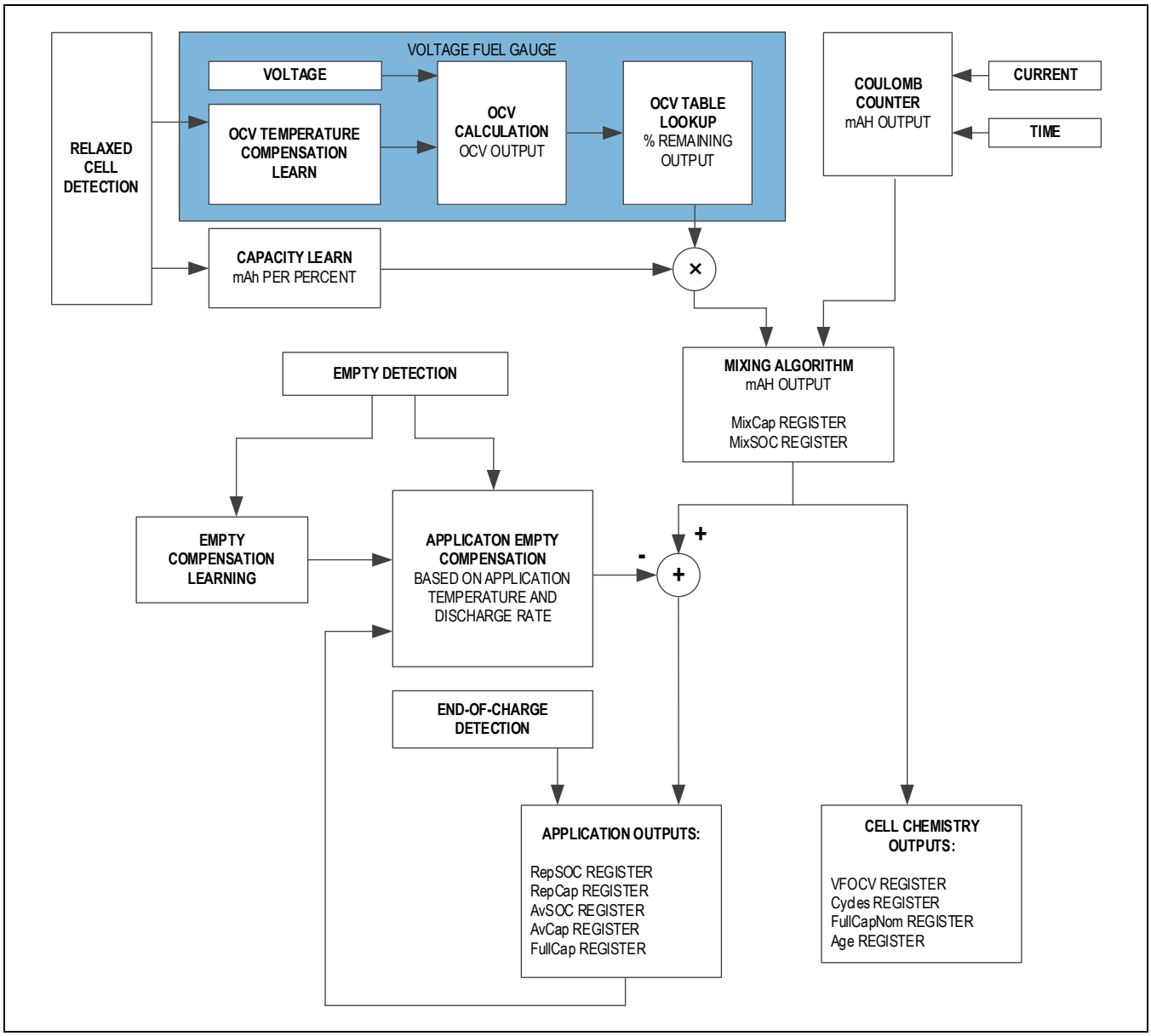


Figure 10. ModelGauge m5 EZ Block Diagram

ModelGauge m5 EZ Performance

ModelGauge m5 EZ performance provides plug-and-play operation when the IC is connected to most lithium batteries. While the IC can be custom tuned to the application's specific battery through a characterization process for ideal performance, the IC can provide good performance for most applications with no custom characterization required. *Table 8* and *Figure 11* show the performance of the ModelGauge m5 algorithm in applications using ModelGauge m5 EZ configuration.

The ModelGauge m5 EZ provides good performance for most cell types. For some chemistries, such as lithium-iron-phosphate ($LiFePO_4$) and Panasonic NCR/NCA series cells, it is suggested that the customer request a custom model from ADI for best performance.

For even better fuel-gauging accuracy than ModelGauge m5 EZ, contact Analog for information regarding cell characterization.

Table 8. ModelGauge m5 EZ Performance

DESCRIPTION	AFTER FIRST CYCLE* (%)	AFTER SECOND CYCLE* (%)
Tests with less than 3% error	95	97
Tests with less than 5% error	98.7	99
Tests with less than 10% error	100	100

**Test conditions: +20°C and +40°C, run time of > 3 hours.*

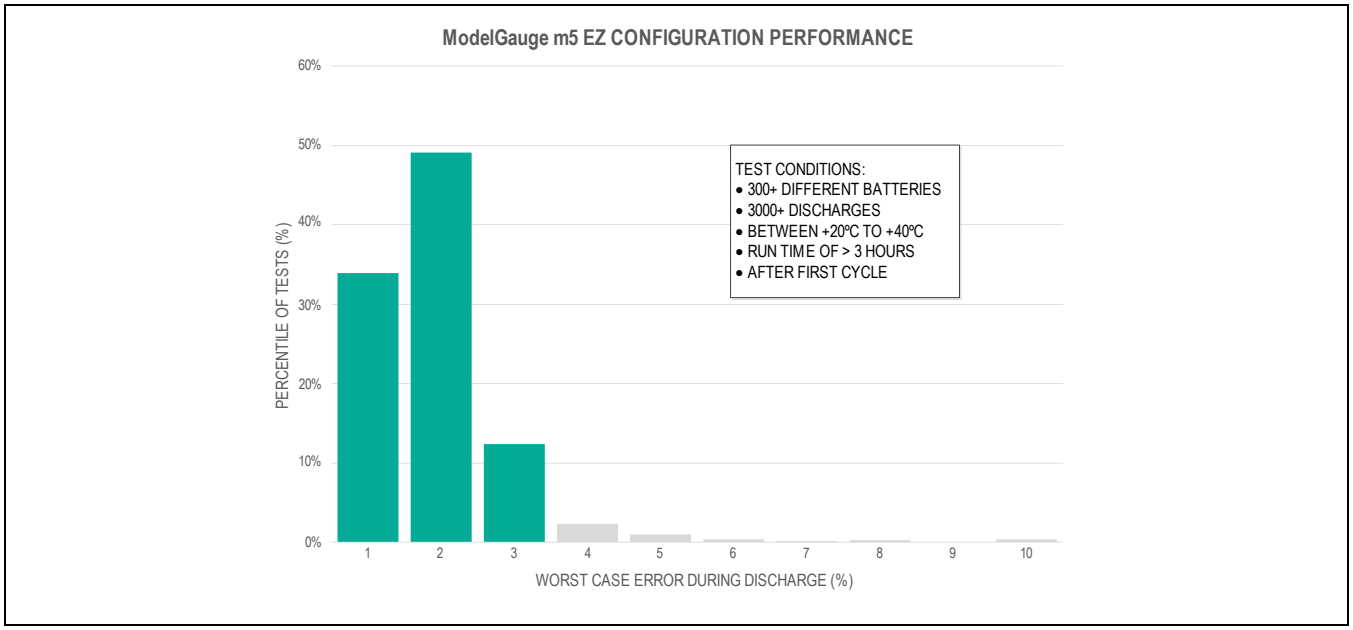


Figure 11. ModelGauge m5 EZ Configuration Performance

OCV Estimation and Coulomb-Count Mixing

The core of the ModelGauge m5 algorithm is a mixing algorithm that combines the OCV state estimation with the coulomb counter. After the power-on reset of the IC, coulomb-count accuracy is unknown. The OCV state estimation is weighted heavily compared to the Coulomb count output. As the cell progresses through cycles in the application, coulomb-counter accuracy improves, and the mixing algorithm alters the weighting so that the coulomb-counter result is dominant. From this point forward, the IC switches to servo mixing. Servo mixing provides a fixed magnitude continuous error correction to the coulomb count, up or down, based on the direction of error from the OCV estimation. This allows differences between the coulomb count and OCV estimation to be corrected quickly. See *Figure 12* for more details.

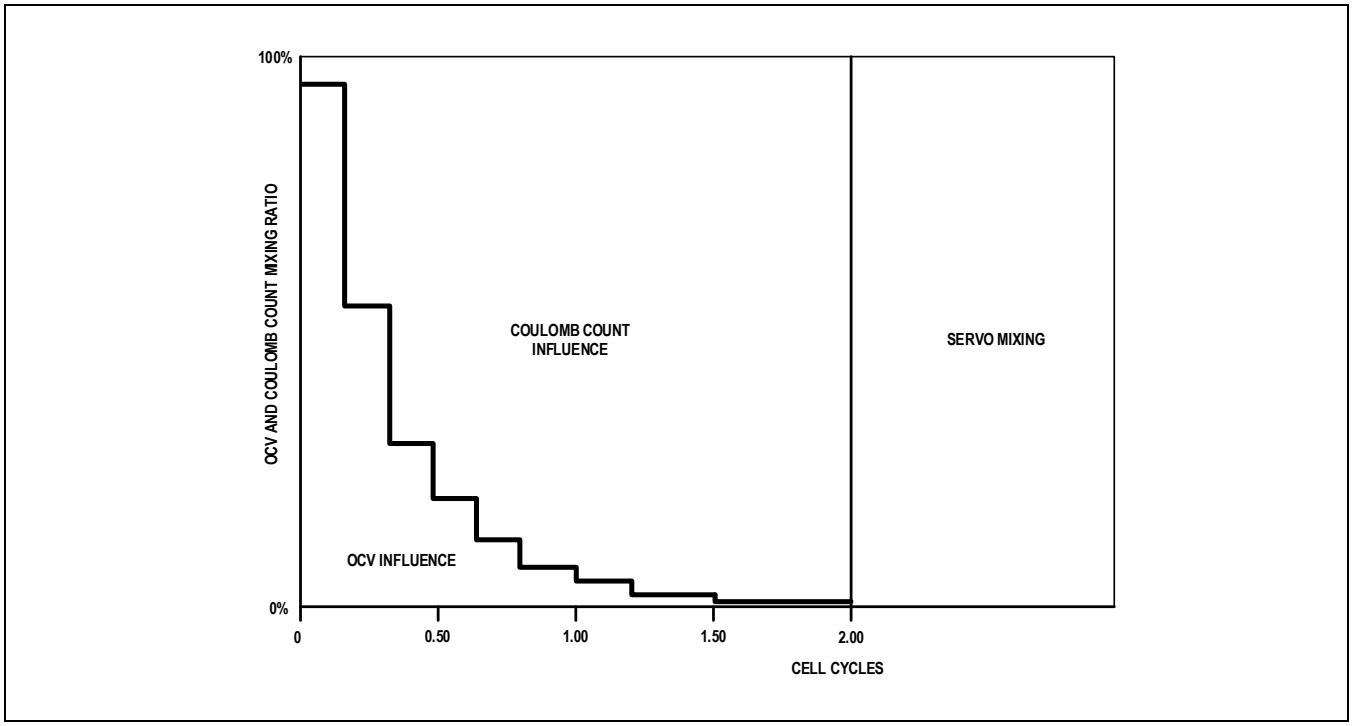


Figure 12. Voltage and Coulomb Count Mixing

The resulting output from the mixing algorithm does not suffer drift from current measurement offset error and is more stable than a stand-alone OCV estimation algorithm. Initial accuracy depends on the relaxation state of the cell. See *Figure 13*. The highest initial accuracy is achieved with a fully relaxed cell.

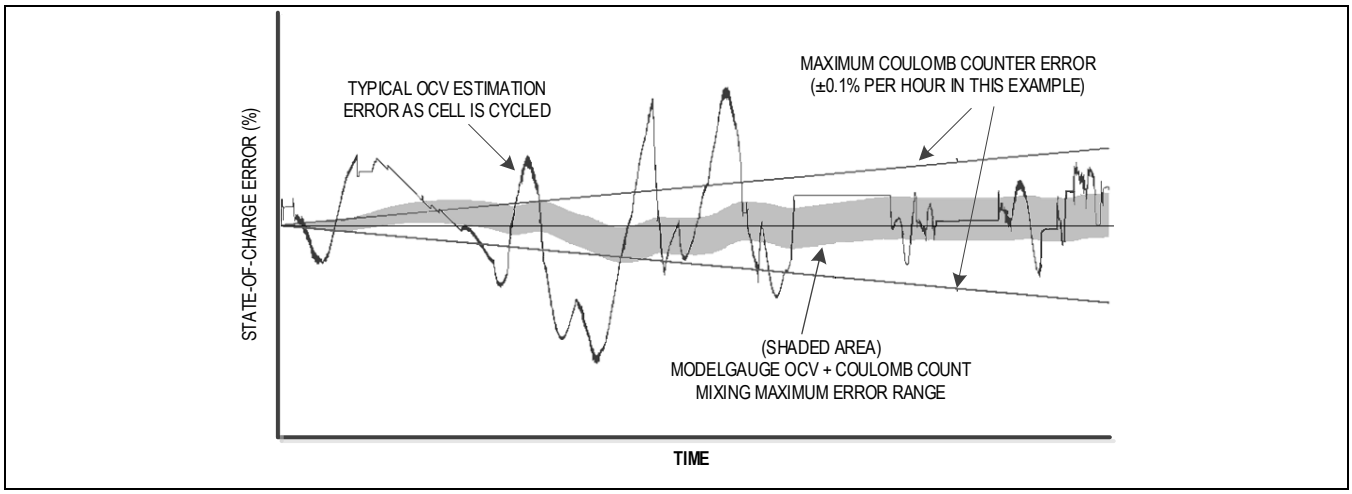


Figure 13. ModelGauge m5 Typical Accuracy Example

ModelGauge m5 EZ Registers

For accurate results, ModelGauge m5 EZ uses information about the cell and the application as well as the real-time information measured by the IC. *Figure 14* shows inputs and outputs to the algorithm grouped by category. Analog input registers are the real-time measurements of voltage, temperature, and current performed by the IC. Application-specific registers are programmed by the customer to reflect the operation of the application. The Cell Characterization Information registers hold characterization data that models the behavior of the cell over the operating range of the application. The Algorithm Configuration registers allow the host to adjust the performance of the IC for its application. The Learned Information registers allow an application to maintain the accuracy of the fuel gauge as the cell ages.

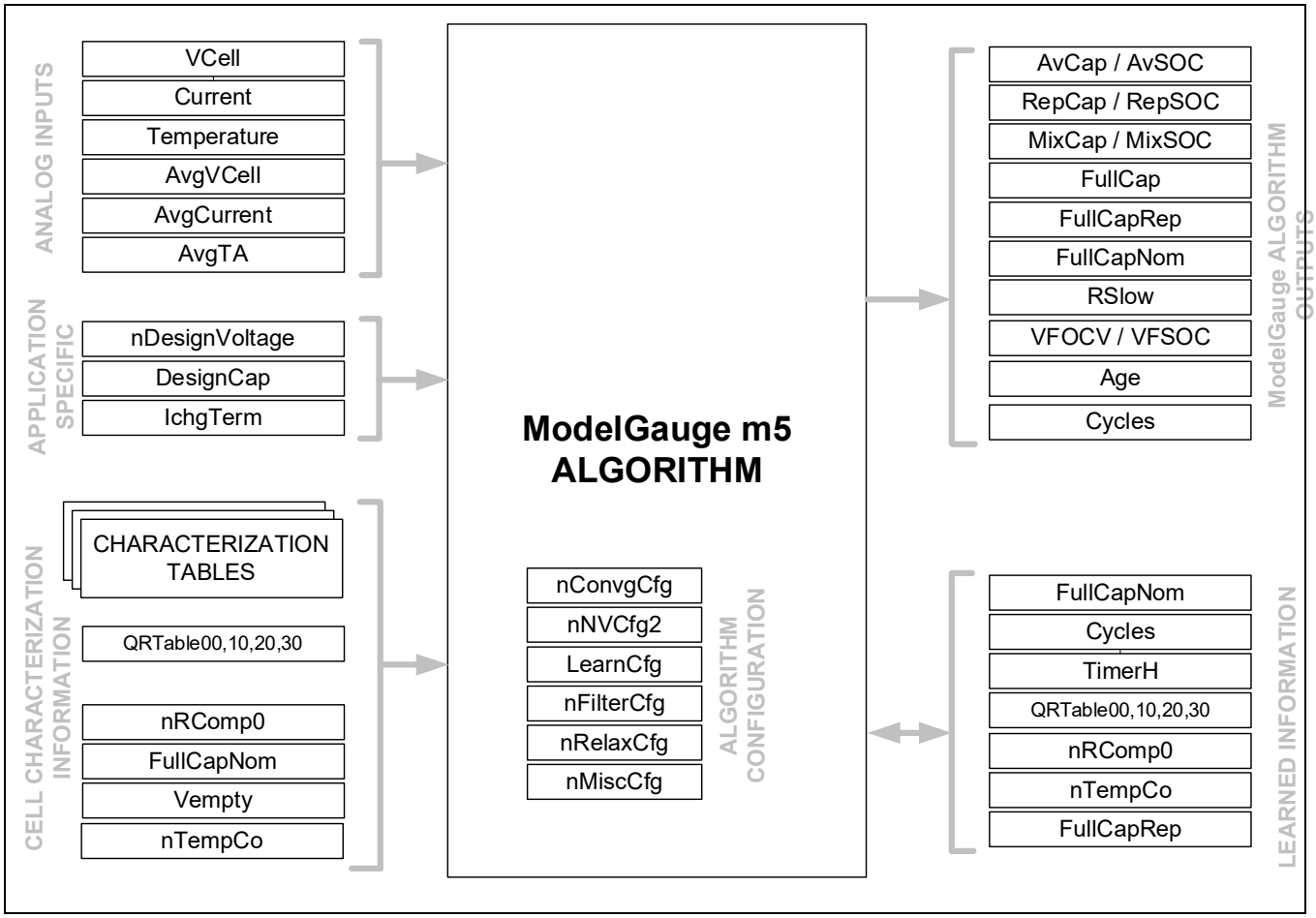


Figure 14. ModelGauge m5 EZ Registers

Fuel Gauge Learning

The MAX77972 periodically makes internal adjustments to cell characterization and application information to remove initial errors and maintain accuracy as the cell ages. These adjustments always occur as small under-corrections to prevent instability of the learning process and prevent any noticeable jumps in the fuel-gauge outputs. Learning occurs automatically without any input from the host. In addition to estimating the state of charge, the IC observes the battery's relaxation response and adjusts the dynamics of the voltage fuel gauge. To maintain learned accuracy through power loss, the host must periodically save learned information and restore it after power is returned. Registers used by the algorithm include:

- **Application Capacity (FullCapRep Register).** This is the total capacity available to the application at full, set through the IChgTerm registers as described in the *Top-Off State* section.
- **Cell Capacity (FullCapNom Register).** This is the total cell capacity at full, including some capacity that sometimes is not available to the application due to high loads and/or low temperature. The IC periodically compares the percent change based on an open circuit voltage measurement with the coulomb-count change as the cell charges and discharges, maintaining an accurate estimation of the cell capacity in mAh as the cell ages. See *Figure 15*.
- **Voltage Fuel-Gauge Adaptation**. The IC observes the battery's relaxation response and adjusts the dynamics of the voltage fuel gauge. This adaptation adjusts the nRComp0 register during qualified cell relaxation events. The learning can occur during relaxation events with a charge/discharge cycle. The
- doesn't require charge-to-full or discharge-to-empty.
- **Empty Compensation Adaptation.** The IC updates internal data whenever a cell empty is detected (VCell or AvgVCell < VE) to account for cell age or other cell deviations from the characterization information.

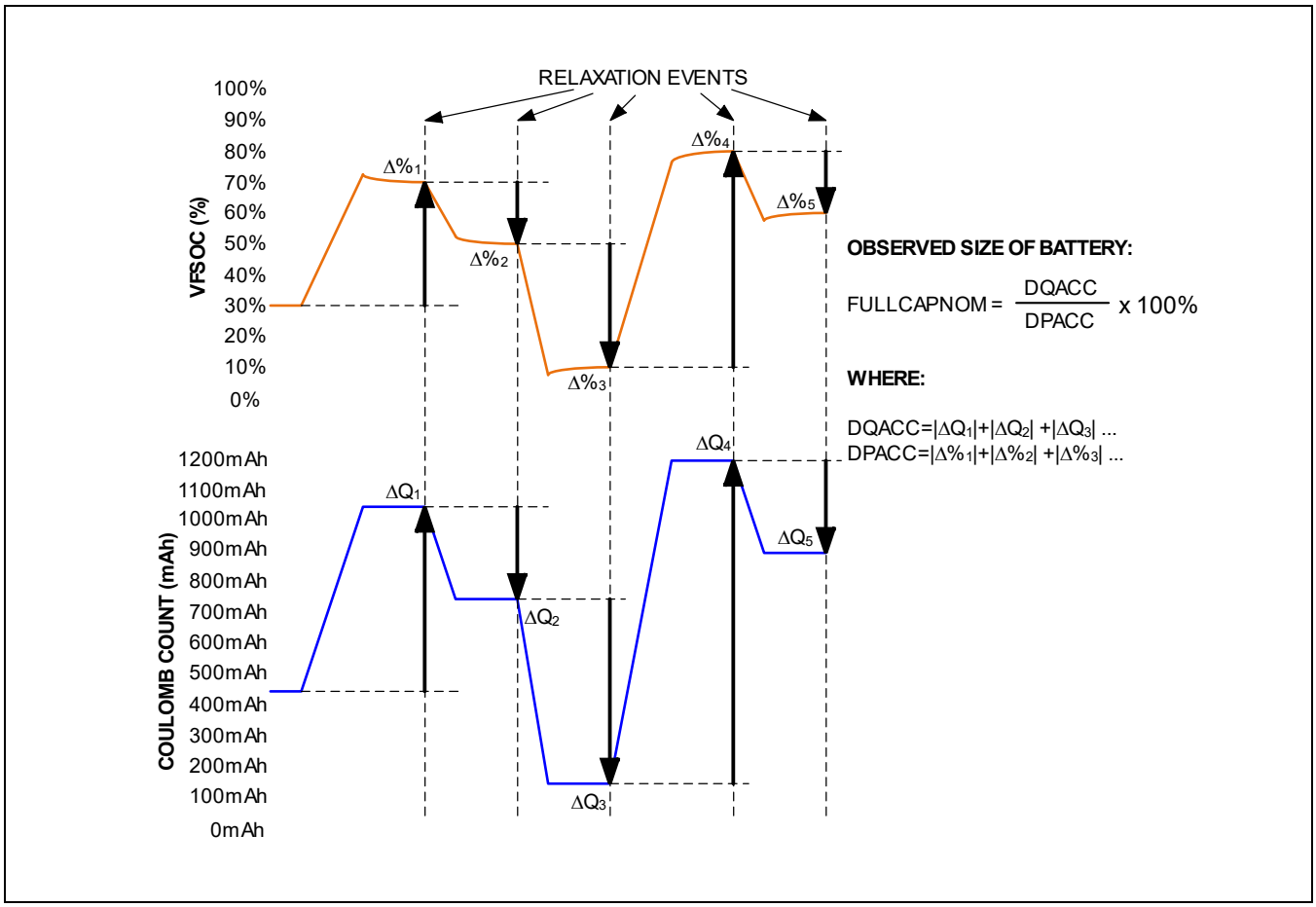


Figure 15. ModelGauge m5 Learns Full Capacity during Arbitrary Cycling

Empty Compensation

As the temperature and discharge rate of an application changes, the amount of charge available to the application also changes. The ModelGauge m5 algorithm distinguishes between remaining capacity of the cell, remaining capacity of the application, and reports both results to the user.

The MixCap output register tracks the charge state of the cell. This is the theoretical mAh of charge that can be removed from the cell under ideal conditions—extremely low discharge current and independent of cell voltage. This result is not affected by application conditions such as cell impedance or minimum operating voltage of the application. ModelGauge m5 continually tracks the expected empty point of the application in mAh. This is the amount of charge that cannot be removed from the cell by the application because of minimum voltage requirements and internal losses of the cell. The IC subtracts the amount of charge not available to the application from the MixCap register and reports the result in the AvCap register.

Since available remaining capacity is highly dependent on discharge rate, the AvCap register can be subject to large instantaneous changes as the application load current changes. The result can increase, even while discharging if the load current suddenly drops. This result, although correct, can be very counter-intuitive to the host software or end user. The RepCap output register contains a filtered version of AvCap that removes any abrupt changes in remaining capacity. RepCap converges with AvCap over time to correctly predict the application empty point while discharging or the application full point while charging. *Figure 16* shows the relationship of these registers.

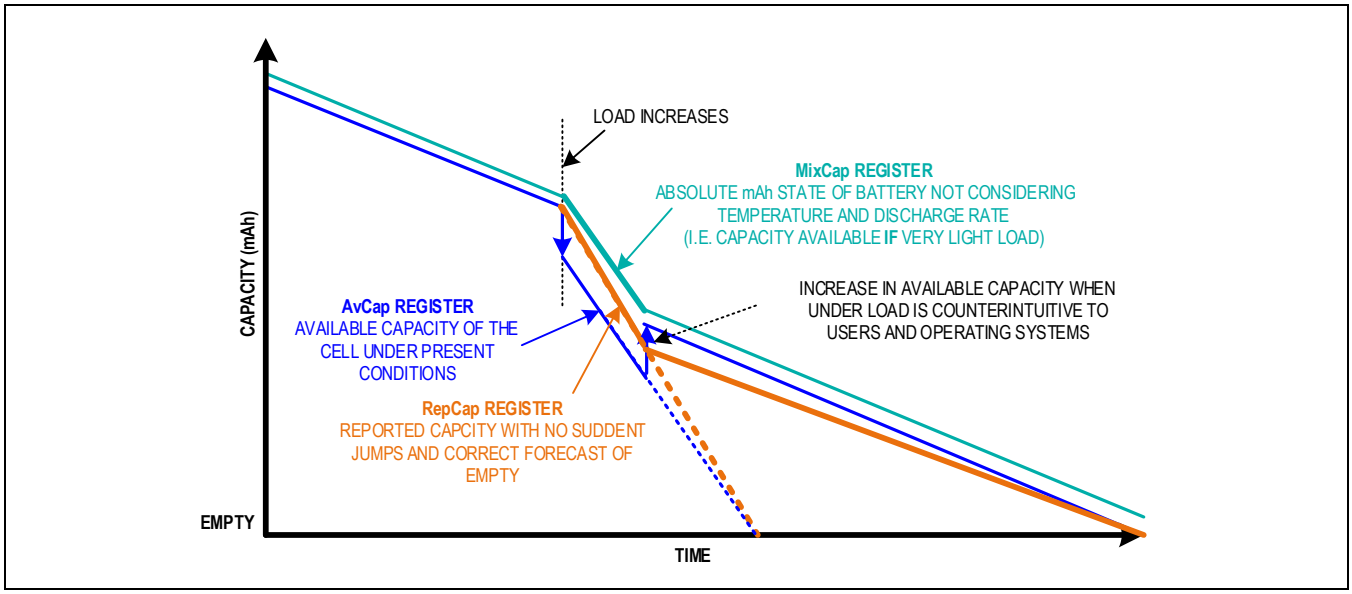


Figure 16. Handling Changes in Empty Calculation

Converge-To-Empty

The MAX77972 includes a feature that guarantees the fuel gauge output smoothly converges to 0% as the cell voltage approaches the empty voltage. As the cell voltage approaches the target empty voltage (AvgVCell approaches VEmpty) the IC smoothly adjusts the rate of change of RepSOC so that the fuel gauge reports 0% at the same time that the cell voltage reaches empty as shown in *Figure 17*. This prevents early or late empty reporting by the fuel gauge, maximizing application run-time.

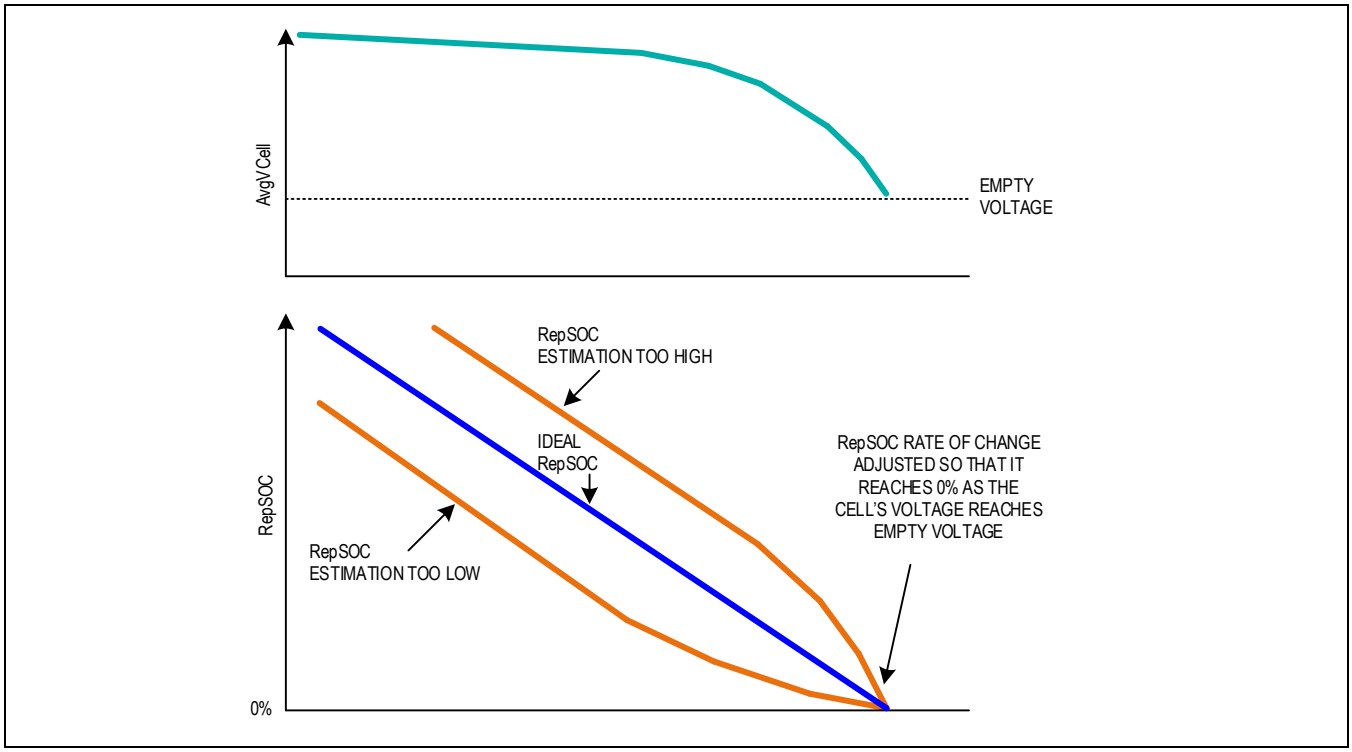


Figure 17. Converge-To-Empty Performance

Determining Fuel-Gauge Accuracy

To determine the true accuracy of a fuel gauge as experienced by end users, the battery should be exercised in a dynamic manner. The end-user accuracy cannot be understood with only simple cycles. To challenge a correction-based fuel gauge such as a coulomb counter, test the battery with partial loading sessions. For example, a typical user can operate the device for ten minutes and then stop use for an hour or more. A robust test method includes these kinds of sessions many times at various loads, temperatures, and durations. Refer to the *Application Note 4799: Cell Characterization Procedure for a ModelGauge m3/ModelGauge m5 Fuel Gauge*.

Initial Accuracy

The IC uses the first voltage reading after power-up or after the cell is connected to the IC to determine the starting output of the fuel gauge. It is assumed that the cell is fully relaxed prior to this reading. However, this is not always the case. If there is a load or charge current present, the initial reading is compensated using the characterized internal impedance of the cell to estimate the cell's relaxed voltage. If the cell was recently charged or discharged, the voltage measured by the IC might not represent the true state-of-charge of the cell, resulting in an initial error in the fuel gauge outputs. In most cases, this error is minor and is quickly removed by the fuel gauge algorithm during the first hour of normal operation.

99% and Empty Hold

The MAX77972 supports two modes that limit the RepSOC% reported until a specific condition is reached.

- **99% Hold**. This feature limits RepSOC not to exceed 99% until a charge termination event is detected. Disable this feature by setting SOCHold.HoldEn99 to 0 (default enabled).

- **Empty Hold**. This feature limits RepSOC to not fall below x% (1% default) until the empty voltage is crossed. This can be useful with operating systems which force system shutdown at a particular battery percentage. A Windows computer, for example, may force the system shutdown or hibernate when the fuel gauge crosses 5%. So setting Empty Hold to 6% can guarantee deeper discharge to a specified voltage level, and thereby often extend runtime. Set desired empty SOC in SOCHold.EmptySOCHold. The MAX77972 holds the SOC until battery voltage drop below Vempty + SOCHold.EmptyVoltHold, as shown in *Figure 18*.

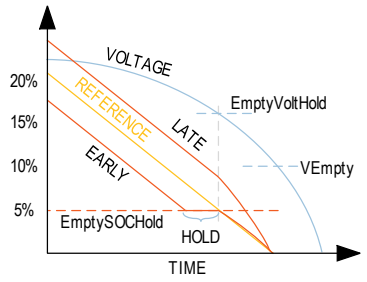


Figure 18. SOC Hold Conceptual Drawing

Cell Relaxation Detection

The nRelaxCfg register defines how the IC detects if the cell is in a relaxed state. See *Figure 19*. For a cell to be considered relaxed, current flow through the cell must be kept at a minimum while the change in the cell's voltage over time (dV/dt) shows little or no change. If AvgCurrent remains below the nRelaxCfg.LOAD threshold while VCell changes less than the nRelax.dV threshold over two consecutive periods of nRelaxCfg.dt, the cell is considered to be relaxed. FStat.RelDt is set after cell relaxation. If the cell remains in this state after 48 to 96 minutes after FStat.RelDt is set, FStat.RelDt2 is set, which indicates the cell is in long relaxation.

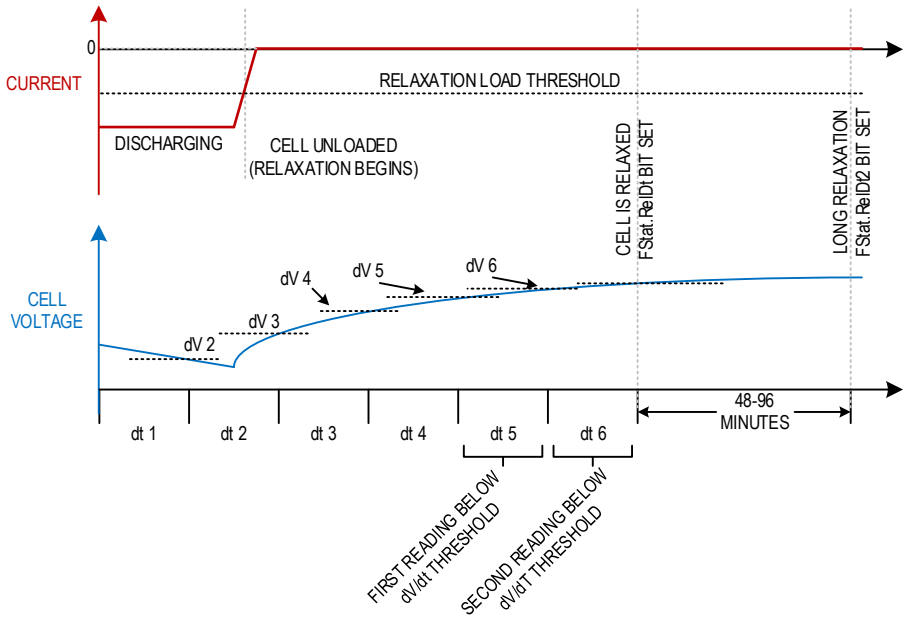


Figure 19. Cell Relaxation Detection

Save and Restore Registers

The device is designed to operate outside the battery pack and can, therefore, be exposed to power loss when in the application. To prevent the loss of learned information during power cycles, a save-and-restore procedure can be used to maintain register values in non-volatile memory external to the device. The registers must be stored externally and then rewritten to the device after power-up to maintain a learned state of operation. Note that some registers are application outputs, some registers are for internal calculations, and some are characterization setup registers. Registers that are not internal are described in their own sections. These values should be stored by the application at periodic intervals. Some recommended backup events are:

- End-of-charge
- End-of-discharge
- Before the application enters the shutdown state

The host is responsible for loading the default characterization data at the device's first power-up and restoring the default characterization data, plus learned information on subsequent power-up events.

Fuel Gauge Operation Modes

The MAX77972 fuel gauge supports two power modes: active mode and hibernate mode. If Hibernate mode is enabled through nHibCfg.EnHib, MAX77972 enters hibernate mode from active mode when the Current register reading falls below the nHibCfg.HibThreshold for longer than HibEnterTime. If the Current register reading goes above the nHibCfg.HibThreshold for longer than the nHibCfg.HibExitTime, the MAX77972 goes from hibernate to active mode. The current consumption is reduced in the hibernate mode due to the extended gauge and ADC being on time. Status2.Hib bit indicates if MAX77972 is in the hibernate mode.

- Active mode: Gauge and ADC update every 176ms.
- Hibernate mode: Gauge and ADC update every 1.4s.

Fuel Gauge Alert (ALRT)

The MAX77972 allows interrupts to be generated by detecting a high or low voltage, current, temperature, or state of charge. Interrupts are generated on the ALRT pin open-drain output driver. An external pullup is required to generate a logic-high signal. Any of the following conditions can trigger alerts:

- **Battery removal:** THM is floating, and battery removal detection enabled (Config.Ber = 1). Status.Br is set to 1 with a battery removal event.
- **Battery insertion:** THM is connected to a thermistor, and battery insertion detection enabled (Config.Bei = 1). Status.Bi is set to 1 with a battery insertion event.
- **Over/undervoltage:** VAlrtTh register threshold violation (upper or lower) and alerts enabled (Config.Aen = 1). Status.Vmn and Status.Vmx are set to 1 for the upper and lower thresholds accordingly.
- **Over/undertemperature:** TAlrtTh register threshold violation (upper or lower) and alerts enabled (Config.Aen = 1). Status.Tmn and Status.Tmx are set to 1 for the upper and lower thresholds accordingly.
- **Over/undercurrent:** IAlrtTh register threshold violation (upper or lower) and alerts enabled (Config.Aen = 1). Status.Imn and Status.Imx are set to 1 for the upper and lower thresholds accordingly.
- **Over/under SOC:** SAlrtTh register threshold violation (upper or lower) and alerts enabled (Config.Aen = 1). Status.Smn and Status.Smx are set to 1 for the upper and lower thresholds accordingly.
- **1% SOC change:** RepSOC register bit d8 (1% bit) changed (Config2.dSOCEn = 1).

To prevent false interrupts, the threshold registers should be initialized before setting the Config.Aen bit. Alerts generated by battery insertion or removal can only be reset by clearing the corresponding bit in the Status register. Alerts generated by a threshold-level violation can be configured to be cleared only by software, or cleared automatically when the threshold level is no longer violated. See the Config and Config2 register descriptions for details of the alert function configuration.

Analog Measurements

The MAX77972 continually monitors the voltage, current and temperature for the fuel gauge and charging functions. The following sections detail how these measurements occur.

Voltage Measurements

The MAX77972 performs battery voltage measurement between the BATTSP and BATTSN pins and input voltage measurement between BYP and GND pins.

- **VCell:** In each update cycle, the reading of the cell voltage measurement is placed in the VCell register.
- **AvgVCell:** The AvgVCell register reports an average of the VCell register readings. The averaging time period is configurable from 12 seconds to 24 minutes. Set FilterCfg.VOLT accordingly for the desired averaging time filter.
- **VByp:** Every 2.8s, the reading of the input voltage measurement is placed in the VByp register.
- **VSys:** Every 2.8s, the reading of the input voltage measurement is placed in the VSys register.

Current Measurements

The MAX77972 performs input current measurement using Q_{CHGIN} FET.

- **ICHGIN:** Every 1.4s, the reading of the input current measurement is placed in the ICHGIN register.

There are two options for battery current measurement: internal current sensing through Q_{BAT} FET and an external sense resistor between CSP and BATTSP/CSN.

- **Internal current sensing:** For MAX77972, when the internal current sensing is selected, the current measurement is done using Q_{BAT} FET. The internal current sense is equivalent to 10mΩ. The measurement range is ±5.12A, and the resolution is 156.25µA.
- **External current sensing:** Set nADCCfg.RsnsEn to 1 to select the external sense resistor. When an external resistor is selected, current flow through the battery is determined by making voltage measurements across the sensing element. The measurement range is ±51.2mV, and the reporting resolution is 1.5625µV. Please note that if the selected sense resistor is not 10mΩ, ADC outputs scale with it, but it does not apply to ChargingCurrent. The resolution mismatch between ChargingCurrent and Current/AvgCurrent may lead to an error entering next charging step. See *Step Charging* section for more details. It is recommended to use 10mΩ external sense resistor to avoid the error. Also, even if the external sense is selected, the battery over-discharge current protection is still measured from Q_{BAT}.

The battery current is reported in the following registers:

- **Current:** In each update cycle, the battery measurement result is stored as a two's complement value in the Current register. Measurement results outside the minimum and maximum register values are reported as the minimum or maximum value.
- **AvgCurrent:** The AvgCurrent register reports an average of Current register readings over a configurable 0.7-second to 6.4-hour time period. Set FilterCfg.CURR to select the desired time filter. The first Current register reading after returning to active mode sets the starting point of the AvgCurrent filter.

The current measurement A/D is factory-trimmed to datasheet accuracy without the need for the user to make further adjustments. The recommended default applies no gain or offset adjustments to the Current register reading. For specific application requirements where adjustment is needed, the gain and offset of battery current measurement can be adjusted through the nCGain register.

Temperature Measurements

The MAX77972 can measure and report its own internal temperature or report an external temperature by using an NTC Thermistor divider network connected to the THM pin. The temperature can be from 3 sources:

- Thermistor connected to THM pin (default). The temp register reported value is converted from voltage measurement through the THM pin. Toggle the ADCCFG2.R100 bit to select between 10kΩ and 100kΩ thermistors.
- Die temperature sensor. Set nADCCFG.ThEn = 0 to enable die temperature measurement. The temperature register reported value is from the on-chip temperature sensor.
- External overwrite. Set Config.Tex = 1 to disable thermistor/internal temperature detection. The MAX77972 stops updating the Temp register. The temp register is overwritten through I^2C.

External NTC thermistors generate a temperature-related voltage measured at the THM pin. Set the nThermCfg register to compensate the thermistor for an accurate temperature translation. *Table 9* lists common NTC thermistors with their associated Beta value and the nThermCfg value. The thermistors in the table translate within ±1°C from -40°C to +85°C. For other thermistors, use the equation in *Table 9* to translate within ±2.5°C.

Table 9. Register Settings for Common Thermistor Types

THERMISTOR	R_{25C}(kΩ)	BETA at 25°C to 85°C	nThermCfg
Murata NCP15XH103F03RC	10	3435	71DEh
Semitec 103AT-2	10	3435	91C3h
TDK B57560G1103 7003	10	3610	5183h
Murata NCU15WF104F6SRC	100	4250	48EBh
NTC TH11-4H104F	100	4510	08D9h
TDK NTCG064EF104FTBX	100	4225	58EFh
Other 10K	10	nThermCfg = 7000h + (3245919/Beta* - 512)	
Other 100K	100	nThermCfg = 3000h + (3245919/Beta* - 512)	

**Use Beta 25°C to 85°C.*

Temperature is reported in the following registers:

- **Temp:** Every 1.4s, the temperature measurement result used for the fuel gauge algorithm is stored in the Temp register. The Temp register reflects the thermistor, die temperature or external overwrite as configured in the nADCCfg or Config register.
- **AvgTA:** The AvgTA register reports an average of the readings from the Temp register. The averaging period is configurable from 6 minutes to 12 hours, as set by the FilterCfg.TEMP. The first Temp register reading after returning to active mode sets the starting point of the averaging filters.
- **DieTemp:** In each update cycle, the internal die temperature measurement result is stored in the DieTemp register.

Power

The MAX77972 reports battery power in the following registers:

- **Power:** Instant power calculated from Current and VCell.
- **AvgPower:** Average power calculated from AvgCurrent and AvgVCell.

Standard Register Formats

Unless otherwise stated in register map, all fuel gauge registers follow the same format depending on the type of register. See *Table 10* for the resolution and range of any register. Note that current and capacity values are based on 10mΩ.

Table 10. ModelGauge m5 Register Standard Resolutions

REGISTER TYPE	LSb SIZE	MINIMUM VALUE	MAXIMUM VALUE	NOTES
Capacity	0.5mAh	0.0µVh	32767.5mAh	—
Percentage	1/256%	0.0%	255.9961%	1% LSb when reading only the upper byte.
Voltage	78.125µV	0.0V	5.11992V	—
Current	0.15625mA	-5.12A	5.12A	Signed 2's complement format.
Temperature	1/256°C	-128.0°C	127.996°C	Signed 2's complement format. 1°C LSb when reading only the upper byte.
Resistance	1/4096Ω	0.0Ω	15.99976Ω	—
Time	5.625s	0.0s	102.3984h	—

Reset Modes

Factory Ship Mode

All hardware including charger, gauge. ADC and etc. are in the shutdown state when MAX77972 enters ship mode. The only activity alive relates to analog circuits that monitor for wakeup conditions. All registers reset to default after exit.

There are two ways to enter ship mode:

- Through I2C. Write FSHIP_MODE to 1 through I2C. MAX77972 enters ship mode after up to 176ms.
- Pushbutton through DATAMUX pin. If Config.DATAMUX = 1 (default), hold DATAMUX pin low for 12s.

There are two ways to exit ship mode:

- CHGIN valid voltage
- Hold DATAMUX pin low for 1s. The MAX77972 prevents accidental wakeup when the system is boxed and shipped. When awoken from DATAMUX, it debounces 1s to ensure the wakeup is valid. If no valid wakeup is discovered, the device remains in ship mode.

Deep Ship Mode

All hardware including charger, gauge. ADC and etc. are in the shutdown state when MAX77972 enters deep ship mode. The only activity alive relates to analog circuits that monitors for wakeup conditions. All registers reset to default after exit. Compared to ship mode, deep ship mode has less active circuits and even lower power consumption.

To enter deep ship mode:

- Through I2C. Write nChgConfig5.DeepShip to 1 through I2C. MAX77972 enters ship mode after up to 176ms.

To exit deep ship mode:

- CHGIN valid voltage

Soft Reset

Soft reset restores the MAX77972 to its power-up state, the same as if the power had been cycled. This is useful for testing different configurations without writing to nonvolatile memory. Use the following sequences to reset the IC.

- Reset IC hardware by writing 000Fh to the Command register.
- Wait 30ms.
- Follow software implementation guide to initialize MAX77972.

Pushbutton SYS Hard Reset

When nChgConfig5.DATAMUX is set to 0 (default), pushbutton SYS reset feature is enabled on DATAMUX pin. Hold DATAMUX pin low for 6s to cycle the power on SYS pin for 150ms.

I²C Serial Communication

General Description

The IC features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). This device relies on the controller to generate a clock signal. SCL clock rates from 0Hz to 400kHz are supported.

I²C is an open-drain bus and therefore SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

Figure 20 shows the functional diagram for the I²C based communications controller. For additional information on I²C, see the I²C Bus Specification and User Manual which is available for free through the internet.

Features

- I²C Revision 3.0 compatible serial communications channel
- Compatible with any bus timing up to 400kHz
- Does not utilize I²C clock stretching

I²C Simplified Block Diagram

There are three pins (aside from GND) for the I²C-compatible interface. V_{IO} determines the logic level, SCL is the clock line, and SDA is the data line. Note that the interface cannot drive the SCL line.

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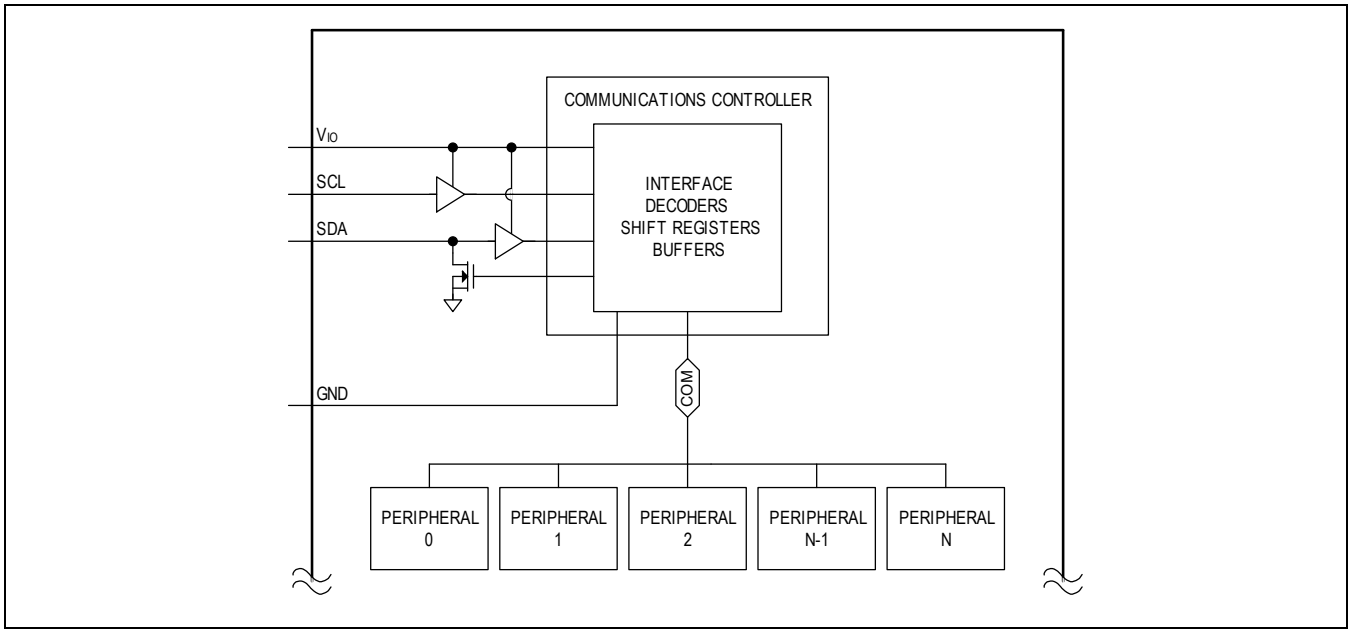


Figure 20. I²C Simplified Block Diagram

I²C System Configuration

The I²C-compatible interface is a multi-controller bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I²C bus that sends data to the bus is called a transmitter, and a device that receives data from the bus is called a receiver. A controller is the device that initiates a data transfer and generates the SCL clock signals to control the data transfer. The I²C-compatible interface operates as a target on the I²C bus with transmit and receive capabilities.

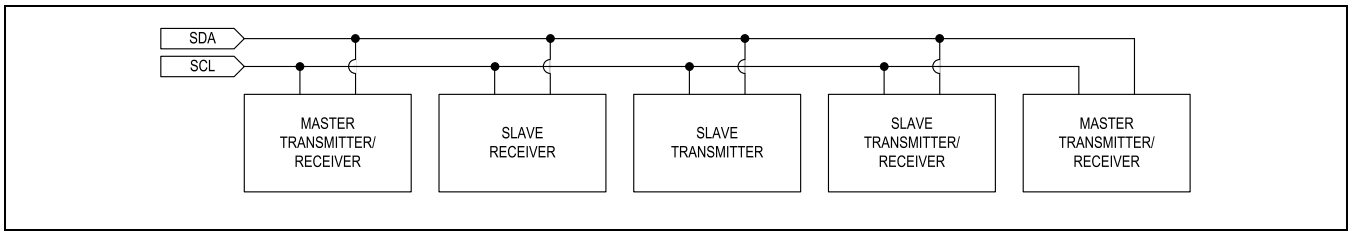


Figure 21. I²C System Configuration

I²C Interface Power

The I²C interface derives its power from V_{IO}. Typically, a power input such as V_{IO} would require a local 0.1µF ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between V_{IO} and the next closest capacitor (≥ 0.1µF) is less than 100mΩ in series with 10nH, then a local capacitor is not needed. Otherwise, bypass V_{IO} to GND with a 0.1µF ceramic capacitor.

V_{IO} accepts voltages from 1.7V to 3.6V (V_{IO}). Cycling V_{IO} does not reset the I²C registers. When V_{IO} is less than V_{IOUVLO} and V_{SYSA} is less than $V_{SYSAUVLO}$, SDA and SCL are high impedance.

I²C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA, while SCL is high, are control signals. See the *I²C Start and Stop Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I²C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A controller device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See *Figure 22*.

A START condition from the controller signals the beginning of a transmission to the device. The controller terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the *I²C Acknowledge Bit* section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the device, the controller can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

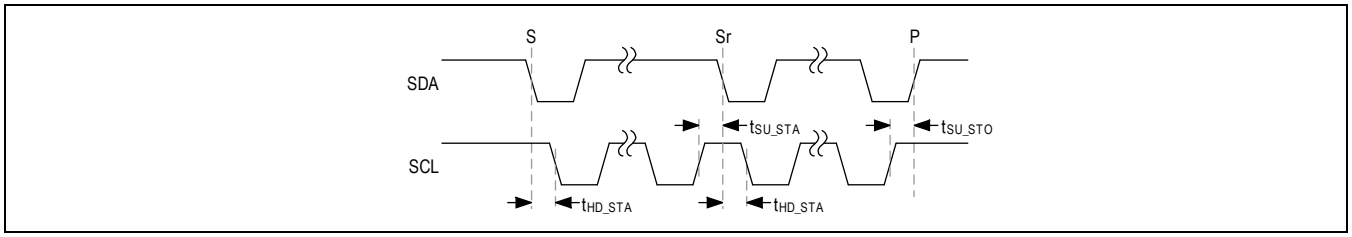


Figure 22. I²C Start and Stop Conditions

I²C Acknowledge Bit

Both the I²C bus controller and devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each ninth-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See *Figure 23*. To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller should reattempt communication at a later time.

This device issues an ACK for all register addresses in the possible address space, even if the particular register does not exist.

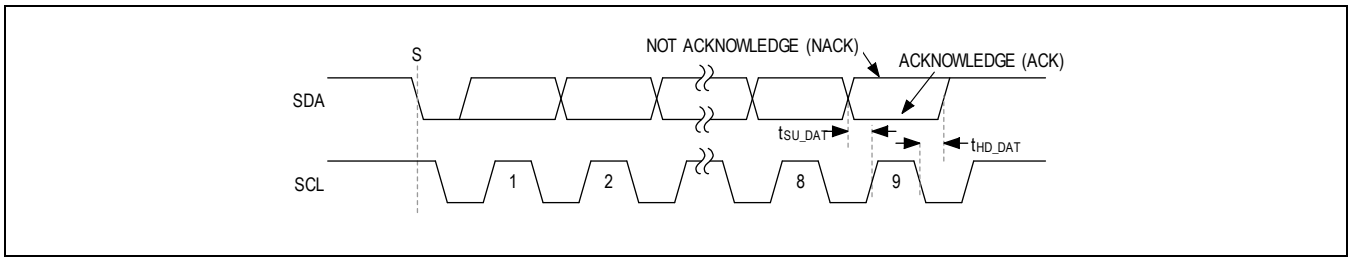


Figure 23. Acknowledge Bit

I²C Device Address

The I²C controller implements 7-bit device addressing. When the bus is idle, the IC continuously monitors for a START condition followed by its device address. When the IC receives a device address that matches its Device Address, it responds with an Acknowledge bit during the clock period following the R/W bit. The supports of the device addresses are shown in *Table 11*.

Note: The addresses shown in *Table 11* are 7-bit device addresses.

Table 11. 2-Wire Addresses

DEVICE ADDRESS (7-BIT)	PROTOCOL	ADDRESS BYTE RANGE	INTERNAL MEMORY RANGE ACCESSED
0x36	I²C	0x00h - 0xFFh	000h - 0FFh
0x37	I²C	0x80h - 0xFFh	180h - 1FFh

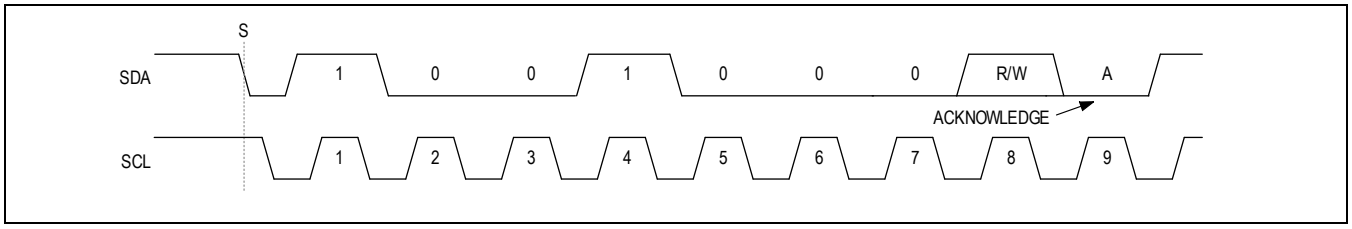


Figure 24. Device Address Example

I²C Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows slow devices to alter the clock signal by holding down the clock line. The process in which a device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

This device does not implement the I²C specifications general call address and does not acknowledge the general call address (0b0000_0000).

I²C Device ID

This device does not support the I²C Device ID feature.

I²C Communication Speed

This device is compatible with any bus timing up to 400kHz. The main consideration when changing bus speed through this range is the combination of the bus capacitance and pullup resistors. Larger values of bus capacitance and pullup resistance increase the time constant (C x R), slowing bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. See the *Pullup Resistor Sizing* section of the I²C Bus Specification and User Manual (available for free on the Internet) for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, and a 400kHz bus needs about 1.5kΩ pullup resistors. Remember that, while the open-drain bus is low, the pullup resistor is dissipating power, and lower-value pullup resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, see the publicly available I²C Bus Specification and User Manual. Major considerations concerning this part are:

- The I²C bus controller uses current source pullups to shorten the signal rise.
- The I²C peripheral must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed controller code.

At power-up and after each stop condition, the bus input filters are set for standard mode, fast mode, and fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed controller code protocols that are described in the *I²C Communication Protocols* section.

I²C Communication Protocols

Both writing to and reading from registers are supported as described in the following subsections.

Writing to a Single 8-bit Register

Figure 25 shows the protocol for the I²C controller device to write one byte of data to this device. This protocol is the same as the SMBus specification's write-byte protocol.

The write byte protocol is as follows:

- The controller sends a start command (S).
- The controller sends the 7-bit device address followed by a write bit ($R/\overline{W} = 0$).
- The addressed device asserts an acknowledge (A) by pulling SDA low.
- The controller sends an 8-bit register pointer.
- The device acknowledges the register pointer.
- The controller sends a data byte.
- The device updates with the new data.
- The device acknowledges or does not acknowledge the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
- The controller sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

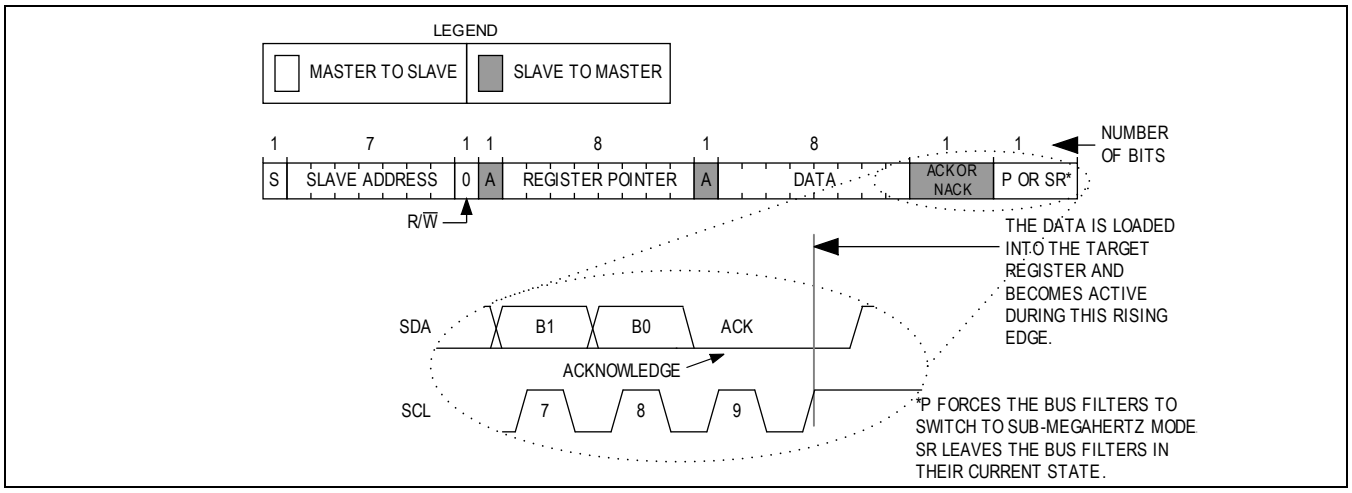


Figure 25. Writing to a Single 8-bit Register with the Write Byte Protocol

Writing Multiple Bytes to Sequential Registers

Figure 26 shows the protocol for writing to sequential registers. This protocol is similar to the write-byte protocol above, except the controller continues to write after it receives the first byte of data. When the controller is done writing, it issues a stop or repeated start.

The writing to sequential registers protocol is as follows:

- The controller sends a start command (S).
- The controller sends the 7-bit device address followed by a write bit ($R/\overline{W}$ = 0).
- The addressed device asserts an acknowledge (A) by pulling SDA low.
- The controller sends an 8-bit register pointer.
- The device acknowledges the register pointer.
- The controller sends a data byte.
- The device acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register, and the data becomes active.
- Steps 6 to 7 are repeated as many times as the controller requires.
- During the last acknowledge-related clock pulse, the controller can issue an acknowledge or a not acknowledge.
- The controller sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

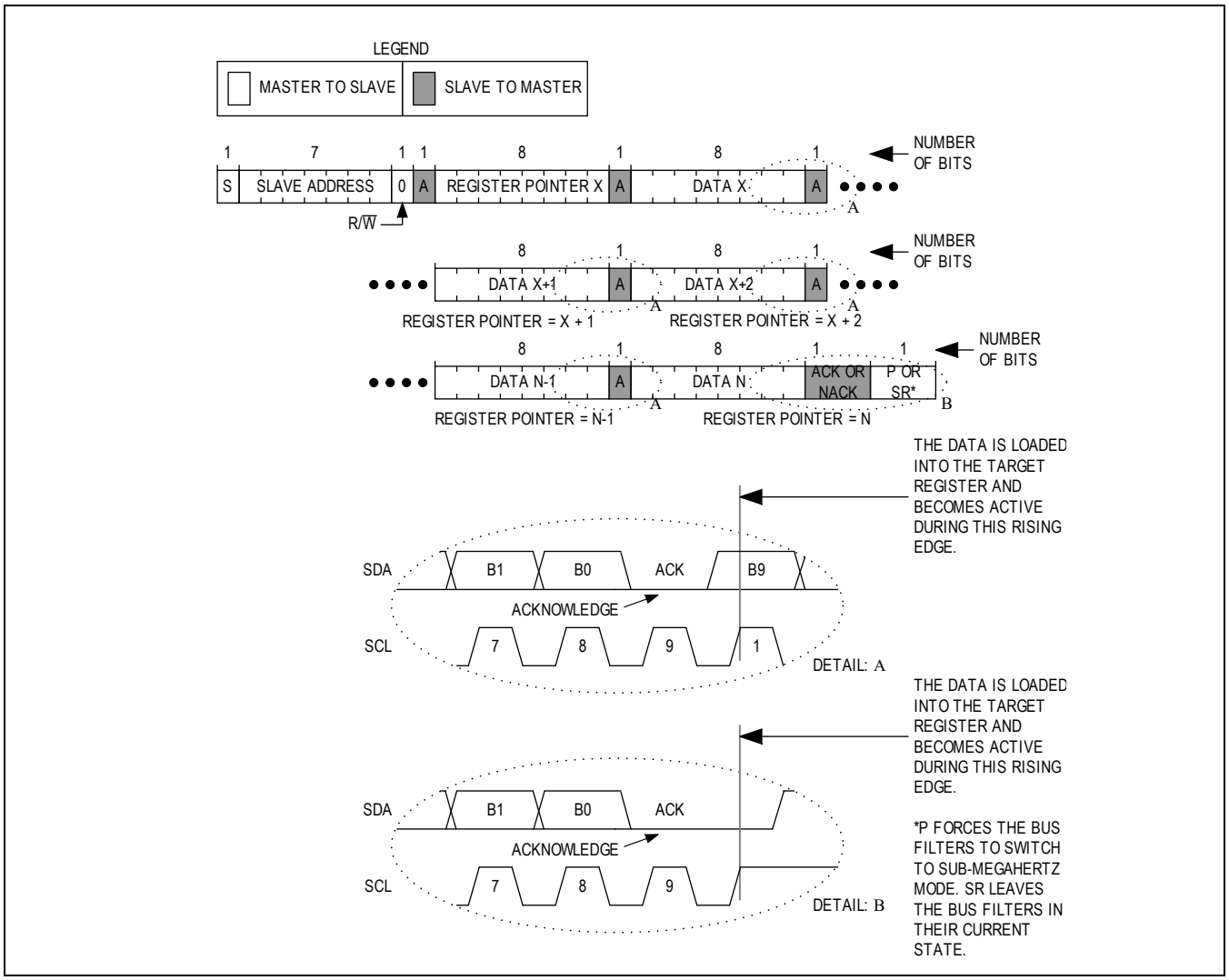


Figure 26. Writing to Sequential Registers X to N

Writing to 16-bit Registers

The Write Data protocol is used to transmit data to the registers of the fuel gauge at memory addresses from 00h to FFh. Addresses 00h to FFh can be written as a block. The memory address is sent by the bus controller as a single-byte value immediately after the device address. The LSB of the data to be stored is written immediately after the memory address byte is acknowledged. Because the address is automatically incremented after the last bit of each 16-bit word received by the IC, the LSB of the data at the next memory address can be written immediately after the acknowledgment of the MSB of data at the previous address. The controller indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit. If the bus controller continues an auto-incremented write transaction beyond address FFh, the IC ignores the data. Data is also ignored on writes to read-only addresses but not reserved addresses. Do not write to reserved address locations. See *Figure 27* for an example of the Write Data communication sequence.

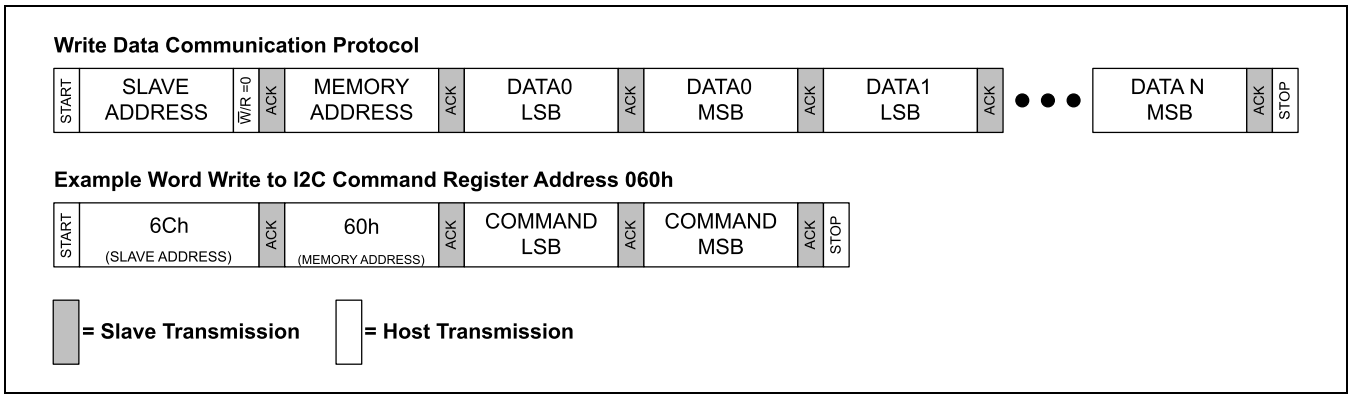


Figure 27. Example I²C Write 16-bit Data Communication Sequence

Reading from a Single Register

Figure 28 shows the protocol for the I²C master device to read one byte of data. This protocol is the same as the SMBus specification's read-byte protocol.

The read byte protocol is as follows:

- The master sends a start command (S).
- The master sends the 7-bit device address followed by a write bit (R/$\overline{W}$ = 0).
- The addressed device asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The device acknowledges the register pointer.
- The master sends a repeated start command (Sr).
- The master sends the 7-bit device address followed by a read bit (R/$\overline{W}$ = 1).
- The addressed device asserts an acknowledge by pulling SDA low.
- The addressed device places 8-bits of data on the bus from the location specified by the register pointer.
- The master issues a not acknowledge (nA).
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, the register pointer is not modified. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

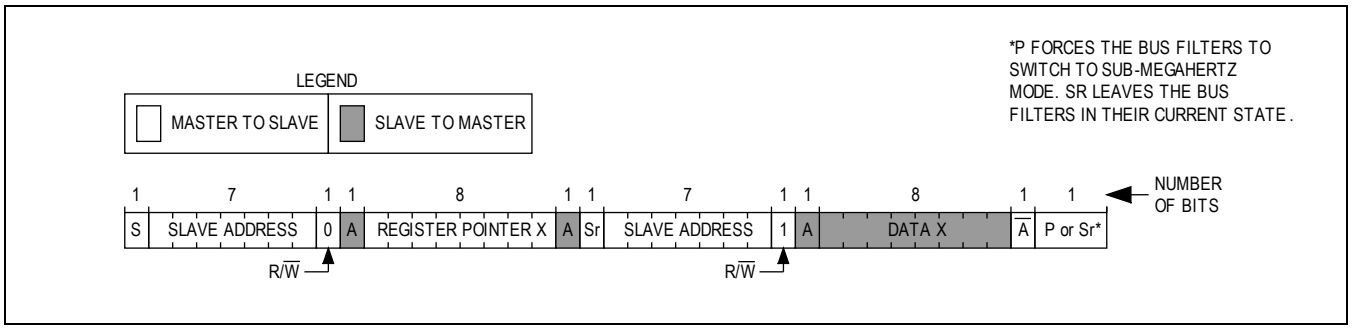


Figure 28. Reading from a Single Register with the Read Byte Protocol

Reading from Sequential Registers

Figure 29 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the controller issues an acknowledge to signal the device that it wants more data: when the controller has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

- The controller sends a start command (S).
- The controller sends the 7-bit device address followed by a write bit (R/$\overline{W}$ = 0).
- The addressed device asserts an acknowledge (A) by pulling SDA low.
- The controller sends an 8-bit register pointer.
- The device acknowledges the register pointer.
- The controller sends a repeated start command (Sr).
- The controller sends the 7-bit device address followed by a read bit (R/$\overline{W}$ = 1).
- The addressed device asserts an acknowledge by pulling SDA low.
- The addressed device places 8-bits of data on the bus from the location specified by the register pointer.
- The controller issues an acknowledge (A) signaling the device that it wishes to receive more data.
- Steps 9 to 10 are repeated as many times as the controller requires. Following the last byte of data, the controller must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
- The controller sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop it does not modify its register pointer. Therefore, if the controller re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

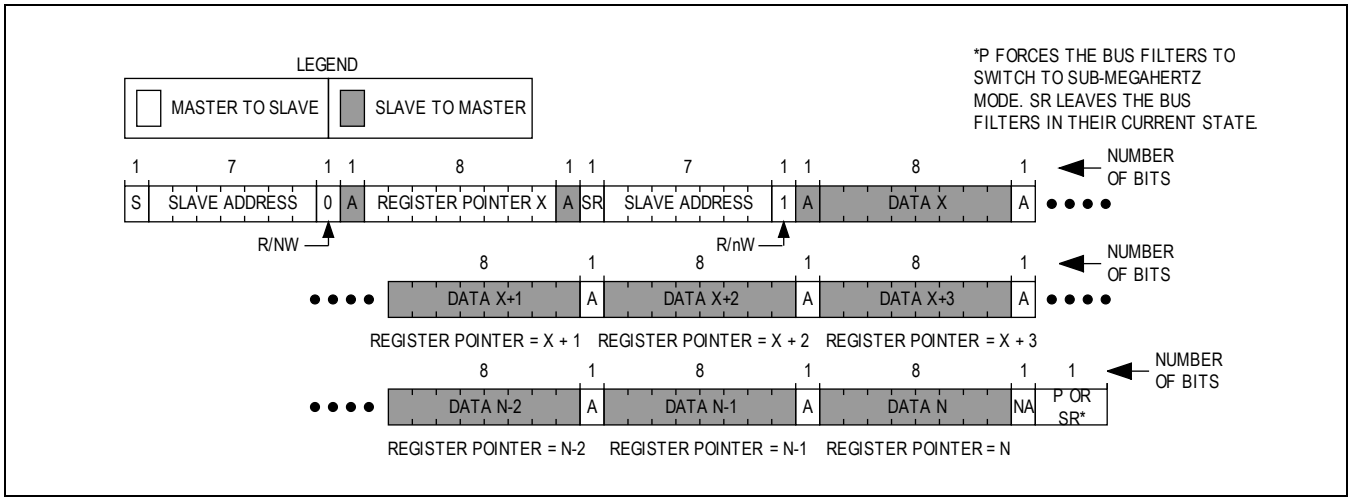


Figure 29. Reading Continuously from Sequential Registers X to N

Register Map

FG_FUNC_MAP

Device address (8-bit): 0x6C
Device address (7-bit): 0x36

ADDRESS	NAME	MSB							LSB
FG_RAM									
0x00	Status[15:8]	Br	Smx	Tmx	Vmx	Bi	Smn	Tmn	Vmn
	Status[7:0]	dSOCi	Imx	–	–	Bst	Imn	POR	–
0x01	ChgMaskSts[15:8]	AICL_M	CHGIN_M	–	CHG_M	BAT_M	Reserved	–	BYP_M
	ChgMaskSts[7:0]	AICL_I	CHGIN_I	–	CHG_I	BAT_I	Reserved	–	BYP_I
0x03	VAlrtTh[15:8]	VMAX[7:0]							
	VAlrtTh[7:0]	VMIN[7:0]							
0x04	TAlrtTh[15:8]	TMAX[7:0]							
	TAlrtTh[7:0]	TMIN[7:0]							
0x05	SAlrtTh[15:8]	SMAX[7:0]							
	SAlrtTh[7:0]	SMIN[7:0]							
0x06	RepCap[15:8]	RepCap[15:8]							
	RepCap[7:0]	RepCap[7:0]							
0x07	RepSOC[15:8]	RepSOC[15:8]							
	RepSOC[7:0]	RepSOC[7:0]							
0x08	IDVolt[15:8]	IDVolt[15:8]							
	IDVolt[7:0]	IDVolt[7:0]							
0x09	MaxMinTemp[15:8]	MaxTemperature[7:0]							
	MaxMinTemp[7:0]	MinTemperature[7:0]							
0x0A	MaxMinCurr[15:8]	MaxCurrent[7:0]							
	MaxMinCurr[7:0]	MinCurrent[7:0]							
0x0B	MaxMinVolt[15:8]	MaxVCELL[7:0]							
	MaxMinVolt[7:0]	MinVCELL[7:0]							

ADDRESS	NAME	MSB							LSB
0x0C	Config[15:8]	–	SS	TS	VS	IS	–	–	Tex
	Config[7:0]	PinConfig	–	–	–	FTHRM	Aen	Bei	Ber
0x0D	MixSOC[15:8]	MixSOC[15:8]							
	MixSOC[7:0]	MixSOC[7:0]							
0x0E	AvSOC[15:8]	AvSOC[15:8]							
	AvSOC[7:0]	AvSOC[7:0]							
0x0F	MiscCfg[15:8]	FUS[3:0]				Reserved	Reserved	MixRate[4:3]	
	MiscCfg[7:0]	MixRate[2:0]			Reserved	–	–	SACFG[1:0]	
0x10	FullCapRep[15:8]	FullCapRep[15:8]							
	FullCapRep[7:0]	FullCapRep[7:0]							
0x12	QRTable00[15:8]	QRTable00[15:8]							
	QRTable00[7:0]	QRTable00[7:0]							
0x14	RSlow[15:8]	RSlow[15:8]							
	RSlow[7:0]	RSlow[7:0]							
0x16	Age[15:8]	Age[15:8]							
	Age[7:0]	Age[7:0]							
0x17	Cycles[15:8]	Cycles[15:8]							
	Cycles[7:0]	Cycles[7:0]							
0x18	DesignCap[15:8]	DesignCap[15:8]							
	DesignCap[7:0]	DesignCap[7:0]							
0x19	AvgVCell[15:8]	AvgVCell[15:8]							
	AvgVCell[7:0]	AvgVCell[7:0]							
0x1A	VCell[15:8]	VCell[15:8]							
	VCell[7:0]	VCell[7:0]							
0x1B	Temp[15:8]	Temp[15:8]							
	Temp[7:0]	Temp[7:0]							

ADDRESS	NAME	MSB							LSB
0x1C	Current[15:8]	Current[15:8]							
	Current[7:0]	Current[7:0]							
0x1D	AvgCurrent[15:8]	AvgCurrent[15:8]							
	AvgCurrent[7:0]	AvgCurrent[7:0]							
0x1F	VEmpty[15:8]	VE[8:1]							
	VEmpty[7:0]	VE[0]	VR[6:0]						
0x21	DevName[15:8]	DevName[15:8]							
	DevName[7:0]	DevName[7:0]							
0x22	QRTable10[15:8]	QRTable00[15:8]							
	QRTable10[7:0]	QRTable00[7:0]							
0x23	FullCapNom[15:8]	FullCapNom[15:8]							
	FullCapNom[7:0]	FullCapNom[7:0]							
0x24	FullCap[15:8]	FullCap[15:8]							
	FullCap[7:0]	FullCap[7:0]							
0x25	VFRemCap[15:8]	VFRemCap[15:8]							
	VFRemCap[7:0]	VFRemCap[7:0]							
0x26	MixCap[15:8]	MixCap[15:8]							
	MixCap[7:0]	MixCap[7:0]							
0x27	AvCap[15:8]	AvCap[15:8]							
	AvCap[7:0]	AvCap[7:0]							
0x28	ChargingCurrent[15:8]	ChargingCurrent[15:8]							
	ChargingCurrent[7:0]	ChargingCurrent[7:0]							
0x29	IChgTerm[15:8]	IChgTerm[15:8]							
	IChgTerm[7:0]	IChgTerm[7:0]							

ADDRESS	NAME	MSB							LSB
0x2A	ChargingVoltage[15:8]	ChargingVoltage[15:8]							
	ChargingVoltage[7:0]	ChargingVoltage[7:0]							
0x2E	QResidual[15:8]	QResidual[15:8]							
	QResidual[7:0]	QResidual[7:0]							
0x2F	LearnCfg[15:8]	FiltEmpty	Reserved[1:0]		Reserved[2:0]			Reserved[1:0]	
	LearnCfg[7:0]	Reserved	LearnStage[2:0]			Reserved[1:0]		MixEn	Reserved
0x32	QRTable20[15:8]	QRTable20[15:8]							
	QRTable20[7:0]	QRTable20[7:0]							
0x34	DieTemp[15:8]	DieTemp[15:8]							
	DieTemp[7:0]	DieTemp[7:0]							
0x35	AvgTA[15:8]	AvgTA[15:8]							
	AvgTA[7:0]	AvgTA[7:0]							
0x39	SOCHold[15:8]	–	–	–	HoldEn99	EmptyVoltHold[6:3]			
	SOCHold[7:0]	EmptyVoltHold[2:0]			EmptySOCHold[4:0]				
0x3A	ProtStatus[15:8]	–	TooHotC	Full	TooColdC	–	–	–	–
	ProtStatus[7:0]	–	–	–	–	–	–	–	–
0x3C	FStat2[15:8]	Reserved	–	Reserved	FDet	OCV_OutLimits	Reserved	Reserved	Reserved
	FStat2[7:0]	–	–	–	–	–	Reserved[1:0]		Reserved
0x3D	FStat[15:8]	–	Reserved	–	–	–	Reserved	RelDt	EDet
	FStat[7:0]	FQ	RelDt2	Reserved	–	Reserved	–	Reserved	DNR
0x3E	FProtStat[15:8]	–	–	–	–	–	–	StepID[2:1]	
	FProtStat[7:0]	StepID[0]	–	IsDis	–	–	Tempid[2:0]		
0x3F	Timer[15:8]	Timer[15:8]							
	Timer[7:0]	Timer[7:0]							

ADDRESS	NAME	MSB							LSB
0x42	QRTable30[15:8]	QRTable30[15:8]							
	QRTable30[7:0]	QRTable30[7:0]							
0x45	dQAcc[15:8]	dQAcc[15:8]							
	dQAcc[7:0]	dQAcc[7:0]							
0x46	dPAcc[15:8]	dPAcc[15:8]							
	dPAcc[7:0]	dPAcc[7:0]							
0x4D	QH[15:8]	QH[15:8]							
	QH[7:0]	QH[7:0]							
0x51	ICHGIN[15:8]	ICHGIN[15:8]							
	ICHGIN[7:0]	ICHGIN[7:0]							
0x52	VSys[15:8]	VSys[15:8]							
	VSys[7:0]	VSys[7:0]							
0x80	OCVTable0[15:8]	OCVTable0[15:8]							
	OCVTable0[7:0]	OCVTable0[7:0]							
0x81	OCVTable1[15:8]	OCVTable1[15:8]							
	OCVTable1[7:0]	OCVTable1[7:0]							
0x82	OCVTable2[15:8]	OCVTable2[15:8]							
	OCVTable2[7:0]	OCVTable2[7:0]							
0x83	OCVTable3[15:8]	OCVTable3[15:8]							
	OCVTable3[7:0]	OCVTable3[7:0]							
0x84	OCVTable4[15:8]	OCVTable4[15:8]							
	OCVTable4[7:0]	OCVTable4[7:0]							
0x85	OCVTable5[15:8]	OCVTable5[15:8]							
	OCVTable5[7:0]	OCVTable5[7:0]							
0x86	OCVTable6[15:8]	OCVTable6[15:8]							
	OCVTable6[7:0]	OCVTable6[7:0]							

ADDRESS	NAME	MSB							LSB
0x87	OCVTable7[15:8]	OCVTable7[15:8]							
	OCVTable7[7:0]	OCVTable7[7:0]							
0x88	OCVTable8[15:8]	OCVTable8[15:8]							
	OCVTable8[7:0]	OCVTable8[7:0]							
0x89	OCVTable9[15:8]	OCVTable9[15:8]							
	OCVTable9[7:0]	OCVTable9[7:0]							
0x8A	OCVTable10[15:8]	OCVTable10[15:8]							
	OCVTable10[7:0]	OCVTable10[7:0]							
0x8B	OCVTable11[15:8]	OCVTable11[15:8]							
	OCVTable11[7:0]	OCVTable11[7:0]							
0x8C	OCVTable12[15:8]	OCVTable12[15:8]							
	OCVTable12[7:0]	OCVTable12[7:0]							
0x8D	OCVTable13[15:8]	OCVTable13[15:8]							
	OCVTable13[7:0]	OCVTable13[7:0]							
0x8E	OCVTable14[15:8]	OCVTable14[15:8]							
	OCVTable14[7:0]	OCVTable14[7:0]							
0x8F	OCVTable15[15:8]	OCVTable15[15:8]							
	OCVTable15[7:0]	OCVTable15[7:0]							
0x90	XTable0[15:8]	XTable0[15:8]							
	XTable0[7:0]	XTable0[7:0]							
0x91	XTable1[15:8]	XTable1[15:8]							
	XTable1[7:0]	XTable1[7:0]							
0x92	XTable2[15:8]	XTable2[15:8]							
	XTable2[7:0]	XTable2[7:0]							
0x93	XTable3[15:8]	XTable3[15:8]							
	XTable3[7:0]	XTable3[7:0]							

ADDRESS	NAME	MSB							LSB
0x94	XTable4[15:8]	XTable4[15:8]							
	XTable4[7:0]	XTable4[7:0]							
0x95	XTable5[15:8]	XTable5[15:8]							
	XTable5[7:0]	XTable5[7:0]							
0x96	XTable6[15:8]	XTable6[15:8]							
	XTable6[7:0]	XTable6[7:0]							
0x97	XTable7[15:8]	XTable7[15:8]							
	XTable7[7:0]	XTable7[7:0]							
0x98	XTable8[15:8]	XTable8[15:8]							
	XTable8[7:0]	XTable8[7:0]							
0x99	XTable9[15:8]	XTable9[15:8]							
	XTable9[7:0]	XTable9[7:0]							
0x9A	XTable10[15:8]	XTable10[15:8]							
	XTable10[7:0]	XTable10[7:0]							
0x9B	XTable11[15:8]	XTable11[15:8]							
	XTable11[7:0]	XTable11[7:0]							
0x9C	XTable12[15:8]	XTable12[15:8]							
	XTable12[7:0]	XTable12[7:0]							
0x9D	XTable13[15:8]	XTable13[15:8]							
	XTable13[7:0]	XTable13[7:0]							
0x9E	XTable14[15:8]	XTable14[15:8]							
	XTable14[7:0]	XTable14[7:0]							
0x9F	XTable15[15:8]	XTable15[15:8]							
	XTable15[7:0]	XTable15[7:0]							
0xA3	ModelCfg[15:8]	Refresh	–	–	–	–	VChg	–	Reserved
	ModelCfg[7:0]	ModelID[3:0]				–	–	–	–

ADDRESS	NAME	MSB							LSB
0xA4	MaxPeakPower[15:8]	MaxPeakPower[15:8]							
	MaxPeakPower[7:0]	MaxPeakPower[7:0]							
0xA5	SusPeakPower[15:8]	SusPeakPower[15:8]							
	SusPeakPower[7:0]	SusPeakPower[7:0]							
0xA6	PackResistance[15:8]	PackResistance[15:8]							
	PackResistance[7:0]	PackResistance[7:0]							
0xA7	SysResistance[15:8]	SysResistance[15:8]							
	SysResistance[7:0]	SysResistance[7:0]							
0xA8	MinSysVoltage[15:8]	MinSysVoltage[15:8]							
	MinSysVoltage[7:0]	MinSysVoltage[7:0]							
0xA9	MPPCurrent[15:8]	MPPCurrent[15:8]							
	MPPCurrent[7:0]	MPPCurrent[7:0]							
0xAA	SPPCurrent[15:8]	SPPCurrent[15:8]							
	SPPCurrent[7:0]	SPPCurrent[7:0]							
0xAB	Config2[15:8]	LDMdl	–	–	DPEn	–	–	–	–
	Config2[7:0]	dSOCEn	TAlrtEn	–	–	Reserved[1:0]		–	–
0xAC	IAlrtTh[15:8]	IMAX[7:0]							
	IAlrtTh[7:0]	IMIN[7:0]							
0xB0	Status2[15:8]	–	–	–	DPReady	–	–	–	–
	Status2[7:0]	–	–	–	–	–	–	Hib	Reserved
0xB1	Power[15:8]	Power[15:8]							
	Power[7:0]	Power[7:0]							
0xB3	AvgPower[15:8]	AvgPower[15:8]							

ADDRESS	NAME	MSB							LSB
	AvgPower[7:0]	AvgPower[7:0]							
0xB8	CGTempCo[15:8]	Reserved[15:8]							
	CGTempCo[7:0]	Reserved[7:0]							
0xBB	FOTPStat[15:8]	PatchID[3:0]				–	–	–	PinDraft
	FOTPStat[7:0]	Reserved	–	–	–	–	–	–	–
0xBE	TimerH[15:8]	TimerH[15:8]							
	TimerH[7:0]	TimerH[7:0]							
0xCC	PinID[15:8]	iid[7:0]							
	PinID[7:0]	vid[7:0]							
0xD0	nChgConfig0[15:8]	PQEN	LSEL	Reserved[1:0]		RECYCLE_EN	FCHGTIME[2:0]		
	nChgConfig0[7:0]	–	DISIBS	–	WDTEN	MODE[3:0]			
0xD1	nChgConfig1[15:8]	–	MINVSYS[2:0]			B2SOVRC[3:0]			
	nChgConfig1[7:0]	OTG_ILIM[1:0]		–	–	–	–	–	–
0xD2	nChgConfig2[15:8]	WD_QBATOFF	REGTEMP[3:0]				FSW[1:0]		FSHIP_MODE
	nChgConfig2[7:0]	B2SOVRC_DTC	SLOWLX[1:0]		DIS_AICL	–	–	WDTCLR[1:0]	
0xD3	nChgConfig3[15:8]	–	VBYPSET[6:0]						
	nChgConfig3[7:0]	Reserved	CHGIN_ILIM[6:0]						
0xD4	nChgConfig4[15:8]	CHGIN_INLIM_Gate	SDPMaxCurr[1:0]		CDPMaxCurr	DCDCpl	DCPDet3A	–	CHGDETEN
	nChgConfig4[7:0]	NO_AUTOISET	DATAMUX	Reserved	VCHGIN_REG[1:0]		INLIM_CLK[1:0]		DISKIP
0xD5	nChgConfig5[15:8]	–	–	–	–	–	–	–	–
	nChgConfig5[7:0]	–	–	–	–	RestartChg	DeepShip	ChgEnable	CCDetEn
0xD6	ChgDetails00[15:8]	AICL_OK	CHGIN_OK	–	CHG_OK	BAT_OK	Reserved	–	BYP_OK
	ChgDetails00[7:0]	–	CHGIN_DTLS[1:0]		–	–	–	–	CHGEN

ADDRESS	NAME	MSB							LSB
0xD7	ChgDetails01[15:8]	TREG	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
	ChgDetails01[7:0]	BAT_dis_OC	–	–	–	BYP_DTLS[3:0]			
0xD8	UsbDetails[15:8]	–	CHGTYP[1:0]		PRCHGTYP[2:0]			CC_CURR[1:0]	
	UsbDetails[7:0]	–	USB_INLIM[6:0]						
0xDB	VByp[15:8]	VByp[15:8]							
	VByp[7:0]	VByp[7:0]							
MG									
0xE0	Command[15:8]	CMD[15:8]							
	Command[7:0]	CMD[7:0]							
0xE1	USR[15:8]	–	–	–	–	–	–	–	–
	USR[7:0]	–	–	–	–	–	–	–	NLOCK
0xFB	VFOCV[15:8]	VFOCV[15:8]							
	VFOCV[7:0]	VFOCV[7:0]							
0xFF	VFSOC[15:8]	VFSOC[15:8]							
	VFSOC[7:0]	VFSOC[7:0]							

Register Details

Status (0x0)

The Status register maintains all flags related to alert thresholds and battery insertion or removal.

BIT	15	14	13	12	11	10	9	8
Field	Br	Smx	Tmx	Vmx	Bi	Smn	Tmn	Vmn
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BIT	7	6	5	4	3	2	1	0
Field	dSOCi	Imx	–	–	Bst	Imn	POR	–

Reset	0b0	0b0	–	–	0b0	0b0	0b1	–
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
Br	15	Battery removal. It is useful when the IC is used in a host-side application. This bit is set to 1 when the system detects that a battery has been removed from the system by monitoring the THM pin. This bit must be cleared by system software to detect the next removal event. Br is set to 1 at power-up. Valid when Config.Ber = 1.	0x0: Br not detected 0x1: Br detected
Smx	14	Maximum SOC alert threshold exceeded. This bit is set to 1 whenever SOC is above the SAlrtTh thresholds. Check MiscCfg.SACFG for the SOC type. This bit can be configured as a level or edge trigger by nAlrtCfg.Edge. When configured as a level trigger, it may or may not need to be cleared by system software to detect the next event. See the Config.SS description. Smx is cleared to 0 at power-up.	0x0: Smx not detected 0x1: Smx detected
Tmx	13	Maximum temperature alert threshold exceeded. This bit is set to 1 whenever the Temp register reading is above the TAlrtTh thresholds. This bit can be configured as a level or edge trigger by nAlrtCfg.Edge. When configured as a level trigger, it may or may not need to be cleared by system software to detect the next event. See Config.TS bit description. Tmx is cleared to 0 at power-up.	0x0: Tmx not detected 0x1: Tmx detected
Vmx	12	Maximum voltage alert threshold exceeded. This bit is set to a 1 whenever the VCell register reading is above the VAlrtTh thresholds. This bit can be configured as a level or edge trigger by nAlrtCfg.Edge. When configured as a level trigger, it may or may not need to be cleared by system software to detect the next event. See the Config.VS bit description. Vmx is cleared to 0 at power-up.	0x0: Vmx not detected 0x1: Vmx detected
Bi	11	Battery insertion. It is useful when the IC is used in a host-side application. This bit is set to 1 when the device detects that a battery has been inserted into the system by monitoring the THM pin. This bit must be cleared by the system software to detect the next insertion event. Bi is set to 0 at power-up. Valid when Config.Bei = 1.	0x0: Bi not detected 0x1: Bi detected
Smn	10	Minimum SOC alert threshold exceeded. These bits are set to a 1 whenever SOC is below the SAlrtTh thresholds. This bit can be configured as a level or edge trigger by nAlrtCfg.Edge. When configured as	0x0: Smn not detected 0x1: Smn detected

BITFIELD	BITS	DESCRIPTION	DECODE
		a level trigger, These bits may or may not need to be cleared by system software to detect the next event. See the Config.SS description. Smn is cleared to 0 at power-up.	
Tmn	9	Minimum temperature alert threshold exceeded. This bit is set to a 1 whenever a Temp register reading is below the TAlrtTh thresholds. This bit can be configured as a level or edge trigger by nAlrtCfg.Edge. When configured as a level trigger, it may or may not need to be cleared by system software to detect the next event. See Config.TS bit description. Tmn is cleared to 0 at power-up.	0x0: Tmn not detected 0x1: Tmn detected
Vmn	8	Minimum voltage alert threshold exceeded. This bit is set to a 1 whenever a VCell register reading is below the VAlrtTh thresholds. This bit can be configured as a level or edge trigger by nAlrtCfg.Edge. When configured as a level trigger, it may or may not need to be cleared by system software to detect the next event. See the Config.VS bit description. Vmn is cleared to 0 at power-up.	0x0: Vmn not detected 0x1: Vmn detected
dSOCi	7	State of charge 1% change alert. This is set to 1 whenever the SOC register crosses an integer percentage boundary such as 50.0%, 51.0%, etc. It must be cleared by the host software. dSOCi is set to 1 at power-up. Check MiscCfg.SACFG for the SOC type.	0x0: dSOCi not detected 0x1: dSOCi detected
Imx	6	Maximum current alert threshold exceeded. This bit is set to a 1 whenever a Current register reading is above the IAlrtTh thresholds. This bit can be configured as a level or edge trigger by nAlrtCfg.Edge. When configured as a level trigger, it may or may not need to be cleared by system software to detect the next event. See Config.IS bit description. Imx is cleared to 0 at power-up.	0x0: Imx not detected 0x1: Imx detected
Bst	3	Battery status. It is useful when the IC is used in a host-side application. This bit is set to 0 when a battery is present in the system and set to 1 when the battery is absent by monitoring the THM pin. Bst is set to 0 at power-up.	0x0: Bst not detected 0x1: Bst detected
Imn	2	Minimum current alert threshold exceeded. This bit is set to a 1 whenever a Current register reading is below the IAlrtTh thresholds. This bit can be configured as a level or edge trigger by nAlrtCfg.Edge. When configured as a level trigger, it may or may not need to be cleared by system software to detect the next event. This bit may or may not need to be cleared by system software to	0x0: Imn not detected 0x1: Imn detected

BITFIELD	BITS	DESCRIPTION	DECODE
		detect the next event. See the Config.IS bit description. Imn is cleared to 0 at power-up.	
POR	1	Power-on reset. This bit is set to a 1 when the device detects that a software or hardware POR event has occurred. This bit must be cleared by system software to detect the next POR event. POR is set to 1 at power-up.	0x0: POR not detected 0x1: POR detected

ChgMaskSts (0x1)

This register maintains all mask and alert bits related to charger

BIT	15	14	13	12	11	10	9	8
Field	AICL_M	CHGIN_M	–	CHG_M	BAT_M	Reserved	–	BYP_M
Reset	0b1	0b1	–	0b1	0b1	0b1	–	0b1
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	–	Write, Read
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	AICL_I	CHGIN_I	–	CHG_I	BAT_I	Reserved	–	BYP_I
Reset	0b0	0b0	–	0b0	0b0	0b0	–	0b0
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_M	15	AICL interrupt mask	0x0: Unmask. AICL_I goes to ALRT. 0x1: Mask. AICL_I does not go to ALRT.
CHGIN_M	14	CHGIN interrupt mask	0x0: Unmask. CHGIN_I goes to ALRT. 0x1: Mask. CHGIN_I does not go to ALRT.
CHG_M	12	Charge status interrupt mask	0x0: Unmask. CHG_I goes to ALRT. 0x1: Mask. CHG_I does not go to ALRT.
BAT_M	11	Battery status interrupt mask	0x0: Unmask. BAT_I goes to ALRT. 0x1: Mask. BYP_I does not go to ALRT.
Reserved	10	Reserved, do not modify.	Reserved
BYP_M	8	BYP_I interrupt Mask	0x0: Unmask. BYP_I goes to ALRT. 0x1: Mask. BYP_I does not go to ALRT.
AICL_I	7	AICL interrupt. AICL_OK has changed. Write 0 to clear.	0x0: AICL_I not detected 0x1: AICL_I detected
CHGIN_I	6	CHGIN interrupt. CHGIN_OK has changed. Write 0 to clear.	0x0: CHGIN_I not detected 0x1: CHGIN_I detected
CHG_I	4	Charger interrupt. CHG_OK has changed. Write 0 to clear.	0x0: CHG_I not detected 0x1: CHG_I detected

BITFIELD	BITS	DESCRIPTION	DECODE
BAT_I	3	Battery status interrupt. BAT_OK has changed. Write 0 to clear.	0x0: BAT_I not detected 0x1: BAT_I detected
Reserved	2	Reserved, do not modify.	Reserved
BYP_I	0	BYP status interrupt. BYP_OK has changed. Write 0 to clear.	0x0: BYP_I not detected 0x1: BYP_I detected

VAlrtTh (0x3)

The VAlrtTh register sets upper (VMAX) and lower (VMIN) limits that generate an alert if exceeded by the VCell register value.

BIT	15	14	13	12	11	10	9	8
Field	VMAX[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	VMIN[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VMAX	15:8	Maximum voltage reading. The VMIN field sets the upper limit to generate an alert if exceeded by the VCell register value.	Type = voltage Scalar = 20 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 5100.0 MinimumScaled = 0.0
VMIN	7:0	Minimum voltage reading. The VMIN field sets the lower limit to generate an alert if exceeded by the VCell register value.	Type = voltage Scalar = 20 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 5100.0 MinimumScaled = 0.0

TAlrtTh (0x4)

The TAlrtTh register sets upper (TMAX) and lower (TMIN) limits that generate an alert if exceeded by Temp register value.

BIT	15	14	13	12	11	10	9	8

Field	TMAX[7:0]							
Reset	0x7F							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	TMIN[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TMAX	15:8	Maximum temperature reading. The TMAX field sets the upper limit to generate an alert if exceeded by the Temp register value.	Type = temperature Scalar = 1.0 Lsbunit = 1ºC Offset = 0.0 Signed = True MaximumScaled = 127.0 MinimumScaled = -128.0
TMIN	7:0	Minimum temperature reading. The TMIN field sets the lower limit to generate an alert if exceeded by the Temp register value.	Type = temperature Scalar = 1.0 Lsbunit = 1ºC Offset = 0.0 Signed = True MaximumScaled = 127.0 MinimumScaled = -128.0

SAlrtTh (0x5)

The SAlrtTh register sets upper (SMAX) and lower (SMIN) limits that generate an alert if exceeded.

BIT	15	14	13	12	11	10	9	8
Field	SMAX[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	SMIN[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SMAX	15:8	Maximum state-of-charge threshold. The SMAX field sets an upper limit that generates an alert if the SOC threshold is exceeded. Check MiscCfg.SACFG for SOC type.	Type = percent Scalar = 1.0 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 255.0 MinimumScaled = 0.0
SMIN	7:0	Minimum state-of-charge threshold. The SMIN field sets a lower limit that generates an alert if the SOC threshold is exceeded. Check MiscCfg.SACFG for SOC type.	Type = percent Scalar = 1.0 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 255.0 MinimumScaled = 0.0

RepCap (0x6)

BIT	15	14	13	12	11	10	9	8
Field	RepCap[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	RepCap[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RepCap	15:0	Reported remaining capacity. RepCap or reported remaining capacity (mAh) is a filtered version of the AvCap register. The ModelGauge m5 algorithm prevents remaining capacity from making sudden jumps during load changes.	Type = capacity Scalar = 0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

RepSOC (0x7)

BIT	15	14	13	12	11	10	9	8
Field	RepSOC[15:8]							
Reset	0x3200							
Access Type	Write, Read							

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	RepSOC[7:0]							
Reset	0x3200							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RepSOC	15:0	Reported state-of-charge. RepSOC is a filtered version of the AvSOC register that prevents large jumps in the reported value caused by changes in the application, such as abrupt changes in load current. RepSOC corresponds to RepCap and FullCapRep. RepSOC is intended to be the final state of charge percentage output for application use.	Type = percent Scalar = 0.00390625 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 255.99609375 MinimumScaled = 0.0

IDVolt (0x8)

BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	IDVolt[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	IDVolt[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
IDVolt	15:0	Battery ID. When an external thermister is not used, connect a fixed resistor on THM for battery identification. Enable through Config.FTHRM.

MaxMinTemp (0x9)

Maximum and Minimum temperature register. This register updates the maximum or minimum temperature reading since the last fuel-gauge reset or until cleared by host software.

BIT	15	14	13	12	11	10	9	8
Field	MaxTemperature[7:0]							
Reset	0x80							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	MinTemperature[7:0]							
Reset	0x7F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MaxTemperature	15:8	Maximum temperature register reading. The MaxTemperature register maintains the maximum Temperature register value since the last fuel-gauge reset or until cleared by host software. At power-up, the maximum value is set to 0x80 (most negative). The value is changed to the Temperature register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x80.	Type = temperature Scalar = 1.0 Lsbunit = 1ºC Offset = 0.0 Signed = True MaximumScaled = 127.0 MinimumScaled = -128.0
MinTemperature	7:0	Minimum temperature register reading. The MinTemperature register maintains the minimum temperature register value since the last fuel-gauge reset or until cleared by host software. At power-up, the minimum value is set to 0x7F (most positive). Therefore, the value is changed to the temperature register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x7F.	Type = temperature Scalar = 1.0 Lsbunit = 1ºC Offset = 0.0 Signed = True MaximumScaled = 127.0 MinimumScaled = -128.0

MaxMinCurr (0xA)

Maximum and minimum of current register. This register updates the maximum or minimum values from the last IC reset or until cleared by host software.

BIT	15	14	13	12	11	10	9	8
Field	MaxCurrent[7:0]							
Reset	0x80							
Access Type	Write, Read							

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	MinCurrent[7:0]							
Reset	0x7F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MaxCurrent	15:8	Maximum current register reading. The MaxCurrent register maintains the maximum Current register values since the last reset or until cleared by host software. At power-up, the maximum current value is set to 0x80h (most negative). Therefore, the value is changed to the Current register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x80.	Type = current Scalar = 40 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 50.8 MinimumScaled = -51.2
MinCurrent	7:0	Minimum current register reading. The MinCurrent register maintains the minimum Current register values since the last reset or until cleared by host software. At power-up, the minimum current value is set to 0x7Fh (most positive). Therefore, the value is changed to the Current register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x7F.	Type = current Scalar = 40 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 50.8 MinimumScaled = -51.2

MaxMinVolt (0xB)

Host software can reset this register by writing it to its power-up value of 0x00FF. The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution.

BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	MaxVCELL[7:0]							
Reset	0x00							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	MinVCELL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MaxVCELL	15:8	Maximum VCell register reading. The MaxVCELL register maintains the maximum current register values from the last reset or until cleared by host software. At power-up, the maximum current value is set to 0x00h. Therefore, the value is changed to the VCell register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x00.	Type = voltage Scalar = 20 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 5100.0 MinimumScaled = 0.0
MinVCELL	7:0	Minimum VCell register reading. The MinCurrent register maintains the minimum Current register values since the last reset or until cleared by host software. At power-up, the minimum current value is set to 0xFFh. Therefore, the value is changed to the Current register reading after the first update. Host software can reset this register by writing it to its power-up value of 0xFF.	Type=voltage Scalar=20 Lsbunit=mV Offset=0.0 Signed=False MaximumScaled=5100.0 MinimumScaled=0.0

Config (0xC)

The Config registers hold all shutdown enable, alert enable, and temperature enable control bits. Writing a bit location enables the corresponding function within one task period.

BIT	15	14	13	12	11	10	9	8
Field	–	SS	TS	VS	IS	–	–	Tex
Reset	–	0b0	0b1	0b0	0b0	–	–	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PinConfig	–	–	–	FTHRM	Aen	Bei	Ber
Reset	0b0	–	–	–	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SS	14	SOC ALRT sticky. When SS = 1, SOC alerts can only be cleared through software. When SS = 0, SOC alerts are cleared automatically when the threshold is no longer exceeded.	0x0: SS off 0x1: SS on
TS	13	Temperature ALRT sticky. When TS = 1, temperature alerts can only be cleared through	0x0: TS off 0x1: TS on

BITFIELD	BITS	DESCRIPTION	DECODE
		software. When TS = 0, temperature alerts are cleared automatically when the threshold is no longer exceeded.	
VS	12	Voltage ALRT sticky. When VS = 1, voltage alerts can only be cleared through software. When VS = 0, voltage alerts are cleared automatically when the threshold is no longer exceeded.	0x0: VS off 0x1: VS on
IS	11	Current ALRT sticky. When IS = 1, current alerts can only be cleared through software. When IS = 0, current alerts are cleared automatically when the threshold is no longer exceeded.	0x0: IS off 0x1: IS on
Tex	8	External temperature overwrite. When set to 1, the temperature register stops updating. The fuel gauge requires external temperature measurements to be written from the host. When set to 0, the IC's own measurements are used instead. This bit is ignored when nADCCfg.ThEn = 0.	0x0: Tex false 0x1: Tex true
PinConfig	7	ICHG/VCHG pin configuration reset. Detect the ICHG and VCHG pin and reset the related registers according to the ICHG/VCHG resistance. Set to 0x1 to reset the related registers. Auto-cleared when the process is completed.	0x0: PinConfig off 0x1: PinConfig on
FTHRM	3	Force thermistor bias. This allows the host to control the bias of the thermistor switch or enable fast detection of battery removal. Set FTHRM = 1 to always enable the thermistor bias switch. With a standard 10kΩ thermistor, this adds an additional ~200µA to the current drain of the circuit.	0x0: FTHRM off 0x1: FTHRM on
Aen	2	Enable alert on fuel-gauge outputs. When Aen = 1, a violation of any of the alert threshold register values by temperature, voltage, or SOC triggers an alert. This bit only affects the ALRT pin operation. The Smx, Smn, Tmx, Tmn, Vmx, Vmn, Imx, and Imn bits of the Status register (00h) are not disabled. The Charger interrupts ALRT operation is not enabled by this bit.	0x0: Aen disabled 0x1: Aen enabled
Bei	1	Enable alert on battery insertion. When Bei = 1, a battery-insertion condition, as detected by the THM pin voltage, triggers an alert.	0x0: Bei disabled 0x1: Bei enabled
Ber	0	Enable alert on battery removal. When Ber = 1, a battery-removal condition, as detected by the THM pin voltage, triggers an alert.	0x0: Ber disabled 0x1: Ber enabled

MixSOC (0xD)

BIT	15	14	13	12	11	10	9	8
Field	MixSOC[15:8]							
Reset	0x3200							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	MixSOC[7:0]							
Reset	0x3200							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MixSOC	15:0	Uncompensated SOC from MixCap. The MixSOC register holds the calculated present state-of-charge of the cell before any empty compensation adjustments are performed. MixSOC corresponds with MixCap and FullCapNom.	Type = percent Scalar = 0.00390625 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 255.99609375 MinimumScaled = 0.0

AvSOC (0xE)

BIT	15	14	13	12	11	10	9	8
Field	AvSOC[15:8]							
Reset	0x3200							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	AvSOC[7:0]							
Reset	0x3200							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvSOC	15:0	Available, unfiltered state of charge. The AvSOC register holds the calculated available state-of-charge of the cell based on all inputs from the ModelGauge m5 algorithm, including empty compensation. The AvSOC percentage corresponds with AvCap and FullCapNom. The AvSOC register value is an unfiltered calculation. Jumps in the reported value can be caused by changes in the application, such as abrupt changes in load current or temperature.	Type = percent Scalar = 0.00390625 Lsb unit = % Offset = 0.0 Signed = False MaximumScaled = 255.99609375 MinimumScaled = 0.0

MiscCfg (0xF)

The MiscCfg control register enables various other functions of the device.

BIT	15	14	13	12	11	10	9	8
Field	FUS[3:0]				Reserved	Reserved	MixRate[4:3]	
Reset	0x3				0b0	0b0	0b00011	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	MixRate[2:0]			Reserved	–	–	SACFG[1:0]	
Reset	0b00011			0b1	–	–	0b00	
Access Type	Write, Read			Write, Read	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
FUS	15:12	Full update slope. This field prevents jumps in the RepSOC and FullCapRep registers by setting the rate of adjustment of FullCapRep near the end of a charge cycle.	Type = percent Scalar = 2.0 Lsbunit = % per minutes Offset = 0.0 Signed = False MaximumScaled = 32.0 MinimumScaled = 2.0
Reserved	11	Reserved, do not modify, keep this at 0x0.	Reserved
Reserved	10	Reserved, do not modify, keep this at 0x0.	Reserved
MixRate	9:5	Mixing rate. This value sets the strength of the servo mixing rate after the final mixing state has been reached (> 2.08 complete cycles). Setting this value to 0b0000 disables servo mixing, and the IC continues with time-constant mixing indefinitely.	Type = capacity Scalar = 0.625 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 19.375 MinimumScaled = 0.0
Reserved	4	Reserved, do not modify, keep this at 0x1.	Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
SACFG	1:0	SOC alert config. SOC Alerts can be generated by monitoring any of the SOC registers as follows. SACFG defaults to 00 at power-up.	0x0: SOC Alerts are generated based on the RepSOC register. 0x1: SOC Alerts are generated based on the AvSOC register. 0x2: SOC Alerts are generated based on the MixSOC register. 0x3: SOC Alerts are generated based on the VFSOC register.

FullCapRep (0x10)

BIT	15	14	13	12	11	10	9	8
Field	FullCapRep[15:8]							
Reset	0x05DC							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	FullCapRep[7:0]							
Reset	0x05DC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FullCapRep	15:0	Full capacity. This register reports the full capacity that goes with RepCap, generally used for reporting to the GUI. Most applications should only monitor FullCapRep, instead of FullCap or FullCapNom. A new full-capacity value is calculated at the end of every charge cycle in the application.	Type = capacity Scalar = 0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

QRTable00 (0x12)

The QRTable00 to QRTable30 register locations contain characterization information regarding cell capacity that is unavailable under certain application conditions.

BIT	15	14	13	12	11	10	9	8
Field	QRTable00[15:8]							
Reset	0x3C00							
Access Type	Write, Read							

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	QRTable00[7:0]							
Reset	0x3C00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
QRTable00	15:0	The QRTable00 to QRTable30 register locations contain characterization information regarding cell capacity that is unavailable under certain application conditions.

RSlow (0x14)

BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	RSlow[15:8]							
Reset	0x0290							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	RSlow[7:0]							
Reset	0x0290							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RSlow	15:0	Slow battery impedance.	Type = resistance Scalar = 0.244140625 Lsbunit = mΩ Offset = 0.0 Signed = False MaximumScaled = 15.999755859375 MinimumScaled = 0.0

Age (0x16)

BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Age[15:8]							

Reset	0x6400							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Age[7:0]							
Reset	0x6400							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
Age	15:0	Age. The Age register contains a calculated percentage value of the application's present cell capacity compared to its original design capacity. The result can be used by the host to gauge the battery pack's health as compared to a new pack of the same type. The equation for the register output is Age Register(%) = 100% x (FullCapRep Register / DesignCap Register). For example, if DesignCap = 2000mAh and FullCapRep = 1800mAh, then Age=90% (or 0x5A00).	Type = percent Scalar = 0.00390625 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 255.99609375 MinimumScaled = 0.0

Cycles (0x17)

BIT	15	14	13	12	11	10	9	8
Field	Cycles[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Cycles[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
Cycles	15:0	Cycles. The Cycles register maintains a total count of the number of charge/discharge cycles of the cell. The result is stored as a fraction of a full cycle. For example, a full charge/discharge cycle results in the Cycles register incrementing by 100%. The Cycles register accumulates fractional or whole cycles. For example, if a battery is cycled 10% x 10 times, then it is equivalent to 100% of one cycle.	Type = cycles Scalar = 1.0 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 65535.0 MinimumScaled = 0.0

DesignCap (0x18)

BIT	15	14	13	12	11	10	9	8
Field	DesignCap[15:8]							
Reset	0x05DC							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	DesignCap[7:0]							
Reset	0x05DC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DesignCap	15:0	Design capacity. The DesignCap register holds the nominal capacity of the cell. This value is used to determine the age and health of the cell by comparing it against the measured present cell capacity.	Type = capacity Scalar = 0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

AvgVCell (0x19)

BIT	15	14	13	12	11	10	9	8
Field	AvgVCell[15:8]							
Reset	0xB400							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AvgVCell[7:0]							
Reset	0xB400							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvgVCell	15:0	Average cell voltage. The AvgVCell register reports an average of the VCell register readings. The time period for averaging is configurable from a 12-second to 24-minute time period. See the FilterCfg.VOLT for details on setting the time filter. The first VCell register reading after power-up or exiting shutdown mode sets the starting point of the AvgVCell register. Note that when a cell relaxation event is detected, the averaging period changes to the period defined by the RelaxCfg.dt setting. The register reverts to its normal averaging period when a charge or discharge current is detected.	Type = voltage Scalar = 78.125 Lsbunit = µV Offset = 0.0 Signed = False MaximumScaled = 5119921.875 MinimumScaled = 0.0

VCell (0x1A)

BIT	15	14	13	12	11	10	9	8
Field	VCell[15:8]							
Reset	0xB400							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	VCell[7:0]							
Reset	0xB400							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VCell	15:0	Cell Voltage. VCell reports the voltage measured between BATT and GND.	Type = voltage Scalar = 78.125 Lsbunit = µV Offset = 0.0 Signed = False MaximumScaled = 5119921.875 MinimumScaled = 0.0

Temp (0x1B)

BIT	15	14	13	12	11	10	9	8
Field	Temp[15:8]							
Reset	0x1600							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	Temp[7:0]							
Reset	0x1600							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
Temp	15:0	Temperature. The IC can be configured to measure its own internal die temperature or an external NTC thermistor. Set nADCCfg.ThEn = 1 (default) to enable thermistor measurement. Thermistor conversions are initiated by periodically connecting the THM and BATT pins internally. Measurement results of the THM pin are compared to the voltage of the BATT pin and converted to a ratiometric value from 0% to 100%. The active pullup is disabled when temperature measurements are complete. This reduces the current consumption. Set nADCCfg.ThEn = 0 to enable die temperature measurement.	Type = temperature Scalar = 0.00390625 Lsbunit = 1ºC Offset = 0.0 Signed = True MaximumScaled = 127.99609375 MinimumScaled = -128.0

Current (0x1C)

BIT	15	14	13	12	11	10	9	8
Field	Current[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	Current[7:0]							

Reset	0x0000
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Current	15:0	Battery current. The IC can be configured to measure the current flow through the battery through the internal current sense or the voltage across the external sense resistor over a ±51.2mV range, and the result is stored as a two's complement value in the Current register. Set nADCCfg.RsnsEn = 0 (default) to measure the current through internal sense (equivalent to 10mΩ). If the external sense is preferred (nADCCfg.RsnsEn = 1), it is highly recommended to use 10mΩ to avoid rescaling charger registers.	Type = current Scalar = 0.15625 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 51198.4375 MinimumScaled = -51200.0

AvgCurrent (0x1D)

BIT	15	14	13	12	11	10	9	8
Field	AvgCurrent[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	AvgCurrent[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvgCurrent	15:0	Average current. The AvgCurrent register reports an average of Current register readings. See the FilterCfg.CURR for details on setting the time filter.	Type = current Scalar = 0.15625 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 51198.4375 MinimumScaled = -51200.0

VEmpty (0x1F)

The VEmpty register sets thresholds related to empty detection during operation.

BIT	15	14	13	12	11	10	9	8
Field	VE[8:1]							
Reset	0b101001010							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	VE[0]	VR[6:0]						
Reset	0b101001010	0b1100001						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
VE	15:7	Empty voltage target. The fuel gauge provides capacity and percentage relative to the empty voltage target, eventually declaring 0% at VE.	Type = voltage Scalar = 10 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 5100.0 MinimumScaled = 0.0
VR	6:0	Recovery voltage. Sets the voltage level for clearing empty detection. Once the cell voltage rises above this point, empty voltage detection is reenabled. This value defaults to 3.88V, which is recommended for most applications.	Type = voltage Scalar = 40 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 5080.0 MinimumScaled = 0.0

DevName (0x21)

BIT	15	14	13	12	11	10	9	8
Field	DevName[15:8]							
Reset	0x5030							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	DevName[7:0]							
Reset	0x5030							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DevName	15:0	Device Name. Device name. The DevName register holds device type and firmware revision information. This allows host software to identify the type of IC being communicated to easily.	0x5030: MAX77972

QRTable10 (0x22)

The QRTable00 to QRTable30 register locations contain characterization information regarding cell capacity that is not available under certain application conditions.

BIT	15	14	13	12	11	10	9	8
Field	QRTable00[15:8]							
Reset	0x1B80							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	QRTable00[7:0]							
Reset	0x1B80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
QRTable00	15:0	The QRTable00 to QRTable30 register locations contain characterization information regarding cell capacity that is not available under certain application conditions.

FullCapNom (0x23)

BIT	15	14	13	12	11	10	9	8
Field	FullCapNom[15:8]							
Reset	0x05DC							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	FullCapNom[7:0]							

Reset	0x05DC
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FullCapNom	15:0	Calculated cell full capacity. This register holds the calculated full capacity of the cell, not including temperature and empty compensation. A new full-capacity nominal value is calculated each time a cell relaxation event is detected. This register is used to calculate other outputs of the ModelGauge m5 algorithm.	Type = capacity Scalar = 0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

FullCap (0x24)

BIT	15	14	13	12	11	10	9	8
Field	FullCap[15:8]							
Reset	0x05DC							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	FullCap[7:0]							
Reset	0x05DC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FullCap	15:0	This register holds the calculated full capacity of the cell based on all inputs from the ModelGauge m5 EZ algorithm, including empty compensation. A new full-capacity value is calculated continuously as application conditions change (temperature and load).	Type = capacity Scalar = 0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

VFRemCap (0x25)

BIT	15	14	13	12	11	10	9	8
Field	VFRemCap[15:8]							

Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	VFRemCap[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VFRemCap	15:0	Remaining capacity by the voltage fuel gauge. VFRemCap holds the remaining capacity of the cell as determined by the voltage fuel gauge before any compensation applies.	Type = capacity Scalar=0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

MixCap (0x26)

BIT	15	14	13	12	11	10	9	8
Field	MixCap[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	MixCap[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MixCap	15:0	Mixed capacity. The MixCap register holds the calculated remaining capacity of the cell before any empty compensation adjustments are performed.	Type = capacity Scalar = 0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

AvCap (0x27)

BIT	15	14	13	12	11	10	9	8
Field	AvCap[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	AvCap[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvCap	15:0	Available capacity. The AvCap and AvSOC registers hold the calculated available capacity and percentage of the battery based on all inputs from the ModelGauge m5 algorithm, including empty compensation. These registers provide unfiltered results. Jumps in the reported values can be caused by abrupt changes in load current or temperature.	Type = capacity Scalar = 0.5 Lsbunit=mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

ChargingCurrent (0x28)

BIT	15	14	13	12	11	10	9	8
Field	ChargingCurrent[15:8]							
Reset	0x2800							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	ChargingCurrent[7:0]							
Reset	0x2800							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ChargingCurrent	15:0	Charging Current. Charging current setting at the operating step.	0: 0mA 0x280 to 0x4EC0: ChargingCurrent (hex) x 0.15625mA, 50mA per step, round down. 0x41C1 to 0x7FFF: 3150mA 0x8000 to 0xFFFF: 100mA

IChgTerm (0x29)

BIT	15	14	13	12	11	10	9	8
Field	IChgTerm[15:8]							
Reset	0x0280							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	IChgTerm[7:0]							
Reset	0x0280							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
IChgTerm	15:0	Charge termination current threshold.	0x0 to 0x7F: 20mA 0x80 to 0xC80: IChgTerm x 0.015625mA 0xC80 to 0xFFFF: 500mA

ChargingVoltage (0x2A)

BIT	15	14	13	12	11	10	9	8
Field	ChargingVoltage[15:8]							
Reset	0xCD00							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	ChargingVoltage[7:0]							
Reset	0xCD00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ChargingVoltage	15:0	Battery regulation voltage setting at the operating step.	0x0 to 0xAEFF: 3.4V 0xAF00 to 0xB17F: 3.5V 0xB180 to 0xB3FF: 3.55V 0xB400 to 0xCAAF: ChargingVoltage (hex) x 0.078125mV, 100mV per step, round down. 0xCAB0 to 0xCCFF: 4.05V 0xCD00 to 0xE800: ChargingVoltage (hex) x 0.078125mV, 10mV per step, round down. 0xE801 to 0xFFFF: 4.64V

QResidual (0x2E)

BIT	15	14	13	12	11	10	9	8
Field	QResidual[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	QResidual[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
QResidual	15:0	Capacity not accessible. The QResidual register provides the calculated amount of charge in mAh that is presently inside of but cannot be removed from the cell under present application conditions (load and temperature). This value is subtracted from the MixCap value to determine the capacity available to the user under present conditions (AvCap).	Type = capacity Scalar = 0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

LearnCfg (0x2F)

The ChargingVoltage register reports the prescribed charging voltage.

BIT	15	14	13	12	11	10	9	8
Field	FiltEmpty	Reserved[1:0]		Reserved[2:0]			Reserved[1:0]	
Reset	0b0	0b10		0b001			0b10	

Access Type	Write, Read	Write, Read		Write, Read			Write, Read	
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved	LearnStage[2:0]			Reserved[1:0]		MixEn	Reserved
Reset	0b0	0b000			0b01		0b1	0b0
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FiltEmpty	15	FiltEmpty chooses whether empty is determined by a filtered (AvgVCell) or unfiltered (VCell) voltage.	0x0: Detect empty using VCell. 0x1: Detect empty using AvgVCell.
Reserved	14:13	Reserved, do not modify.	Reserved
Reserved	12:10	Reserved, do not modify.	Reserved
Reserved	9:8	Reserved, do not modify.	Reserved
Reserved	7	Reserved, do not modify.	Reserved
LearnStage	6:4	Learn stage. The Learn Stage value controls the influence of the voltage fuel gauge on the mixing algorithm. The Learn Stage defaults to 0h, making the voltage fuel gauge dominate. The Learn Stage then advances to 7h over the course of two full cell cycles to make the coulomb counter dominate. The host software can write the Learn Stage value to 7h to advance to the final stage at any time. Writing any value between 1h and 6h is ignored.	0x0: Learn Stage 0 0x1: Learn Stage 1 0x2: Learn Stage 2 0x3: Learn Stage 3 0x4: Learn Stage 4 0x5: Learn Stage 5 0x6: Learn Stage 6 0x7: Learn Stage 7
Reserved	3:2	Reserved, do not modify.	Reserved
MixEn	1	Mix Enable.	0x0: MixEn disabled 0x1: MixEn enabled
Reserved	0	Reserved, do not modify.	Reserved

QRTable20 (0x32)

BIT	15	14	13	12	11	10	9	8
Field	QRTable20[15:8]							
Reset	0x0B04							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Field	QRTable20[7:0]
Reset	0x0B04
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION
QRTable20	15:0	The QRTable00 to QRTable30 register locations contain characterization information regarding cell capacity that is unavailable under certain application conditions.

DieTemp (0x34)

BIT	15	14	13	12	11	10	9	8
Field	DieTemp[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	DieTemp[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DieTemp	15:0	Die temperature. The DieTemp register provides the internal die temperature measurement. If nADCCfg.ThEn = 0, both DieTemp and Temperature registers have the value of the die temperature.	Type = temperature Scalar = 0.00390625 Lsbunit = 1ºC Offset = 0.0 Signed = True MaximumScaled = 127.99609375 MinimumScaled = -128.0

AvgTA (0x35)

BIT	15	14	13	12	11	10	9	8
Field	AvgTA[15:8]							
Reset	0x1600							
Access Type	Write, Read							

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	AvgTA[7:0]							
Reset	0x1600							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvgTA	15:0	Average temp reading. The AvgTA register reports an average of the readings from the Temperature register.	Type = temperature Scalar = 0.00390625 Lsbunit = 1ºC Offset = 0.0 Signed = True MaximumScaled = 127.99609375 MinimumScaled = -128.0

SOCHold (0x39)

The SOCHold register configures the operation of the hold before the empty feature and also the enable bit for 99% hold during charge.

BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	HoldEn99	EmptyVoltHold[6:3]			
Reset	–	–	–	0b1	0b0000000			
Access Type	–	–	–	Write, Read	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	EmptyVoltHold[2:0]			EmptySOCHold[4:0]				
Reset	0b0000000			0b00010				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
HoldEn99	12	Enable bit for 99% hold feature during charging. When enabled, RepSOC holds a maximum value of 99% until Full Qualified is reached.	0x0: HoldEn99 disabled 0x1: HoldEn99 enabled
EmptyVoltHold	11:5	The positive voltage offset will be added to VEmpty. At VCell = VE + EmptyVoltHold point, the empty detection/learning is occurred.	Type = voltage Scalar = 10 Lsbunit = mV Offset = 0.0 signed = False MaximumScaled = 1270.0 MinimumScaled = 0.0

BITFIELD	BITS	DESCRIPTION	DECODE
EmptySOCHold	4:0	It is the RepSOC at which RepSOC is held constant until the EmptyVoltHold condition is crossed. After empty detection occurs, the RepSOC update will continue as expected.	Type = percent Scalar = 0.5 Lsbunit = % Offset = 0.0 signed = False MaximumScaled = 15.5 MinimumScaled = 0.0

ProtStatus (0x3A)

The Protection Status register contains the Fault States of the Protection State Machine.

BIT	15	14	13	12	11	10	9	8
Field	–	TooHotC	Full	TooColdC	–	–	–	–
Reset	–	0b0	0b0	0b0	–	–	–	–
Access Type	–	Write, Read	Write, Read	Write, Read	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TooHotC	14	TooHot protection for charging.	0x0: Not in TooHot state. 0x1: TooHot stop charging.
Full	13	Full detected.	0x0: Not in Full state. 0x1: Full qualified.
TooColdC	12	TooCold protection for charging.	0x0: Not in the TooCold protection state. 0x1: TooCold stop charging.

FStat2 (0x3C)

The FStat2 register is a read-only register that monitors the status of the ModelGauge algorithm. Do not write to this register location.

BIT	15	14	13	12	11	10	9	8
Field	Reserved	–	Reserved	FDet	OCV_OutLimits	Reserved	Reserved	Reserved
Reset	0b0	–	0b1	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	Reserved[1:0]		Reserved
Reset	–	–	–	–	–	0b00		0b0
Access Type	–	–	–	–	–	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	15	Reserved, do not modify.	Reserved
Reserved	13	Reserved, do not modify.	Reserved
FDet	12	FDET is set to 1 when full is detected. FDET is cleared when loading starts or charging restarts.	0x0: FDet not detected. 0x1: FDet detected.
OCV_OutLimits	11	Battery voltage is out of the keep-out region. It is valid only when a special chemistry battery is used when ModelCfg.ModelID = 0x6 or nNVCfg2.enSC = 0x1.	0x0: OCV_OutLimits not detected. 0x1: OCV_OutLimits detected.
Reserved	10	Reserved, do not modify.	Reserved
Reserved	9	Reserved, do not modify.	Reserved
Reserved	8	Reserved, do not modify.	Reserved
Reserved	2:1	Reserved, do not modify.	Reserved
Reserved	0	Reserved, do not modify.	Reserved

FStat (0x3D)

The FStat register is a read-only register that monitors the status of the ModelGauge algorithm. Do not write to this register location.

BIT	15	14	13	12	11	10	9	8
Field	–	Reserved	–	–	–	Reserved	RelDt	EDet
Reset	–	0b0	–	–	–	0b0	0b0	0b0
Access Type	–	Write, Read	–	–	–	Write, Read	Write, Read	Write, Read
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	FQ	RelDt2	Reserved	–	Reserved	–	Reserved	DNR
Reset	0b0	0b0	0b0	–	0b0	–	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	14	Reserved, do not modify.	Reserved
Reserved	10	Reserved, do not modify.	Reserved
RelDt	9	Relaxed cell detection. This bit is set to 1 whenever the ModelGauge m5 algorithm detects that the cell is in a fully relaxed state. This bit is cleared to 0 whenever a current greater than the Load threshold is detected.	0x0: RelDt false 0x1: RelDt true
EDet	8	Empty detection. This bit is set to 1 when the IC detects that the cell empty point has been reached. This bit is reset to 0 when the cell voltage rises above the recovery threshold.	0x0: EDet false. 0x1: EDet true.
FQ	7	Fully qualified. This bit is set when all charge termination conditions have been met. Both Current and AvgCurrent are less than 1.25 times of IChgTerm while charging.	0x0: FQ false. 0x1: FQ true.
RelDt2	6	Long relaxation. This bit is set to a 1 whenever the ModelGauge m5 algorithm detects that the cell has been relaxed for a period of 48 to 96 minutes or longer. This bit is cleared to 0 whenever the cell is no longer in a relaxed state.	0x0: RelDt2 false. 0x1: RelDt2 true.
Reserved	5	Reserved, do not modify.	Reserved
Reserved	3	Reserved, do not modify.	Reserved
Reserved	1	Reserved, do not modify.	Reserved
DNR	0	Data not ready. This bit is set to 1 at cell insertion and remains set until the output registers have been updated. Afterwards, the IC clears this bit indicating the fuel gauge calculations are up to date.	0x0: DNR false. 0x1: DNR true.

FProtStat (0x3E)

This register stores step charging status.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	StepID[2:1]	
Reset	–	–	–	–	–	–	0b000	
Access Type	–	–	–	–	–	–	Write, Read	
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Field	StepID[0]	–	IsDis	–	–	Tempid[2:0]
Reset	0b000	–	0b1	–	–	0b000
Access Type	Write, Read	–	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
StepID	9:7	Indicates Step-Charge Region.	0x0: Step 0. 0x1: Step 1. 0x2: Step 2. 0x3: Step 3. 0x4: Step 4.
IsDis	5	Battery discharging state.	0x0: Battery is not in discharging state. 0x1: Battery is in discharging state.
Tempid	2:0	JEITA temperature zone status.	0x4: TooCold. 0x5: Cold2. 0x6: Cold1. 0x7: Cool. 0x0: Room. 0x1: Warm. 0x2: Hot1. 0x3: Hot2/TooHot.

Timer (0x3F)

BIT	15	14	13	12	11	10	9	8
Field	Timer[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	Timer[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
Timer	15:0	This register holds timing information for the fuel gauge. It is available to the user for debugging purposes.	Type = time Scalar = 175.8 Lsbunit = ms Offset = 0.0 Signed = False MaximumScaled = 3.2Hr MinimumScaled = 0.0

QRTable30 (0x42)

BIT	15	14	13	12	11	10	9	8
Field	QRTable30[15:8]							
Reset	0x0885							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	QRTable30[7:0]							
Reset	0x0885							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
QRTable30	15:0	The QRTable00 to QRTable30 register locations contain characterization information regarding cell capacity that is unavailable under certain application conditions.

dQAcc (0x45)

BIT	15	14	13	12	11	10	9	8
Field	dQAcc[15:8]							
Reset	0x00BB							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	dQAcc[7:0]							
Reset	0x00BB							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
dQAcc	15:0	This register tracks changes in battery charge between relaxation points. It is available to the user for debugging purposes.	Type = capacity Scalar = 0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False

BITFIELD	BITS	DESCRIPTION	DECODE
			MaximumScaled = 32767.5 MinimumScaled = 0.0

dPAcc (0x46)

BIT	15	14	13	12	11	10	9	8
Field	dPAcc[15:8]							
Reset	0x0320							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	dPAcc[7:0]							
Reset	0x0320							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
dPAcc	15:0	This register tracks changes in battery state-of-charge between relaxation points. It is available to the user for debugging purposes.	Type = percent Scalar = 0.00390625 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 255.99609375 MinimumScaled = 0.0

QH (0x4D)

BIT	15	14	13	12	11	10	9	8
Field	QH[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	QH[7:0]							
Reset	0x0000							

Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
QH	15:0	The QH register displays the raw coulomb count generated by the device. This register is used internally as an input to the mixing algorithm. Monitoring changes in QH over time can be useful for debugging device operation.	Type = capacity Scalar=0.5 Lsbunit = mAh (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 32767.5 MinimumScaled = 0.0

ICHGIN (0x51)

BIT	15	14	13	12	11	10	9	8
Field	ICHGIN[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	ICHGIN[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ICHGIN	15:0	The CHGIN current register reports input current from the adapter.	Type = current Scalar = 0.15625 Lsb unit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 51198.4375 MinimumScaled = -51200.0.

VSys (0x52)

BIT	15	14	13	12	11	10	9	8
Field	VSys[15:8]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	VSys[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VSys	15:0	SYS Voltage	Type = voltage Scalar = 78.125 Lsbunit = µV Offset = 0.0 Signed = False MaximumScaled = 5119921.875 MinimumScaled = 0.0.

OCVTable0 (0x80)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable0[15:8]							
Reset	0x9760							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	OCVTable0[7:0]							
Reset	0x9760							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable0	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable1 (0x81)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable1[15:8]							
Reset	0xA510							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable1[7:0]							
Reset	0xA510							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable1	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable2 (0x82)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable2[15:8]							
Reset	0xB100							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable2[7:0]							
Reset	0xB100							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable2	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable3 (0x83)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable3[15:8]							
Reset	0xB600							

Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	OCVTable3[7:0]							
Reset	0xB600							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable3	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable4 (0x84)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable4[15:8]							
Reset	0xB7A0							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	OCVTable4[7:0]							
Reset	0xB7A0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable4	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable5 (0x85)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable5[15:8]							
Reset	0xB900							

Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	OCVTable5[7:0]							
Reset	0xB900							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable5	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable6 (0x86)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable6[15:8]							
Reset	0xBA70							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	OCVTable6[7:0]							
Reset	0xBA70							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable6	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable7 (0x87)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable7[15:8]							
Reset	0xBC70							

Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	OCVTable7[7:0]							
Reset	0xBC70							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable7	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable8 (0x88)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable8[15:8]							
Reset	0xBDE0							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	OCVTable8[7:0]							
Reset	0xBDE0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable8	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable9 (0x89)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable9[15:8]							
Reset	0xBFC0							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable9[7:0]							
Reset	0xBFC0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable9	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable10 (0x8A)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable10[15:8]							
Reset	0xC250							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable10[7:0]							
Reset	0xC250							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable10	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable11 (0x8B)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable11[15:8]							
Reset	0xC510							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable11[7:0]							
Reset	0xC510							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable11	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable12 (0x8C)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable12[15:8]							
Reset	0xC990							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable12[7:0]							
Reset	0xC990							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable12	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable13 (0x8D)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable13[15:8]							
Reset	0xCEA0							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable13[7:0]							
Reset	0xCEA0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable13	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable14 (0x8E)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable14[15:8]							
Reset	0xD040							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable14[7:0]							
Reset	0xD040							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable14	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

OCVTable15 (0x8F)

BIT	15	14	13	12	11	10	9	8
Field	OCVTable15[15:8]							
Reset	0xD750							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OCVTable15[7:0]							
Reset	0xD750							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OCVTable15	15:0	OCVTable0 - OCVTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable0 (0x90)

BIT	15	14	13	12	11	10	9	8
Field	XTable0[15:8]							
Reset	0x0060							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable0[7:0]							
Reset	0x0060							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable0	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable1 (0x91)

BIT	15	14	13	12	11	10	9	8
Field	XTable1[15:8]							
Reset	0x0120							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable1[7:0]							
Reset	0x0120							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable1	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable2 (0x92)

BIT	15	14	13	12	11	10	9	8
Field	XTable2[15:8]							
Reset	0x0240							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable2[7:0]							
Reset	0x0240							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable2	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable3 (0x93)

BIT	15	14	13	12	11	10	9	8
Field	XTable3[15:8]							
Reset	0x0D80							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable3[7:0]							
Reset	0x0D80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable3	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable4 (0x94)

BIT	15	14	13	12	11	10	9	8
Field	XTable4[15:8]							
Reset	0x08B0							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable4[7:0]							
Reset	0x08B0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable4	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable5 (0x95)

BIT	15	14	13	12	11	10	9	8
Field	XTable5[15:8]							
Reset	0x0590							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable5[7:0]							
Reset	0x0590							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable5	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable6 (0x96)

BIT	15	14	13	12	11	10	9	8
Field	XTable6[15:8]							
Reset	0x1200							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable6[7:0]							
Reset	0x1200							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable6	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable7 (0x97)

BIT	15	14	13	12	11	10	9	8
Field	XTable7[15:8]							
Reset	0x3210							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable7[7:0]							
Reset	0x3210							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable7	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable8 (0x98)

BIT	15	14	13	12	11	10	9	8
Field	XTable8[15:8]							
Reset	0x0EE0							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable8[7:0]							
Reset	0x0EE0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable8	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable9 (0x99)

BIT	15	14	13	12	11	10	9	8
Field	XTable9[15:8]							
Reset	0x0A40							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable9[7:0]							
Reset	0x0A40							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable9	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable10 (0x9A)

BIT	15	14	13	12	11	10	9	8
Field	XTable10[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable10[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable10	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable11 (0x9B)

BIT	15	14	13	12	11	10	9	8
Field	XTable11[15:8]							
Reset	0x08E0							

Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	XTable11[7:0]							
Reset	0x08E0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable11	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable12 (0x9C)

BIT	15	14	13	12	11	10	9	8
Field	XTable12[15:8]							
Reset	0x0800							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	XTable12[7:0]							
Reset	0x0800							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable12	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable13 (0x9D)

BIT	15	14	13	12	11	10	9	8
Field	XTable13[15:8]							
Reset	0x0780							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable13[7:0]							
Reset	0x0780							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable13	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable14 (0x9E)

BIT	15	14	13	12	11	10	9	8
Field	XTable14[15:8]							
Reset	0x06B0							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable14[7:0]							
Reset	0x06B0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable14	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

XTable15 (0x9F)

BIT	15	14	13	12	11	10	9	8
Field	XTable15[15:8]							
Reset	0x06B0							

Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	XTable15[7:0]							
Reset	0x06B0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XTable15	15:0	XTable0 - XTable15 stores cell characterization information used by the ModelGauge algorithm to determine capacity versus operating conditions.

ModelCfg (0xA3)

The ModelCfg register controls basic options of the EZ algorithm.

BIT	15	14	13	12	11	10	9	8
Field	Refresh	–	–	–	–	VChg	–	Reserved
Reset	0b0	–	–	–	–	0b1	–	0b0
Access Type	Write, Read	–	–	–	–	Write, Read	–	Write, Read
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	ModelID[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Refresh	15	Set Refresh to 1 to command the model reload. Auto clear to 0 after the ez config is loaded.	0x0: Refresh off. 0x1: Refresh on.
VChg	10	ModelGauge ez config charge termination voltage option.	0x0: Charge termination voltage is 4.2V. 0x1: Charge termination voltage is higher than 4.25V (4.3V to 4.4V).
Reserved	8	Reserved, do not modify.	Reserved
ModelID	7:4	Choose from one of the following Lithium models. For the majority of batteries, use ModelID = 0.	0: Used for most lithium cobalt-oxide variants (a large majority of lithium in the marketplace). Supported by EZ without characterization. 2: Used for lithium NCR or NCA cells such as Panasonic.

BITFIELD	BITS	DESCRIPTION	DECODE
			Custom characterization is recommended in this case. 6: Used for lithium iron-phosphate (LiFePO4). Custom characterization is recommended in this case. Other: Reserved. Do not write.

MaxPeakPower (0xA4)

BIT	15	14	13	12	11	10	9	8
Field	MaxPeakPower[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	MaxPeakPower[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MaxPeakPower	15:0	The fuel gauge computes and returns the maximum instantaneous peak output power of the battery pack, which is available for up to 10ms, given the external resistance and required minimum system voltage. The MaxPeakPower value is expected to be negative and has to be updated at least once every second. MaxPeakPower is initialized to the present value of MaxPeakPower on reset or power-up. The internal configuration of the fuel gauge should allow the maximum value of this parameter to be configured, which accounts for various system limitations, such as limiting the cell discharge current to the 4C rate and allowing for the safe operating area specifications for devices in the power path, such as MOSFETs. It is suggested that these parameters be user-defined. MaxPeakPower = MPPCurrent x AvgVCell.	Type = power Scalar = 0.8 Lsbunit = mW Offset = 0.0 signed = false MaximumScaled = 52428.0 MinimumScaled = 0.0

SusPeakPower (0xA5)

BIT	15	14	13	12	11	10	9	8

Field	SusPeakPower[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	SusPeakPower[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SusPeakPower	15:0	The fuel gauge computes and returns the sustained peak output power of the battery pack in cW, which is available for up to 10s, given the external resistance and required minimum voltage of the voltage regulator. The SusPeakPower value is expected to be negative and has to be updated at least once every second. SusPeakPower is initialized to the present value of SusPeakPower on reset or power-up. The internal configuration of the fuel gauge should allow the maximum value of this parameter to be configured, which accounts for various system limitations, such as limiting the cell discharge current to the 2C rate and allowing for the safe operating area specifications for devices in the power path, such as MOSFETs. It is suggested that these parameters be user-defined. SusPeakPower = SPPCurrent x AvgVCell.	Type = power Scalar = 0.8 Lsbunit = mW Offset = 0.0 signed = false MaximumScaled = 52428.0 MinimumScaled = 0.0

PackResistance (0xA6)

BIT	15	14	13	12	11	10	9	8
Field	PackResistance[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	PackResistance[7:0]							

Reset	0x0000
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PackResistance	15:0	The PackResistance register configures the total noncell pack resistance value to account for the resistances due to cell interconnect, sense resistor, FET, fuse, connector, and other impedances between the cells and output of the battery pack. The cell's internal resistance should NOT be included. PackResistance is initialized to a default value from the nPackResistance at power up.	Type = resistance Scalar = 0.244140625 Lsbunit = mΩ Offset = 0.0 Signed = False MaximumScaled = 15.999755859375 MinimumScaled = 0.0

SysResistance (0xA7)

BIT	15	14	13	12	11	10	9	8
Field	SysResistance[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	SysResistance[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SysResistance	15:0	The SysResitance register configures the total resistance value into fuel gauge to account for the resistances due to the resistance of power/ground metal, sense resistor, FET, and other parasitic resistance on the system main board. SysResistance is initialized to a default value of 0mΩ. The system designer is expected to overwrite the default value with the value from the system in question. This allows a single pack to be used in multiple systems which may have various values for SysResistance.	Type=resistance Scalar=0.244140625 Lsbunit=mΩ Offset=0.0 Signed=False MaximumScaled=15.999755859375 MinimumScaled=0.0

MinSysVoltage (0xA8)

BIT	15	14	13	12	11	10	9	8
Field	MinSysVoltage[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	MinSysVoltage[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MinSysVoltage	15:0	The MinSysVoltage register configures the required minimum system input voltage in mV into the fuel gauge. The system regulator will still operate normally if its input voltage is at this level. MinSysVoltage is initialized to a default value from the upper byte of the nDesignVoltage register at power up. The system designer can write the MinSysVoltage register directly during normal operation to change from the default setting. This allows a single pack to be used in multiple systems, which may have various values for MinSysVoltage. Writing MinSysVoltage above or below the empty point should not change the empty point. However, calculations for MPPCurrent, SPPCurrent, MaxPeakPower and SusPeakPower will report 0x0000 when VCell is less than the MinSysVoltage. For accurate performance, the system should normally update MinSysVoltage according to its requirements.	Type = voltage Scalar = 78.125 Lsbunit = µV Offset = 0.0 Signed = False MaximumScaled = 5119921.875 MinimumScaled = 0.0.

MPPCurrent (0xA9)

BIT	15	14	13	12	11	10	9	8
Field	MPPCurrent[15:8]							
Reset	0x0000							
Access Type	Write, Read							

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	MPPCurrent[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MPPCurrent	15:0	The fuel gauge computes and returns the maximum instantaneous peak current of the battery pack in the standard current register format, which is available for up to 10ms, given the external resistance and required minimum voltage of the voltage regulator. The MPPCurrent value is expected to be negative and has to be updated at least once every second. MPPCurrent is initialized to the present value of MPPCurrent on reset or power-up. MPPCurrent = (AvgVCell - MinSySVoltage) / [(PackResistance + SysResistance) x Rgain1].	Type = current Scalar = 0.15625 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 51198.4375 MinimumScaled = -51200.0.

SPPCurrent (0xAA)

BIT	15	14	13	12	11	10	9	8
Field	SPPCurrent[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	SPPCurrent[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPPCurrent	15:0	The fuel gauge computes and returns the sustained peak current of the battery pack in the standard current register format, which is available for up to	Type = current Scalar = 0.15625 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True

BITFIELD	BITS	DESCRIPTION	DECODE
		10s, given the external resistance and required minimum system voltage. The SPPCurrent value is expected to be negative and has to be updated at least once every second. SPPCurrent is initialized to the present value of SPPCurrent on reset or power-up. SPPCurrent = (AvgVCell - MinSySVoltage) / (RSlow x Rgain2).	MaximumScaled = 51198.4375 MinimumScaled = -51200.0.

Config2 (0xAB)

BIT	15	14	13	12	11	10	9	8
Field	LDMdl	–	–	DPEn	–	–	–	–
Reset	0b0	–	–	0b0	–	–	–	–
Access Type	Write, Read	–	–	Write, Read	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	dSOCEn	TAlrtEn	–	–	Reserved[1:0]		–	–
Reset	0b0	0b0	–	–	0b00		–	–
Access Type	Write, Read	Write, Read	–	–	Write, Read		–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LDMdl	15	The host sets this bit to 1 in order to initiate firmware to finish processing a newly loaded model. Firmware clears this bit to zero to indicate that model loading is finished.	0x0: LDMdl False. 0x1: LDMdl True.
DPEn	12	Dynamic power enable.	0x0: DPEn disabled. 0x1: DPEn enabled.
dSOCEn	7	SOC change alert enable. Set this bit to 1 to enable alert output with the Status.dSOCi bit function. Write this bit to 0 to disable alert output with the Status. dSOCi bit.	0x0: dSOCEn disabled. 0x1: dSOCEn enabled.
TAlrtEn	6	Temperature alert enable. Set this bit to 1 to enable temperature-based alerts. Write this bit to 0 to disable temperature alerts.	0x0: TAlrtEn disabled. 0x1: TAlrtEn enabled.
Reserved	3:2	Reserved, do not modify.	Reserved

IAlrtTh (0xAC)

Sets upper and lower limits that generate an alert if exceeded by the Current register value.

BIT	15	14	13	12	11	10	9	8
Field	IMAX[7:0]							
Reset	0x7F							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	IMIN[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
IMAX	15:8	Maximum current threshold. Maximum current reading. An alert is generated if the current register reading exceeds this value. Interrupt threshold limits are selectable with 0.4mV/R_{SENSE} (with external sense resistor) or 40mA (with internal FET current sensing) resolution over the full operating range of the Current register.	Type = current Scalar = 40 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 50.8 MinimumScaled = -51.2
IMIN	7:0	Minimum current threshold. Minimum current reading. An alert is generated if the current register reading falls below this value. Interrupt threshold limits are selectable with 0.4mV/R_{SENSE} (with external sense resistor) or 40mA (with internal FET current sensing) resolution over the full operating range of the Current register.	Type = current Scalar = 40 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 50.8 MinimumScaled = -51.2

Status2 (0xB0)

The Status2 register maintains the status of hibernate mode.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	DPReady	–	–	–	–
Reset	–	–	–	0b0	–	–	–	–
Access Type	–	–	–	Write, Read	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	Hib	Reserved
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DPReady	12	If DPReady = 1, Dynamic Power output registers are filled by the firmware and ready to be read by the host.	0x0: DPReady not detected. 0x1: DPReady detected.
Hib	1	Hibernate Status.	0x0: Hib not detected 0x1: Hib detected
Reserved	0	Reserved, do not modify.	Reserved

Power (0xB1)

BIT	15	14	13	12	11	10	9	8
Field	Power[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Power[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
Power	15:0	Instant power calculation from Current and VCell registers.	Type = power Scalar = 0.2 Lsbunit = mW (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 13107.0 MinimumScaled = 0.0.

AvgPower (0xB3)

BIT	15	14	13	12	11	10	9	8

Field	AvgPower[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	AvgPower[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvgPower	15:0	Average power calculation from AvgCurrent and AvgVCell registers.	Type = power Scalar = 0.2 Lsbunit = mW (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 13107.0 MinimumScaled = 0.0.

CGTempCo (0xB8)

BIT	15	14	13	12	11	10	9	8
Field	Reserved[15:8]							
Reset	0x0025							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x0025							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Reserved	15:0	Temperature coefficient of battery current measurement.

FOTPStat (0xBB)

BIT	15	14	13	12	11	10	9	8
Field	PatchID[3:0]				–	–	–	PinDraft
Reset	0x4				–	–	–	0b1
Access Type	Write, Read				–	–	–	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	Reserved	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PatchID	15:12	Firmware Patch ID.	
PinDraft	8	ICHG/VCHG pin conversion indicator.	0x0: ICHG/VCHG pin conversion is on going. 0x1: ICHG/VCHG pin is fully filtered and all related registers are updated according to ICHG/VCHG table.
Reserved	7	Reserved. Do not modify.	Reserved

TimerH (0xBE)

BIT	15	14	13	12	11	10	9	8
Field	TimerH[15:8]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	TimerH[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TimerH	15:0	This register allows the IC to track the age of the cell. An LSb of 3.2 hours gives a full-scale range for the register of up to 23.94 years.

PinID (0xCC)

High-byte indicates ICHG pin selection ID, low-byte indicates VCHG pin selection ID.

BIT	15	14	13	12	11	10	9	8
Field	iid[7:0]							
Reset	0x00							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	vid[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
iid	15:8	ICHG pin selection ID.
vid	7:0	VCHG pin selection ID.

nChgConfig0 (0xD0)

This register maintains charging status and configuration settings.

BIT	15	14	13	12	11	10	9	8
Field	PQEN	LSEL	Reserved[1:0]		RECYCLE_EN	FCHGTIME[2:0]		
Reset	0b1	0b0	0b00		0b1	0b100		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		
BIT	7	6	5	4	3	2	1	0
Field	–	DISIBS	–	WDTEN	MODE[3:0]			

Reset	–	0b0	–	0b0	0x5
Access Type	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PQEN	15	Low-battery prequalification mode enable.	0x0: PQEN disabled. 0x1: PQEN enabled.
LSEL	14	Inductor selection.	0x0: 0.47µH 0x1: 2.0µH
Reserved	13:12	Reserved, Do not modify.	Reserved
RECYCLE_EN	11	BAT to SYS over-current or DISIBS event recycle option do not modify.	Reserved
FCHGTIME	10:8	Fast-Charge timer setting. The Fast-Charge timer starts at the end of Trickle and the beginning of CC Fast-Charge.	0x0: Disabled 0x1: 3hr 0x2: 4hr 0x3: 5hr 0x4: 6hr 0x5: 7hr 0x6: 8hr 0x7: 10hr
DISIBS	6	BATT to SYS FET disable control to power cycle SYS. Auto cleared to 0.	0x0: BATT to SYS FET is controlled by the power path state machine. 0x1: SYS hard reset. QBAT FET is forced off, and SYS is discharged for 150ms.
WDTEN	4	Watchdog timer enable.	0x0: WDTEN disabled. 0x1: WDTEN enabled.
MODE	3:0	Smart power selector configuration.	0x0, 0x1: Battery Only. Buck is off. 0x4: Charger disabled. Buck is on to supply SYS. 0x5: Charger is controlled by step/JEITA charging algorithm. 0x8, 0x9: Reverse Boost to BYP. 0xA, 0xB: OTG to CHGIN. 0x2, 0x3, 0x6, 0x7, 0xC, 0xD, 0xE, 0xF: N/A. No change.

nChgConfig1 (0xD1)

BIT	15	14	13	12	11	10	9	8
Field	–	MINVSYS[2:0]			B2SOVRC[3:0]			
Reset	–	0b101			0xE			
Access Type	–	Write, Read			Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	OTG_ILIM[1:0]		–	–	–	–	–	–
Reset	0b11		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MINVSYS	14:12	Minimum system regulation voltage.	0x0: 3.0V 0x1: 3.1V 0x2: 3.2V 0x3: 3.3V 0x4: 3.4V 0x5: 3.5V 0x6: 3.6V 0x7: 3.7V Settings below 3.4V ends trickle charge at V_{BATT} 2.7V. Settings above 3.4V ends trickle charge at V_{BATT} 3.1V.
B2SOVRC	11:8	BATT to SYS discharge over-current threshold.	0x0: Disabled 0x1: 3.0A 0x2: 3.5A 0x3: 4.0A 0x4: 4.2A 0x5: 4.4A 0x6: 4.5A 0x7: 4.6A 0x8: 4.8A 0x9: 5.0A 0xa: 5.2A 0xb: 5.4A 0xc: 5.6A 0xd: 5.8A 0xe: 6.0A 0xf: 6.2A
OTG_ILIM	7:6	CHGIN output current limit.	0x0: 0.5A 0x1: 0.9A 0x2: 1.2A 0x3: 1.5A

nChgConfig2 (0xD2)

BIT	15	14	13	12	11	10	9	8
Field	WD_QBATOFF	REGTEMP[3:0]				FSW[1:0]		FSHIP_MODE
Reset	0b0	0x9				0b10		0b0
Access Type	Write, Read	Write, Read				Write, Read		Write, Read
BIT	7	6	5	4	3	2	1	0
Field	B2SOVRC_DTC	SLOWLX[1:0]		DIS_AICL	–	–	WDTCLR[1:0]	
Reset	0b0	0b00		0b0	–	–	0b00	
Access Type	Write, Read	Write, Read		Write, Read	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WD_QBATOFF	15	QBAT FET control under watchdog condition.	0x0: When watchdog timer expires, turn off only the charger.

BITFIELD	BITS	DESCRIPTION	DECODE
			0x1: When watchdog timer expires, turn off buck, charger, QBAT switch and cycle SYS power for 150ms.
REGTEMP	14:11	Junction temperature thermal regulation. The charger's target current limit starts to foldback, and the TREG bit is set if the junction temperature is greater than the REGTEMP setpoint.	0x0: 85ºC 0x1: 90ºC 0x2: 95ºC 0x3: 100ºC 0x4: 105ºC 0x5: 110ºC 0x6: 115ºC 0x7: 120ºC 0x8: 125ºC 0x9: 130ºC
FSW	10:9	Switching frequency options.	0x0: 3MHz 0x1: 2MHz 0x2: 1.5MHz 0x3: Reserved
FSHIP_MODE	8	Factory ship mode.	0x0: No factory ship mode. 0x1: Send MAX77972 in factory ship mode in up to 175.8ms.
B2SOVRC_DTC	7	BAT to SYS over-current protection debounce time.	0x0: 6ms (minimum) 0x1: 100ms (minimum)
SLOWLX	6:5	LX slope control options.	0x0: Fastest LX slope without control. 0x1: Slower LX slope. 0x2: Further slower LX slope. 0x3: Slowest LX slope.
DIS_AICL	4	Disable AICL	0x0: AICL loop is not disabled. 0x1: AICl loop is disabled.
WDTCLR	1:0	Watchdog timer clear. Writing 0x1 to clear the watchdog timer when the watchdog timer is enabled. The watchdog timer needs to be clear periodically within the 80s.	0x0, 0x2, or 0x3: The watchdog timer is not cleared. 0x1: The watchdog timer is cleared.

nChgConfig3 (0xD3)

BIT	15	14	13	12	11	10	9	8
Field	–	VBYPSET[6:0]						
Reset	–	0b0000001						
Access Type	–	Write, Read						
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved	CHGIN_ILIM[6:0]						
Reset	0b0	0b0010011						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
VBYPSET	14:8	VBYP target output voltage in reverse boost mode.	0: 5.0V 1: 5.1V 2: 5.2V 3: 5.3V 4: 5.4V 0x5 to 0x3f: 5.5V
Reserved	7	Reserved, do not modify, keep this at 0x0.	Reserved
CHGIN_ILIM	6:0	CHGIN input current limit. 7-bit adjustment from 100mA to 3.2A in 25mA steps. Note that the first 4 codes are all 100mA.	0x0 to 0x3: 100mA 0x4 to 0x7F: (CHGIN_ILIM + 1) x 25mA

nChgConfig4 (0xD4)

BIT	15	14	13	12	11	10	9	8
Field	CHGIN_INLIM_Gate	SDPMaxCurr[1:0]		CDPMaxCurr	DCDCpl	DCPDet3A	–	CHGDETEN
Reset	0b0	0b00		0b0	0b1	0b0	–	0b1
Access Type	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	–	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	NO_AUTOISET	DATAMUX	Reserved	VCHGIN_REG[1:0]		INLIM_CLK[1:0]		DISKIP
Reset	0b0	0b0	0b1	0b00		0b10		0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_INLIM_Gate	15	CHGIN_INLIM control options.	0x0: No gating of CHGIN_INLIM setting by BC1.2 FSM. 0x1: Gate changes in CHGIN_ILIM until BC1.2 FSM is completed.
SDPMaxCurr	14:13	SDP non-standard Type-C cable control. Requires CHGIN_INLIM_Gate = 0x1.	0x0: No modification of CHGIN_INLIM. 0x1: CHGIN_INLIM = 500mA (0x0F). 0x2: CHGIN_INLIM = 1A (0x1E). 0x3: CHGIN_INLIM = 1.5A (0x2D).
CDPMaxCurr	12	CDP non-standard Type-C control. Requires CHGIN_INLIM_Gate = 0x1.	0x0: No modification of CHGIN_INLIM. 0x1: CHGIN_INLIM = 1.5A (0x2D).
DCDCpl	11	Data contact detection time out.	0x0: 2s 0x1: 900ms
DCPDet3A	10	3A DCP Detection.	0x0: DCPDet3A disabled. 0x1: DCPDet3A enabled.
CHGDETEN	8	When set to 1, enables BC1.2.	0x0: BC1.2 does not run. 0x1: BC1.2 runs automatically when CHGIN is valid.
NO_AUTOISET	7	Disable USBC auto input current limit setting.	0x0: The charger input current limit is set by the USBC register (USB_INLIM). 0x1: The charger input current limit is set by the charger register (CHGIN_INLIM).

BITFIELD	BITS	DESCRIPTION	DECODE
DATAMUX	6	Set to 0 to enable the push button reset on the DATAMUX pin. Set to 1 to enable the USB data mux function on the DATAMUX pin.	0x0: Push the button reset, and factory ship mode is on, DATAMUX is off. 0x1: DATAMUX on, push button reset off.
Reserved	5	Reserved, Do not modify.	Reserved
VCHGIN_REG	4:3	AICL loop CHGIN voltage threshold. The CHGIN to GND Minimum Turn-On Threshold (VCHGIN_UVLO) also scales with this adjustment.	0x0: VCHGIN_REG = 4.5V and VCHGIN_UVLO = 4.7V. 0x1: VCHGIN_REG = 4.6V and VCHGIN_UVLO = 4.8V. 0x2: VCHGIN_REG = 4.7V and VCHGIN_UVLO = 4.9V. 0x3: VCHGIN_REG = 4.85V and VCHGIN_UVLO = 5.05V.
INLIM_CLK	2:1	Input current limit soft start clock.	0x0: 8µs 0x1: 256µs 0x2: 1024µs 0x3: 4096µs
DISKIP	0	Charger skip mode disable.	0x0: Auto skip mode. 0x1: Disable skip mode.

nChgConfig5 (0xD5)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	–	RestartChg	DeepShip	ChgEnable	CCDetEn
Reset	–	–	–	–	0b0	0b0	0b1	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RestartChg	3	Restart step charging from step 0.	0x0: No step charging restart. 0x1: Restart step charging from step 0 within 176ms. Auto clear to 0.
DeepShip	2	DeepShip mode.	0x0: No DeepShip mode. 0x1: Enter DeepShip mode within 176ms.
ChgEnable	1	Force charger to stop within upto 176ms.	0x0: Disable charger (effective within 176ms). 0x1: Enable charger (effective within 176ms). JEITA and step-charging algorithm controls charger.
CCDetEn	0	Enable CC pin detection	0x0: CCDetEn disabled 0x1: CCDetEn enabled

ChgDetails00 (0xD6)

BIT	15	14	13	12	11	10	9	8
Field	AICL_OK	CHGIN_OK	–	CHG_OK	BAT_OK	Reserved	–	BYP_OK
Reset	0b0	0b0	–	0b0	0b0	0b0	–	0b0
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	–	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	–	CHGIN_DTLS[1:0]		–	–	–	–	CHGEN
Reset	–	0b00		–	–	–	–	0b0
Access Type	–	Write, Read		–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_OK	15	AICL loop status indicator.	0x0: AICL mode. 0x1: Not in AICL mode.
CHGIN_OK	14	CHGIN input status indicator.	0x0: CHGIN voltage is invalid. 0x1: CHGIN voltage is valid.
CHG_OK	12	Charger status indicator.	0x0: Charger is suspended : 1. CHGEN pin low; 2. Charger time out; 3. Thermal shutdown; 4. Watchdog timer expires. 0x1: Charger is charging or charger is turned off. charger can be turned off with conditions: 1. nChgConfig5.ChgEnable bit is set to 0; 2. Battery is full; 3. TooHot/TooCold charger suspension.
BAT_OK	11	Battery status indicator.	0x0: BAT_DTLS is not 0x3, 0x4, 0x7. 0x1: BAT_DTLS is 0x3, 0x4 or 0x7.
Reserved	10	Reserved, Do not modify.	Reserved
BYP_OK	8	Bypass status indicator.	0x0: BYP_DTLS is not 0x0. 0x1: BYP_DTLS is 0x0.
CHGIN_DTLS	6:5	Charger input status	0x0: VCHGIN is invalid.VCHGIN rising: VCHGIN < VCHGIN_UVLO. VCHGIN falling: VCHGIN < VCHGIN_REG (AICL). 0x1: VCHGIN is invalid.VCHGIN < VSYS + 0.2V and VCHGIN > VCHGIN_UVLO. 0x2: VCHGIN is invalid.VCHGIN > VCHGIN_OVLO. 0x3: VCHGIN is valid.VCHGIN > VCHGIN_UVLO and VCHGIN > VSYS + 0.2V and VCHGIN < VCHGIN_OVLO.
CHGEN	0	ChgEn pin status.	0x0: ChgEn pin low. 0x1: ChgEn pin high.

ChgDetails01 (0xD7)

BIT	15	14	13	12	11	10	9	8
Field	TREG	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
Reset	0b0	0b000			0x0			

Access Type	Write, Read	Write, Read			Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	BAT_dis_OC	–	–	–	BYP_DTLS[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TREG	15	Temperature regulation status.	0x0: The junction temperature is less than the threshold set by nChgConfig2.REGTEMP and the full charge current limit are available. 0x1: The junction temperature is greater than the threshold set by nChgConfig2.REGTEMP and the charge current limit may be folded back to reduce power dissipation.
BAT_DTLS	14:12	Battery details.	0x0: CHGEN pin is pulled low. 0x1: $V_{BATT} < V_{TRICKLE}$. This condition is also reported in the CHG_DTLS as 0x0. 0x2: The battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery or something else. Charging has been suspended, and the charger is in its timer fault mode. This condition is also reported in the CHG_DTLS as 0x06. 0x3: The battery is okay, and its voltage is greater than the minimum system voltage, QBAT FET is on, and V_{SYS} is approximately equal to V_{BATT}. 0x4: The battery is okay, but its voltage is low: $V_{TRICKLE} < V_{BATT} < V_{SYSMIN}$. QBAT is operating like an LDO to regulate VSYS to nChgConfig1.MINVSYS. 0x5: The battery voltage has been greater than the battery overvoltage flag threshold (ChargingVoltage + 200mV) for the last 30ms. Note that this flag is only generated when there is a valid CHGIN input. 0x7: Battery only.
CHG_DTLS	11:8	Charger details	0x0: Charger is in dead-battery prequalification or low-battery prequalification mode. $V_{BATT} < V_{TRICKLE}$ and $T_J < T_{SHDN}$. 0x1: The charger is in fast-charge constant current mode. $V_{TRICKLE} < V_{BATT} < V_{BATTREG}$ and $T_J < T_{SHDN}$. 0x2: The charger is in fast-charge constant voltage mode. V_{BATT} = ChargingVotlage and $T_J < T_{SHDN}$. 0x6: Charger timer fault. 0x7: CHGEN pin is low. 0x8: The charger is off, the charger input is invalid and/or the charger is disabled. 0x9: The charger is in reverse boost mode and supplies power from the battery to the BYP pin. 0xA: Charger under die overtemperature protection. $T_J > T_{SHDN}$. 0xB: The charger is off because the watchdog timer expired. 0xF: The charger is in OTG mode and supplies power from the battery to CHGIN. Other: Reserved.
BAT_dis_OC	7	Battery over-discharge protection (discharge current > 6A by default). Stay set to 1 until AP writes 0 to clear.	0x0: Battery over-discharge not detected. 0x1: Battery over-discharge detected. Write 0 to BAT_dis_OC to clear.

BITFIELD	BITS	DESCRIPTION	DECODE
BYP_DTLS	3:0	BYP and revers boost details.	0: The BYP node is okay. 1: The BYP to CHGIN switch (OTG switch) current limit was reached within the last 37.5ms. The current limit is set by nChgConfig1.OTG_ILIM. Valid only in OTG mode (nChgConfig0.MODE = 0xA or 0xB). Write BYP_DTLS[1] to 0 to clear the fault. 2: The BYP reverse boost converter overcurrent and condition persists for 30ms. 4: The BYP buck converter has a negative overcurrent. 8: VBYP reached the VBYPSET target in reverse boost mode. Other: Reserved.

UsbDetails (0xD8)

BIT	15	14	13	12	11	10	9	8
Field	–	CHGTYP[1:0]		PRCHGTYP[2:0]			CC_CURR[1:0]	
Reset	–	0b00		0b000			0b00	
Access Type	–	Write, Read		Write, Read			Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	–	USB_INLIM[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
CHGTYP	14:13	Readback BC1.2 standard adaptor detection.	0x0: No adaptor found. 0x1: SDP (500mA input current). 0x2: CDP (1.5A input current). 0x3: DCP (1.5A input current).
PRCHGTYP	12:10	Readback type of proprietary adaptor detected.	0x0: No proprietary charger. 0x1: Samsung 2A. 0x2: Apple 500mA. 0x3: Apple 1A. 0x4: Apple 2A. 0x5: Apple 12W (Input current = 2.5A). 0x6: DCP 3A. 0x7: Unknown.
CC_CURR	9:8	Readback CC current capability detection.	0x0: Not connected. 0x1: 0.5A 0x2: 1.5A 0x3: 3.0A
USB_INLIM	6:0	Readback USB adaptor input current limit.	0x13: 0.5A 0x27: 1.0A 0x3b: 1.5A 0x4f: 2.0A 0x5f: 2.4A 0x77: 3.0A

VByp (0xDB)

BIT	15	14	13	12	11	10	9	8
Field	VByp[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	VByp[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VByp	15:0	The ADC output of BYP voltage.	Type = voltage Scalar = 0.625 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 40959.375 MinimumScaled = 0.0

Command (0xE0)

BIT	15	14	13	12	11	10	9	8
Field	CMD[15:8]							
Reset	0x0000							
Access Type	Write, Read, Ext							
BIT	7	6	5	4	3	2	1	0
Field	CMD[7:0]							
Reset	0x0000							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION	DECODE
CMD	15:0	Command register to issue reset/wakeup commands.	0x000F: Hardware reset. 0xC400: Same as SOFT_POR.

USR (0xE1)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	NLOCK
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
NLOCK	0	Lock for the non-volatile portion of the RAM. Write 0 twice consecutively to set it to 0. Write 1 twice consecutively to set it to 1.	0x0: Not locked. 0x1: Locked.

VFOCV (0xFB)

BIT	15	14	13	12	11	10	9	8
Field	VFOCV[15:8]							
Reset	0x0000							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	VFOCV[7:0]							
Reset	0x0000							

Access Type	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VFOCV	15:0	Calculated open-circuit voltage of the cell as determined by the voltage fuel gauge. This value is used in other internal calculations.	Type = voltage Scalar = 78.125 Lsbunit = µV Offset = 0.0 signed = False MaximumScaled = 5119921.875 MinimumScaled = 0.0

VFSOC (0xFF)

BIT	15	14	13	12	11	10	9	8
Field	VFSOC[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	VFSOC[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VFSOC	15:0	Calculated present state-of-charge of the battery according to the voltage fuel gauge.	Type = percent Scalar = 0.00390625 Lsbunit = % Offset = 0.0 signed = False MaximumScaled = 255.99609375 MinimumScaled = 0.0

FG_DEBUG_MAP

Device address (8-bit): 0x6E
Device address (7-bit): 0x37

ADDRESS	NAME	MSB							LSB
FG_DEBUG									
0x19D	nFilterCfg[15:8]	–	–	TEMP[2:0]			MIX[3:1]		
	nFilterCfg[7:0]	MIX[0]	VOLT[2:0]			CURR[3:0]			
0x1A6	nRComp0[15:8]	nRComp0[15:8]							
	nRComp0[7:0]	nRComp0[7:0]							
0x1A7	nTempCo[15:8]	nTempCo[15:8]							
	nTempCo[7:0]	nTempCo[7:0]							
0x1AB	nRGain[15:8]	RGain1[7:0]							
	nRGain[7:0]	RGain2[3:0]				SusToPeakRatio[3:0]			
0x1B6	nRelaxCfg[15:8]	LOAD[6:0]							dV[4]
	nRelaxCfg[7:0]	dV[3:0]				dt[3:0]			
0x1B7	nConvgCfg[15:8]	RepLow[3:0]				VoltLowOff[4:1]			
	nConvgCfg[7:0]	VoltLowOff[0]	MinSlopeX[3:0]				RepL_per_stage[2:0]		
0x1BA	nNVCfg2[15:8]	–	enSC	–	–	–	–	–	–
	nNVCfg2[7:0]	–	–	–	–	–	–	–	–
0x1BB	nHibCfg[15:8]	EnHib	HibEnterTime[2:0]			HibThreshold[3:0]			
	nHibCfg[7:0]	–	–	–	HibExitTime[1:0]		HibScalar[2:0]		
0x1C2	nChgCfg0[15:8]	StepChgMode	–	–	–	–	–	–	–
	nChgCfg0[7:0]	–	–	–	–	–	–	–	–
0x1C4	nStepCurr[15:8]	StepCurr4[3:0]				StepCurr3[3:0]			
	nStepCurr[7:0]	StepCurr2[3:0]				StepCurr1[3:0]			
0x1C5	nStepVolt[15:8]	StepVolt0[3:0]				StepVolt1[3:0]			
	nStepVolt[7:0]	StepVolt2[3:0]				StepVolt3[3:0]			
0x1C7	nAlrtCfg[15:8]	–	–	–	–	–	–	–	–
	nAlrtCfg[7:0]	–	–	–	–	–	Edge	–	–
0x1C8	nCGain[15:8]	CGain[9:2]							

ADDRESS	NAME	MSB							LSB
	nCGain[7:0]	CGain[1:0]		COff[5:0]					
0x1C9	nADCCfg[15:8]	Reserved[2:0]			–	Reserved	Reserved	Reserved	Reserved
	nADCCfg[7:0]	R100	–	–	ThEn	–	RsnsEn	Reserved	Reserved
0x1CA	nThermCfg[15:8]	nThermCfg[15:8]							
	nThermCfg[7:0]	nThermCfg[7:0]							
0x1CC	nVChgCfg1[15:8]	WarmChargeVolt[3:0]				RoomChargeVolt[7:4]			
	nVChgCfg1[7:0]	RoomChargeVolt[3:0]				CoolChargeVolt[3:0]			
0x1CD	nVChgCfg2[15:8]	Hot2ChargeVolt[3:0]				Hot1ChargeVolt[3:0]			
	nVChgCfg2[7:0]	Cold1ChargeVolt[3:0]				Cold2ChargeVolt[3:0]			
0x1CE	nIChgCfg1[15:8]	WarmChargeCurr[4:0]					RoomChargeCurr[5:3]		
	nIChgCfg1[7:0]	RoomChargeCurr[2:0]			CoolChargeCurr[4:0]				
0x1CF	nIChgCfg2[15:8]	Hot2ChargeCurr[3:0]				Hot1ChargeCurr[3:0]			
	nIChgCfg2[7:0]	Cold1ChargeVolt[3:0]				Cold2ChargeCurr[3:0]			
0x1D1	nTPrtTh1[15:8]	Tcold2[3:0]				Tcold1[3:0]			
	nTPrtTh1[7:0]	Tcool[3:0]				Troom[3:0]			
0x1D5	nTPrtTh2[15:8]	Ttoohot[3:0]				Thot2[3:0]			
	nTPrtTh2[7:0]	Thot1[3:0]				Twarm[3:0]			
0x1D6	nProtMiscTh[15:8]	–	–	–	–	–	–	–	–
	nProtMiscTh[7:0]	CurrDet[3:0]				–	–	–	–
0x1D7	nProtCfg[15:8]	–	–	FullEn	–	–	–	–	–
	nProtCfg[7:0]	–	–	–	–	–	–	–	–
0x1DC	nDelayCfg[15:8]	–	–	FullTimer[2:0]			–	–	–
	nDelayCfg[7:0]	–	–	–	–	–	–	–	–
0x1E1	nScOcvLim[15:8]	OCV_Low_Lim[8:1]							
	nScOcvLim[7:0]	OCV_Low_Lim[0]	OCV_Delta[6:0]						
0x1E3	nDesignVoltage[15:8]	Vminsys[7:0]							

ADDRESS	NAME	MSB							LSB
	nDesignVoltage[7:0]	–	–	–	–	–	–	–	–

Register Details

nFilterCfg (0x19D)

The nFilterCfg register sets the averaging time period for all A/D readings, for mixing OCV results and coulomb count results. It is recommended that these values are not changed unless absolutely required by the application. Table 14 shows the FilterCfg register format.

BIT	15	14	13	12	11	10	9	8
Field	–	–	TEMP[2:0]			MIX[3:1]		
Reset	–	–	0b001			0xD		
Access Type	–	–	Write, Read			Write, Read		
BIT	7	6	5	4	3	2	1	0
Field	MIX[0]	VOLT[2:0]			CURR[3:0]			
Reset	0xD	0b010			0x4			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TEMP	13:11	Sets the time constant for the AvgTA register. The default POR value of 0001b gives a time constant of 1.5min.	AvgTA time constant = 45s × 2^{TEMP}
MIX	10:7	Sets the time constant for the mixing algorithm. The default POR value of 1101b gives a time constant of 12.8 hours.	Mixing Period = 45s × $2^{(MIX-3)}$
VOLT	6:4	Sets the time constant for the AvgVCell register. The default POR value of 010b gives a time constant of 45.0s.	AvgVCell time constant = 45s × $2^{(VOLT-2)}$
CURR	3:0	Sets the time constant for the AvgCurrent register. The default POR value of 0100b gives a time constant of 5.625s.	AvgCurrent time constant = 45s × $2^{(CURR-7)}$

nRComp0 (0x1A6)

BIT	15	14	13	12	11	10	9	8
Field	nRComp0[15:8]							
Reset	0x07A0							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	nRComp0[7:0]							
Reset	0x07A0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
nRComp0	15:0	Critical characterization information to compute the open circuit voltage of a cell under loaded conditions.

nTempCo (0x1A7)

BIT	15	14	13	12	11	10	9	8
Field	nTempCo[15:8]							
Reset	0x223E							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	nTempCo[7:0]							
Reset	0x223E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
nTempCo	15:0	Temperature compensation information for the nRComp0 register value.

nRGain (0x1AB)

BIT	15	14	13	12	11	10	9	8
Field	RGain1[7:0]							
Reset	0x80							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	RGain2[3:0]				SusToPeakRatio[3:0]			
Reset	0x8				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RGain1	15:8	Gain resistance used for maximum peak current and power calculation. The range of RGain1 is between 80~120%.	80% + 0.15625% × RGain1
RGain2	7:4	Gain resistance used for sustained peak current and power calculation. The range of RGain2 is between 60~140%.	60% + 5% × RGain2
SusToPeakRatio	3:0	Used to calculate the maximum ratio between SPPCurrent to MPPCurrent.	SPPCurrent (MAX) = MPPCurrent × (0.75 - SusToPeakRatio × 0.04).

nRelaxCfg (0x1B6)

The RelaxCfg register defines how the IC detects if the cell is in a relaxed state.

BIT	15	14	13	12	11	10	9	8
Field	LOAD[6:0]							dV[4]
Reset	0b0000100							0b00011
Access Type	Write, Read							Write, Read
BIT	7	6	5	4	3	2	1	0
Field	dV[3:0]				dt[3:0]			
Reset	0b00011				0x9			

Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOAD	15:9	Sets the threshold against which the AvgCurrent register is compared. The AvgCurrent register must remain below this threshold value for the cell to be considered unloaded.	Type = current Scalar=5 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = False MaximumScaled = 635.0 MinimumScaled = 0.0
dV	8:4	Sets the threshold against which VCell is compared. If the cell's voltage changes by less than dV over two consecutive periods set by dT, it is considered relaxed.	Type = voltage Scalar = 1.25 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 38.75 MinimumScaled = 0.0.
dt	3:0	Sets the time period over which change in VCell is compared against nRelaxCfg.dV. If the cell voltage changes by less than nRelaxCfg.dV over two consecutive periods set by nRelaxCfg.dt, the cell is considered relaxed.	0: Relaxation is never detected. 0x1 to 0xF: 175.8ms x $2^{(dt-1)}$

nConvgCfg (0x1B7)

The nConvgCfg register configures the operation of the converge-to-empty feature. Setting nConvgCfg = 0x0000 disables the converge-to-empty functionality.

BIT	15	14	13	12	11	10	9	8
Field	RepLow[3:0]				VoltLowOff[4:1]			
Reset	0x2				0b00100			
Access Type	Write, Read				Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	VoltLowOff[0]	MinSlopeX[3:0]				RepL_per_stage[2:0]		
Reset	0b00100	0x8				0b001		
Access Type	Write, Read	Write, Read				Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RepLow	15:12	Sets the threshold below which RepCap begins to bend upwards.	Type = percent Scalar = 2.0 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 30.0 MinimumScaled = 0.0.

BITFIELD	BITS	DESCRIPTION	DECODE
VoltLowOff	11:7	When the AvgVCell register value drops below the VEmpty + VoltLow threshold, RepCap begins to converge towards 0%.	Type = voltage Scalar = 20.0 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 620.0 MinimumScaled = 0.0.
MinSlopeX	6:3	Sets the amount of slope-shallowing which occurs when RepSOC falls below RepLow.	Type = percent Scalar = 0.0625 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 0.9375 MinimumScaled = 0.0.
RepL_per_stage	2:0	Adjusts the RepLow threshold setting depending on the present learning stage using the following equation. This allows the RepLow threshold to be at higher levels for earlier learning states. RepLow Threshold = RepLow Field Setting + RemainingStages x RepL_per_stage.	Type = percent Scalar = 1.0 Lsbunit = % Offset = 0.0 Signed = False MaximumScaled = 7.0 MinimumScaled = 0.0

nNVCfg2 (0x1BA)

BIT	15	14	13	12	11	10	9	8
Field	–	enSC	–	–	–	–	–	–
Reset	–	0b0	–	–	–	–	–	–
Access Type	–	Write, Read	–	–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
enSC	14	Enable special chemistry model. Set this bit to 1 if a special chemistry model is used. This bit enables the use of nScOcvLim.	0x0: enSC disabled. 0x1: enSC enabled.

nHibCfg (0x1BB)

The nHibCfg register controls hibernate mode functionality. The IC enters hibernate mode if the measured system current falls below the HibThreshold setting for longer than the HibEnterTime delay. While in hibernate mode, the IC reduces its operating current by slowing down its task period as defined by the HibScalar setting. The IC automatically

returns to an active mode of operation if current readings go above the HibThreshold setting for longer than the HibExitTime delay.

BIT	15	14	13	12	11	10	9	8
Field	EnHib	HibEnterTime[2:0]			HibThreshold[3:0]			
Reset	0b1	0b000			0x9			
Access Type	Write, Read	Write, Read			Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	HibExitTime[1:0]		HibScalar[2:0]		
Reset	–	–	–	0b01		0b001		
Access Type	–	–	–	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
EnHib	15	Enable Hibernate Mode. When set to 1, the IC enters hibernate mode if conditions are met. When set to 0, the IC always remains in active mode of operation.	0x0: Hibernate disabled. 0x1: Hibernate enabled.
HibEnterTime	14:12	Sets the time period that consecutive current readings must remain below the HibThreshold value before the IC enters hibernate mode as defined by the following equation. The default HibEnterTime value of 000b causes the IC to enter hibernate mode if all current readings are below the HibThreshold for a period of 5.625 seconds, but the IC could enter hibernate mode as quickly as 2.812 seconds.	$2.812s \times 2^{(HibEnterTime)} <$ Hibernate Mode Entry Time $< 2.812s \times 2^{(HibEnterTime + 1)}$
HibThreshold	11:8	Sets the threshold level for entering or exiting hibernate mode. The threshold is calculated as a fraction of the full capacity of the cell.	Hibernate Mode Threshold(mA) = (FullCap(mAh)/0.8 hours)/$2^{(HibThreshold)}$
HibExitTime	4:3	Sets the required time period of consecutive current readings above the HibThreshold value before the IC exits hibernate and returns to active mode of operation.	Hibernate Mode Exit Time(s) = (HibExitTime + 1) x 702ms x $2^{(HibScalar)}$
HibScalar	2:0	Sets the task period while in hibernate mode.	Hibernate Mode Task Period(s) = 702ms x $2^{(HibScalar)}$

nChgCfg0 (0x1C2)

Various charging settings.

BIT	15	14	13	12	11	10	9	8

Field	StepChgMode	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
StepChgMode	15	Step-charging mode.	0x0: CV step-charging. 0x1: CC step-charging.

nStepCurr (0x1C4)

Step charge current at room temperature. Any step can be disabled by setting the associated nibbles to 0. Disable step charging by setting both nStepCurr and nStepVolt to 0x0000. Note: Setting nStepCurr and nStepVolt does not disable the JEITA charging control algorithm.

BIT	15	14	13	12	11	10	9	8
Field	StepCurr4[3:0]				StepCurr3[3:0]			
Reset	0x5				0x5			
Access Type	Write, Read				Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	StepCurr2[3:0]				StepCurr1[3:0]			
Reset	0x5				0x5			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
StepCurr4	15:12	Step4 room-temperature charge current. Read the ChargingCurrent register for real-time charging in the current setting.	$I_{CHG[Step4][Room]} = I_{CHG[Step3][Room]}$ - StepCurr4 × 50mA

BITFIELD	BITS	DESCRIPTION	DECODE
StepCurr3	11:8	Step3 room-temperature charge current. Read the ChargingCurrent register for real-time charging in the current setting.	$I_{CHG[Step3][Room]} = I_{CHG[Step2][Room]}$ - StepCurr3 × 50mA
StepCurr2	7:4	Step2 room-temperature charge current. Read the ChargingCurrent register for real-time charging in the current setting.	$I_{CHG[Step2][Room]} = I_{CHG[Step1][Room]}$ - StepCurr2 × 50mA
StepCurr1	3:0	Step1 room-temperature charge current. Read the ChargingCurrent register for real-time charging in the current setting.	$I_{CHG[Step1][Room]} = I_{CHG[Step0][Room]}$ - StepCurr1 × 100mA

nStepVolt (0x1C5)

Step charge voltage at room temperature. Any step can be disabled by setting the associated nibbles to 0. Disable step charging by setting both nStepCurr and nStepVolt to 0x0000. **Note:** Setting nStepCurr and nStepVolt does not disable the JEITA charging control algorithm.

BIT	15	14	13	12	11	10	9	8
Field	StepVolt0[3:0]				StepVolt1[3:0]			
Reset	0x5				0x5			
Access Type	Write, Read				Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	StepVolt2[3:0]				StepVolt3[3:0]			
Reset	0x5				0x5			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
StepVolt0	15:12	Step0 room temperature charge voltage. Read the ChargingVoltage register for real-time charging voltage settings.	$V_{CHG[Step0][Room]} = V_{CHG[Step1][Room]}$ - StepVolt0 × 10mV
StepVolt1	11:8	Step1 room temperature charge voltage. Read the ChargingVoltage register for real-time charging voltage settings.	$V_{CHG[Step1][Room]} = V_{CHG[Step2][Room]}$ - StepVolt1 × 10mV
StepVolt2	7:4	Step2 room temperature charge voltage. Read the ChargingVoltage register for real-time charging voltage settings.	$V_{CHG[Step2][Room]} = V_{CHG[Step3][Room]}$ - StepVolt2 × 10mV

BITFIELD	BITS	DESCRIPTION	DECODE
StepVolt3	3:0	Step3 room temperature charge voltage. Read the ChargingVoltage register for real-time charging voltage settings.	$V_{CHG[Step3][Room]} = V_{CHG[Step4][Room]}$ - StepVolt3 × 10mV

nAlrtCfg (0x1C7)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	Edge	–	–
Reset	–	–	–	–	–	0b0	–	–
Access Type	–	–	–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Edge	2	ALRT edge trigger of ModelGauge battery voltage, current and temperature alerts.	0x0: Edge disabled. 0x1: Edge enabled.

nCGain (0x1C8)

The nCGain register adjusts the gain and offset of the current measurement result. The current measurement A/D is factory-trimmed to data sheet accuracy without the need for the user to make further adjustments. The recommended default for the nCGain register is 0x4000, which applies no adjustments to the Current register reading. For specific application requirements, the CGain and COff values can be used to adjust readings as follows: Current register = (current A/D reading x (CGain/256)) + COff.

BIT	15	14	13	12	11	10	9	8
Field	CGain[9:2]							
Reset	0b0100000000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0

Field	CGain[1:0]	COff[5:0]
Reset	0b0100000000	0b000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CGain	15:6	The recommended default value of CGain = 0x100 corresponds to a gain of 1.	CGain (hex) = (MeasuredCurrent/ReportedCurrent) x 0x0100
COff	5:0	Battery current offset adjustment. However, It is normally not recommended to calibrate COff. COff = 0 is recommended for most applications.	Type = current Scalar = 0.15625 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 0.0 Signed = True MaximumScaled = 51198.4375 MinimumScaled = -51200.0

nADCCfg (0x1C9)

ADC configurations.

BIT	15	14	13	12	11	10	9	8
Field	Reserved[2:0]			–	Reserved	Reserved	Reserved	Reserved
Reset	0b000			–	0b0	0b0	0b0	0b0
Access Type	Write, Read			–	Write, Read	Write, Read	Write, Read	Write, Read
BIT	7	6	5	4	3	2	1	0
Field	R100	–	–	ThEn	–	RsnsEn	Reserved	Reserved
Reset	0b0	–	–	0b1	–	0b0	0b0	0b0
Access Type	Write, Read	–	–	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	15:13	Reserved, Do not modify.	Reserved
Reserved	11	Reserved, Do not modify.	Reserved
Reserved	10	Reserved, Do not modify.	Reserved
Reserved	9	Reserved, Do not modify.	Reserved
Reserved	8	Reserved, Do not modify.	Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
R100	7	THM internal 10kΩ or 100kΩ pullup selection.	0x0: 10kΩ pullup 0x1: 100kΩ pullup
ThEn	4	Thermistor or die temperature selection for Temperature register.	0x0: DieTemp 0x1: THM Thermistor (Config.Tex = 0x0, default) or external temperature overwrite (Config.Tex = 0x1)
RsnsEn	2	Internal or external battery current sense selection.	0x0: Internal R_{SENSE} (10mΩ equivalent). 0x1: External R_{SENSE}. Recommend to use 10mΩ.
Reserved	1	Reserved, Do not modify.	Reserved
Reserved	0	Reserved, Do not modify.	Reserved

nThermCfg (0x1CA)

BIT	15	14	13	12	11	10	9	8
Field	nThermCfg[15:8]							
Reset	0x71BE							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	nThermCfg[7:0]							
Reset	0x71BE							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
nThermCfg	15:0	External NTC thermistors generate a temperature-related voltage that is measured at the THM pin. Set the nThermCfg register to compensate the thermistor for the accurate temperature translation. Common NTC thermistors with their associated Beta value and the nThermCfg value are in the decode chart. The thermistors in the table translate within ±1°C from -40°C to +85°C. For other thermistors, use the equation in the external table to translate within ±2.5°C. Use Beta 25°C to 85°C. Other 10kΩ: nThermCfg = 7000h + (3245919/Beta - 512) Other 100kΩ: nThermCfg = 3000h + (3245919/Beta - 512) Use Beta 25°C to 85°C.	0x71de: Murata NCP15XH103F03RC 0x91c3: Semitec 103AT-2 0x5183: TDK B57560G1103 7003 0x48eb: Murata NCU15WF104F6SRC 0x8d9: NTC TH11-4H104F 0x58ef: TDK NTCG064EF104FTBX

nVChgCfg1 (0x1CC)

Step4 charge voltage over JEITA temperature regions. The charge voltages over JEITA temperature zones are set relative to the RoomChargeVoltage based on the temperature. To disable JEITA charge voltage reduction, set RoomChargeVoltage as desired and configure the other settings with a value of 0x0.

BIT	15	14	13	12	11	10	9	8
Field	WarmChargeVolt[3:0]				RoomChargeVolt[7:4]			
Reset	0x5				0x5A			
Access Type	Write, Read				Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	RoomChargeVolt[3:0]				CoolChargeVolt[3:0]			
Reset	0x5A				0x5			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
WarmChargeVolt	15:12	Warm temperature step4 charge voltage.	$V_{CHG[Step4][Warm]} = V_{CHG[Step4][Room]}$ - WarmChargeVolt × 10mV
RoomChargeVolt	11:4	Sets the nominal room-temperature charging voltage in the room-temperature region and step 4 charging voltage (Highest-charging voltage).	$V_{CHG[Step4][Room]}$ = 3.4V + (RoomChargeVolt × 10mV)
CoolChargeVolt	3:0	Cool temperature step4 charge voltage.	$V_{CHG[Step4][Cool]} = V_{CHG[Step4][Room]}$ - CoolChargeVolt × 10mV

nVChgCfg2 (0x1CD)

Step4 charge voltage over JEITA temperature regions. The charge voltages over JEITA temperature zones are set relative to the RoomChargeVoltage based on the temperature. To disable JEITA charge voltage reduction, set RoomChargeVoltage as desired and configure the other settings with a value of 0x0.

BIT	15	14	13	12	11	10	9	8
Field	Hot2ChargeVolt[3:0]				Hot1ChargeVolt[3:0]			
Reset	0x5				0x5			
Access Type	Write, Read				Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	Cold1ChargeVolt[3:0]				Cold2ChargeVolt[3:0]			

Reset	0x5	0x5
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Hot2ChargeVolt	15:12	Hot2 temperature step4 charge voltage.	$V_{CHG[Step4][Hot2]} = V_{CHG[Step4][Hot1]}$ - Hot2ChargeVolt × 10mV
Hot1ChargeVolt	11:8	Hot1 temperature step4 charge voltage.	$V_{CHG[Step4][Hot1]} = V_{CHG[Step4][Warm]}$ - Hot1ChargeVolt × 10mV
Cold1ChargeVolt	7:4	Cold1 temperature step4 charge voltage.	$V_{CHG[Step4][Cold1]} = V_{CHG[Step4][Cool]}$ - Cold1ChargeVolt × 10mV
Cold2ChargeVolt	3:0	Cold2 temperature step4 charge voltage.	$V_{CHG[Step4][Cold2]} = V_{CHG[Step4][Cold1]}$ - Cold2ChargeVolt × 10mV

nIChgCfg1 (0x1CE)

Step0 charging current over JEITA temperature regions. The charge current over JEITA temperature zones is set relative to the RoomChargeCurr based on the temperature. To disable JEITA charge current reduction, set RoomChargeCurr as desired and set the other thresholds with a value of 0.

BIT	15	14	13	12	11	10	9	8
Field	WarmChargeCurr[4:0]					RoomChargeCurr[5:3]		
Reset	0b00100					0b011111		
Access Type	Write, Read					Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	RoomChargeCurr[2:0]			CoolChargeCurr[4:0]				
Reset	0b011111			0b01000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
WarmChargeCurr	15:11	Warm temperature step0 charge current.	$I_{CHG[Step0][Warm]} = I_{CHG[Step0][Room]}$ – WarmChargeCurr × 50mA
RoomChargeCurr	10:5	Room temperature step0 charge current.	$I_{CHG[Step0][Room]}$ = (RoomChargeCurr +1) × 50mA
CoolChargeCurr	4:0	Cool temperature step0 charge current.	$I_{CHG[Step0][Cool]} = I_{CHG[Step0][Room]}$ – CoolChargeCurr × 50mA

nIChgCfg2 (0x1CF)

Step0 charging current over JEITA temperature regions. The charge current over JEITA temperature zones is set relative to the RoomChargeCurr based on the temperature. To disable JEITA charge current reduction, set RoomChargeCurr as desired and set the other thresholds with a value of 0.

BIT	15	14	13	12	11	10	9	8
Field	Hot2ChargeCurr[3:0]				Hot1ChargeCurr[3:0]			
Reset	0x5				0x5			
Access Type	Write, Read				Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	Cold1ChargeVolt[3:0]				Cold2ChargeCurr[3:0]			
Reset	0x5				0x5			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Hot2ChargeCurr	15:12	Hot2 temperature step0 charge current.	$I_{CHG[Step0][Hot2]} = I_{CHG[Step0][Hot1]}$ – Hot2ChargeCurr × 50mA
Hot1ChargeCurr	11:8	Hot1 temperature step0 charge current.	$I_{CHG[Step0][Hot1]} = I_{CHG[Step0][Warm]}$ – Hot1ChargeCurr × 50mA
Cold1ChargeVolt	7:4	Cold1 temperature step0 charge current.	$I_{CHG[Step0][Cold1]} = I_{CHG[Step0][Cool]}$ – Cold1ChargeCurr × 50mA
Cold2ChargeCurr	3:0	Cold2 temperature step0 charge current.	$I_{CHG[Step0][Cold2]} = I_{CHG[Step0][Cold1]}$ – Cold2ChargeCurr × 50mA

nTPrtTh1 (0x1D1)

JEITA temperature regions thresholds (Tcold2, Tcold1, Tcool, Troom).

BIT	15	14	13	12	11	10	9	8
Field	Tcold2[3:0]				Tcold1[3:0]			
Reset	0x3				0x1			
Access Type	Write, Read				Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	Tcool[3:0]				Troom[3:0]			
Reset	0x1				0x2			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Tcold2	15:12	Cold2 temperature threshold. Set to 0x0 to skip this zone.	$T_{COLD2} = T_{COLD1}$ - (Tcold2 + 1) × 2.5°C
Tcold1	11:8	Cold1 temperature threshold. Set to 0x0 to skip this zone.	$T_{COLD1} = T_{COOL}$ - (Tcold1 + 1) × 2.5°C
Tcool	7:4	Cool temperature threshold. Set to 0x0 to skip this zone.	$T_{COOL} = T_{ROOM}$ - (Tcool + 1) × 2.5°C
Troom	3:0	Room temperature threshold.	T_{ROOM} = Troom × 2.5°C + 10°C

nTPrtTh2 (0x1D5)

JEITA temperature regions thresholds (Twarm, Thot1, Thot2, Ttoohot).

BIT	15	14	13	12	11	10	9	8
Field	Ttoohot[3:0]				Thot2[3:0]			
Reset	0x7				0x1			
Access Type	Write, Read				Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	Thot1[3:0]				Twarm[3:0]			
Reset	0x1				0x5			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Ttoohot	15:12	TooHot temperature threshold. Set to 0x0 to skip this zone.	$T_{TOOHOT} = T_{HOT2}$ + (Ttoohot + 1) × 2.5°C
Thot2	11:8	Hot2 temperature threshold. Set to 0x0 to skip this zone.	$T_{HOT2} = T_{HOT1}$ + (Thot2 + 1) × 2.5°C
Thot1	7:4	Hot1 temperature threshold. Set to 0x0 to skip this zone.	$T_{HOT1} = T_{WARM}$ + (Thot1 + 1) × 2.5°C
Twarm	3:0	Warm temperature threshold. Highly recommend to set to a higher than 0x1 to keep enough room temperature zone.	$T_{WARM} = T_{ROOM}$ + (Twarm + 1) × 2.5°C

nProtMiscTh (0x1D6)

The nProtMiscTh register sets a few miscellaneous protection thresholds.

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	CurrDet[3:0]				–	–	–	–
Reset	0x2				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CurrDet	7:4	Threshold to detect discharging and charging events from the device perspective. If (current > CurrDet) charging; if (current < -CurrDet) discharging.	Type = current Scalar = 2.5 Lsbunit = mA (10mΩ R_{SENSE}) Offset = 2.5 Signed = False MaximumScaled = 40.0 MinimumScaled = 2.5

nProtCfg (0x1D7)

The Protection Configuration register contains enable bits for various protection functions.

BIT	15	14	13	12	11	10	9	8
Field	–	–	FullEn	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
FullEn	13	Full Charge Protection Enable. If the full charge protection feature is enabled, charging stops at full.	0x0: FullEn disabled. 0x1: FullEn enabled.

nDelayCfg (0x1DC)

Set nDelayCfg to configure debounce timers for various protection faults. A fault state is concluded only if the condition persists throughout the duration of the timer.

BIT	15	14	13	12	11	10	9	8
Field	–	–	FullTimer[2:0]			–	–	–
Reset	–	–	0b101			–	–	–
Access Type	–	–	Write, Read			–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
FullTimer	13:11	Set FullTimer to configure the timing for full detection. When charge-termination conditions are detected, and after the timeout, the FET turns off (if the feature is enabled).	0x0: 33s to 40s 0x1: 45s to 67s 0x2: 1.5min to 2.25min 0x3: 3min to 4.5min 0x4: 6min to 9min 0x5: 12min to 18min 0x6: 24min to 36min 0x7: 72min to 1.6hr

nScOcvLim (0x1E1)

This register only has usage when ModelCfg.ModelID is selected as 0x6 or nNVCfg2.enSC = 1 (LiFePO4).

BIT	15	14	13	12	11	10	9	8
Field	OCV_Low_Lim[8:1]							
Reset	0b000000000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0

Field	OCV_Low_Lim[0]	OCV_Delta[6:0]
Reset	0b000000000	0b0000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OCV_Low_Lim	15:7	Lower limit for the OCV keep-out region.	Type = voltage Scalar = 5.0 Lsbunit = mV Offset = 2560 Signed = False MaximumScaled = 5120.0 MinimumScaled = 2560.0
OCV_Delta	6:0	Delta between lower and upper limits for the OCV keep-out region.	Type = voltage Scalar = 2.5 Lsbunit = mV Offset = 0 Signed = False MaximumScaled = 320.0 MinimumScaled = 0.0

nDesignVoltage (0x1E3)

BIT	15	14	13	12	11	10	9	8
Field	Vminsys[7:0]							
Reset	0x96							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Vminsys	15:8	Minimum system voltage used for dynamic power calculation. Generates MinSysVoltage value.	Type = voltage Scalar = 20.0 Lsbunit = mV Offset = 0.0 Signed = False MaximumScaled = 5100.0 MinimumScaled = 0.0

PCB Layout Guidance

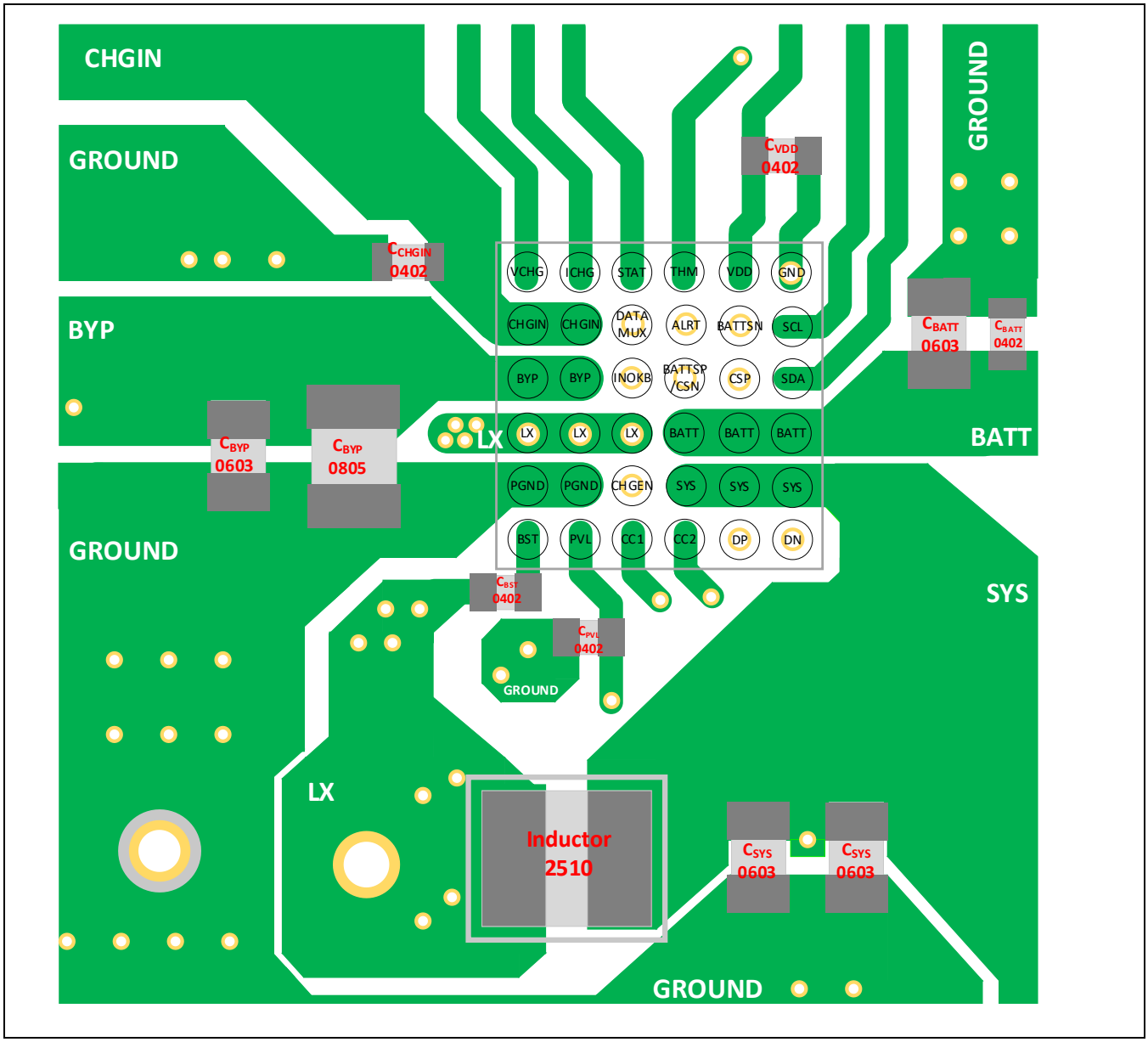


Figure 30. PCB Layout Guidance

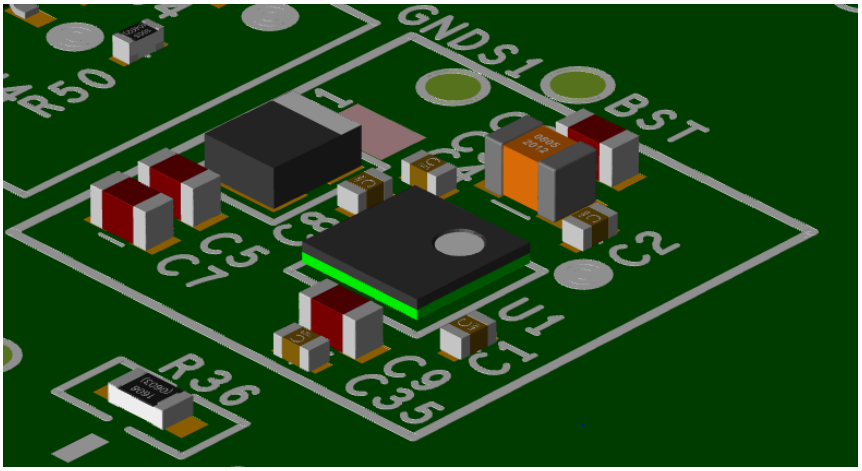
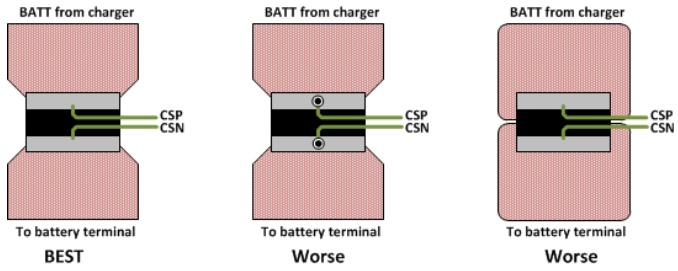


Figure 31. PCB Component Placement

Table 12. PCB Layout Guidance

PIN	LAYOUT GIUIDANCE
CHGIN	Input from Charger Source. Connect to CHGIN plane with decent wide trace. Recommend having ground plane close to CHGIN plane to achieve low impedance return path. Bypass to PGND with the capacitor, place the CHGIN capacitor (C_{CHGIN}) close to the CHGIN pin. Proximity to the IC provides a stable supply for the internal circuitry.
BYP	System Power Connection. Connect to BYP plane with decent wide trace. Prefer having ground plane close to BYP plane to achieve low impedance return path. Bypass to PGND with the capacitor, place the BYP capacitors (C_{BYP}) close to the BYP pin. Proximity to the IC provides a stable supply for the internal circuitry.
LX	Switching Node. Connect Inductor between LX and SYS. If running the LX trace in another layer to go around the GND trace (see *Figure 30*), use at least four vias to connect different layers in the PCB. Make the LX node area large enough to carry current but also minimize the area to lower interference. Avoid routing any other sensitive trace getting close or crossing over.
BST	Provides Drive to High-Side Internal nMOS. Place a bootstrap capacitor (C_{BST}) between the BST pin and LX trace, keeping it close to the BST pin. Proximity to the IC provides a stable supply for the internal circuitry. Avoid routing any other sensitive trace getting close or crossing over.
PVL	Output of On-chip LDO. Noisy rail due to bootstrap operation. Bypass with the PVL capacitor (C_{PVL}) and place the capacitor close to the BST pin. Proximity to the IC provides a stable supply for the internal circuitry.
SYS	System power path. Connect to the SYS plane with a decent-wide trace. Bypass with capacitors. Place the SYS capacitors (C_{SYS}) close to the inductor.
BATT	Battery power connection. Connect to BATT plane with decent wide trace. Bypass with capacitors (C_{BATT}).
VDD	Always-on regulator path. Bypass with the capacitor (C_{VDD}).
CC1	USB Type-C connections. No special consideration. Use parallel traces for CC1 and CC2.
CC2	
DP	Common positive/negative output. Connect to Type-C or micro-USB connector. No special consideration. Use parallel traces for DP and DN.
DN	
CHGEN	Charge enable. No special consideration.

<table>
<tr><td>CSP</td><td rowspan="3">MAX77972 can operate with or without external sense resistor.
Using external sense resistor:
CSP and CSN sense the voltage across the external current sense resistor. The sense voltage across CSR is a few tens mV at best since the resistance is very low, 5mV with 1A. CSP and CSN are recommended to be probed the center of pad without via on the pad. Route the CSP and CSN with dedicated traces with sufficient width in parallel from the sense resistor to the IC.
 

Using internal resistor:
BATTSP and BATTSN are remote sensing pins that are used to regulate charge voltage. BATTSP shares the same pin with CSN. These signals sense battery voltage for fuel gauging. It should be routed clearly without overlapping power traces and digital logic signals in upper or lower layer.</td></tr>
<tr><td>BATTSP/CSN</td></tr>
<tr><td>BATTSN</td></tr>
<tr><td>INOKB</td><td>Charger input valid. No special consideration.</td></tr>
<tr><td>ALRT</td><td>Alert open drain output. No special consideration.</td></tr>
<tr><td>DATAMUX</td><td>External USB data mux select. No special consideration.</td></tr>
<tr><td>SDA</td><td rowspan="2">I2C Lines. Route two parallel traces for SDA and SCL.</td></tr>
<tr><td>SCL</td></tr>
<tr><td>THM</td><td>10kΩ/100kΩ Thermistor Input. Place the thermistor in the general proximity of the controller.</td></tr>
<tr><td>STAT</td><td>Open drain charge status indication output. No special consideration.</td></tr>
<tr><td>ICHG</td><td>Current configuration. Place the ICHG programming resistor in the general proximity of the controller.</td></tr>
<tr><td>VCHG</td><td>Voltage configuration. Place the VCHG programming resistor in the general proximity of the controller.</td></tr>
<tr><td>GND</td><td rowspan="2">Care should be taken to connect PGND since it is switching node ground of Charger BUCK. It should be connected to ground of SYS capacitors and BYP capacitors and connected to ground plane directly without sharing other grounds.</td></tr>
<tr><td>PGND</td></tr>
</table>

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX77972EWX+	-40°C to +85°C	36 WLP
MAX77972EWX+T	-40°C to +85°C	36 WLP

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	04/24	Initial release	—