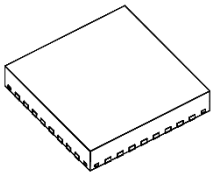
Bi-CMOS Linear Integrated Circuit Silicon Monolithic

TB67Z830SFTG TB67Z830HFTG
TB67Z833SFTG TB67Z833HFTG
TB67Z850SFTG TB67Z850HFTG
TB67Z853SFTG TB67Z853HFTG

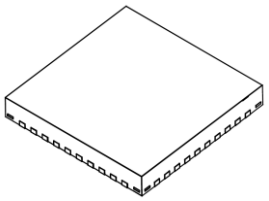
3-Phase Gate Driver

TB67Z830SFTG/830HFTG
TB67Z850SFTG/850HFTG



P-VQFN32-0505-0.50-007

TB67Z833SFTG/833HFTG
TB67Z853SFTG/853HFTG



P-WQFN40-0606-0.50-003

Weight:
P-VQFN32-0505-0.50-007 0.065g (typ.)
P-WQFN40-0606-0.50-003 0.09g (typ.)

1. Overview

TB67Z830xFTG/833xFTG/850xFTG/853xFTG includes three half-bridge gate drivers that can drive N-channel MOSFETs. It supports a wide voltage range from 8 V to 75 V and has a drive capability of up to 1 A source current and 2 A sink current.
TB67Z833xFTG/853xFTG has three built-in amplifiers with adjustable gain, which can be used for shunt current sensing.

2. Applications

Brushless DC Motors, Fans, Pumps, Power Tools, etc.

3. Features

- Gate driver for high-side and low-side N-channel MOSFET
- Adjustable gate drive capability
  - Source current capability: 10 mA to 1 A (peak)
  - Sink current capability: 20 mA to 2 A (peak)
- Operating Voltage Range: 8 to 75 V
- Built-in Voltage Regulator
- Built-in 3-channel current sense amplifiers (TB67Z833xFTG/853xFTG)
- SPI and Hardware interface
- 6-PWM Input Mode, 3-PWM Input Mode, Hall Input Mode, and Independent PWM Mode
- Standby Mode (1 μA @ VM = 24 V)
- Built-in Protection Function
  Under voltage lockout, Charge pump under voltage lockout, Gate driver voltage monitoring, Over current detection, High temperature warning, Thermal shutdown, and Flag Output (nFAULT)

Start of commercial production
2024-08

Table 3.1 Comparison table for each product

Product Name	Built-in regulator voltage	Number of current sense amplifiers	Interface	Package
TB67Z830HFTG	3.3 V	0 ch	Hardware	P-VQFN32-0505-0.50-007
TB67Z830SFTG			SPI	
TB67Z833HFTG		3 ch	Hardware	P-WQFN40-0606-0.50-003
TB67Z833SFTG			SPI	
TB67Z850HFTG	5 V	0 ch	Hardware	P-VQFN32-0505-0.50-007
TB67Z850SFTG			SPI	
TB67Z853HFTG		3 ch	Hardware	P-WQFN40-0606-0.50-003
TB67Z853SFTG			SPI	

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4. Block Diagram

Some of the functional blocks, circuits or constants labels in the block diagram may have been omitted or simplified for clarity.

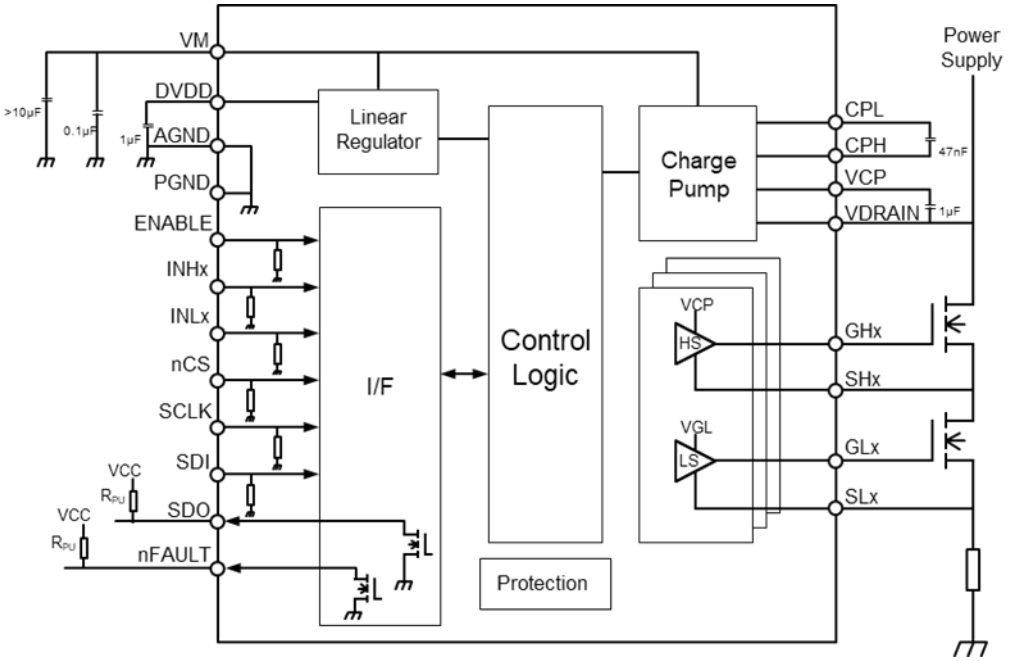


Fig. 4.1 TB67Z830SFTG/TB67Z850SFTG

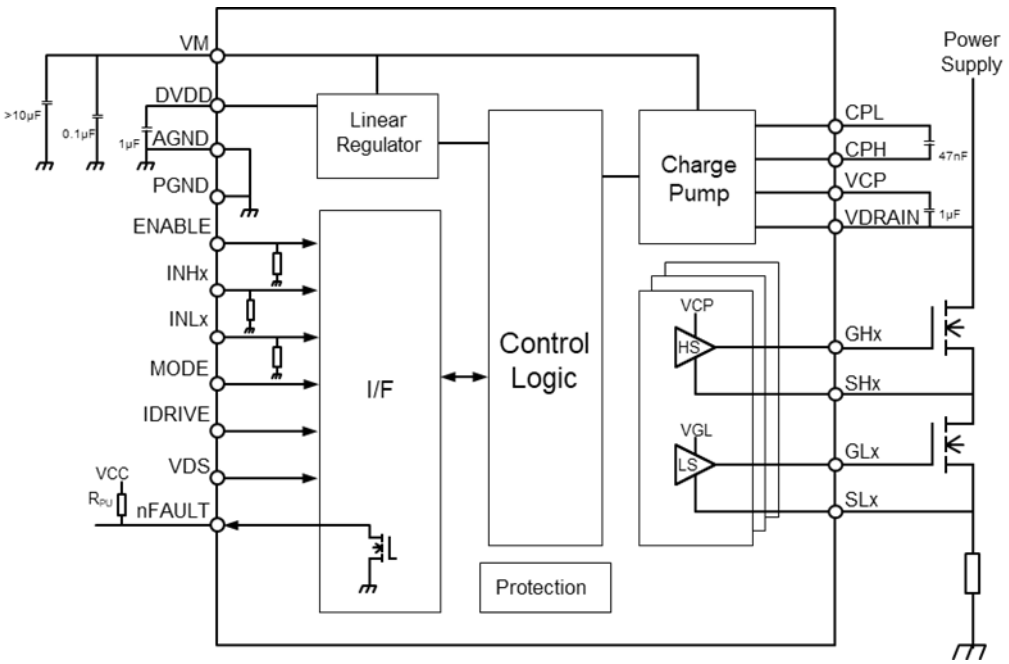


Fig. 4.2 TB67Z830HFTG/TB67Z850HFTG

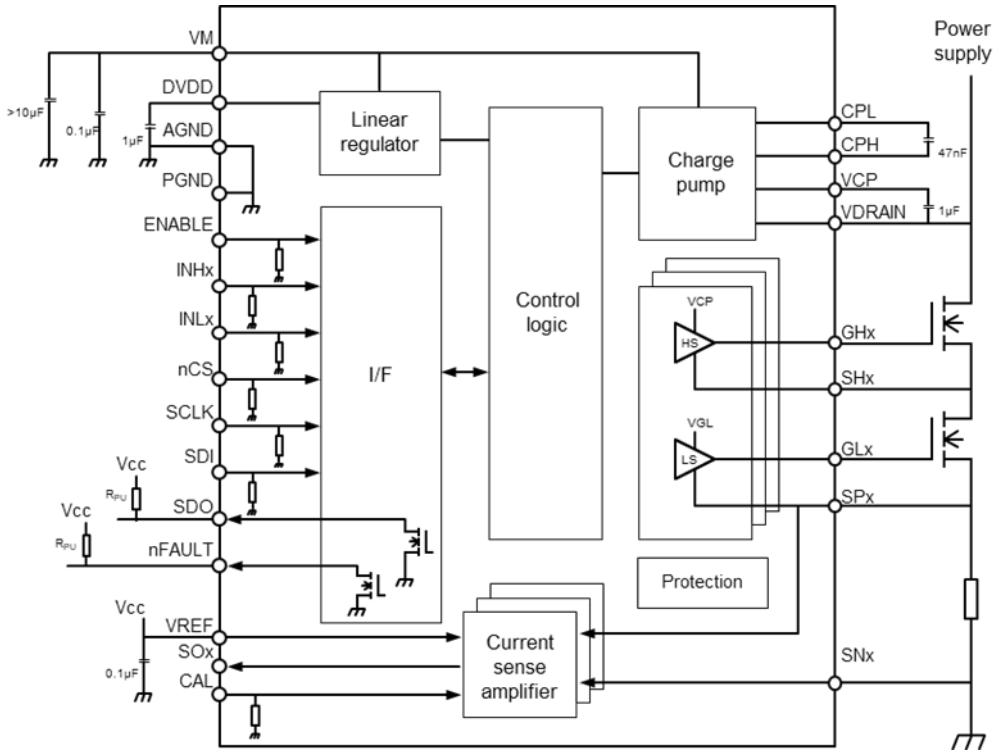


Fig. 4.3 TB67Z833SFTG/TB67Z853SFTG

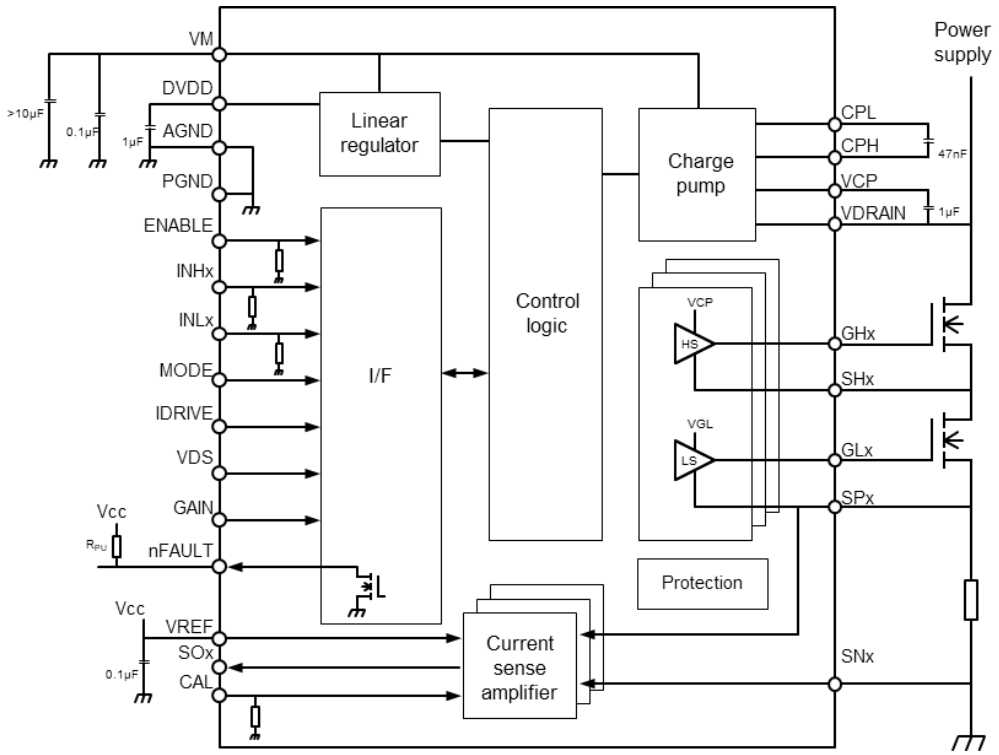
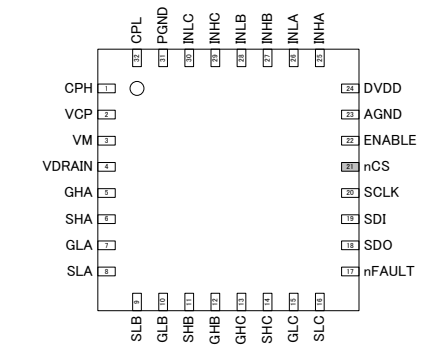
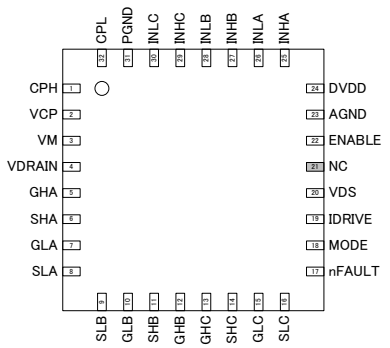


Fig. 4.4 TB67Z833HFTG/TB67Z853HFTG

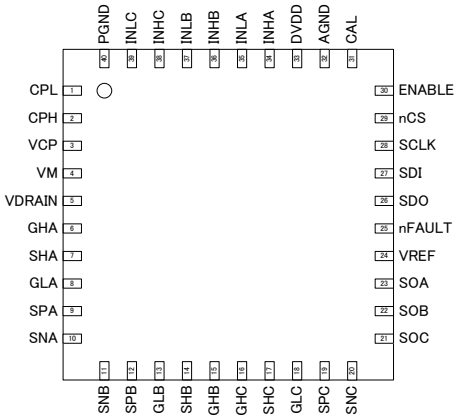
5. Pin Assignments



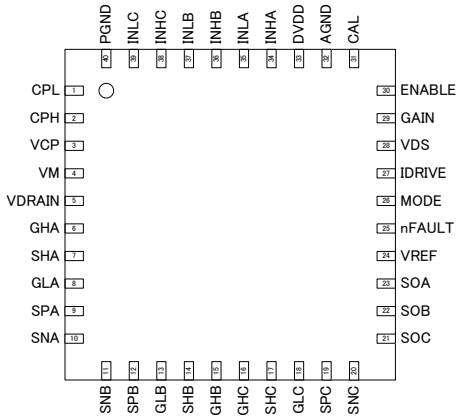
TB67Z830SFTG / TB67Z850SFTG



TB67Z830HFTG / TB67Z850HFTG



TB67Z833SFTG / TB67Z853SFTG



TB67Z833HFTG / TB67Z853HFTG

Fig. 5.1 Pin Assignments (top view)

6. Pin Description

Table 6.1 Pin Description for TB67Z830H/SFTG, TB67Z850H/SFTG

Pin No.	Pin name		Type	Pin description
1	CPH	TB67Z8x0H / SFTG	Power	Flying capacitor for charge pump pin
2	VCP	TB67Z8x0H / SFTG	Power	Reservoir capacitor for charge pump pin
3	VM	TB67Z8x0H / SFTG	Power	Power supply pin
4	VDRAIN	TB67Z8x0H / SFTG	Input	High-side drain voltage monitoring pin Charge pump reference voltage monitoring pin
5	GHA	TB67Z8x0H / SFTG	Output	High-side gate drive output pin (A channel)
6	SHA	TB67Z8x0H / SFTG	Input	High-side source voltage monitoring pin (A channel)
7	GLA	TB67Z8x0H / SFTG	Output	Low-side gate drive output pin (A channel)
8	SLA	TB67Z8x0H / SFTG	Input	Low-side source voltage monitoring pin (A channel)
9	SLB	TB67Z8x0H / SFTG	Input	Low-side source voltage monitoring pin (B channel)
10	GLB	TB67Z8x0H / SFTG	Output	Low-side gate drive output pin (B channel)
11	SHB	TB67Z8x0H / SFTG	Input	High-side source voltage monitoring pin (B channel)
12	GHB	TB67Z8x0H / SFTG	Output	High-side gate drive output pin (B channel)
13	GHC	TB67Z8x0H / SFTG	Output	High-side gate drivel output pin (C channel)
14	SHC	TB67Z8x0H / SFTG	Input	High-side source voltage monitoring pin (C channel)
15	GLC	TB67Z8x0H / SFTG	Output	Low-side gate drive output pin (C channel)
16	SLC	TB67Z8x0H / SFTG	Input	Low-side source voltage monitoring pin (C channel)
17	nFAULT	TB67Z8x0H / SFTG	Open Drain	Flag signal output pin
18	MODE	TB67Z8x0HFTG	Input	PWM control mode setting pin
	SDO	TB67Z8x0SFTG	Open Drain	Serial communication data output pin
19	IDRIVE	TB67Z8x0HFTG	Input	Gate drive current setting pin
	SDI	TB67Z8x0SFTG	Input	Serial communication data input pin
20	VDS	TB67Z8x0HFTG	Input	VDS monitoring threshold voltage setting pin
	SCLK	TB67Z8x0SFTG	Input	Serial communication clock pin
21	NC	TB67Z8x0HFTG	NC	Non-connection
	nCS	TB67Z8x0SFTG	Input	Serial communication chip select pin
22	ENABLE	TB67Z8x0H / SFTG	Input	Enable pin
23	AGND	TB67Z8x0H / SFTG	Ground	Analog ground
24	DVDD	TB67Z8x0H / SFTG	Power	Regulator voltage output pin
25	INHA	TB67Z8x0H / SFTG	Input	High-side gate control pin (A channel)
26	INLA	TB67Z8x0H / SFTG	Input	Low-side gate control pin (A channel)
27	INHB	TB67Z8x0H / SFTG	Input	High-side gate control pin (B channel)
28	INLB	TB67Z8x0H / SFTG	Input	Low-side gate control pin (B channel)
29	INHC	TB67Z8x0H / SFTG	Input	High-side gate control pin (C channel)
30	INLC	TB67Z8x0H / SFTG	Input	Low-side gate control pin (C channel)
31	PGND	TB67Z8x0H / SFTG	Ground	Power ground
32	CPL	TB67Z8x0H / SFTG	Power	Flying capacitor for charge pump pin

Note: When the SLx pins are not in use, do not leave them open but connect them to the ground.

Table 6.2 Pin Description for TB67Z833H/SFTG, TB67Z853H/SFTG

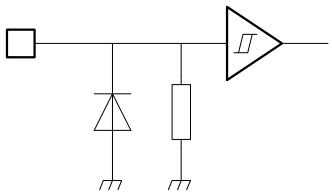
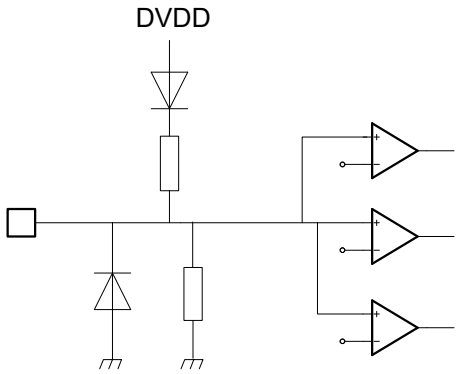
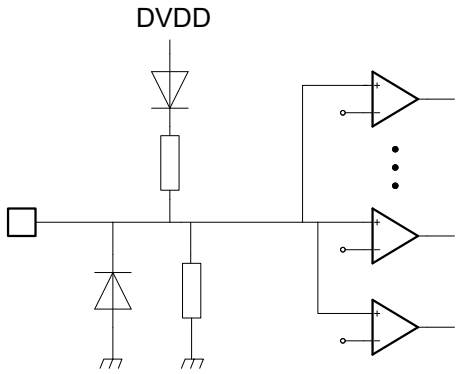
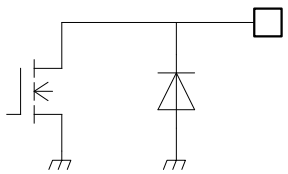
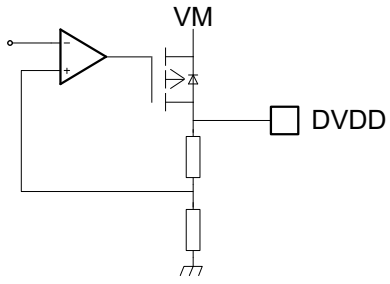
Pin No.	Pin name		Type	Pin description
1	CPL	TB67Z8x3H / SFTG	Power	Flying capacitor for charge pump pin
2	CPH	TB67Z8x3H / SFTG	Power	Flying capacitor for charge pump pin
3	VCP	TB67Z8x3H / SFTG	Power	Reservoir capacitor for charge pump pin
4	VM	TB67Z8x3H / SFTG	Power	Power supply pin
5	VDRAIN	TB67Z8x3H / SFTG	Input	High-side drain voltage monitoring pin Charge pump reference voltage monitoring pin
6	GHA	TB67Z8x3H / SFTG	Output	High-side gate drive output pin (A channel)
7	SHA	TB67Z8x3H / SFTG	Input	High-side source voltage monitoring pin (A channel)
8	GLA	TB67Z8x3H / SFTG	Output	Low-side gate drive output pin (A channel)
9	SPA	TB67Z8x3H / SFTG	Input	Low-side source voltage monitoring pin (A channel) Current sense amplifier input pin (A channel)
10	SNA	TB67Z8x3H / SFTG	Input	Current sense amplifier input pin (A channel)
11	SNB	TB67Z8x3H / SFTG	Input	Current sense amplifier input pin (B channel)
12	SPB	TB67Z8x3H / SFTG	Input	Low-side source voltage monitoring pin (B channel) Current sense amplifier input pin (B channel)
13	GLB	TB67Z8x3H / SFTG	Output	Low-side gate drive output pin (B channel)
14	SHB	TB67Z8x3H / SFTG	Input	High-side source voltage monitoring pin (B channel)
15	GHB	TB67Z8x3H / SFTG	Output	High-side gate drive output pin (B channel)
16	GHC	TB67Z8x3H / SFTG	Output	High-side gate drive output pin (C channel)
17	SHC	TB67Z8x3H / SFTG	Input	High-side source voltage monitoring pin (C channel)
18	GLC	TB67Z8x3H / SFTG	Output	Low-side gate drive signal output pin (C channel)
19	SPC	TB67Z8x3H / SFTG	Input	Low-side source voltage monitoring pin (C channel) Current sense amplifier input pin (C channel)
20	SNC	TB67Z8x3H / SFTG	Output	Current sense amplifier input pin (C channel)
21	SOC	TB67Z8x3H / SFTG	Output	Current sense amplifier input pin (C channel)
22	SOB	TB67Z8x3H / SFTG	Output	Current sense amplifier input pin (B channel)
23	SOA	TB67Z8x3H / SFTG	Output	Current sense amplifier input pin (A channel)
24	VREF	TB67Z8x3H / SFTG	Power	Current sense amplifier power supply and reference voltage
25	nFAULT	TB67Z8x3H / SFTG	Open Drain	Flag signal output pin
26	MODE	TB67Z8x3HFTG	Input	PWM control mode setting pin
	SDO	TB67Z8x3SFTG	Open Drain	Serial communication data output pin
27	IDRIVE	TB67Z8x3HFTG	Input	Gate drive current setting pin
	SDI	TB67Z8x3SFTG	Input	Serial communication data input pin
28	VDS	TB67Z8x3HFTG	Input	VDS monitoring threshold voltage setting pin
	SCLK	TB67Z8x3SFTG	Input	Serial communication clock pin
29	GAIN	TB67Z8x3HFTG	Input	Current sense amplifier gain setting pin
	nCS	TB67Z8x3SFTG	Input	Serial communication chip select pin
30	ENABLE	TB67Z8x3H / SFTG	Input	Enable pin
31	CAL	TB67Z8x3H / SFTG	Input	Current sense amplifier offset calibration pin
32	AGND	TB67Z8x3H / SFTG	Ground	Analog ground

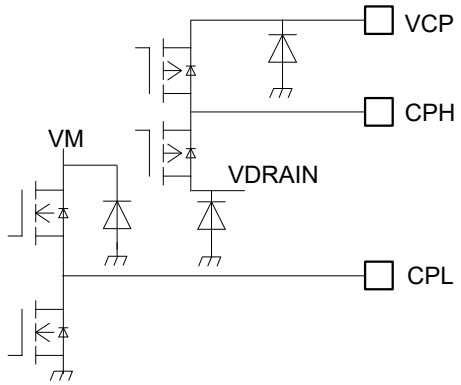
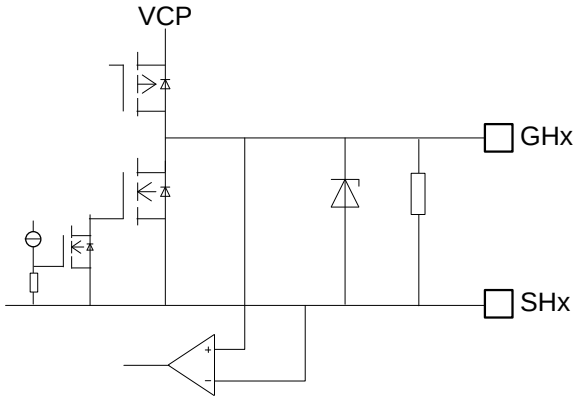
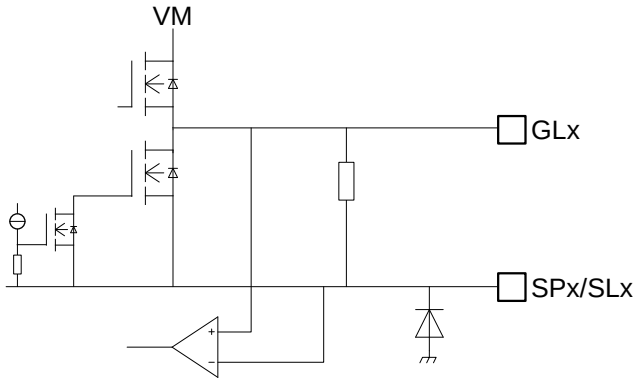
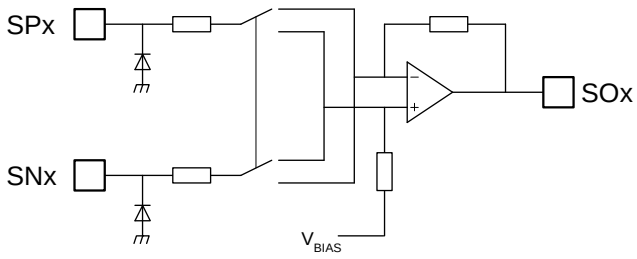
Table 6.2 Pin Description for TB67Z833H/SFTG, TB67Z853H/SFTG (continued)

Pin No.	Pin name		Type	Pin description
33	DVDD	TB67Z8x3H / SFTG	Power	Regulator voltage output pin
34	INHA	TB67Z8x3H / SFTG	Input	High-side gate control pin (A channel)
35	INLA	TB67Z8x3H / SFTG	Input	Low-side gate control pin (A channel)
36	INHB	TB67Z8x3H / SFTG	Input	High-side gate control pin (B channel)
37	INLB	TB67Z8x3H / SFTG	Input	Low-side gate control pin (B channel)
38	INHC	TB67Z8x3H / SFTG	Input	High-side gate control pin (C channel)
39	INLC	TB67Z8x3H / SFTG	Input	Low-side gate control pin (C channel)
40	PGND	TB67Z8x3H / SFTG	Ground	Power ground

Note: When the SPx pins are not in use, do not leave them open but connect them to the ground.

7. Equivalent Circuit

Pin name	Pin description	Equivalent circuit
INHx INLx ENABLE nCS SCLK SDI CAL	Digital input pin	
MODE GAIN	4-level input pin	
IDRIVE VDS	7-level input pin	
SDO nFAULT	Open drain output pin	
DVDD	Linear regulator pin	

Pin name	Pin description	Equivalent circuit
VCP CPH CPL	Charge pump pin	
GHx SHx	High-side gate driver pin	
GLx SPx/SLx	Low-side gate driver pin	
SPx SNx SOX	Current sense amplifier input output pin	

8. Absolute maximum ratings

Table 8.1 Absolute Maximum Ratings (Ta = 25 °C unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{VM}	-0.3 to 80	V
Differential voltage between GND pins (between PGND and AGND)		ΔV_G	-0.3 to 0.3	V
VDRAIN pin voltage		V_{VDR}	-0.3 to 80	V
VDRAIN voltage slew rate		SR_{VDR}	2	V/μs
Voltage regulator		V_{DVDD}	-0.3 to 6 (note 1)	V
Charge pump pin voltage (VCP, CPP)		V_{CP}	-0.3 to V_{VDR}+13.5 (note 1)	V
Charge pump pin voltage (CPM)		V_{CPM}	-0.3 to V_{VDR} (note 1)	V
Input voltage	ENABLE, MODE, VDS, GAIN, IDRIVE, CAL, INHx, INLx, nSCS, SCLK, SDI, SDO, nFAULT	V_{IN}	-0.3 to 6	V
	SHx (continuous)		-5 to V_{VDR} +5 (note 2)	V
	SHx (200 ns pulse)		-10 to V_{VDR} +10 (note 2)	V
	SLx (continuous)		-1 to 1 (note 3)	V
	SLx (200 ns pulse)		-5 to 5 (note 3)	V
	SPx, SNx (continuous)		-1 to 1 (note 3)	V
	SPx, SNx (200 ns pulse)		-5 to 5 (note 3)	V
	VREF		-0.3 to 6	V
Output Voltage	GHx (continuous)	V_{OUT}	-5 to V_{VCP}+0.5 (note 2)	V
	GHx (200 ns pulse)		-10 to V_{VCP}+0.5 (note 2)	V
	GHx – SHx		-0.3 to 13.5	V
	GLx (continuous)		-1 to 13.5 (note 3)	V
	GLx (200 ns pulse)		-5 to 13.5 (note 3)	V
	SOx		-0.3 to V_{VREF}+0.3	V
Output current	DVDD	I_{DVDD}	30 (note 4)	mA
Input current	nFAULT	I_{IN}	10	mA
Power dissipation	WQFN40	P_D	4.0 (note 5)	W
	VQFN32		3.1 (note 6)	
Junction temperature during operation		$T_{j(opr)}$	-40 to 150	°C
Storage temperature		T_{stg}	-55 to 150	°C

The absolute maximum ratings are standards that must not be exceeded even momentarily. Exceeding the rating(s) may cause destruction, degradation, or damage of device and may also cause destruction, damage, or degradation other than the device. Design the application so that the absolute Maximum ratings are not exceeded under any operating conditions. Use this device within the operating range described in this data sheet.

Note 1: DVDD, VCP, VCPP, and VCPM voltages are generated inside the device.
Do not apply any voltages externally.
Note 2: The SHx and GHx voltages are limited by the VCP voltage.
Design the voltages of (VCP-SHx) and (VCP-GHx) not to exceed the range from -0.5 to 96 V.
Note 3: GLx, SLx, SPx, and SNx voltages are limited by VM voltage. Design the voltages of (VM-GLx), (VM-SLx), (VM-SPx), and (VM-SNx) not to exceed the range from -0.5 V to 80 V.
Note 4: Output current may be limited by ambient temperature and mounting method.
Design the application so that the junction temperature is not exceeded.
Note 5: On PCB (JEDEC 4 layers) and Ta=25 °C. When Ta exceeds 25 °C, derating with 32 mW/°C is necessary.
Note 6: On PCB (JEDEC 4 layers) and Ta=25 °C. When Ta exceeds 25 °C, derating with 25 mW/°C is necessary.

9. Operating range

Table 9.1 Operating range (Ta = -40 to 125 °C unless otherwise specified)

Characteristics	Symbol	Min	Typ.	Max	Unit
VM supply voltage	V_{VM}	8	–	75	V
VDRAIN voltage	V_{VDR}	6	–	75	V
Input voltage	V_{IN}	0	–	5.5	V
Switching slew rate (SHx)	SR_{SH}	–	–	2	V/ns
PWM signal (INHx, INLx)	f_{PWM}	0	–	200 (note1)	kHz
High-side average drive current	I_{GATE_HS}	0	–	25 (note1)	mA
Low-side average drive current	I_{GATE_LS}	0	–	25 (note1)	mA
DVDD output current	I_{DVDD}	0	–	30 (note1)	mA
Open drain pull-up voltage	V_{OD}	0	–	5.5	V
Open drain sink current	I_{OD}	0	–	5	mA
VREF voltage	V_{VREF}	3	–	5.5	V
Operating ambient temperature	T_a	-40	–	125	°C

Note 1: Do not exceed absolute maximum ratings for the power dissipation and the junction temperature.

10. Electrical Characteristics

Table 10.1 Electrical Characteristics (at VM = VDRAIN= 12 V, Ta = 25 °C unless otherwise specified)

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
Power supply							
Power supply current	Normal operation	I_{VM}	VM = VDRAIN = 24 V, ENABLE = 3.3 V, INHx / INLx = 0 V H/W I/F: MODE = 0 V GAIN, MODE, IDRIVE, VDS = Open SPI I/F: default register setting	–	15	20	mA
		I_{VDRAIN}		–	4	6	mA
	Standby	I_{STBY} (I_{VM}+I_{VDRAIN})	VM = 8 to 75 V, VDRAIN = 8 to 75 V, ENABLE = 0 V T_j = -40 to 125 °C	–	–	1	μA
Wake up time		t_{WAKE}	Period from VM>V_{VMUP}, ENABLE=3.3 V to output Ready. Capacitor at DVDD: 1 μF Capacitor between VCP and VDRAIN: 1 μF	–	–	1	ms
Standby transition time		t_{STBY}	Period from ENABLE = 0 V to Standby mode. Capacitor at DVDD: 1 μF	–	–	1	ms
Reset time		t_{RESET}	Period from ENABLE = 0 V to error reset. f_{OSC} = 20 MHz	5	–	40	μs
DVDD voltage	TB67Z83x	V_{DVDD}	VM = 8 to 75 V, I_{OUT} = 0 to 30 mA	3	3.3	3.6	V
	TB67Z85x		VM = 8 to 75 V, I_{OUT} = 0 to 30 mA	4.5	5	5.5	V
Charge pump voltage (VCP-VDRAIN)		V_{CP}	VM = 13 V I_{VCP} = 0 to 25 mA	8.4	11	12.5	V
			VM = 10 V I_{VCP} = 0 to 20 mA	6.3	9	10	
			VM = 8 V I_{VCP} = 0 to 13 mA	5.4	7	8	
Internal oscillator frequency		f_{OSC}	VM = 8 to 75 V, T_j = -40 to 125 °C	17	20	24	MHz
Digital input pins							
ENABLE	Input voltage	V_{IL}	High input	0	–	0.8	V
		V_{IH}	Low input	1.8	–	5.5	V
		V_{HYS}	–	–	100	–	mV
	Input current	I_{IL}	V_{IL} = 0 V	–	–	5	μA
		I_{IH}	V_{IH} = 5 V	–	50	70	μA
	Pull-down resistor	R_{PD}	–	–	100	–	kΩ
INHx, INLx, nCS, SCLK, SDI CAL	Input voltage	V_{IL}	High input	0	–	0.8	V
		V_{IH}	Low input	1.5	–	5.5	V
		V_{HYS}	V_{DVDD} = 3.3 V TB67Z83x	–	140	–	mV
			V_{DVDD} = 5 V TB67Z85x	–	60	–	
	Input current	I_{IL}	V_{IL} = 0 V	–	–	5	μA
		I_{IH}	V_{IH} = 5 V	–	50	70	μA
	Pull-down resistor	R_{PD}	–	–	100	–	kΩ
	Propagation time	t_{PD}	INHx / INLx → GHx / GLx	–	175	–	ns

Characteristics		Symbol	Condition		Min	Typ.	Max	Unit
4-level input pins								
GAIN, MODE	Mode 1	V_1	Short to AGND		–	0	–	V
	Mode 2	V_2	Connect to AGND via 45 kΩ ± 5% resistor	TB67Z83x	–	1.2	–	
				TB67Z85x	–	1.8	–	
	Mode 3	V_3	Open	TB67Z83x	–	2.0	–	
				TB67Z85x	–	3.1	–	
	Mode 4	V_4	Short to DVDD		–	V_{DVDD}	–	
	Pull-up resistor	R_{PU}	–		–	50	–	kΩ
	Pull-down resistor	R_{PD}	–		–	84	–	kΩ
7-level input pins								
IDRIVE, VDS	Mode 1	V_1	Short to AGND		–	0	–	V
	Mode 2	V_2	Connect to AGND via 18 kΩ ± 5% resistor	TB67Z83x	–	0.5	–	
				TB67Z85x	–	0.8	–	
	Mode 3	V_3	Connect to AGND via 75 kΩ ± 5% resistor	TB67Z83x	–	1.1	–	
				TB67Z85x	–	1.7	–	
	Mode 4	V_4	Open	TB67Z83x	–	1.65	–	
				TB67Z85x	–	2.5	–	
	Mode 5	V_5	Connect to DVDD via 75 kΩ ± 5% resistor	TB67Z83x	–	2.2	–	
				TB67Z85x	–	3.3	–	
	Mode 6	V_6	Connect to DVDD via 18 kΩ ± 5% resistor	TB67Z83x	–	2.8	–	
				TB67Z85x	–	4.2	–	
	Mode 7	V_7	Short to DVDD		–	V_{DVDD}	–	
	Pull-up resistor	R_{PU}	–		–	73	–	kΩ
	Pull-down resistor	R_{PD}	–		–	73	–	kΩ
Open Drain pins								
nFAULT SDO	Output Low voltage	V_{OL}	I_{OUT} = 5 mA		–	–	0.1	V
	Output leakage current	I_{OH}	V_{OUT} = 5 V		–	–	1.0	μA

Characteristics		Symbol	Condition		Min	Typ.	Max	Unit
Gate driver								
Gate drive voltage	High-side voltage (GHx-SHx)	$V_{GSH(H)}$	VM = 13 V, I_{VCP} = 0 to 25 mA, Source current capability = 1 A (design value)		8.4	11	12.5	V
			VM = 10 V, I_{VCP} = 0 to 20 mA, Source current capability = 1 A (design value)		6.3	9	10	
			VM = 8 V, I_{VCP} = 0 to 13 mA, Source current capability = 1 A (design value)		5.4	7	8	
		$V_{GSH(L)}$	During HOLD period, I_{SINK} = 0.5 mA		–	–	0.5	V
	Low-side voltage (GLx-PGND)	$V_{GSL(H)}$	VM = 12 V, I_{GL} = 0 to 25 mA, Source current capability = 1 A (design value)		9	11	12	V
			VM = 10 V, I_{GL} = 0 to 20 mA, Source current capability = 1 A (design value)		7.5	9	10	
			VM = 8 V, I_{GL} = 0 to 13 mA, Source current capability = 1 A (design value)		5.5	7	8	
		$V_{GSL(L)}$	During HOLD period, I_{SINK} = 0.5 mA		–	–	0.5	V
Gate drive Source current capability		I_{DRIVEP}	SPI	Reg = 0000b	–	10	–	mA
				Reg = 0001b	–	30	–	
				Reg = 0010b	–	60	–	
				Reg = 0011b	–	80	–	
				Reg = 0100b	–	120	–	
				Reg = 0101b	–	140	–	
				Reg = 0110b	–	170	–	
				Reg = 0111b	–	190	–	
				Reg = 1000b	–	260	–	
				Reg = 1001b	–	330	–	
				Reg = 1010b	–	370	–	
				Reg = 1011b	–	440	–	
				Reg = 1100b	–	570	–	
				Reg = 1101b	–	680	–	
				Reg = 1110b	–	820	–	
				Reg = 1111b	–	1000	–	
			Hardware	IDRIVE = Mode 1	–	10	–	
				IDRIVE = Mode 2	–	30	–	
				IDRIVE = Mode 3	–	60	–	
				IDRIVE = Mode 4	–	120	–	
				IDRIVE = Mode 5	–	260	–	
				IDRIVE = Mode 6	–	570	–	
				IDRIVE = Mode 7	–	1000	–	

Characteristics	Symbol	Condition		Min	Typ.	Max	Unit
Gate drive Sink current capability	I_{DRIVEN}	SPI	Reg = 0000b	–	20	–	mA
			Reg = 0001b	–	60	–	
			Reg = 0010b	–	120	–	
			Reg = 0011b	–	160	–	
			Reg = 0100b	–	240	–	
			Reg = 0101b	–	280	–	
			Reg = 0110b	–	340	–	
			Reg = 0111b	–	380	–	
			Reg = 1000b	–	520	–	
			Reg = 1001b	–	660	–	
			Reg = 1010b	–	740	–	
			Reg = 1011b	–	880	–	
			Reg = 1100b	–	1140	–	
			Reg = 1101b	–	1360	–	
			Reg = 1110b	–	1640	–	
			Reg = 1111b	–	2000	–	
		Hardware	IDRIVE = Mode 1	–	20	–	
			IDRIVE = Mode 2	–	60	–	
			IDRIVE = Mode 3	–	120	–	
			IDRIVE = Mode 4	–	240	–	
			IDRIVE = Mode 5	–	520	–	
			IDRIVE = Mode 6	–	1140	–	
			IDRIVE = Mode 7	–	2000	–	
Hold current	I_{HOLD_SRC}	Source current capability after t_{DRIVE}		–	10	–	mA
	I_{HOLD_SNK}	Sink current capability after t_{DRIVE}		–	60	–	
Turn-on prevention current	I_{STRONG}	Sink current capability		–	2000	–	mA
Turn-on prevention resistor	R_{OFF}	ENABLE = 0 V		–	150	–	kΩ
Drive time	t_{DRIVE}	SPI	Reg = 00b	–	600	–	ns
			Reg = 01b	–	1000	–	
			Reg = 10b	–	2000	–	
			Reg = 11b	–	4000	–	
		Hardware		–	4000	–	ns
Dead time	t_{DEAD}	SPI	Reg = 00b	–	50	–	ns
			Reg = 01b	–	100	–	
			Reg = 10b	–	200	–	
			Reg = 11b	–	400	–	
		Hardware		–	100	–	ns

Characteristics	Symbol	Condition		Min	Typ.	Max	Unit
Current sense amplifier							
Gain	G_{CSA}	SPI VREF_DIV = 1b CSA_FET = 0b	CSA_GAIN = 00b	4.85	5	5.15	V/V
			CSA_GAIN = 01b	9.7	10	10.3	
			CSA_GAIN = 10b	19.4	20	20.6	
			CSA_GAIN = 11b	38.8	40	41.2	
		Hardware	GAIN = Mode 1	4.85	5	5.15	
			GAIN = Mode 2	9.7	10	10.3	
			GAIN = Mode 3	19.4	20	20.6	
			GAIN = Mode 4	38.8	40	41.2	
Setting time (until within ±1%)	t_{SET}	V_{O_STEP} = 0.5 V, G_{CSA} = 5 V/V (design value)		–	200	–	ns
		V_{O_STEP} = 0.5 V, G_{CSA} = 10 V/V (design value)		–	300	–	
		V_{O_STEP} = 0.5 V, G_{CSA} = 20 V/V (design value)		–	600	–	
		V_{O_STEP} = 0.5 V, G_{CSA} = 40 V/V (design value)		–	1200	–	
Common mode input range	V_{COM}	–		-0.15	–	0.15	V
Differential mode input range	V_{DIFF}	–		-0.3	–	0.3	V
Input offset	V_{OFF}	V_{SPX} = V_{SNX} = 0 V, V_{VREF} = 3.3 V, after calibration Bi-directional current detection mode, T_a = -40 to 125 °C		-3	–	3	mV
Drift	V_{DRIFT}	V_{SPX} = V_{SNX} = 0 V (design value)		–	10	–	µV/°C
Linear output range	V_{LINEAR}	V_{VREF} = 3 to 5.5 V, after calibration		0.25	–	V_{VREF} - 0.25	V
Output bias voltage	V_{BIAS}	SPI	VREF_DIV = 0b, SOx output open	V_{VREF} - 0.25	–	V_{VREF}	V
			VREF_DIV = 1b, SOx output open	–	V_{VREF}/2	–	V
		Hardware	SOx output open	–	V_{VREF}/2	–	V
Input bias current	I_{BIAS}	Bi-directional current detection mode	SPx = SNx = -0.3 V Current flowing out of SPx pin	–	–	1.2	mA
			SPx = SNx = -0.3 V Current flowing out of SNx pin	–	–	130	µA
Output slew rate	SR_{SO}	Load capacitor = 60 pF (design value)		–	10	–	V/µs
Reference voltage input current	I_{VREF}	V_{VREF} = 5 V		–	3	4.5	mA
Unity gain bandwidth	UGB	Load capacitor = 60 pF (design value)		–	1	–	MHz

Characteristics		Symbol	Condition		Min	Typ.	Max	Unit
Protection Functions								
VM under voltage detection	Detect voltage	V_{VMDN}	During VM voltage falling		5.4	5.6	5.8	V
	Release voltage	V_{VMUP}	During VM voltage rising		5.6	5.8	6	V
	Hysteresis	V_{VM_UVHys}	–		–	0.2	–	V
	Filter time	t_{VM_UVD}	During VM voltage falling		–	10	–	µs
VDRAIN under voltage detection	UVLO detect	V_{VDRDN}	During VDRAIN voltage falling		5.4	5.6	5.8	V
	UVLO release	V_{VDRUP}	During VDRAIN voltage rising		5.6	5.8	6	V
	Hysteresis	V_{VDR_UVHys}	–		–	0.2	–	V
	Filter time	t_{VDR_UVD}	During VDRAIN voltage falling		–	10	–	µs
DVDD under voltage detection	UVLO detect	V_{DVDDDN}	During VDD voltage falling		2.6	2.75	2.9	V
	UVLO release	V_{DVDDUP}	During VDD voltage rising		2.7	2.85	3.0	V
	Hysteresis	V_{VDD_UVHys}	–		–	0.1	–	V
Charge pump under voltage detection	Detection voltage	V_{VCPDN}	During VCP voltage falling VCP-VDRAIN		4.7	5	5.3	V
	Recovery voltage	V_{VCPUP}	During VCP voltage rising VCP-VDRAIN		5.2	5.5	5.8	V
	Hysteresis	V_{VCP_UVHys}	–		–	0.5	–	V
	Filter time	t_{VCP_UVD}	During VCP voltage falling		–	10	–	µs
High-side clamp	High output	V_{GS_CLAMPH}	T_a = -40 to 125 °C		13.0	14.5	19.0	V
	Low output	V_{GS_CLAMPL}			–	-0.7	–	V
VDS over current detection voltage		V_{DS_OCP}	SPI	Reg = 0000b	0.03	0.06	0.09	V
				Reg = 0001b	–	0.13	–	
				Reg = 0010b	–	0.2	–	
				Reg = 0011b	–	0.26	–	
				Reg = 0100b	–	0.31	–	
				Reg = 0101b	–	0.45	–	
				Reg = 0110b	–	0.53	–	
				Reg = 0111b	–	0.6	–	
				Reg = 1000b	–	0.68	–	
				Reg = 1001b	–	0.75	–	
				Reg = 1010b	–	0.94	–	
				Reg = 1011b	–	1.13	–	
				Reg = 1100b	–	1.3	–	
				Reg = 1101b	–	1.5	–	
				Reg = 1110b	–	1.7	–	
				Reg = 1111b	–	1.88	–	
			Hardware	VDS = Mode 1	0.03	0.06	0.09	
				VDS = Mode 2	–	0.13	–	
				VDS = Mode 3	–	0.26	–	
				VDS = Mode 4	–	0.6	–	
				VDS = Mode 5	–	1.13	–	
				VDS = Mode 6	–	1.88	–	
				VDS = Mode 7	–	Disabled	–	

Characteristics		Symbol	Condition		Min	Typ.	Max	Unit
VSENSE over current detection voltage		V_{SEN_OCP}	SPI	Reg = 00b	–	0.25	–	V
				Reg = 01b	–	0.5	–	
				Reg = 10b	–	0.75	–	
				Reg = 11b	–	1	–	
			Hardware		–	1	–	
Over current filter time		t_{OCP_MASK}	SPI	Reg = 00b	–	1	–	µs
				Reg = 01b	–	2	–	
				Reg = 10b	–	4	–	
				Reg = 11b	–	8	–	
			Hardware		–	4	–	
Over current auto recovery time		t_{RETRY}	SPI	Reg = 00b	–	4	–	ms
				Reg = 01b	–	50	–	µs
			Hardware		–	4	–	ms
Gate drive voltage monitoring threshold voltage		V_{GS_LT}	T_j = -40 to 125 °C, VDRAIN = 8 to 75 V		0.5	1.0	1.5	V
		V_{GS_HT}	T_j = -40 to 125 °C, VDRAIN = 8 to 75 V		2.5	3.0	3.5	V
High temperature warning	Detect	T_{OTW}	(design value)		140	150	160	°C
	Release	T_{OTWR}	(design value)		110	120	130	°C
	Hysteresis	T_{OTW_Hys}	(design value)		–	30	–	°C
TSD	Detect	T_{TSD}	(design value)		155	165	175	°C
	Release	T_{TSDR}	(design value)		125	135	145	°C
	Hysteresis	T_{TSD_Hys}	(design value)		–	30	–	°C

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
SPI Timing						
Preparation period	t_{READY}	VM > V_{VMUP}, period after ENABLE = 3.3 V until SPI communication is ready.	–	–	1	ms
SCLK cycle	t_{CLK}	–	100	–	–	ns
SCLK H period	t_{CLKH}	–	50	–	–	ns
SCLK L period	t_{CLKL}	–	50	–	–	ns
SDI setup time	t_{SU_SDI}	Period from SDI input to SCLK falling edge	20	–	–	ns
SDI hold time	t_{HD_SDI}	Period of maintain SDI from SCLK falling edge	30	–	–	ns
SDO output Delay	t_{D_SDO}	Period from SCLK High to SDO output	–	–	30	ns
nCS setup time	t_{SU_nCS}	Period from nCS Low to SCLK rising edge	50	–	–	ns
nCS hold time	t_{HD_nCS}	Preiod form SCLK falling edge to nCS High	50	–	–	ns
nCS H period	t_{H_nCS}	High period until nCS Low	400	–	–	ns
nCS disable period	t_{DIS_nCS}	Period from nCS High to SDO Hi-Z (design value)	–	10	–	ns

Note: Unless otherwise noted, electrical characteristics are shown for the conditions described.
When operating the product under different conditions, the characteristics shown in the electrical characteristics may not be obtained.

11. Feature Description

11.1. 3-Phase gate driver

11.1.1. PWM control modes

TB67Z830xFTG/833xFTG/850xFTG/853xFTG supports four types of PWM control modes. The PWM control mode can be set by the MODE pin (Hardware I/F) or the PWM_MODE register (SPI I/F). Please do not change the PWM control mode while driving external MOSFETs. Please ensure that the PWM control mode is set when the INHx and INLx pins are all Low and all external MOSFETs are in the OFF state.

11.1.1.1. 6-PWM input mode

In 6-PWM input mode, each of the three half-bridges can be controlled independently. The state of each half-bridge can be controlled to Low, High, and High impedance (Hi-Z) through the inputs of the INHx and INLx pins.

Table 11.1 6-PWM input mode

INLx	INHx	GLx	GHx	SHx
L	L	L	L	Hi-Z
L	H	L	H	H
H	L	H	L	L
H	H	L	L	Hi-Z

GLx / GHx = L: able to flow Sink/Hold current.
GLx / GHx = H: able to flow Source/Hold current.

11.1.1.2. 3-PWM input mode

Table 11.2 3-PWM input mode

INLx (Enable)	INHx (PWM)	GLx	GHx	SHx
L	X	L	L	Hi-Z
H	L	H	L	L
H	H	L	H	H

GLx / GHx = L: able to flow Sink/Hold current.
GLx / GHx = H: able to flow Source/Hold current.

11.1.1.3. Hall input mode

In the Hall input mode, it is easy to achieve square wave driving (120-degree energization). The three-phase Hall signals are inputted to the INLA, INHB, and INLB pins. The INHA pin controls the frequency and duty of the output PWM, while the INHC pin controls the rotation direction. Additionally, the INLC pin is be used to enable the BRAKE.

The Hardware I/F version and SPI I/F version operate in synchronous rectification mode by default. The operation of the device is as follows.

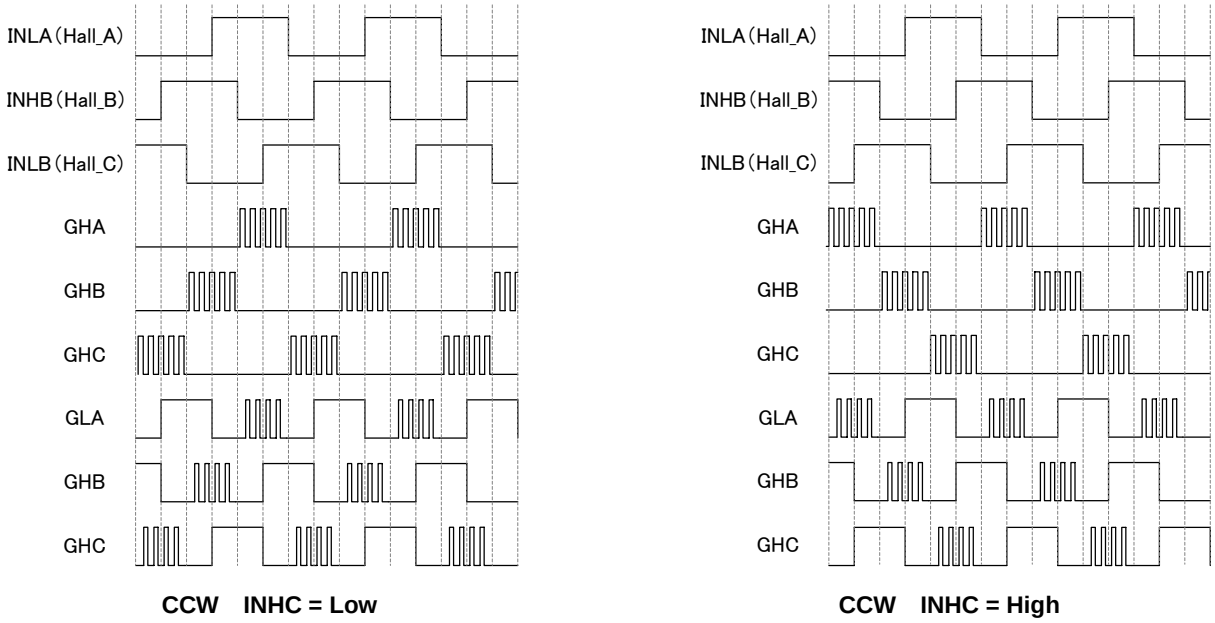


Fig. 11.1 Timing chart of synchronous rectification mode

Table 11.3 Synchronous rectification mode (CCW)

STATE	Logic Input CCW (INHC = L)				Gate drive output					
	INLC (nBRAKE)	INLA (Hall_A)	INHB (Hall_B)	INLB (Hall_C)	GHA	GLA	GHB	GLB	GHC	GLC
BRAKE	L	X	X	X	L	H	L	H	L	H
STOP	H	L	L	L	L	L	L	L	L	L
Align		H	H	H	INHA	/INHA	L	H	L	H
A → C		H	L	L	INHA	/INHA	L	L	L	H
A → B		H	L	H	INHA	/INHA	L	H	L	L
C → B		L	L	H	L	L	L	H	INHA	/INHA
C → A		L	H	H	L	H	L	L	INHA	/INHA
B → A		L	H	L	L	H	INHA	/INHA	L	L
B → C		H	H	L	L	L	INHA	/INHA	L	H

Table 11.4 Synchronous rectification mode (CW)

STATE	Logic Input CW (INHC=H)				Gate drive output					
	INLC (nBRAKE)	INLA (Hall_A)	INHB (Hall_B)	INLB (Hall_C)	GHA	GLA	GHB	GLB	GHC	GLC
BRAKE	L	X	X	X	L	H	L	H	L	H
STOP	H	L	L	L	L	L	L	L	L	L
Align		H	H	H	INHA	/INHA	L	H	L	H
A → C		L	H	H	INHA	/INHA	L	L	L	H
A → B		L	H	L	INHA	/INHA	L	H	L	L
C → B		H	H	L	L	L	L	H	INHA	/INHA
C → A		H	L	L	L	H	L	L	INHA	/INHA
B → A		H	L	H	L	H	INHA	/INHA	L	L
B → C		L	L	H	L	L	INHA	/INHA	L	H

The SPI I/F version also supports asynchronous rectification mode, the operation is as follows.

Table 11.5 Asynchronous rectification mode (CCW) (SPI I/F version only)

STATE	Logic Input CCW (INHC = L)				Gate drive output					
	INLC (nBRAKE)	INLA (Hall_A)	INHB (Hall_B)	INLB (Hall_C)	GHA	GLA	GHB	GLB	GHC	GLC
BRAKE	L	X	X	X	L	H	L	H	L	H
STOP	H	L	L	L	L	L	L	L	L	L
Align		H	H	H	INHA	L	L	H	L	H
A → C		H	L	L	INHA	L	L	L	L	H
A → B		H	L	H	INHA	L	L	H	L	L
C → B		L	L	H	L	L	L	H	INHA	L
C → A		L	H	H	L	H	L	L	INHA	L
B → A		L	H	L	L	H	INHA	L	L	L
B –> C		H	H	L	L	L	INHA	L	L	H

Table 11.6 Asynchronous rectification mode (CW) (SPI I/F version only)

STATE	Logic Input CW (INHC=H)				Gate drive output					
	INLC (nBRAKE)	INLA (Hall_A)	INHB (Hall_B)	INLB (Hall_C)	GHA	GLA	GHB	GLB	GHC	GLC
BRAKE	L	X	X	X	L	H	L	H	L	H
STOP	H	L	L	L	L	L	L	L	L	L
Align		H	H	H	INHA	L	L	H	L	H
A → C		L	H	H	INHA	L	L	L	L	H
A → B		L	H	L	INHA	L	L	H	L	L
C → B		H	H	L	L	L	L	H	INHA	L
C → A		H	L	L	L	H	L	L	INHA	L
B → A		H	L	H	L	H	INHA	L	L	L
B → C		L	L	H	L	L	INHA	L	L	H

11.1.1.4. Independent PWM mode

In independent PWM mode, high-side and low-side gate drive is controlled separately.

Table 11.7 Independent PWM mode

INLx	INHx	GLx	GHx
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

GLx / GHx = L: able to flow Sink/Hold current.
GLx / GHx = H: able to flow Source/Hold current.

When using both the high-side and low-side of the same half-bridge simultaneously in Independent PWM mode, please disable the VDS over current detection function to avoid false detection.

11.1.2. External MOSFET gate drive

TB67Z830xFTG/833xFTG/850xFTG/853xFTG incorporate gate driver circuits that can drive external Nch + Nch MOSFETs. The gate drive current and drive time of the external MOSFETs are adjustable. In addition, it also has a built-in drive sequence to prevent shoot-through.

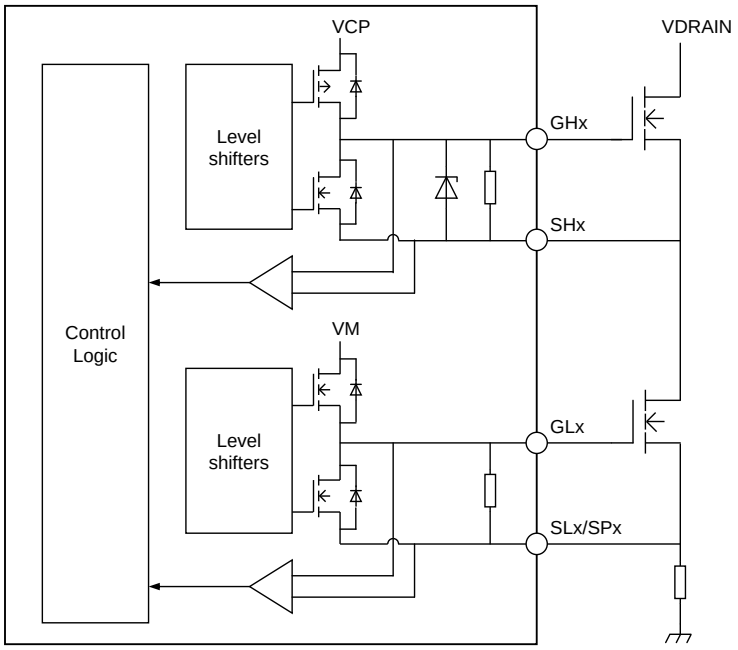


Fig. 11.2 Block Diagram for Gate Drive circuit

11.1.2.1. Drive current capability

To control the ON and OFF speed of the external MOSFET, the capability of the gate drive current (source current and sink current) can be adjusted. The source current capability can be set from 10 mA to 1 A. The sink current capability can be set from 20 mA to 2 A. In the SPI I/F version, the gate drive current capability can be set by registers. In the Hardware I/F version, the gate drive current capability can be set by the IDRIVE pin.

Table 11.8 SPI I/F Gate drive current setting register

Register	Setting contents
IDRIVEP_HS	High-side gate drive source current capability
IDRIVEN_HS	High-side gate drive sink current capability
IDRIVEP_LS	Low-side gate drive source current capability
IDRIVEN_LS	Low-side gate drive sink current capability

Table 11.9 Gate drive current capability setting

Source current capability (mA)	Sink current capability (mA)	SPI I/F Register value	Hardware I/F IDRIVE
10	20	0000b	Mode 1
30	60	0001b	Mode 2
60	120	0010b	Mode 3
80	160	0011b	--
120	240	0100b	Mode 4
140	280	0101b	--
170	340	0110b	--
190	380	0111b	--
260	520	1000b	Mode 5
330	660	1001b	--
370	740	1010b	--
440	880	1011b	--
570	1140	1100b	Mode 6
680	1360	1101b	--
820	1640	1110b	--
1000	2000	1111b	Mode 7

11.1.2.2. Driver sequence

A drive sequence is built into the device to prevent shoot-through. The details are explained using the 6-PWM input mode as an example.

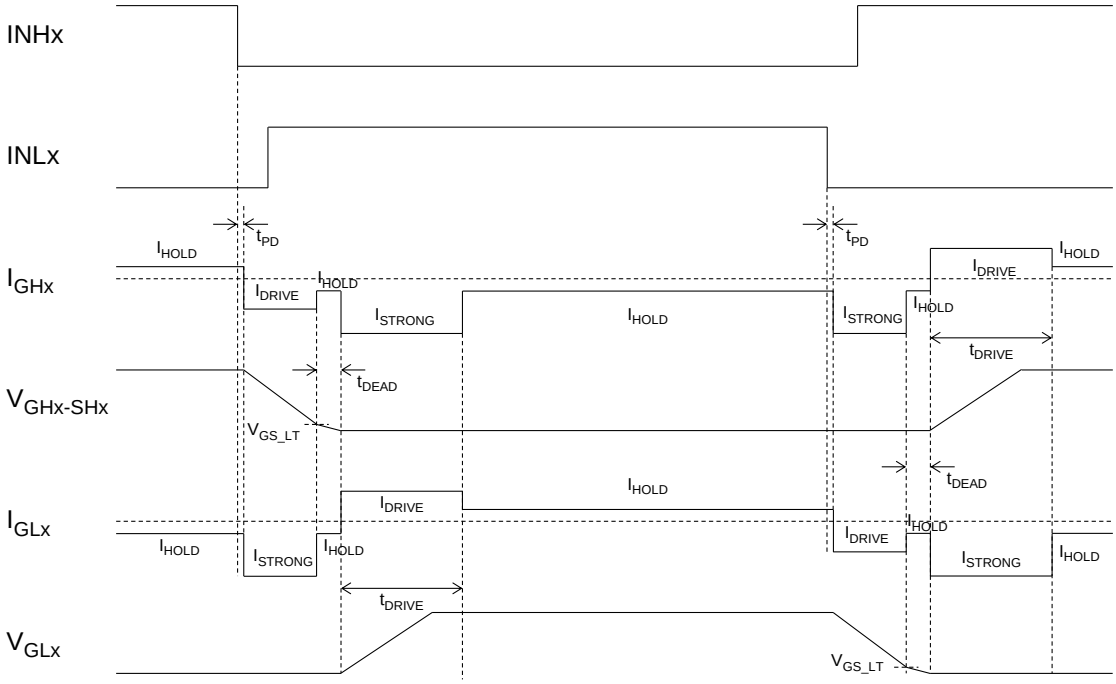


Fig. 11.3 Example of gate drive sequence

The sequence for transitioning from a state where the high-side external MOSFET is ON and the low-side external MOSFET is OFF, to a state where the high-side MOSFET is OFF and the low-side external MOSFET is ON, is as follows:

After receiving the command to turn off the high-side external MOSFET (INHx = H → L), the gate drive current of the high-side external MOSFET switches from source (I_{HOLD}) to sink (I_{DRIVE}). At the same time, to prevent self-turn-on of the low-side external MOSFET, the gate drive sink current capability of the low-side external MOSFET switches to the I_{STRONG}.

During the period of turning off the high-side external MOSFET, the gate-source voltage (V_{GS}) of the external MOSFET is monitored. After it falls below the threshold (V_{GS_LT}) of 1.0 V (typ.), a dead-time period is inserted. The duration of the dead-time period, t_{DEAD}, is fixed at 100 ns (typ.) in the Hardware I/F version and can be set with the DEAD_TIME register in the SPI I/F version. If the V_{GS} voltage does not fall below V_{GS_LT} even after t_{DRIVE} has elapsed, it is detected as a gate drive voltage fault.

To prevent the shoot-through current, the low-side external MOSFET is turned on after the dead-time period. The period for turning on the low-side external MOSFET is t_{DRIVE}, during which the gate drive source current capability of the low-side external MOSFET is I_{DRIVE}. Also, to prevent self-turn-on of the high-side external MOSFET, the gate drive sink current capability of the high-side external MOSFET switches to I_{STRONG}. During the period of turning on the low-side external MOSFET, the V_{GS} voltage is monitored, and if it exceeds the threshold (V_{GS_HT}) of 3.0 V (typ.), the device can transit to other states. If the V_{GS} voltage does not exceed V_{GS_HT} even after t_{DRIVE} has elapsed, it is detected as a gate drive voltage fault.

The same shoot-through prevention sequence is also included when transitioning from a state where the high-side external MOSFET is OFF and the low-side external MOSFET is ON, to a state where the high-side MOSFET is ON and the low-side external MOSFET is OFF.

In the Serial I/F version, when the DRV_SEQ register is set to 0b, the ON and OFF periods of the external MOSFET are fixed at t_{DRIVE}. The drive sequence is as follows.

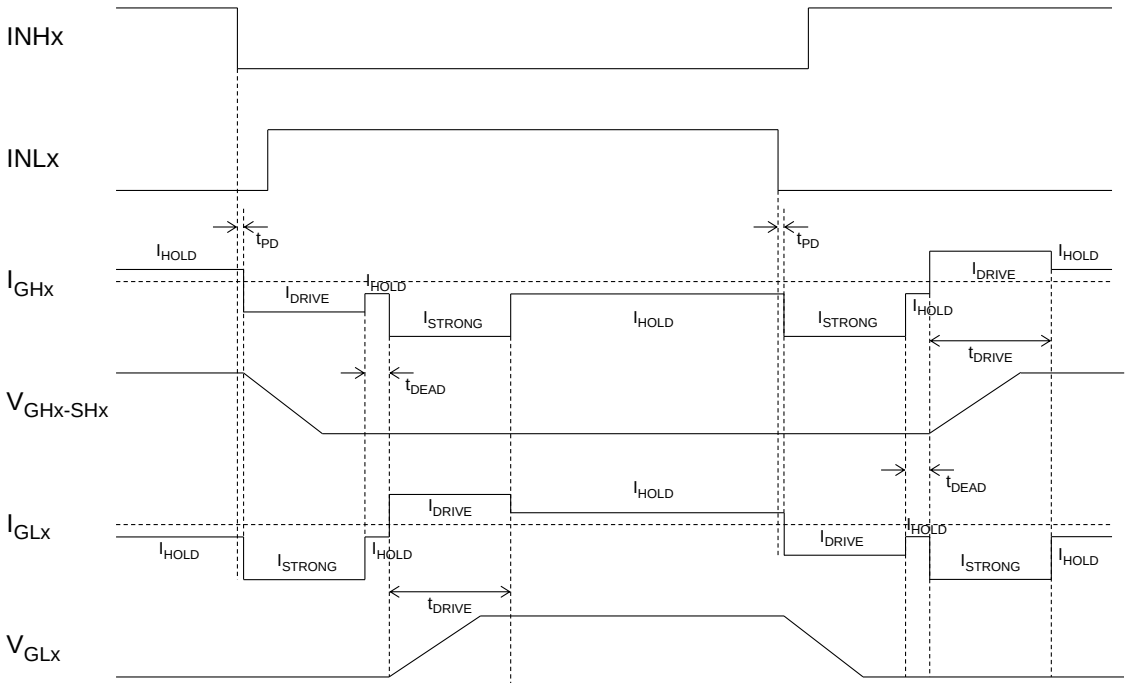


Fig. 11.4 Example of gate drive sequence (DRV_SEQ = 0b)

Note that in the case of DRV_SEQ = 0b, the gate drive voltage fault detection is performed at the end of the t_{DRIVE} period. If the gate-source voltage (V_{GS}) of the external MOSFET is above V_{GS_LT} when turning off the external MOSFET, or below V_{GS_HT} when turning ON the external MOSFET, at the timing of the completion of the t_{DRIVE} period, it is detected as a gate drive voltage fault.

11.1.3. Power supply system

The power supply for driving the low-side external MOSFETs is from VM. The voltage is clamped to 11 V by the V_{GSL} voltage inside the device. However, if the VM voltage is less than 12 V, the voltage decreases according to the VM voltage.

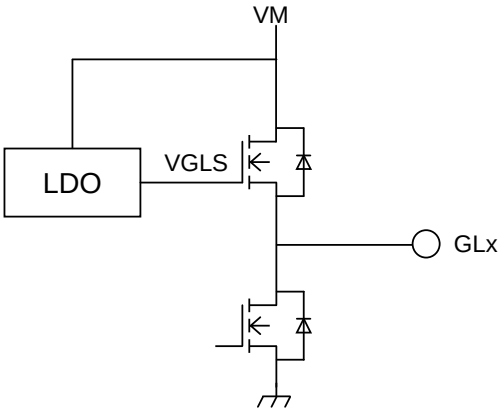


Fig. 11.5 Low-side driving power supply

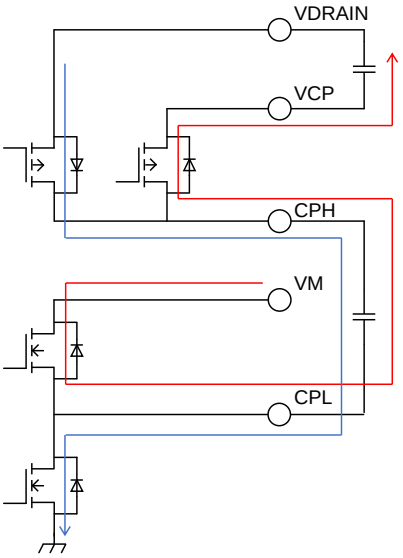


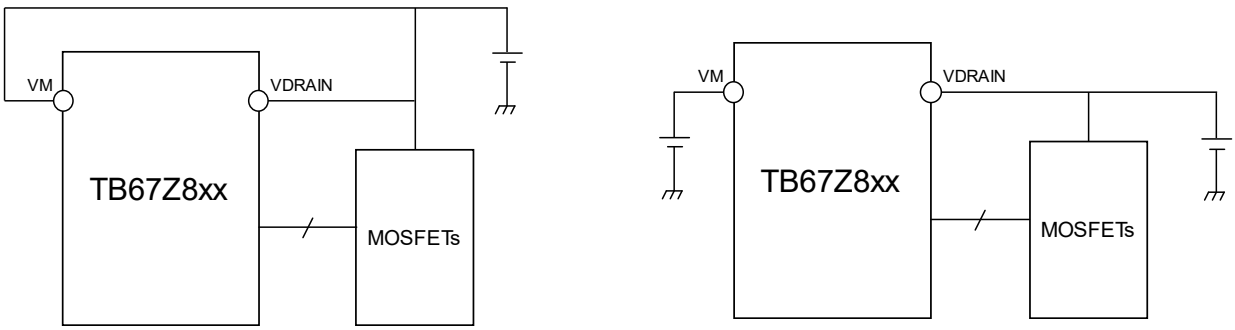
Fig. 11.6 Charge pump and charge current flow

The power supply for driving the high-side external MOSFETs is generated from a charge pump. The charge pump voltage is VDRAIN+11 V and is capable of outputting an average current up to 25 mA. However, if the VM voltage is less than 12 V, the charge pump voltage decreases according to the VM voltage.

Use a ceramic capacitor with a capacitance of 1 uF, a withstand voltage of 16 V or more, and a temperature characteristic of X5R or X7R, between VCP and VDRAIN. Also, use a ceramic capacitor with a capacitance of 47 nF, a withstand voltage above the VDRAIN voltage, and a temperature characteristic of X5R or X7R between CPH and CPL.

If the CPL terminal is shorted to the power supply, there is a risk of device destruction. As the destruction of the device may lead to smoke or fire, please use an appropriate power fuse to ensure that a large current does not continuously flow in such a case.

Since the charge pump voltage is referenced to VDRAIN, it is possible to apply separate power supplies to VM and VDRAIN. The power supply to the device is provided from VM. Therefore, by applying a lower voltage to VM, the power consumption of the device can be reduced.



Single power supply configuration

Dual power supply configuration

Fig. 11.7 Example of power supply configuration

11.2. DVDD Regulator

TB67Z830xFTG/833xFTG incorporates a regulator with an output voltage of 3.3 V (typ.) and output current of 30 mA (max). TB67Z850xFTG/853xFTG incorporates a regulator with an output voltage of 5.0 V (typ.) and output current of 30 mA (max).

Add a ceramic capacitor with a capacitance of 1 µF, a withstand voltage of 6.3 V or more, and a temperature characteristic of X5R or X7R, between the DVDD and AGND pins, and place it as close to the device as possible.

When using the regulator as a power supply for externally circuits, the power consumption of the regulator, P_{LDO}, can be calculated using the following formula.

$$P_{LDO} = (V_{VM} - V_{DVDD}) \times I_{DVDD}$$

Please note that if the VM voltage is high, the power consumption of the regulator will increase. Please be mindful of the heat generation of the device.

11.3. Current sense amplifier

TB67Z833xFTG/TB67Z853xFTG has three built-in amplifiers for sensing the current of the low-side shunt resistor. In addition to the bi-directional current detection, the SPI I/F version also supports uni-directional current detection, VDS voltage detection, and input reverse mode.

The VREF pin is the power supply and reference voltage for the amplifier circuit. Please supply voltage to VREF either from DVDD or from an external power source.

When the current sense amplifier is not in use, please connect SPx and SNx to the ground.

11.3.1. Bi-directional current detection

For bi-directional current detection, the relationship between the SOx voltage and the voltage between SPx and SNx is as follows.

$$V_{SOx} = V_{VREF} / 2 - (V_{SPx} - V_{SNx}) \times G_{CSA}$$
$$= V_{VREF} / 2 - I_{SENSE} \times R_{SENSE} \times G_{CSA}$$

Note: Under the conditions that the voltage between SPx and SNx is within the differential mode input range, and the VSOx voltage is within the linear output range.
The offset and temperature drift of the amplifier also affect the output voltage.
When the current flowing through the shunt resistor is 0, the variation range of the output voltage is $V_{VREF} / 2 \pm (V_{OFF} + V_{DRIFT}) \times G_{CSA}$.

The current flowing through the shunt resistor can be calculated as follows.

$$I_{SENSE} = (V_{VREF} / 2 - V_{SOx}) / (R_{SENSE} \times G_{CSA})$$

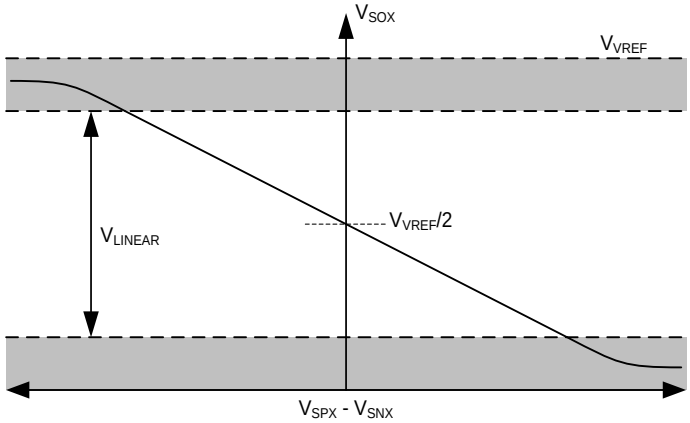


Fig. 11.8 Bi-directional current detection output

The gain of current sense amplifier (G_{CSA}) can be set to four levels: 5 V/V, 10 V/V, 20 V/V, and 40 V/V. In the Hardware I/F version, the gain is set by the GAIN pin. In the SPI I/F version, the gain is set by the CSA_GAIN register.

Table 11.10 Current detection gain setting

Gain	SPI I/F CSA_GAIN	Hardware I/F GAIN
5 V/V	00b	Mode 1
10 V/V	01b	Mode 2
20 V/V	10b	Mode 3
40 V/V	11b	Mode 4

11.3.2. Uni-directional current detection (SPI I/F version only)

By setting the VREF_DIV register to 1b, the reference voltage of the amplifier becomes V_{VREF}, and the uni-directional current detection mode is enabled. For unidirectional current detection, the relationship between the SOx voltage and the voltage between SPx and SNx is as follows.

$V_{SOx} = V_{VREF} – (V_{SPx} - V_{SNx}) \times G_{CSA}$

$= V_{VREF} – I_{SENSE} \times R_{SENSE} \times G_{CSA}$

Note: Under the condition is that the voltage between SPx and SNx is within the differential mode input range, and V_{SOx} voltage is within the linear output range.
The offset and temperature drift of the amplifier also affect the output voltage.

Note: When the current flowing through the shunt resistor is 0, the output voltage is near V_{VREF} and is outside the linear output range.

The current flowing through the shunt resistor can be calculated as follows.

$I_{SENSE} = (V_{VREF} – V_{SOx}) / (R_{SENSE} \times G_{CSA})$

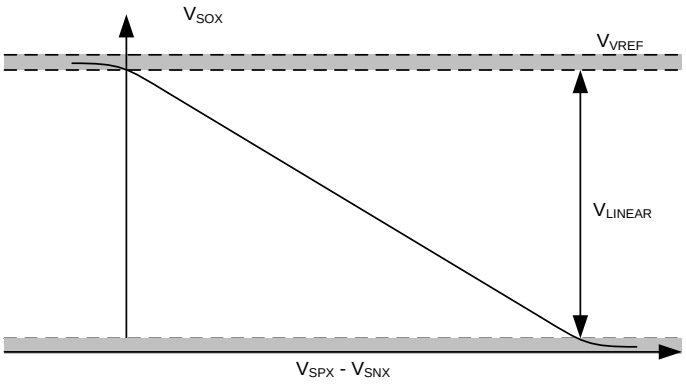


Fig. 11.9 Uni-directional current detection output

11.3.3. VDS voltage sense mode (SPI I/F version only)

In addition to amplifying the voltage of the shunt resistor and outputting it from SOx, the drain-source voltage of the external low-side MOSFETs can be amplified and outputted from SOx This function is enabled by setting the CSA_FET register to 1b.

When VDS voltage sense is enabled, the voltage between SHx and SNx is amplified and output form SOx. However, to prevent high voltage at SHx from damaging the amplifier, the output is available after the external low-side MOSFET is turned ON (after the t_{DRIVE} period).

The relationship between the SOx voltage and the voltage between SHx and SNx is as follows.

$V_{SOx} = V_{VREF} / 2 – (V_{SHx} - V_{SNx}) \times G_{CSA}$

Note: Under the conditions that the voltage between SHx and SNx is within the differential mode input range, and the V_{SOx} voltage is within the linear output range. The offset and temperature drift of the amplifier also affect the output voltage.

Additionally, when VDS voltage detection is enabled, the LS_REF register is automatically set to 1b, and VDS over current is detected by the voltage between SHx and SNx of the external low-side MOSFET."

11.3.4. Input reverse mode (SPI I/F version only)

The inputs of the current sense amplifiers can be reversed by set INV_SEN register to 1b.

Table 11.11 Input setting for current sense amplifier

INV_SEN	CAS_FET	Amp input (+)	Amp input (-)
0b	0b	SNx	SPx
	1b	SNx	SHx
1b	0b	SPx	SNx
	1b	SHx	SNx

11.3.5. Input offset calibration

A calibration function is incorporated to minimize the input offset of the current sense amplifiers. Calibration can be performed by CAL pin or register settings (SPI I/F version only).

Before executing the calibration, ensure that all external MOSFETs are turned off by setting the INHx and INLx pins. Also, set SPx and SNx to the ground level.

During calibration executing, the device automatically switches to bi-directional current detection while the gain setting remains unchanged. Since the offset varies depending on the gain setting, it is recommended to perform calibration again after changing the gain setting.

The required time for the calibration process is 100 µs (max). The calibration state is maintained after the calibration process is completed unless the CAL pin or register settings are released. In the calibration state, the INHx and INLx signals are not accepted.

When performing calibration using the CAL pin, the calibration process is started by set CAL pin to High. Calibrations for all three amplifiers are executed simultaneously. Once the calibration process is complete and the CAL pin becomes Low, the calibration state is released, and the device is resumed to normal operation. The mode setting of the current sense amplifiers are automatically returned to the setting before the calibration.

When performing calibration using register settings, calibration is executed only for the amplifier that the CAL_x register is set to 1b. Do not change the register settings during calibration execution. Once the calibration process is complete and all CAL_x registers become 0b, the calibration state is released, and the device is resumed to normal operation. The mode setting of the current sense amplifiers are automatically returned to the setting before the calibration.
For example, After the calibration of amplifiers A and B by setting CAL_A and CAL_B to 1b, if set only CAL_A back to 0b, please note that the calibration for amplifier B will be executed again.

11.4. Protection function

Table 11.12 List of protection functions

Function	Detection condition	Setting	nFAULT	Gate driver	Charge pump	Logic circuit	Release condition
DVDD under voltage	$V_{DVDD} < V_{DVDDDN}$	–	L	GLx = OFF GHx = OFF	Stop	Stop	Auto Recovery: $V_{DVDD} > V_{DVDDUP}$
VM under voltage	$V_{VM} < V_{VMDN}$	–	L	GLx = OFF GHx = OFF	Stop	Active	Auto Recovery: $V_{VM} > V_{VMUP}$
VDRAIN under voltage	$V_{VDR} < V_{VDRDN}$	–	L	GLx = OFF GHx = OFF	Stop	Active	Auto Recovery: $V_{VDR} > V_{VDRUP}$
Charge pump under voltage	$V_{VCP} < V_{VCPDN}$	DIS_CPUV = 0b	L	GLx = OFF GHx = OFF	Stop	Active	Auto Recovery: $V_{VCP} > V_{VCPUP}$
		DIS_CPUV = 1b	No change	Normal	Active	Active	–
VDS over current	$V_{DS} > V_{DS\_OCP}$	OCP_MODE = 00b	L	GLx = L GHx = L	Active	Active	Latched: CLR_FLT, ENABLE pulse
		OCP_MODE = 01b	L	GLx = L GHx = L	Active	Active	Auto Recovery: after t_{RETRY}
		OCP_MODE = 10b	L	Normal	Active	Active	–
		OCP_MODE = 11b	No change	Normal	Active	Active	–
VSESE over current	$V_{SP} > V_{SEN\_OCP}$	OCP_MODE = 00b	L	GLx = L GHx = L	Active	Active	Latched: CLR_FLT, ENABLE pulse
		OCP_MODE = 01b	L	GLx = L GHx = L	Active	Active	Auto Recovery: after tRETRY
		OCP_MODE = 10b	L	Normal	Active	Active	–
		OCP_MODE = 11b or DIS_SEN = 1b	No change	Normal	Active	Active	–
Gate drive voltage fault	V_{GS} fails to cross threshold after t_{DRIVER}	DIS_GDF = 0b	L	GLx = OFF GHx = OFF	Active	Active	Latched: CLR_FLT, ENABLE pulse
		DIS_GDF = 1b	No change	Normal	Active	Active	–
High temperature warning	$T_j > T_{OTW}$	OTW_REP = 1b	L	Normal	Active	Active	Auto Recovery: $T_j < T_{OTWR}$
		OTW_REP = 0b	No change	Normal	Active	Active	–
Thermal shutdown	$T_j > T_{TSD}$	–	L	GLx = OFF GHx = OFF	Stop	Active	Auto Recovery: $T_j < T_{TSDR}$

11.4.1. DVDD under voltage lockout

The voltage on the DVDD pin is monitored. If the voltage falls below V_{DVDDDN}, all blocks, including the internal logic circuit, will stop. In this case, the gate driver output goes to high impedance, and all external MOSFETs are turned off by the internal turn-on prevention resistor. The nFAULT output becomes Low, but if the DVDD voltage falls below a certain threshold, it enters the high impedance state.
When the voltage on DVDD pin rises above V_{DVDDUP}, the logic is reset, and operation resumes.

11.4.2. VM under voltage lockout

The voltage on the VM pin is monitored. If the voltage falls below V_{VMDN}, all external MOSFETs are turned off as a low voltage protection feature. By default, the soft shutdown function is enabled, so the external MOSFETs are turned off using the soft shutdown sink current.

Table 11.13 External MOSFETs turn-off operation

Register setting		Sink current	Sink period
DIS_SOFT = 0b	DRV_SEQ = 0b	$I_{SOFTSINK}$	Util cross V_{GS_LT}
	DRV_SEQ = 1b	$I_{SOFTSINK}$	40 µs
DIS_SOFT = 1b	DRV_SEQ = 0b	I_{DRIVEN}	Util cross V_{GS_LT}
	DRV_SEQ = 1b	I_{DRIVEN}	40 µs

After turning off the external MOSFETs, the gate driver output goes to high impedance, and the internal turn-on prevention resistor maintains the external MOSFETs in the OFF state. Additionally, the charge pump also stops.
The nFAULT output becomes Low after detecting VM under voltage. The FAULT register and UVLO register become 1b. When the VM voltage exceeds V_{VMUP}, the charge pump and gate driver automatically resume operation. The low output of nFAULT is also released. However, the UVLO register remains at 1b. It can be cleared by CLR_FLT or a pulse on ENABLE.

11.4.3. VDRAIN under voltage lockout

The voltage on the VDRAIN pin is monitored. If the voltage falls below V_{VDRDN}, all external MOSFETs are turned off as a low voltage protection feature. By default, the soft shutdown function is enabled, so the external MOSFETs are turned off using the soft shutdown sink current.
After turning off the external MOSFETs, the gate driver output goes to high impedance, and the internal turn-on prevention resistor maintains the external MOSFETs in the OFF state. Additionally, the charge pump also stops.
The nFAULT output becomes Low after detecting VDRAIN under voltage. The FAULT register and UVLO register become 1b. When the VDRAIN voltage exceeds V_{VDRUP}, the charge pump and gate driver automatically resume operation. The low output of nFAULT is also released. However, the UVLO register remains at 1b. It can be cleared by CLR_FLT or a pulse on ENABLE.

11.4.4. Charge pump under voltage lockout

The charge pump voltage between the VCP pin and VDRAIN pin is monitored. If the voltage falls below V_{VCPDN}, all external MOSFETs are turned off as a low voltage protection feature. By default, the soft shutdown function is enabled, so the external MOSFETs are turned off using the soft shutdown sink current.
After turning off the external MOSFETs, the gate driver output goes to high impedance, and the internal turn-on prevention resistor maintains the external MOSFETs in the OFF state.
The nFAULT output becomes Low after detecting charge pump undervoltage. The FAULT register and CPUV register become 1b. When the charge pump voltage exceeds V_{VCPUP}, the gate driver automatically resume operation. The low output of nFAULT is also released. However, the CPUV register remains at 1b. It can be cleared by CLR_FLT or a pulse on ENABLE.

11.4.5. VDS over current detection

The V_{DS} voltage of the external MOSFET is monitored. If the V_{DS} voltage remains above V_{DS_OCP} for a duration longer than t_{OCP_MASK}, it is detected as an overcurrent state.

In the SPI I/F version, the behavior after detecting overcurrent can be chosen from four modes by the OCP_MODE register.

1. Stop (Latch)
   The gate driver output goes Low to turn off the external MOSFETs. The nFAULT output becomes Low. The FAULT register, OCP register, and the VDS_xx register corresponding to the detected overcurrent MOSFET become 1b.
   When the V_{DS} voltage falls below the threshold voltage V_{DS_OCP}, the gate drive can be resumed by CLR_FLT or a pulse on ENABLE. In this case, the registers are also cleared.

2. Auto-Recovery
   The gate driver output goes Low to turn off the external MOSFETs. The nFAULT output becomes Low. The FAULT register, OCP register, and the VDS_xx register corresponding to the detected overcurrent MOSFET become 1b.
   If the CBC register is 0b, the registers are cleared after the auto recovery time t_{RETRY}, and the gate drive is resumed. If the CBC register is 1b, the registers are cleared and the gate drive is resumed after t_{RETRY} or when the input state changes.

3. Report
   The gate driver continues operating, but the nFAULT becomes Low. The FAULT register, OCP register, and the VDS_xx register corresponding to the detected overcurrent MOSFET become 1b.
   When the V_{DS} voltage falls below the threshold voltage V_{DS_OCP}, setting CLR_FLT or a pulse on ENABLE can release the nFAULT and clear the registers.

4. Disabled
   The VDS over current detection function is disabled.

In the Hardware I/F version, it is auto-recovery and the t_{RETRY} is 4 ms. Additionally, the VDS over current detection function can be disabled by setting VDS pin to DVDD.

When turning off the external MOSFETs, in the SPI I/F version, the OCP_ACT register can choose which half-bridge to turn off. If the OCP_ACT register is 0b, only the half-bridge with detected overcurrent is turned off. If the OCP_ACT register is 1b, all three half-bridges are turned off. In the Hardware I/F version, all three half-bridges are turned off. By default, the soft shutdown function is enabled, so the external MOSFETs are turned off using the soft shutdown sink current.

11.4.6. VSENSE over current detection

The V_{SP} voltage on shunt resistor is monitored to detect over current in the external MOSFETs. If the V_{SP} voltage remains above V_{SEN_OCP} for a duration longer than t_{OCP_MASK}, it is detected as an overcurrent state.

In the SPI I/F version, the behavior after detecting overcurrent can be chosen from four modes using the OCP_MODE register:

1. Stop (Latch)
   The gate driver output goes Low to turn off the external MOSFETs. The nFAULT output becomes Low. The FAULT register, OCP register, and the Sx_OC register corresponding to the detected overcurrent half-bridge become 1b.
   When the V_{SP} voltage falls below the threshold voltage V_{SEN_OCP}, the gate driver can be resumed by CLR_FLT or a pulse on ENABLE. In this case, the registers are also cleared.

2. Auto-Recovery
   The gate driver output goes Low to turn off the external MOSFETs. The nFAULT output becomes Low. The FAULT register, OCP register, and the Sx_OC register corresponding to the detected overcurrent half-bridge become 1b.
   If the CBC register is 0b, the registers are cleared after the auto recovery time t_{RETRY}, and the gate drive is resumed. If the CBC register is 1b, the registers are cleared and the gate drive is resumed after t_{RETRY} or when the input state changes.

3. Report
   The gate driver continues operating, but the nFAULT becomes Low. The FAULT register, OCP register, and the Sx_OC register corresponding to the detected overcurrent half-bridge become 1b.
   When the V_{SP} voltage falls below the threshold voltage V_{SEN_OCP}, setting CLR_FLT or a pulse on ENABLE can release the nFAULT and clear the registers.

4. Disabled
   The VSENSE over current detection function is disabled. Beside OCP_MODE, setting the DIS_SEN register to 1b can also disable the VSENSE over current detection function.

In the Hardware I/F version, it is auto-recovery and the t_{RETRY} is 4 ms. The detection level is fixed at 1 V.

When turning off the external MOSFETs, in the SPI I/F version, the SEN_ACT and OCP_ACT registers determine which half-bridge to turn off. If SEN_ACT register is 0b, it follows the OCP_ACT setting. If SEN_ACT register is 1b, all three half-bridges are turned off. In the Hardware I/F version, all three half-bridges are turned off. By default, the soft shutdown function is enabled, so the external MOSFETs are turned off using the soft shutdown sink current.

11.4.7. Soft shutdown

After detecting under voltage in VM, VDRAIN and charge pump, as well as over current, the sink current capability is automatically adjusted to gradually turn off the external MOSFETs. The sink current capability during soft shutdown is dependent on the I_{DRIVEN} setting.

Table 11.14 I_{DRIVEN} setting and sink current capability during soft shut down

I_{DRIVEN} setting (mA)	sink current capability during soft shutdown (mA)
2000	880
1640	740
1360	660
1140	520
880	380
740	340
660	280
520	240
380	160
340	120
280	60
20 to 240	20

11.4.8. Gate drive voltage monitor

When turning on and off the external MOSFETs, the voltages at the GLx and GHx terminals are monitored. If the target voltage is not reached after t_{DRIVE} period, a gate drive voltage fault is detected. After the fault is detected, the gate driver output goes to high impedance, and all external MOSFETs are turned off by the internal turn-on prevention resistor. Also, the nFAULT output becomes Low. The FAULT register, GDF register, and the VGS_xx register corresponding to the detected gate output become 1b.
After the fault condition is removed, the gate driver can be resumed by CLR_FLT or a pulse on ENABLE.

In the SPI I/F version, the gate drive voltage monitor function can be disabled by setting the DIS_GDVM register. In the Hardware I/F version, this function is always enabled.

11.4.9. High temperature warning

In the SPI I/F version, when the internal temperature of the device exceeds T_{OTW}, the OTW register is set to 1b. When the internal temperature of the device falls below T_{OTWR}, the OTW register automatically returns to 0b. Additionally, by setting the OTW_REP register to 1b allows the OTW status to be reflected on the nFAULT pin and the FAULT register.
In the Hardware I/F version, this feature is not available.

11.4.10. Thermal shutdown (TSD)

When the internal temperature of the device exceeds T_{TSD}, the gate driver output goes to high impedance, and all external MOSFETs are turned off by the internal turn-on prevention resistor. The charge pump also stops. Additionally, the nFAULT output becomes Low. The FAULT register and the TSD register become 1b.
When the internal temperature of the device falls below T_{TSDR}, the operation resumes automatically. However, the TSD register maintains 1b until it is cleared by CLR_FLT or a pulse on ENABLE.

11.5. Standby mode

When the ENABLE pin remains Low for longer than the t_{RESET} period, the device goes to standby mode. It takes a time of t_{STBY} from the falling edge of the ENABLE signal to enter standby mode.

Before entering standby mode, the gate driver output goes Low to turn off the external MOSFETs. By default, the soft shutdown function is enabled, so the external MOSFETs are turned off using the soft shutdown sink current. The drive time for turning off the external MOSFETs is 40 µs (typ.).

When entering standby mode, the DVDD regulator and charge pump are stopped. The gate driver output becomes high impedance, and the internal turn-on prevention resistors keep all external MOSFETs off. Additionally, the output of the current sense amplifiers become undefined.

If the Low period of the ENABLE signal is within t_{RESET} period, it is recognized as an error reset pulse. It clears any fault flags and allows operation to resume.

During standby mode, applying a High signal to the ENABLE pin will exist standby mode. It takes a time of t_{WAKE} from exiting standby mode to accept other input signals. Also, the nFAULT output is low during exiting standby mode.

The transitions of each state are as follows.

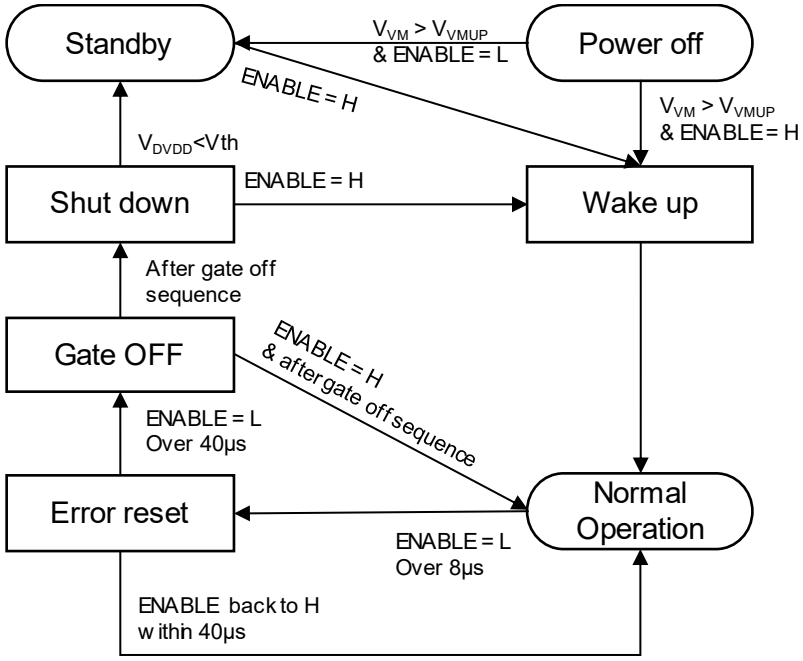


Fig. 11.10 State transition

11.6. Control interface

11.6.1. Hardware interface

In the Hardware I/F version, functions are controlled by GAIN, IDRIVE, MODE and VDS pins.

Table 11.15 Recommendable setting for GAIN pin

GAIN pin setting	Current sense amplifier gain
Short to DVDD	40 V/V
OPEN (≥500 kΩ to AGND)	20 V/V
45 kΩ ± 5% to AGND	10 V/V
Short to AGND	5 V/V

Table 11.16 Recommendable setting for IDRIVE pin

IDRIVE pin setting	Gate drive current capability (source / sink)
Short to DVDD	1 A / 2 A
18 kΩ ± 5% to DVDD	570 mA / 1140 mA
75 kΩ±5% to DVDD	260 mA / 520 mA
OPEN (≥500 kΩ to AGND)	120 mA / 240 mA
75 kΩ±5% to AGND	60 mA / 120 mA
18 kΩ ± 5% to AGND	30 mA / 60 mA
Short to AGND	10 mA / 20 mA

Table 11.17 Recommendable setting for MODE pin

MODE pin setting	PWM control mode
Short to DVDD	Independent PWM mode
OPEN (≥500 kΩ to AGND)	Hall input mode
45 kΩ ± 5% to AGND	3-PWM input mode
Short to AGND	6-PWM input mode

Table 11.18 Recommendable setting for VDS pin

VDS pin setting	VDS over current detection threshold voltage
Short to DVDD	Disabled
18kΩ ± 5% to DVDD	1.88 V
75 kΩ±5% to DVDD	1.13 V
OPEN (≥500 kΩ to AGND)	0.60 V
75 kΩ±5% to AGND	0.26 V
18 kΩ ± 5% to AGND	0.13 V
Short to AGND	0.06 V

11.6.2. SPI interface

In the SPI I/F version, the nCS, SCLK, SDI and SDO pins are used to communication with the device and control functions.
nCS is the chip select pin, communication is enabled when it is Low. SCLK is the clock input pin, SDI is the data input pin, and SDO is data output pin. Additionally, since SDO is an open-drain pin, an external pull-up resistor is required.

11.6.2.1. SPI communication format

Communication is enabled when nCS is Low. when nCS is High, inputs to SCLK and SDI are ignored, and SDO is high impedance. SCLK should keep Low when nCS transitions from High to Low or from Low to High. Additionally, keep nCS High for at least 400 ns between two communications.
The input data from SDI consists of a 1-bit command, a 4-bit address, and 11 bits of data. The first 1 bit (RW) is the read/write command, where RW = 0b is for writing and RW = 1b is for reading. The following 4 bits are the address of the target register. The last 11 bits are the contents of the data.

Table 11.19 Format of SDI input data

R/W	ADDRESS				DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
RW	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The output data from SDO consists of the first 5 bits as Don’t care bits, and the remaining 11 bits as the contents of the register.

Table 11.20 Format of SDO output data

DON’T CARE BITS					DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Data is transmitted and received from the most significant bit (MSB), 16 cycles of the SCLK signal are required for transmitting and receiving. If the data input to SDI is not 16 bits, a frame error occurs, and that data is ignored.
The data on SDI is captured at the falling edge of SCLK. The output data to SDO is prepared from the rising edge of SCLK. Additionally, in the case of a write command, after transmitting the address, the current data of the target register is output from the SDO pin.

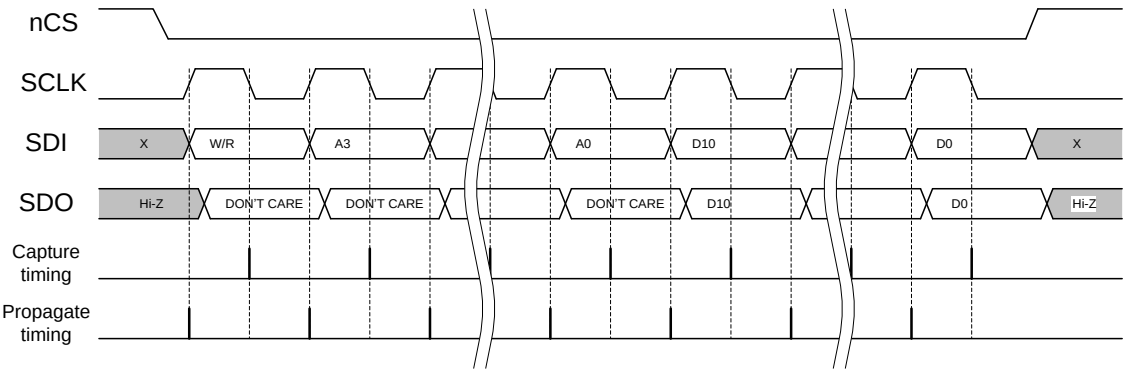


Fig. 11.11 SPI communication timing chart

11.6.2.2. Register maps

Table 11.21 Register map of TB67Z830SFTG and TB67Z850SFTG

Address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Type
0000b	FAULT	OCP	GDF	UVLO	TSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R
0001b	SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R
0010b	OCP_ACT	DIS_CPUV	DIS_GDVM	OTW_REP			COM	DIR	COAST	BRAKE	CLR_FLT	RW
0011b	LOCK [2:0]			IDRIVEP_HS [4:0]				IDRIVEN_HS [4:0]				RW
0100b	CBC	TDRIVE		IDRIVEP_LS [4:0]				IDRIVEN_LS [4:0]				RW
0101b	TRETRY	DEAD_TIME [1:0]		OCP_MODE [1:0]		OCP_MASK [1:0]		VDS_LVL [4:0]				RW
0110b						DIS_SEN				SEN_LVL [1:0]		RW
0111b							SEN_ACT	DIS_SOFT	DRV_SEQ			RW

Table 11.22 Register map of TB67Z833SFTG and TB67Z853SFTG

Address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Type
0000b	FAULT	OCP	GDF	UVLO	TSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R
0001b	SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R
0010b	OCP_ACT	DIS_CPUV	DIS_GDVM	OTW_REP			COM	DIR	COAST	BRAKE	CLR_FLT	RW
0011b	LOCK [2:0]			IDRIVEP_HS [4:0]				IDRIVEN_HS [4:0]				RW
0100b	CBC	TDRIVE		IDRIVEP_LS [4:0]				IDRIVEN_LS [4:0]				RW
0101b	TRETRY	DEAD_TIME [1:0]		OCP_MODE [1:0]		OCP_MASK [1:0]		VDS_LVL [4:0]				RW
0110b	CSA_FET	VREF_DIV	LS_REF	CSA_GAIN [1:0]		DIS_SEN	CAL_A	CAL_B	CAL_C	SEN_LVL [1:0]		RW
0111b							SEN_ACT	DIS_SOFT	DRV_SEQ	INV_SEN		RW

Table 11.23 Address = 0000b

Bit	Name	Type	Default	Description
10	FAULT	R	0b	OR logic of each error flag.
9	OCP	R	0b	Error flag for VDS or VSENSE over current detection
8	GDF	R	0b	Error flag for gate drive voltage fault detection
7	UVLO	R	0b	Error flag for VM or VDRAIN under voltage detection
6	TSD	R	0b	Error flag for thermal shut down detection
5	VDS_HA	R	0b	Error flags for VDS over current detection on A channel High-side
4	VDS_LA	R	0b	Error flags for VDS over current detection on A channel Low-side
3	VDS_HB	R	0b	Error flags for VDS over current detection on B channel High-side
2	VDS_LB	R	0b	Error flags for VDS over current detection on B channel Low-side
1	VDS_HC	R	0b	Error flags for VDS over current detection on C channel High-side
0	VDS_LC	R	0b	Error flags for VDS over current detection on C channel Low-side

Table 11.24 Address = 0001b

Bit	Name	Type	Default	Description
10	SA_OC	R	0b	Error flag of VSENSE over current detection on A channel
9	SB_OC	R	0b	Error flag of VSENSE over current detection on B channel
8	SC_OC	R	0b	Error flag of VSENSE over current detection on C channel
7	OTW	R	0b	Flag for high temperature warning
6	CPUV	R	0b	Error flag for charge pump under-voltage detection
5	VGS_HA	R	0b	Error flag for of gate drive voltage fault detection on A channel High-side
4	VGS_LA	R	0b	Error flag for of gate drive voltage fault detection on A channel Low-side
3	VGS_HB	R	0b	Error flag for of gate drive voltage fault detection on B channel High-side
2	VGS_LB	R	0b	Error flag for of gate drive voltage fault detection on B channel Low-side
1	VGS_HC	R	0b	Error flag for of gate drive voltage fault detection on C channel High-side
0	VGS_LC	R	0b	Error flag for of gate drive voltage fault detection on C channel Low-side

Table 11.25 Address = 0010b

Bit	Name	Type	Default	Description
10	OCP_ACT	RW	0b	0b: Only the half-bridge with detected overcurrent is turned off 1b: all three half-bridges are turned off when over current is detected.
9	DIS_CPUV	RW	0b	0b: Charge pump under voltage lockout is enabled. 1b: Charge pump under voltage lockout is disabled
8	DIS_GDVM	RW	0b	0b: Gate drive voltage monitor is enabled. 1b: Fate drive voltage monitor is disabled.
7	OTW_REP	RW	0b	0b: Not report to nFAULT pin and FAULT register when OTW occurs. 1b: Report to nFAULT pin and FAULT register when OTW occurs
6:5	PWM_MODE [1:0]	RW	00b	00b: 6-PWM Input mode 01b: 3-PWM Input mode 10b: Hall input mode 11b: Independent PWM mode
4	COM	RW	0b	0b: Synchronous rectification mode in Hall Input Mode 1b: Asynchronous rectification mode in Hall Input Mode
3	DIR	RW	0b	0b: In Hall input mode, INCH = Low for CCW, INCH = High for CW 1b: In Hall input mode, INCH = Low for CW, INCH=High for CCW
2	COAST	RW	0b	0b: Normal operation 1b: Turn off all the external MOSFETs
1	BRAKE	RW	0b	0b: Normal operation 1b: High-side MOSFETs OFF, Low-side MOSFETs ON
0	CLR_FLT	RW	0b	Write 1b to clear error flags. CLR_FLT is automatically returned to 0b after writing.

Table 11.26 Address = 0011b

Bit	Name	Type	Default	Description
10-8	LOCK [2:0]	RW	011b	011b: Unlock all the registers 110b: Unable to write to registers other than the LOCK register
7-4	IDRIVEP_HS [3:0]	RW	1111b	High-side source current capability 0000b: 10 mA 0001b: 30 mA 0010b: 60 mA 0011b: 80 mA 0100b: 120 mA 0101b: 140 mA 0110b: 170 mA 0111b: 190 mA 1000b: 260 mA 1001b: 330 mA 1010b: 370 mA 1011b: 440 mA 1100b: 570 mA 1101b: 680 mA 1110b: 820 mA 1111b: 1000 mA
3-0	IDRIVEN_HS [3:0]	RW	1111b	High-side sink current capability 0000b: 20 mA 0001b: 60 mA 0010b: 120 mA 0011b: 160 mA 0100b: 240 mA 0101b: 280 mA 0110b: 340 mA 0111b: 380 mA 1000b: 520 mA 1001b: 660 mA 1010b: 740 mA 1011b: 880 mA 1100b: 1140 mA 1101b: 1360 mA 1110b: 1640 mA 1111b: 2000 mA

Table 11.27 Address = 0100b

Bit	Name	Type	Default	Description
10	CBC	RW	1b	In case of auto-recovery after over current detection (OCP_MODE = 01b) 0b: Fault is clear after t_{RETRY} 1b: Fault is clear after t_{RETRY} or input state changes
9-8	TDRIVE [1:0]	RW	11b	Gate driver period with I_{DRIVE} current capability 00b: 600 ns 01b: 1000 ns 10b: 2000 ns 11b: 4000 ns
7-4	IDRIVEP_LS [3:0]	RW	1111b	Low-side source current capability 0000b: 10 mA 0001b: 30 mA 0010b: 60 mA 0011b: 80 mA 0100b: 120 mA 0101b: 140 mA 0110b: 170 mA 0111b: 190 mA 1000b: 260 mA 1001b: 330 mA 1010b: 370 mA 1011b: 440 mA 1100b: 570 mA 1101b: 680 mA 1110b: 820 mA 1111b: 1000 mA
3-0	IDRIVEN_LS [3:0]	RW	1111b	Low-side sink current capability 0000b: 20 mA 0001b: 60 mA 0010b: 120 mA 0011b: 160 mA 0100b: 240 mA 0101b: 280 mA 0110b: 340 mA 0111b: 380 mA 1000b: 520 mA 1001b: 660 mA 1010b: 740 mA 1011b: 880 mA 1100b: 1140 mA 1101b: 1360 mA 1110b: 1640 mA 1111b: 2000 mA

Table 11.28 Address = 0101b

Bit	Name	Type	Default	Description
10	TRETRY	RW	0b	Auto recovery time after over current detection 0b: 4 ms 1b: 50 µs
9-8	DEAD_TIME [1:0]	RW	01b	Dead time period 00b: 50 ns 01b: 100 ns 10b: 200 ns 11b: 400 ns
7-6	OCP_MODE [1:0]	RW	01b	Operation mode after over current detection 00b: Stop (Latch) 01b: Auto-recovery 10b: Report 11b: Disabled
5-4	OCP_MASK [1:0]	RW	10b	Filter time of over current detection 00b: 1 µs 01b: 2 µs 10b: 4 µs 11b: 8 µs
3-0	VDS_LVL [3:0]	RW	1001b	Threshold voltage of VDS over current detection 0000b: 0.06 V 0001b: 0.13 V 0010b: 0.20 V 0011b: 0.26 V 0100b: 0.31 V 0101b: 0.45 V 0110b: 0.53 V 0111b: 0.60 V 1000b: 0.68 V 1001b: 0.75 V 1010b: 0.94 V 1011b: 1.13 V 1100b: 1.30 V 1101b: 1.50 V 1110b: 1.70 V 1111b: 2.00 V

Table 11.29 Address = 0110b

Bit	Name	Type	Default	Description
10	CSA_FET	RW	0b	TB67Z833SFTG and TB67Z853SFTG only 0b: The voltage between SPx and SNx is sensed 1b: The voltage between SHx and SNx is sensed (LS_REF is set to 1b automatically)
9	VREF_DIV	RW	1b	TB67Z833SFTG and TB67Z853SFTG only 0b: The reference voltage of current sense amplifier is VREF (Uni-directional) 1b: The reference voltage of current sense amplifier is VREF/2 (Bi-directional)
8	LS_REF	RW	0b	TB67Z833SFTG and TB67Z853SFTG only 0b: VDS over current is detect by voltage between SHx and SPx 1b: VDS over current is detect by voltage between SHx and SNx
7-6	CSA_GAIN [1:0]	RW	10b	TB67Z833SFTG and TB67Z853SFTG only Current sense amplifier gain 00b: 5 V/V 01b: 10 V/V 10b: 20 V/V 11b: 40 V/V
5	DIS_SEN	RW	0b	0b: VSENSE over current detection is enabled 1b: VSENSE over current detection is disabled
4	CAL_A	RW	0b	TB67Z833SFTG and TB67Z853SFTG only 0b: Ach current sense amplifier normal operation 1b: Perform Ach current sense amplifier offset calibration
3	CAL_B	RW	0b	TB67Z833SFTG and TB67Z853SFTG only 0b: Bch current sense amplifier normal operation 1b: Perform Bch current sense amplifier offset calibration
2	CAL_C	RW	0b	TB67Z833SFTG and TB67Z853SFTG only 0b: Bch current sense amplifier normal operation 1b: Perform Bch current sense amplifier offset calibration
1-0	SEN_LVL [1:0]	RW	11b	Threshold voltage of VSENSE over current detection 00b: 0.25 V 01b: 0.5 V 10b: 0.75 V 11b: 1.00 V

Table 11.30 Address = 0111b

Bit	Name	Type	Default	Description
10-5	Reserved	RW	000000b	Reserved
4	SEN_ACT	RW	0b	0b: follow OCP_ACT setting 1b: Turn off all three half-bridges
3	DIS_SOFT	RW	0b	0b: Soft shut down is enabled 1b: Soft shut down is disabled
2	DRV_SEQ	RW	1b	0b: Monitor V_{GS} after t_{DRIVE} 1b: Monitor V_{GS} during t_{DRIVE}
1	INV_SEN	RW	0b	TB67Z833SFTG and TB67Z853SFTG only 0b: Current sense amplifier input, + = SNx, - = SPx 1b: Reverse current sense amplifier input, + = SPx, - = SNx
0	Reserved	RW	0b	Reserved

12. Example of Application Circuit

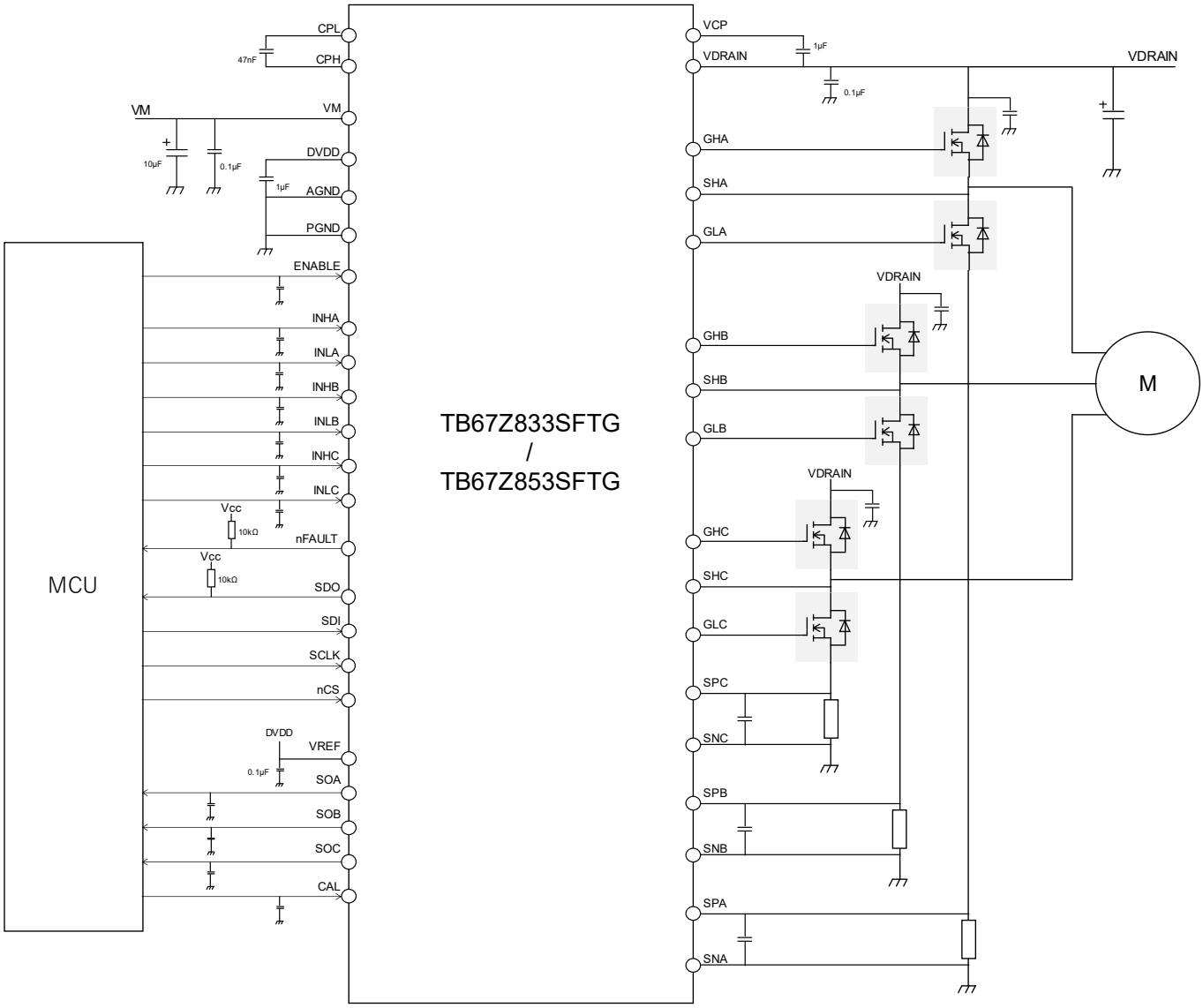


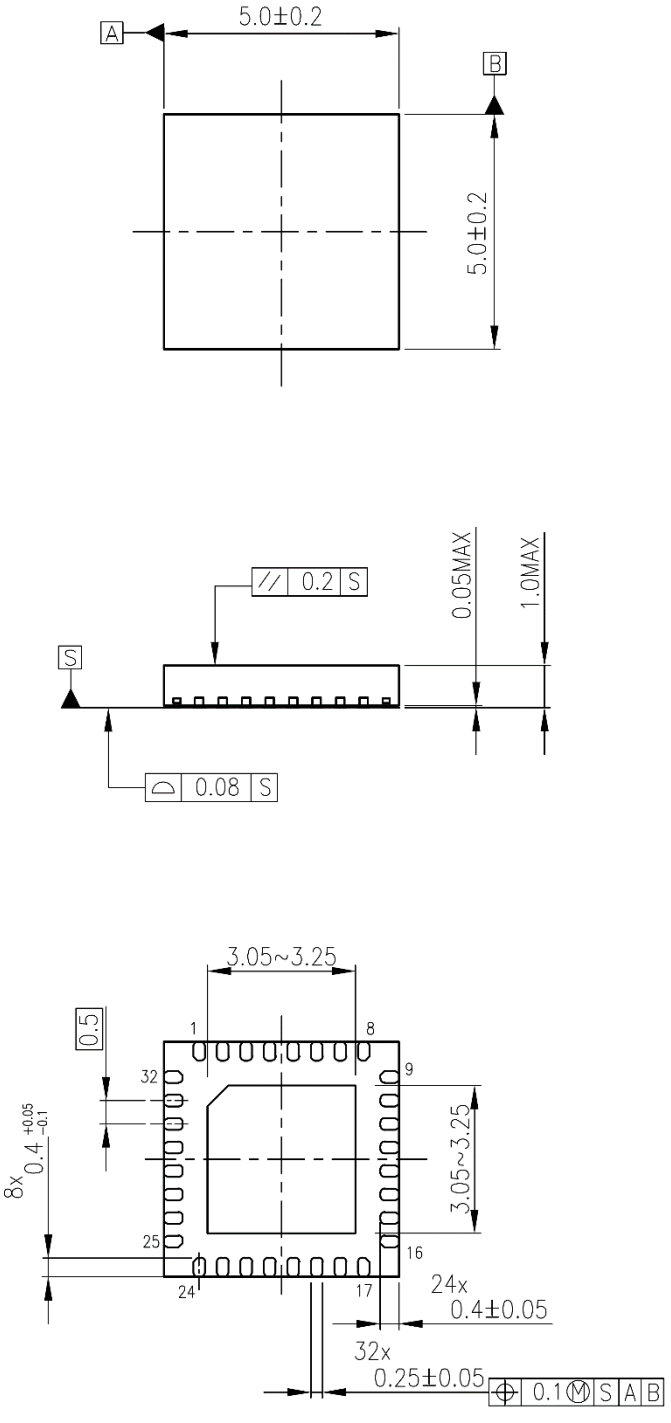
Fig. 12.1 Example of Application Circuit of TB67Z833SFTG/Z853SFTG

Note 1: Add capacitors for noise rejection to the input pins as required.
Note 2: In the event of a short circuit between pins, or a ground/supply fault in output, there is a possibility that device is destroyed or ignited, or over-voltage or over-current may be applied to peripheral components. Therefore, be especially careful when designing the output lines, VM lines, VDRAIN lines and ground lines.
In addition, rotary insertion (reverse insertion) of the device may also cause breakdown or ignition.
Note 3: The application circuit examples are not guaranteed for mass production design.
Thorough evaluation is required, especially at the mass production design stage.
Providing these application circuit examples does not grant a license for industrial property rights.

13. Package Dimensions

13.1. P-VQFN32-0505-0.50-007

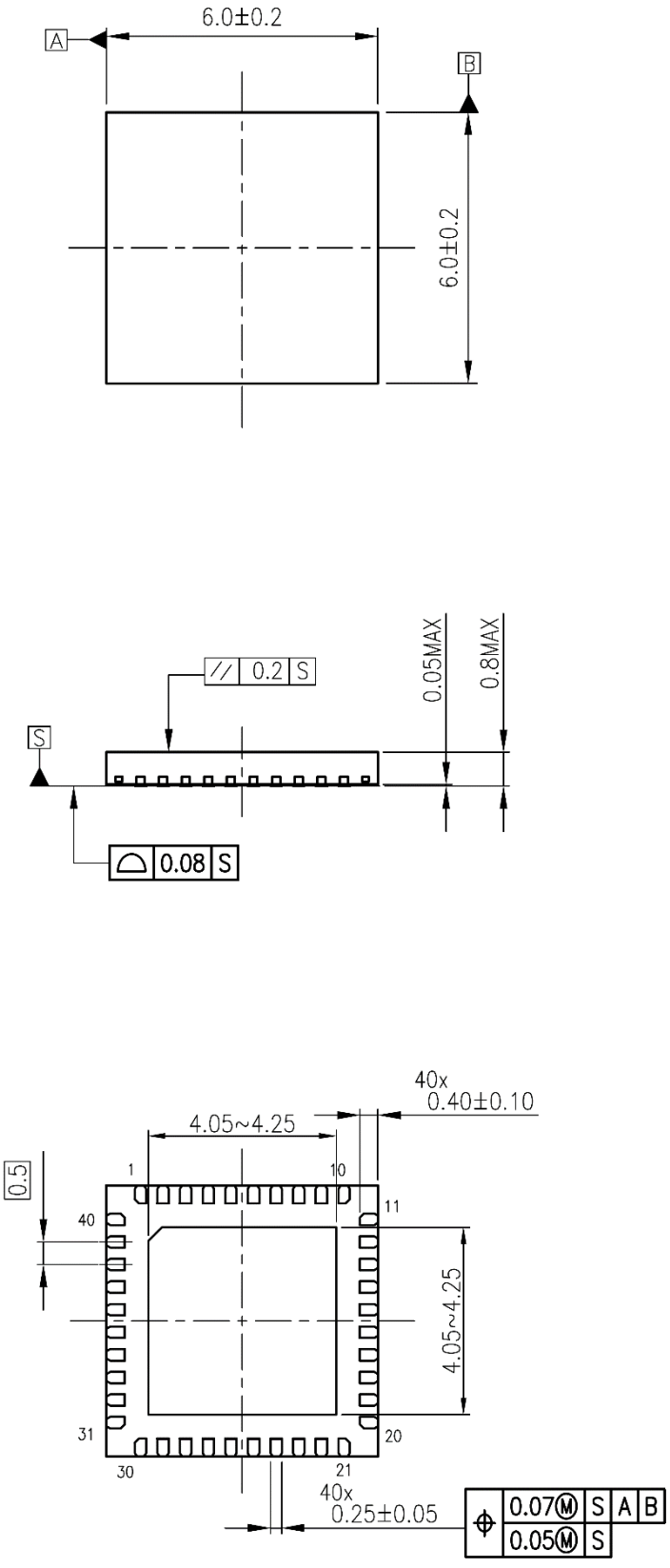
Unit: mm



Weight: 0.065g (typ.)

13.2. P-WQFN40-0606-0.50-003

Unit: mm



Weight: 0.09g (typ.)

14. Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

15. IC Usage Considerations

15.1. Notes on Handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage, or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke, or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

15.2. Points to Remember on Handling of ICs

[1] Over current Protection Circuit

Over current protection circuits do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

[2] Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

[3] Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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