Data Sheet

ADE9178

Energy Management DSP with PEN Fault Detection

FEATURES

- Metrology chip for use with any combination of the following AFEs
  - ADE9113 (3-channel, isolated, Σ-Δ ADC)
  - ADE9112 (2-channel, isolated, Σ-Δ ADC)
  - ADE9103 (3-channel, non-isolated, Σ-Δ ADC)
- Can support up to four ADE9113/ADE9112/ADE9103 daisy-chained ADCs through 4-wire SPI
  - Supports up to a total of 12 ADC channels of data
- 4-wire SPI for Host MCU communications up to 25 MHz
- Total active energy calculation
- Class C accuracy (0.5%), supports the following
  - MID 2014/32/EU Annex V
  - EN 50470-1:2006
  - EN 50470-3:2006
  - EN 50470-3:2022
  - IEC 62052-11:2020
  - IEC 62053-21:2020
  - OIML G 22:2022
  - NIST Handbook 44:2023
- Total apparent energy calculation using filtered RMS
- Energy accumulation, import and export for reverse power/vehicle to grid (V2G) applications
- Basic power quality features
  - Short-duration undervoltage or overvoltage (dip/swell) detection
  - Short-duration undercurrent or overcurrent (dip/swell) detection
  - Line frequency calculation with 10 mHz accuracy
  - Angles between phase voltages and currents
  - Power-factor calculation
- Configurable phase, gain and offset calibration registers for all ADC channels
- Two configurable calibration frequency (CF) pulse outputs
- Configurable: no load detection
- Phase-sequence detection
- RMS on full cycle, half cycle and filtered RMS on all ADC channels
- Supported frequency range: 45 Hz to 65 Hz
- Four user-programmable interrupt outputs (IRQs)
- PEN open fault detection (BS 7671:2018 Amendment 1:2020)
- Waveform streaming through UART transmit pin
- Datapath multiplexing to allow any ADC data to be used for any data processing path
- Temperature range: −40°C to +105°C
- Available in 5 mm × 5 mm, 40-lead TQFN-EP package

APPLICATIONS

- Electric vehicle supply equipment
- Shunt-based polyphase meters
- Solar inverters
- Energy and power monitoring

GENERAL DESCRIPTION

The ADE9178 is a metrology digital signal processor (DSP) for use with a combination of ADE9113/ADE9112/ADE9103 sigma delta analog-to-digital converters (ADCs). The ADE9178 is a high accuracy, 3-phase electrical energy measurement IC primarily for the electric vehicle supply equipment (EVSE) market with serial peripheral interface (SPI) and two flexible pulse outputs. The ADE9178 can interface with up to four daisy-chained ADE9113/ADE9112/ADE9103 devices through SPI protocol. The ADE9178 incorporates all the signal processing required to perform total active energy, apparent energy measurements, and root mean square (RMS) calculations. A fixed function DSP executes this signal processing.

The ADE9178 is well-suited for the EVSE market due to its broad feature set such as protective earth and neutral (PEN) open fault detection without the need for any additional hardware, overcurrent, and overvoltage detection using RMS of half cycle/one cycle and vehicle to grid/home (V2X) capabilities.

The ADE9178 measures active and apparent energy in various 3-phase configurations, such as wye or delta services, with both three and four wires, single phase, and split phase while supporting both 50 Hz and 60 Hz line frequencies. The ADE9178 provides gain, offset, and phase calibration features for each ADC channel. The CF1 and CF2 logic outputs provide power information that is proportional to the measured accumulated energy.

The ADE9178 incorporates some basic power quality measurement features, such as short-duration undervoltage/undercurrent or overvoltage/overcurrent detection, line voltage period measurements, and angles between phase voltages and currents. A Host microcontroller unit (MCU) can be used to communicate with the ADE9178 through 4-wire SPI. Waveform streaming can be accessed by the Host MCU through the WAVEFORM_TX pin of the ADE9178. The ADE9178 also has four user-programmable interrupt pins, $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, and $\overline{\text{IRQ3}}$, to indicate that an enabled interrupt event has occurred. The ADE9178 is available in a 40-lead, TQFN-EP package.

For more details on how to setup the ADE9178 in an EVSE application, refer to the application note Using ADE9178 for EV Charger Metrology Solution.

Rev. 0, 19-101907, 7/24

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

7/2024—Revision 0: Initial Version

TYPICAL APPLICATIONS CIRCUIT

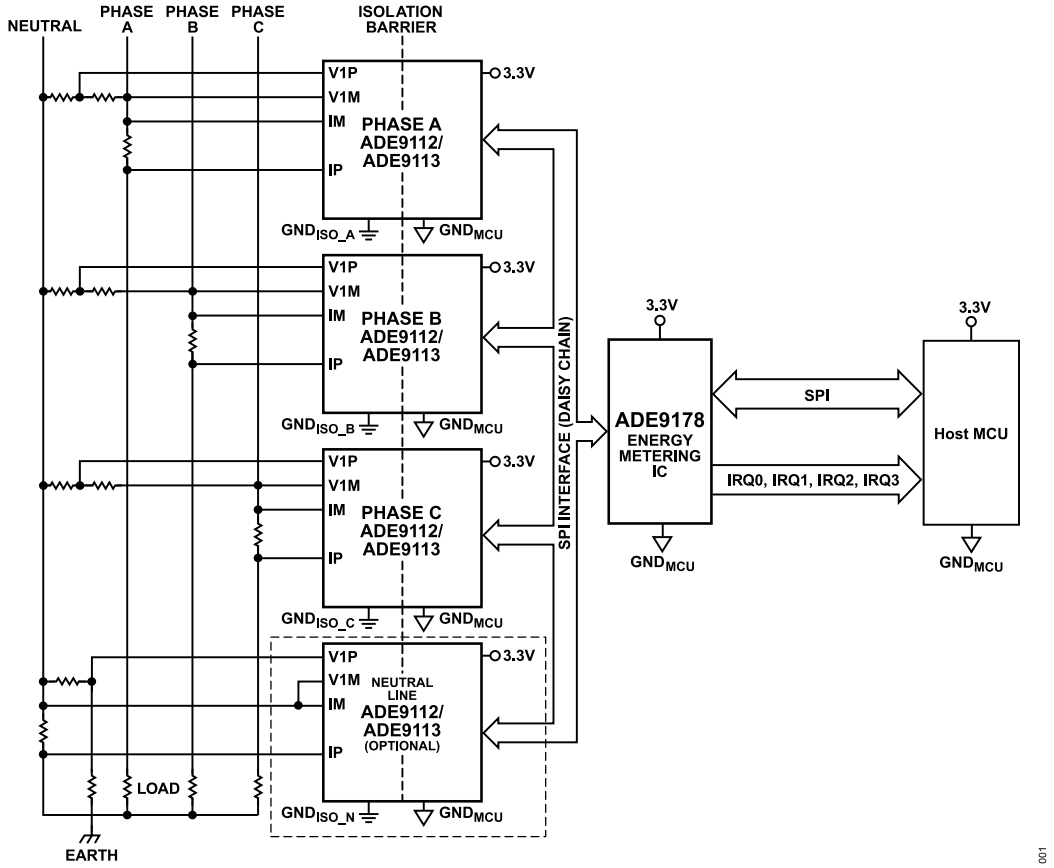

Figure 1. Typical Applications Circuit

FUNCTIONAL BLOCK DIAGRAM

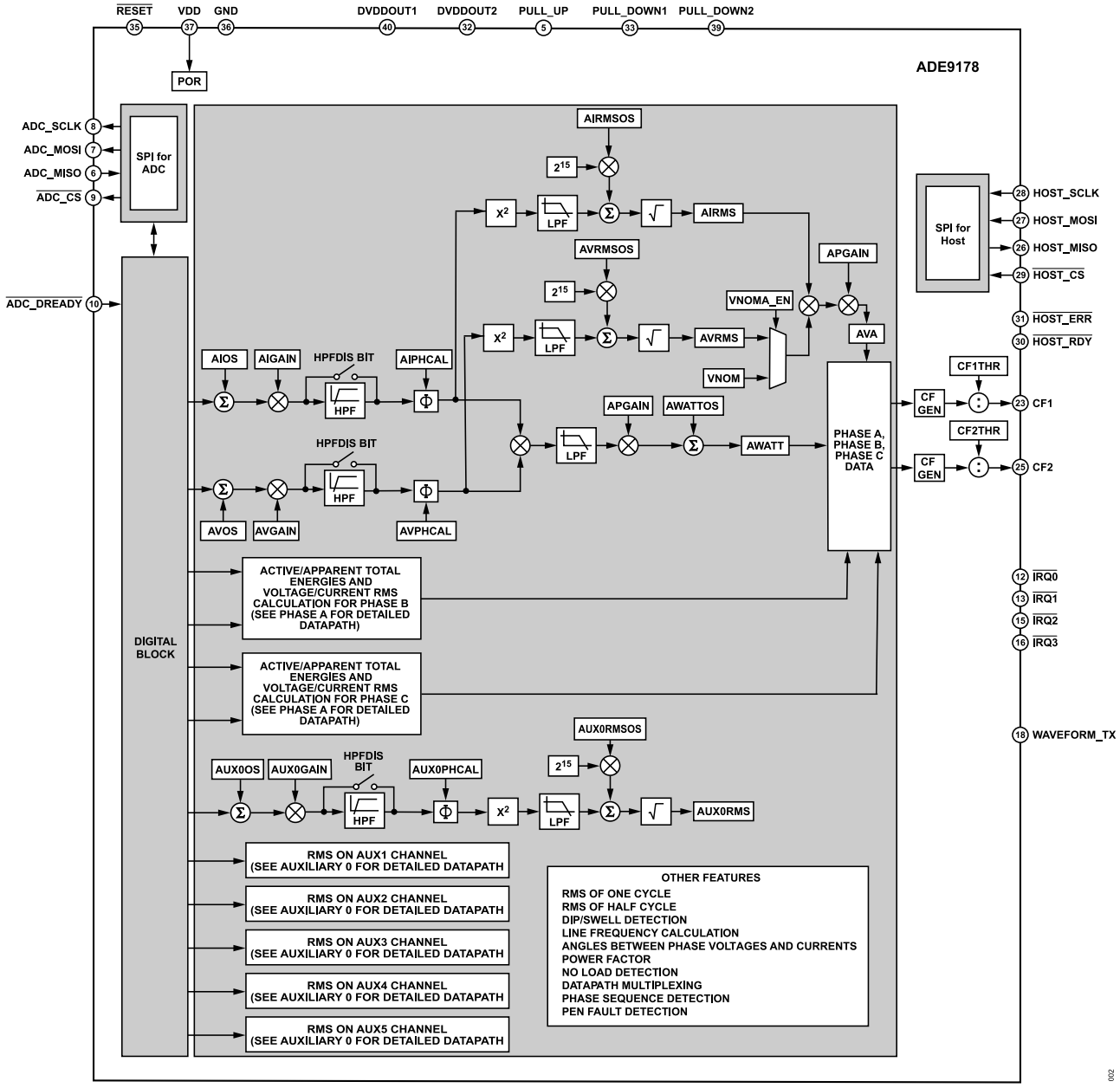

Figure 2. Functional Block Diagram

SPECIFICATIONS

SYSTEM SPECIFICATIONS FOR ADE9178, ADE9103, ADE9112, AND ADE9113

V_{DD} = 3.3 V ± 10%, GND = DGND = 0 V, T_{MIN} to T_{MAX} = −40°C to +105°C, T_{TYP} = +25°C, and high-pass filter (HPF) on, unless otherwise noted.

Table 1. System Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TOTAL ACTIVE ENERGY					
Measurement Error (3-Phases)					
Total Active Energy		0.1		%	Over a dynamic range of 2000 to 1, power factor (PF) = 1, 10 second accumulation, power offset calibration applied
		0.2		%	Over a dynamic range of 2000 to 1, power factor (PF) = 1, 10 second accumulation, no power offset calibration applied
Total Active Energy Bandwidth		1.65		kHz	ADE91xx LPF_BW = 0
TOTAL APPARENT ENERGY					
Measurement Error (3-Phases)					
Total Apparent Energy		0.1		%	Over a dynamic range of 2000 to 1, power factor (PF) = 1, 10 second accumulation, RMS offset calibration applied
		0.6		%	Over a dynamic range of 2000 to 1, power factor (PF) = 1, 10 second accumulation, no RMS offset calibration applied
RMS MEASUREMENTS					
Filtered IRMS		0.4		%	Over a dynamic range of 2000 to 1, average of 1 sample per line cycle for 1 second, RMS offset calibration applied
		0.65		%	Over a dynamic range of 2000 to 1, average of 1 sample per line cycle for 1 second, no RMS offset calibration applied
Filtered VRMS		0.2		%	Over a dynamic range of 2000 to 1, average of 1 sample per line cycle for 1 second, RMS offset calibration applied
		0.2		%	Over a dynamic range of 2000 to 1, average of 1 sample per line cycle for 1 second, no RMS offset calibration applied
IRMS of Half Cycle		2.5		%	Over a dynamic range of 1000 to 1, based on a single result, RMS offset calibration applied
		2.5		%	Over a dynamic range of 1000 to 1, based on a single result, no RMS offset calibration applied
VRMS of Half Cycle		1		%	Over a dynamic range of 1000 to 1, based on a single result, RMS offset calibration applied
		1		%	Over a dynamic range of 1000 to 1, based on a single result, no RMS offset calibration applied
IRMS of Full Cycle		2		%	Over a dynamic range of 1000 to 1, based on a single result, RMS offset calibration applied
		2		%	Over a dynamic range of 1000 to 1, based on a single result, no RMS offset calibration applied
VRMS of Full Cycle		0.5		%	Over a dynamic range of 1000 to 1, based on a single result, RMS offset calibration applied
		0.5		%	Over a dynamic range of 1000 to 1, based on a single result, no RMS offset calibration applied
METROLOGY MESUREMENTS					
Phase Angle					
Measurement Error		0.5		Degrees	Over a dynamic range of 100 to 1, line frequency = 45 Hz to 65 Hz, phase angle = 0° to 360°, HPF on
Power Factor					
Measurement Error		0.005		PF	Over a dynamic range of 2000 to 1, power factor (PF)= −1 to 1

SPECIFICATIONS

Table 1. System Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Period					
Measurement Error		5		mHz	Line frequency = 45 Hz to 65 Hz, CONFIG0:PERIOD_AVG_CFG[4:3] = 0x0 (no period averaging)
CF1, CF2 PULSE OUTPUTS					
Output Frequency			500	Hz	CF saturates at 1 kHz but performance specification is up to 500 Hz
Active-Low Pulse Width	0.2			ms	
CF1 Jitter		0.1		%	Voltage = 50% of full scale, current over dynamic range of 2000 to 1, CF1_THR = d1341078 = 500 Hz at current full scale, CF2 disabled
		0.1		%	Voltage = 50% of full scale, current over dynamic range of 2000 to 1, CF1_THR = d22351312 = 30 Hz at current full scale, CF2 disabled
CF2 Jitter		0.5		%	Voltage = 50% of full scale, current over dynamic range of 2000 to 1, CF1_THR = d1341078 = 500 Hz at current full scale, CF1 enabled
		0.1		%	Voltage = 50% of full scale, current over dynamic range of 2000 to 1, CF1_THR = d22351312 = 30 Hz at current full scale, CF1 enabled
BOOT TIME					
System-Level Boot Time		16		ms	From RSTN pin toggle to RSTDONE flag being set, V_{DD} ≥ 2.97 V
ADE91xx CLOCK					
Input Clock Frequency		16.384		MHz	
Tolerance			1000	ppm	

SPECIFICATIONS

ADE9178 SPECIFICATIONS

Table 2. ADE9178 Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{DD}	2.97	3.3	3.63	V	
I_{DD} Startup		55		mA	During POR, there is a spike in current
I_{DD} Operating		13		mA	Typical I_{DD} during normal operation
LOGIC INPUTS					ADC_MISO, HOST_MOSI, HOST_SCLK, $\overline{\text{HOST\_CS}}$, $\overline{\text{ADC\_DREADY}}$, and $\overline{\text{RESET}}$
Input High Voltage (V_{INH})	2.31			V	
Input Low Voltage (V_{INL})			0.99	V	
Internal Capacitance (C_{IN})		4		pF	
LOGIC OUTPUTS					ADC_MOSI, ADC_SCLK, $\overline{\text{ADC\_CS}}$
Output High Voltage (V_{OH})	2.9			V	
Source Current (I_{SOURCE})		8		mA	
Output Low Voltage (V_{OL})		0.2	0.4	V	
Sink Current (I_{SINK})		8		mA	
LOGIC OUTPUTS					$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{IRQ3}}$, HOST_MISO, and CF1
Output High Voltage (V_{OH})	2.9			V	
Source Current (I_{SOURCE})		12		mA	
Output Low Voltage (V_{OL})		0.2	0.4	V	
Sink Current (I_{SINK})		12		mA	
LOGIC OUTPUTS					CF2, $\overline{\text{HOST\_RDY}}$, and $\overline{\text{HOST\_ERR}}$
Output High Voltage (V_{OH})	2.9			V	
I_{SOURCE}		20		mA	
Output Low Voltage (V_{OL})		0.2	0.4	V	
I_{SINK}		20		mA	

SPECIFICATIONS

SPI TIMING PARAMETERS

Table 3. SPI Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ to SCLK Positive Edge	t_{SS}		10		ns
SCLK Frequency	f_{SCLK}			25	MHz
SCLK Period	t_{SCLK}		$1/f_{SCLK}$		ns
SCLK Low-Pulse Width	t_{SL}		$t_{SCLK}/2$		ns
SCLK High-Pulse Width	t_{SH}		$t_{SCLK}/2$		ns
Data-Input Setup Time Before SCLK Edge	t_{DSU}		5		ns
Data-Input Hold Time After SCLK Edge	t_{DHD}		1		ns
MISO Disable After $\overline{CS}$ Rising Edge	t_{DIS}		10		ns
$\overline{CS}$ High After SCLK Edge	t_{SFS}		10		ns
$\overline{CS}$ High-Pulse Width	t_{CH}		$1/f_{SCLK}$		ns

Timing Diagram

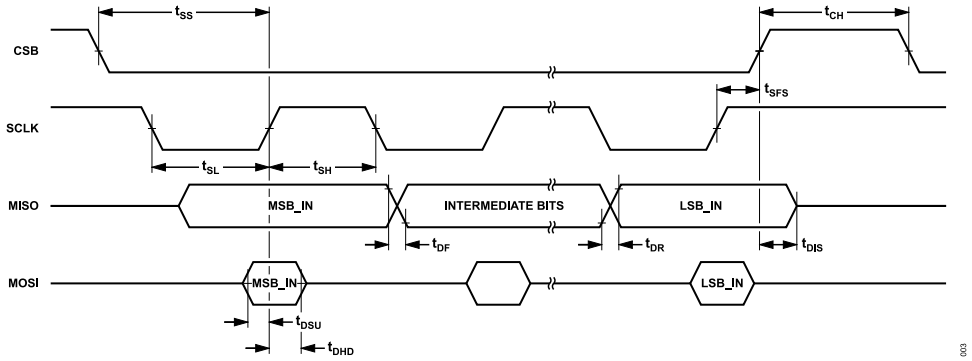

Figure 3. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4. Absolute Maximum Ratings

Parameter	Rating
VDD to GND	−0.3 V to +3.63 V
$\overline{\text{RESET}}$, GPIO's to GND	−0.3 V to VDD + 0.3 V
Total Current into ALL GPIO Combined	100 mA
GND	100 mA
Output Current (sink) by Any GPIO Pin	25 mA
Output Current (source) by Any GPIO Pin	−25 mA
Continuous Package Power Dissipation 40-Lead TQFN-EP (multilayer board), T_A = +70°C (derate 35.7 mW/°C above +70°C)	2857.10 mW
Temperature	
Operating Range	−40°C to +105°C
Storage Range	−65°C to +125°C
Soldering (reflow)	+260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction-to-case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-33	45.0	2.0	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

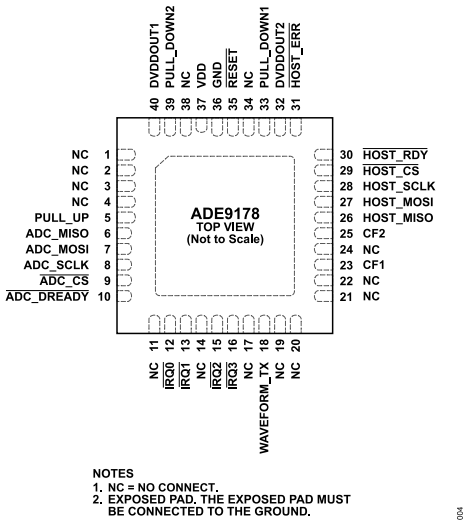

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Input/Output	Active Low/High	Description
1, 2, 3, 4, 11, 14, 17, 19, 20, 21, 22, 24, 34, 38	NC	N/A[1]	N/A[1]	No Connect.
5	PULL_UP	N/A[1]	N/A[1]	10 kΩ Pull-Up to VDD.
6	ADC_MISO	Input	Active High	Data Input for the ADC SPI Port to the supported Analog Front End (AFEs).
7	ADC_MOSI	Output	Active High	Data Output for the ADC SPI Port from the supported AFEs.
8	ADC_SCLK	Output	Active High	Serial-Clock Output for the ADC SPI Port.
9	$\overline{\text{ADC\_CS}}$	Output	Active Low	Chip Select for ADC SPI Port.
10	$\overline{\text{ADC\_DREADY}}$	Input	Active Low	DREADY Input, Signal to let ADE9178 know that ADC samples are ready.
12, 13, 15, 16	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{IRQ3}}$	Output	Active Low	User-Programmable Interrupt Request Output.
18	WAVEFORM_TX	Output	Active High	Waveform Streaming through a UART transmit pin.
23, 25	CF1, CF2	Output	Active High	Calibration Frequency (CF) Logic Output. This output provides power information and is used for operational and calibration purposes.
26	HOST_MISO	Output	Active High	Data Output for the SPI Port to the Host MCU.
27	HOST_MOSI	Input	Active High	Data Input for the SPI Port from the Host MCU.
28	HOST_SCLK	Input	Active High	Serial-Clock Input from the Host MCU.
29	$\overline{\text{HOST\_CS}}$	Input	Active Low	Chip-Select Input for Host SPI Port.
30	$\overline{\text{HOST\_RDY}}$	Output	Active Low	Flag to let the Host MCU know that response from the Host Command is ready.
31	$\overline{\text{HOST\_ERR}}$	Output	Active Low	Flag to let the Host MCU know that there is an error during the Command processing.
32	DVDDOUT2	N/A[1]	N/A[1]	Bypass with 4.7 nF to GND.
33, 39	PULL_DOWN1, PULL_DOWN2	N/A[1]	N/A[1]	1 kΩ Pull-Down to GND.
35	$\overline{\text{RESET}}$	Input	Active Low	External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic) and begins execution.
36	GND	N/A[1]	N/A[1]	Ground Reference for the Input Circuitry.
37	VDD	Input	N/A[1]	Supply Voltage. This pin provides the supply voltage. For specified operation, maintain the supply voltage at 3.3 V ± 10%. Bypass with 100 nF to GND and 1 µF with 10 mΩ to 150 mΩ equivalent series resistance (ESR) to GND.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Input/Output	Active Low/High	Description
40	DVDDOUT1	N/A[1]	N/A[1]	Bypass with 100 nF to GND and 1 µF with 10 mΩ to 150 mΩ ESR to GND.
EP	EPAD	N/A[1]	N/A[1]	Exposed pad. The exposed pad must be connected to the ground.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY LINEARITY OVER SUPPLY AND TEMPERATURE

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale, a sinusoidal current with variable amplitude from 100% of full scale down to 0.05% of full scale. Frequency = 50 Hz and PF = 1.

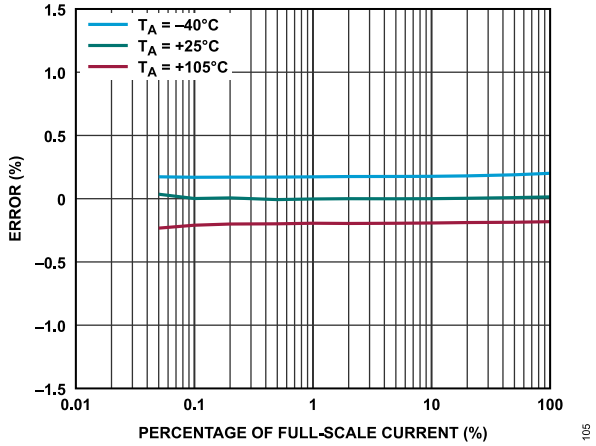

Figure 5. Total Active Energy as a Percentage of Reading Over Temperature

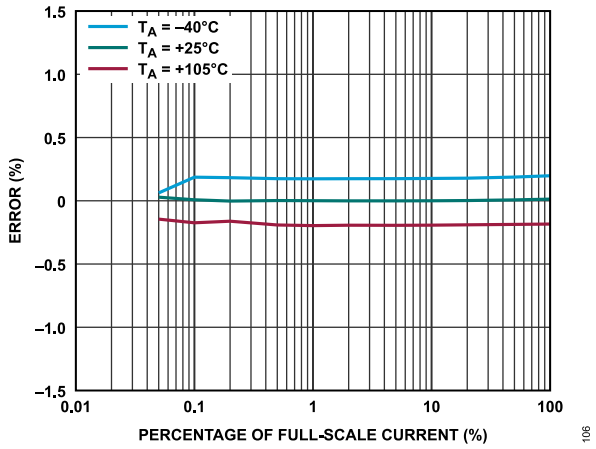

Figure 6. Total Apparent Energy Error as a Percentage of Reading Over Temperature

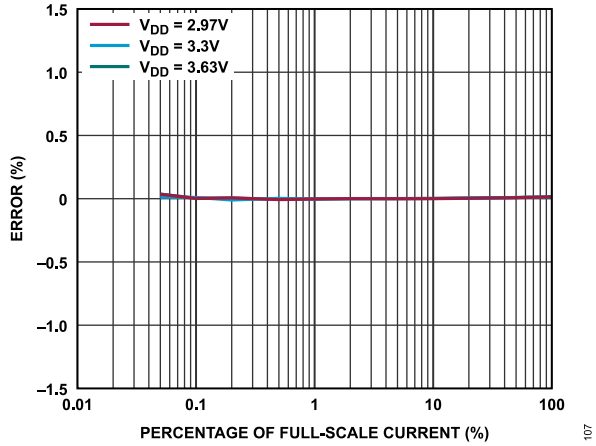

Figure 7. Total Active Energy as a Percentage of Reading Over Supply, T_A = 25°C

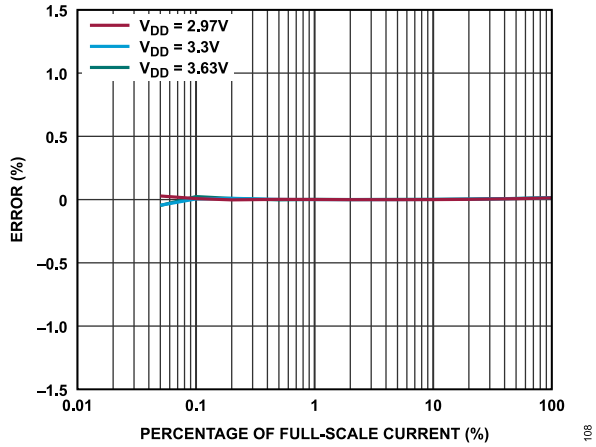

Figure 8. Total Apparent Energy as a Percentage of Reading Over Supply, T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY ERROR OVER FREQUENCY AND POWER FACTOR

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale, a sinusoidal current with an amplitude of 10% of full scale. Variable frequency between 45 Hz and 65 Hz. T_A = 25°C, V_{DD} = 3.3 V.

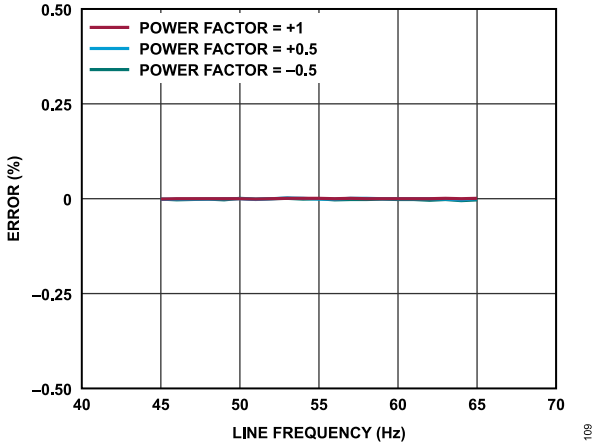

Figure 9. Total Active Energy Error as a Percentage of Reading Over Frequency, PF = +1, +0.5, −0.5

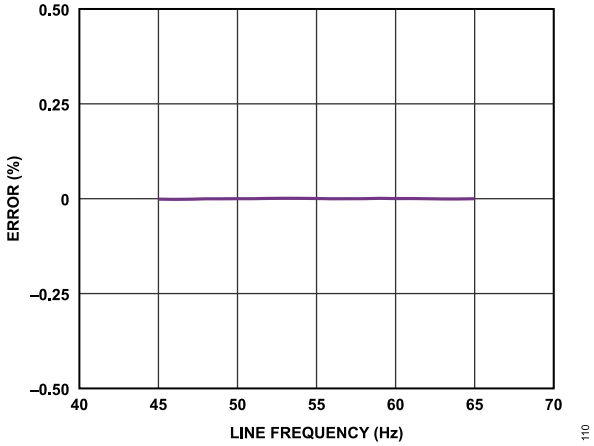

Figure 10. Total Apparent Energy Error as a Percentage of Reading Over Frequency, PF = +1

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY LINEARITY REPEATABILITY

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale, a sinusoidal current with variable amplitude from 100% of full scale down to 0.05% of full scale. Frequency = 50 Hz, PF = 1, T_A = 25°C and V_{DD} = 3.3 V. Measurement repeated 30 times.

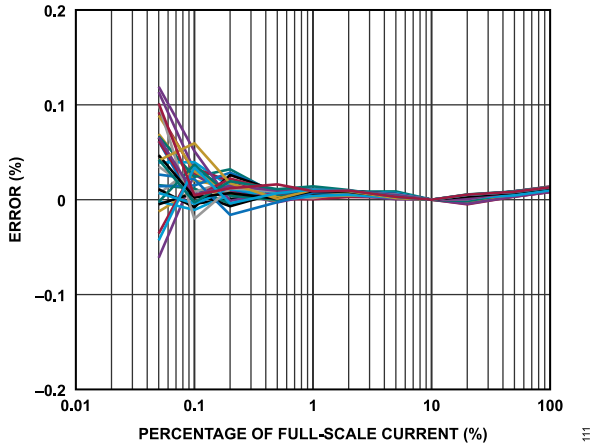

Figure 11. Total Active Energy Error as a Percentage of Full-Scale Current

TYPICAL PERFORMANCE CHARACTERISTICS

RMS LINEARITY OVER TEMPERATURE AND RMS ERROR OVER FREQUENCY

RMS linearity obtained from a variable sinusoidal voltage and current from 100% of full scale down to 0.05% of full scale. Frequency = 50 Hz, PF = 1, V_{DD} = 3.3 V and HPF on.

RMS error obtained from a sinusoidal voltage with an amplitude of 50% of full scale and a sinusoidal current with an amplitude of 50% of full scale. Variable frequency between 45 Hz and 65 Hz. T_A = 25°C, V_{DD} = 3.3 V and HPF on.

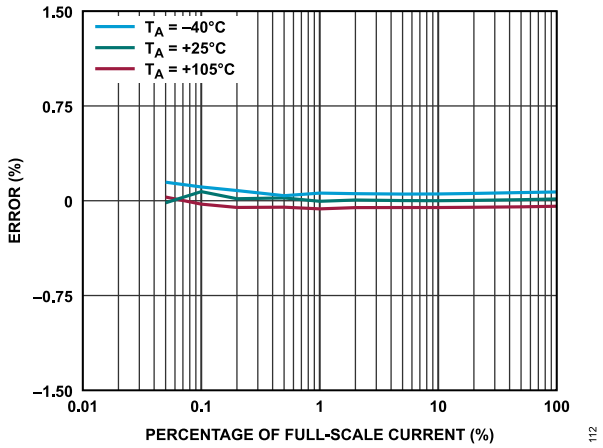

Figure 12. Current Filtered RMS Error as a Percentage of Reading Over Temperature

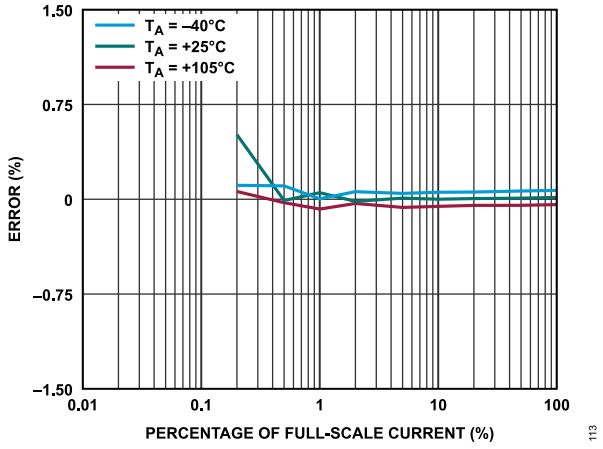

Figure 13. Current One Cycle RMS Error as a Percentage of Reading Over Temperature

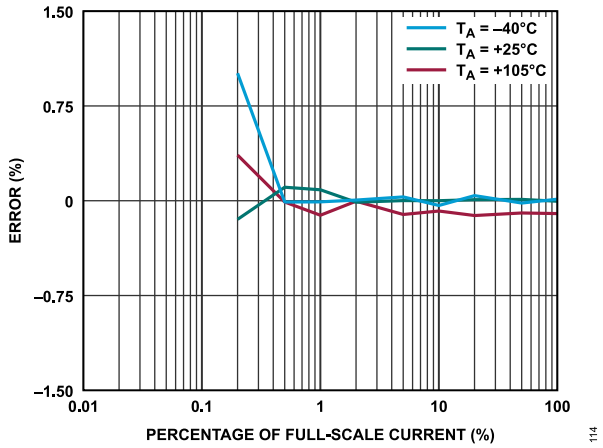

Figure 14. Current Half Cycle RMS Error as a Percentage of Reading Over Temperature

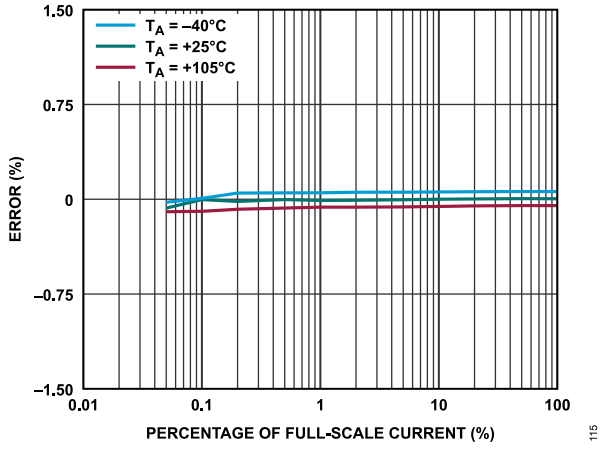

Figure 15. Voltage Filtered RMS Error as a Percentage of Reading Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

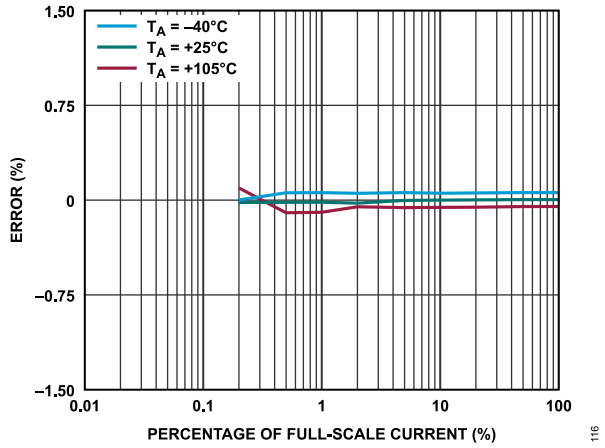

Figure 16. Voltage One Cycle RMS Error as a Percentage of Reading Over Temperature

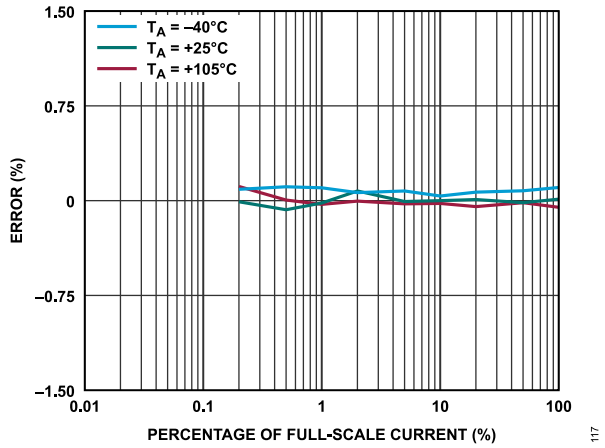

Figure 17. Voltage Half Cycle RMS Error as a Percentage of Reading Over Temperature

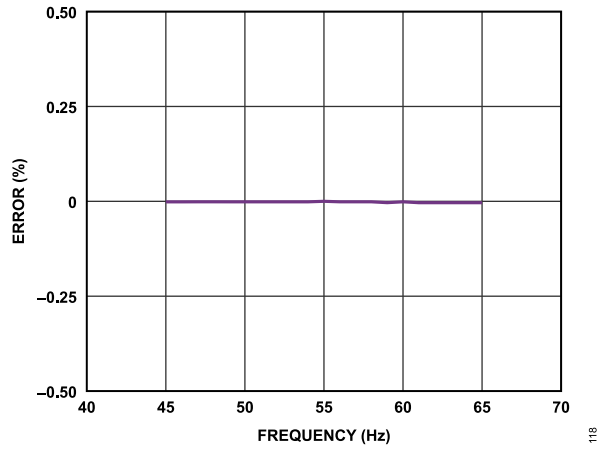

Figure 18. Current Filtered RMS Error as a Percentage of Reading Over Frequency

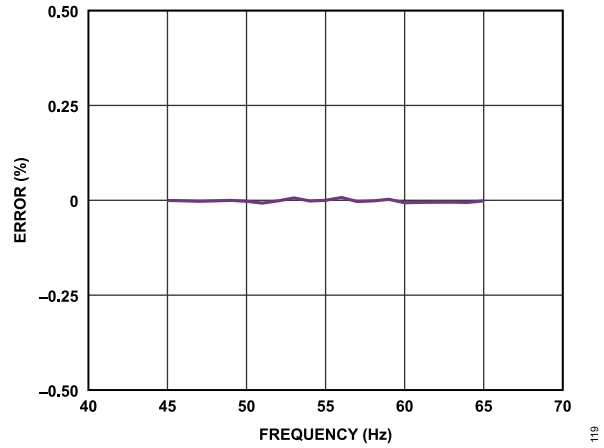

Figure 19. Current One Cycle RMS Error as a Percentage of Reading Over Frequency

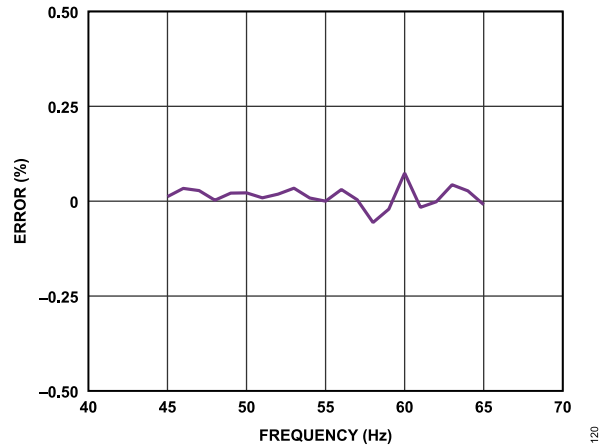

Figure 20. Current Half Cycle RMS Error as a Percentage of Reading Over Frequency

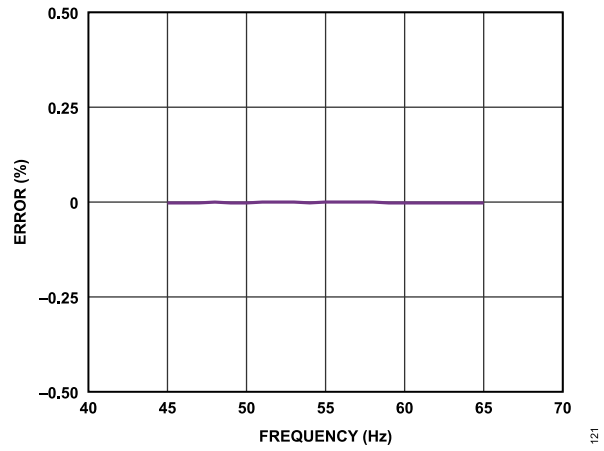

Figure 21. Voltage Filtered RMS Error as a Percentage of Reading Over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

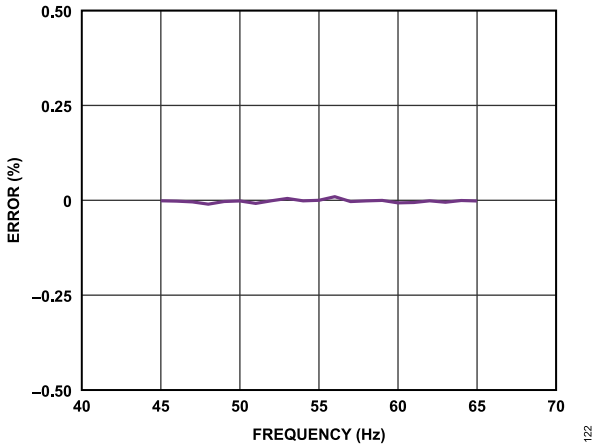

Figure 22. Voltage One Cycle RMS Error as a Percentage of Reading Over Frequency

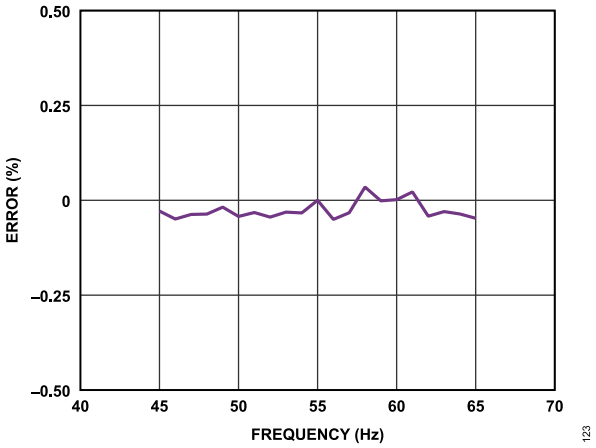

Figure 23. Voltage Half Cycle RMS Error as a Percentage of Reading Over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

CF vs. ENERGY REGISTER CORRELATION AND CF JITTER

CF vs. energy register correlation obtained from a sinusoidal voltage with an amplitude of 50% of full scale, a sinusoidal current with variable amplitude from 100% of full scale down to 0.05% of full scale. Frequency = 50 Hz, PF = 1, T_A = 25°C and V_{DD} = 3.3 V.

CF jitter obtained from a sinusoidal voltage with an amplitude of 50% of full scale, a sinusoidal current with variable amplitude from 100% of full scale down to 0.05% of full scale. Frequency = 50 Hz, PF = 1, T_A = 25°C and V_{DD} = 3.3 V. CFx_THR set to d1341078, which equates to 500 Hz CF output at full-scale current and CFx_THR set to d22351312, which equates to 30 Hz at full-scale current.

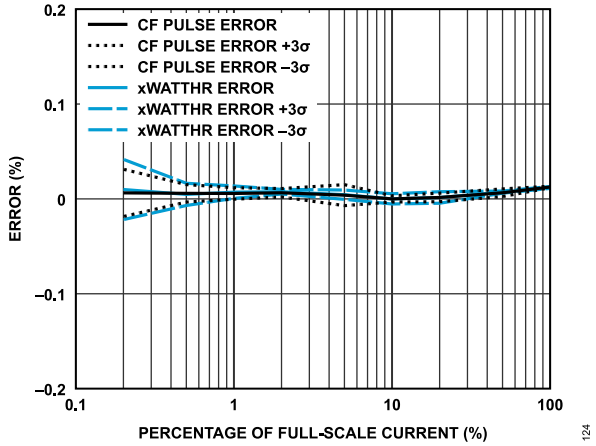

Figure 24. Correlation Between CF Pulse and Registers for Total Active Energy Accumulation

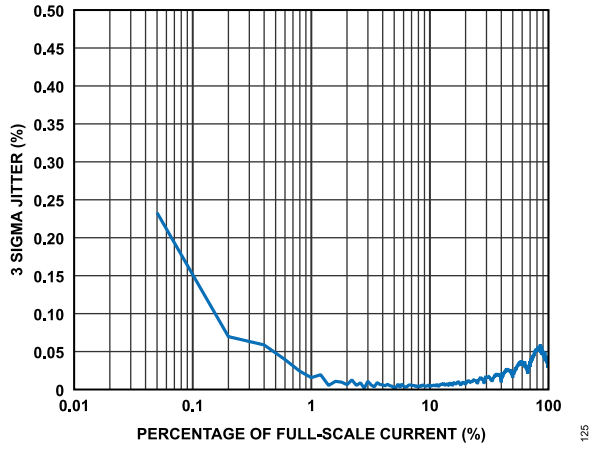

Figure 25. CF1 Jitter Over Current Full Scale, CF1_THR = d1341078, CF2 Disabled

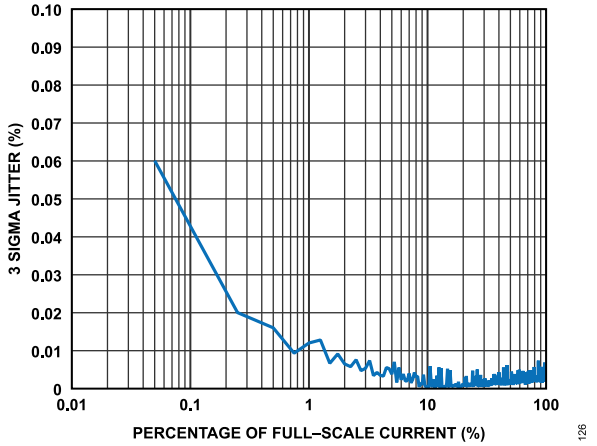

Figure 26. CF1 Jitter Over Current Full Scale, CF1_THR = d22351312, CF2 Disabled

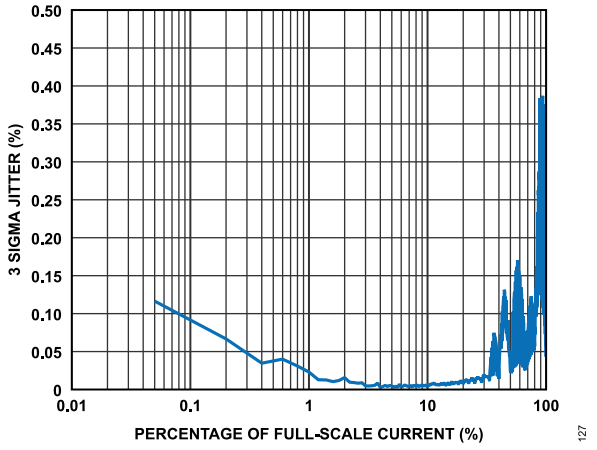

Figure 27. CF2 Jitter Over Current Full Scale, CF2_THR = d1341078, CF1 Enabled

TYPICAL PERFORMANCE CHARACTERISTICS

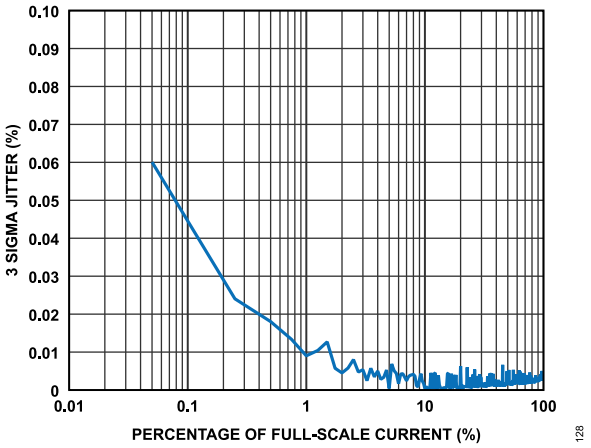

Figure 28. CF2 Jitter Over Current Full Scale, CF2_THR = d22351312, CF1 Enabled

TEST CIRCUIT

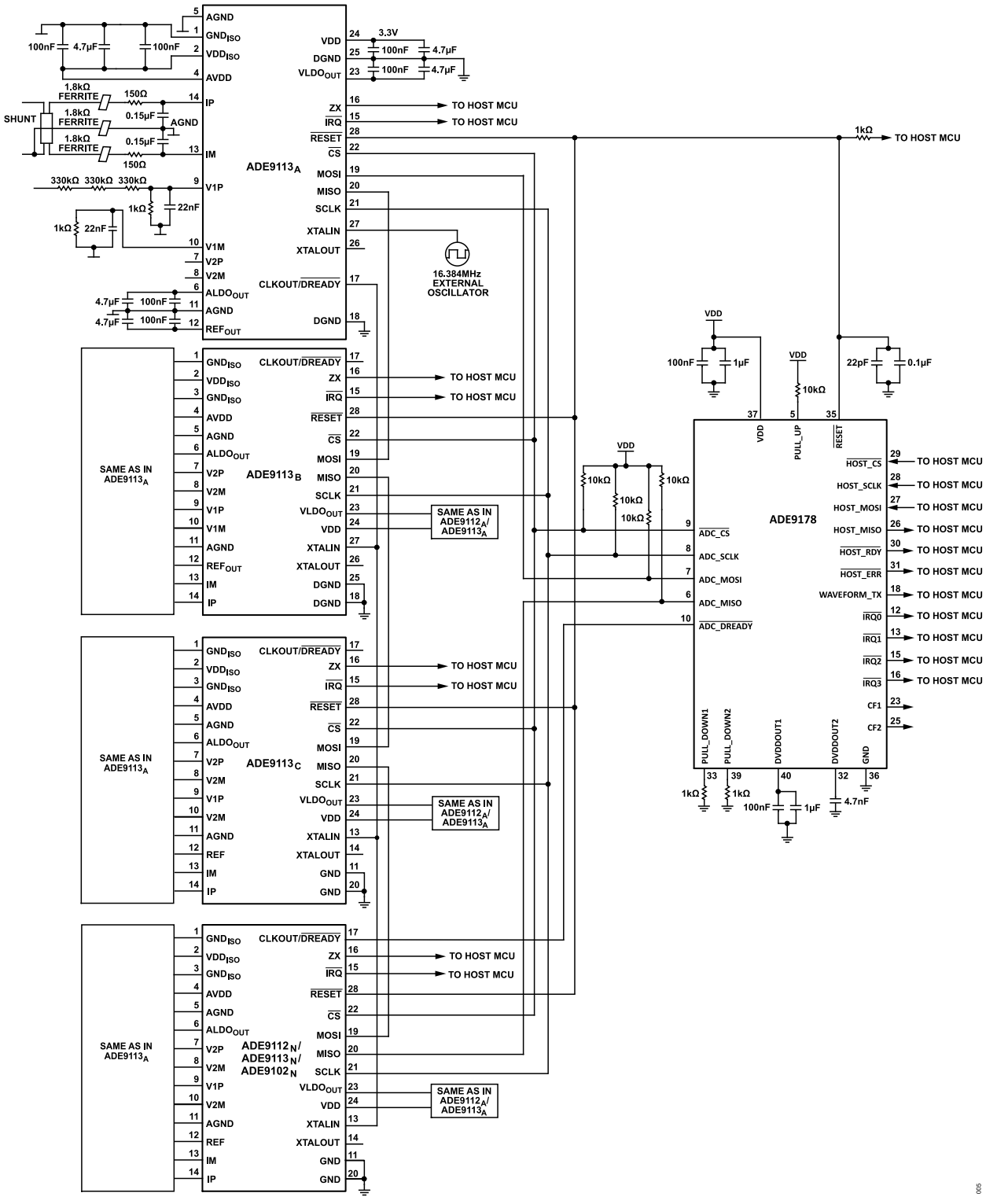

Figure 29. ADE9178 + ADE91xx Test Circuit

TERMINOLOGY

For the common terminology, refer to the Analog Wiki.

THEORY OF OPERATION

ADC AND HOST SPI

ADC SPI

The ADE9178 receives ADC samples through ADC SPI. The application should connect the ADC in daisy-chain mode as explained in ADE9113 data sheet. The ADC clock should be provided by crystal to phase A ADC. Clock for phase B, phase C, and phase N ADC's can be connected to DREADY/CLKOUT of phase A as shown in Figure 30. The DREADY of last ADC in the chain should be connected to DREADY input pin of the ADE9178. Figure 30 and Figure 31 show the required connections when four ADCs and three ADCs are connected to ADE9178, respectively. Single and two ADC configurations are also supported.

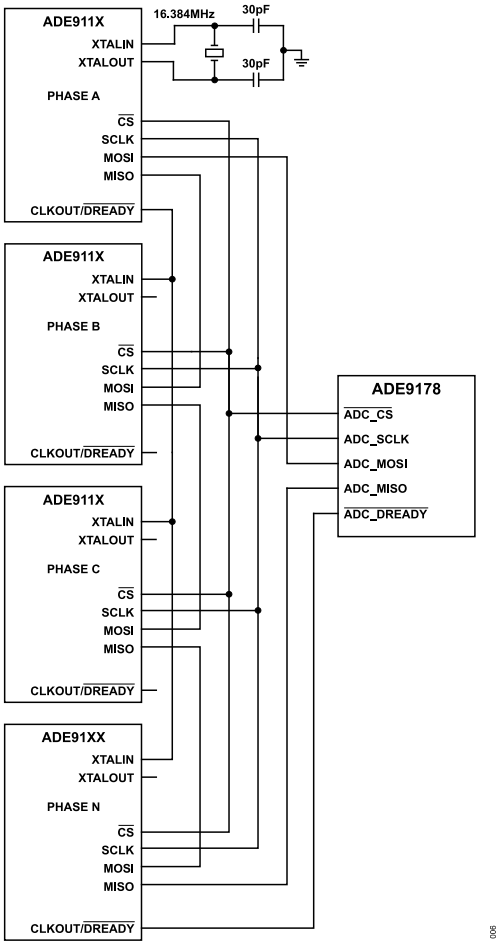

Figure 30. Four ADCs Connection Diagram to ADE9178

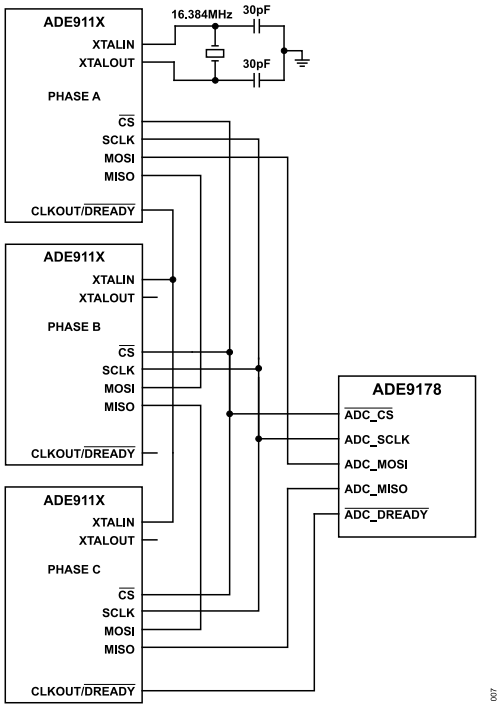

Figure 31. Three ADCs Connection Diagram to ADE9178

The ADE9178 supports three voltage (referred as AV, BV, and CV) and three current channels (referred as AI, BI, and CI) for metrology measurements and six auxiliary channels (AUX0, AUX1, ..., AUX5) for other measurements. The ADE9178 provides a multiplexer option that allows any ADC output to be redirected to any processing datapath by writing appropriate slot number to ADC_REDIRECT0 and ADC_REDIRECT1 register.

In the connections shown in Figure 30 and Figure 31, ADC SPI frames contain the data in the following sequence as shown in Table 7 (with last ADC data comes first). This position in SPI frames is referred as slots in this document where SLOT0 is the I channel of the ADC, which has its MISO connected directly to ADE9178.

THEORY OF OPERATION

Table 7. ADC Channel to ADE9178 SLOT Mapping for Four and Three ADC Configurations

Four ADE9113/ADE9103s Connected (ADC_CONFIG:NUM_ADC = 0x4)			Three ADE9113/ADE9103s Connected (ADC_CONFIG:NUM_ADC = 0x3)			Four ADE9112s Connected (ADC_CONFIG:NUM_ADC = 0x4)		
Phase	**ADC Channel**	**ADE9178 SLOT**	**Phase**	**ADC Channel**	**ADE9178 SLOT**	**Phase**	**ADC Channel**	**ADE9178 SLOT**
N	I	SLOT0	C	I	SLOT0	N	I	SLOT0
N	V1	SLOT1	C	V1	SLOT1	N	V1	SLOT1
N	V2	SLOT2	C	V2	SLOT2	N/A[1]	N/A[1]	SLOT2
C	I	SLOT3	B	I	SLOT3	C	I	SLOT3
C	V1	SLOT4	B	V1	SLOT4	C	V1	SLOT4
C	V2	SLOT5	B	V2	SLOT5	N/A[1]	N/A[1]	SLOT5
B	I	SLOT6	A	I	SLOT6	B	I	SLOT6
B	V1	SLOT7	A	V1	SLOT7	B	V1	SLOT7
B	V2	SLOT8	A	V2	SLOT8	N/A[1]	N/A[1]	SLOT8
A	I	SLOT9	Not present	N/A[1]	SLOT9	A	I	SLOT9
A	V1	SLOT10	Not present	N/A[1]	SLOT10	A	V1	SLOT10
A	V2	SLOT11	Not present	N/A[1]	SLOT11	N/A[1]	N/A[1]	SLOT11

[1] N/A means not applicable.

Note that this means for a change in NUM_ADC value away from default (0x4) the ADC_REDIRECT0 and ADC_REDIRECT1 registers must be updated. For example, with a three ADE91xx configuration shown in Figure 31, SLOT0 is now mapped to the current channel of phase C rather than the current channel of phase N.

For two channel ADCs (ADE9112), the V2 input is not present therefore the V2 data is 0 in the data packet. For the four ADE9112 example shown in Table 7, the ADC_REDIRECT0 and ADC_REDIRECT1 values stay the same as the four ADE9113/ADE9103 example except the data in SLOT2, SLOT5, SLOT8, and SLOT11 is 0.

Table 8 shows the default values to write to ADC_REDIRECT0 and ADC_REDIRECT1 for different NUM_ADC values assuming that the phase sequence matches the examples shown in Table 7 (ADE9178 MOSI connected to the first ADE91xx in the chain and ADE9178 MISO connected to the last ADE91xx in the chain).

For channels that are not present, a slot number of 0x1F should be written to corresponding bitfields of the ADC_REDIRECT0 and ADC_REDIRECT1.

Table 8. Default ADC_REDIRECTx Values

NUM_ADC Value	ADC_REDIRECT0 Value	ADC_REDIRECT1 Value
0x4	0x6431D2A	0x410150B
0x3	0x1190C7	0x3FFF88A8
0x2	0x3FF00464	0x3FFFFC45
0x1	0x3FFFFC01	0x3FFFFFE2

By default, for above connection, following mapping is done where AV1, BV1, and CV1 are mapped to AV, BV, and CV and AV2, BV2, CV2, NI, NV1, and NV2 are mapped to auxiliary channels as shown in Figure 32.

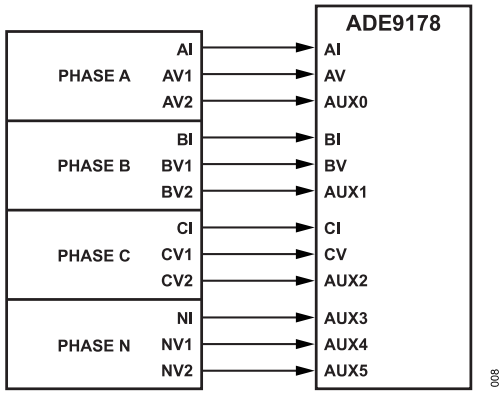

Figure 32. ADC to ADE9178 Channel Mapping

Note that setting ADC_CONTROL RUN bit to 1 sets the sampling rate of the ADCs to 4 kHz.

Multiple ADC Synchronization

If multiple ADCs are connected to ADE9178, the application can periodically issue synchronization of these ADCs through the ADC_CONTROL register. This ensures that all ADCs sample at the same time. The ADC_CONTROL register can be used to synchronize all ADCs periodically. To ensure correct operation, it is recommended to synchronize ADCs by writing ADC_CONTROL = 0x5 (ADC_SYNC = 1, ADC_RUN = 1) once every day. The ADE9178 performs a synchronization sequence if the ADCs are out of synchronization. Note that energy calculation can be disrupted for ~1 ms during synchronization if it is required.

ADC SPI Protocol CRC

The ADE9178 checks whether there are any CRC errors in the data transmitted by ADC over SPI. If there is a CRC error in the data frame transmitted by an ADC, previous correct sample is used for

THEORY OF OPERATION

all calculations for all channels in that ADC. The ADE9178 also raises an error interrupt (ERROR_STATUS:ADC_CRC_ERROR[6]) when this CRC error is detected. It is recommended to check ADC SPI connections if this error persists or raised frequently during development/design time of the application.

Host SPI

The SPI of the ADE9178 always acts as the subordinate and consists of six pins. These pins are shown with prefix HOST in Figure 33. Apart from standard SPI pins, $\overline{\text{HOST\_RDY}}$ or $\overline{\text{HOST\_ERR}}$ signal is used to indicate response is ready or error has occurred.

Data shifts into the device at the MOSI logic input on the falling edge of SCLK, and the device samples the input data on the rising edge of SCLK. Data shifts out of the ADE9178 at the MISO logic output on the falling edge of SCLK and must be sampled by the main device on the rising edge of SCLK. The least significant byte of the word is shifted in and out first. The most significant bit of each byte is sent first.

The ADE9178 is compatible with the following micro controller SPI port clock polarity and phase settings:

CPOL = 1 and CPHA = 1 (typically Mode 3).

The minimum and maximum serial clock frequency supported is 500 kHz and 25 MHz, respectively.

The ADE9178 takes time to a process read or write command. The ADE9178 raises $\overline{\text{HOST\_RDY}}$ when the command is successful. The host program must initiate the SPI read only after this IRQ is raised.

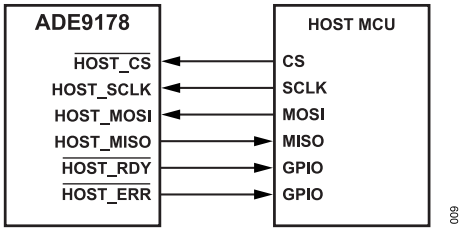

Figure 33. ADE9178 to Host MCU SPI Connection

Table 9. HOST SPI Pin Description

Pins	Description
$\overline{\text{HOST\_CS}}$, HOST_SCLK, HOST_MOSI, HOST_MISO	Standard 4-wire SPI pins.
$\overline{\text{HOST\_ERR}}$	Indicates last command has thrown error.
$\overline{\text{HOST\_RDY}}$	Indicates response for last command is ready.

The $\overline{\text{HOST\_CS}}$ input must stay low for the whole SPI transaction. Bringing $\overline{\text{HOST\_CS}}$ high during a data transfer operation aborts the transfer. A new transfer can be initiated by returning the $\overline{\text{HOST\_CS}}$ logic input low. Therefore, if the application does not need to read back the register value (success case) or the status bits (error case) after a write command the application MCU can toggle $\overline{\text{HOST\_CS}}$ to ignore the returned value.

It is not recommended to connect $\overline{\text{HOST\_CS}}$ to ground because the high-to-low transition on $\overline{\text{HOST\_CS}}$ starts the ADE9178 SPI transaction.

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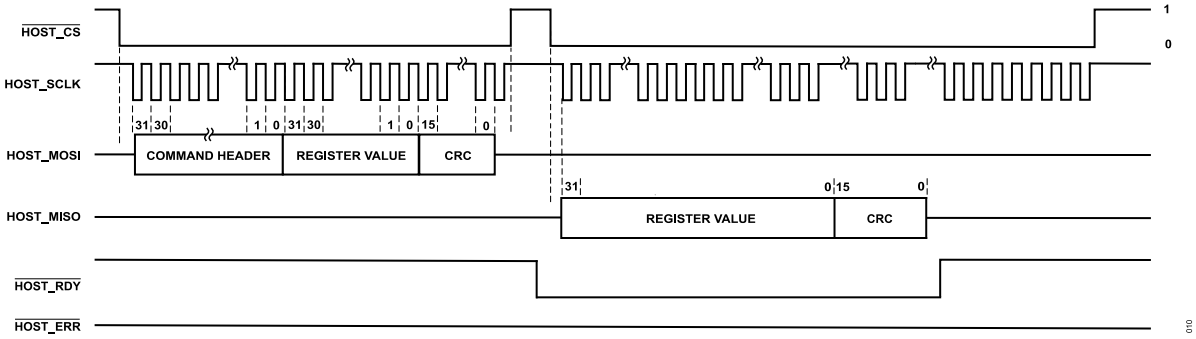

Figure 34. Register Write SPI Protocol − Success Case

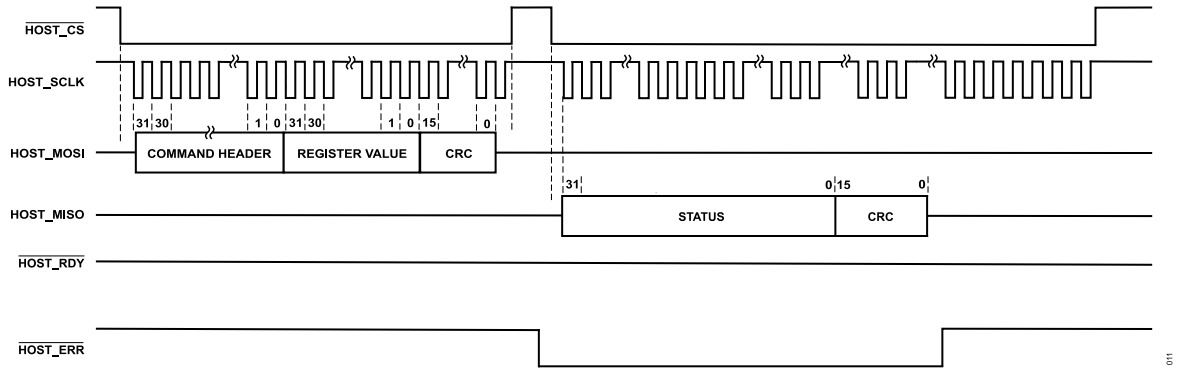

Figure 35. Register Write SPI Protocol − Error Case

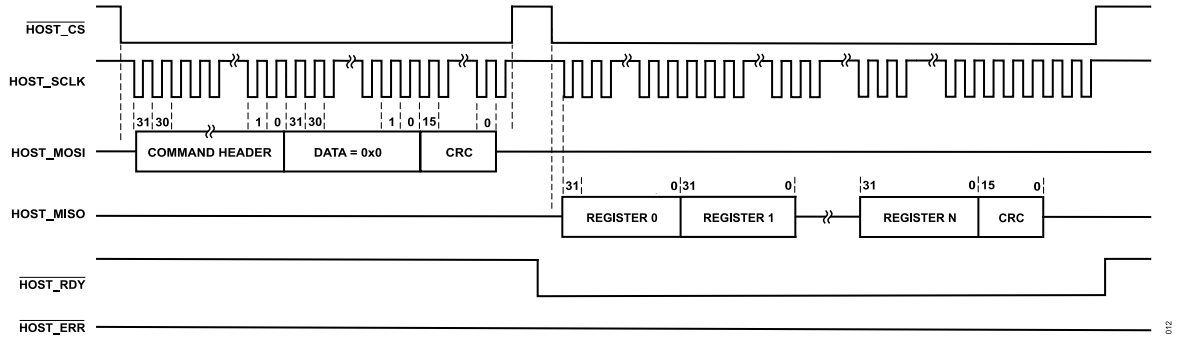

Figure 36. Register Read SPI Protocol − Success Case

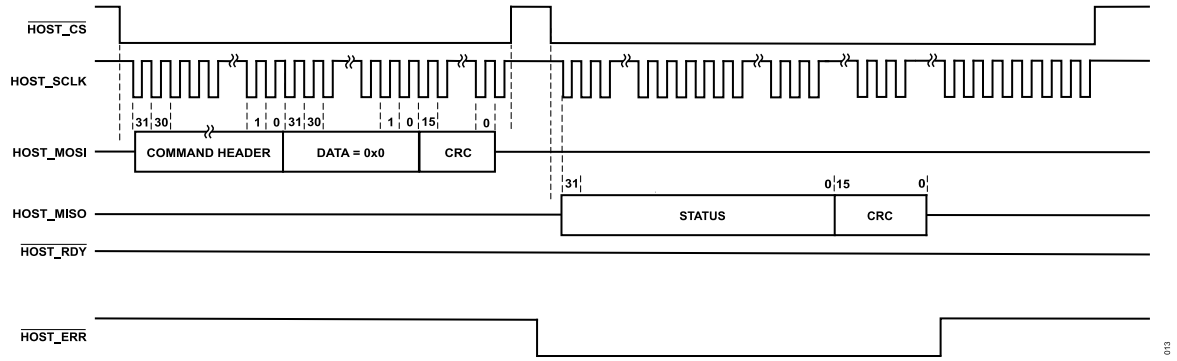

Figure 37. Register Read SPI Protocol − Error Case

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Note that all data including register values for write, read response, and status are 32-bit values and sent over the SPI as least significant byte (LSByte) first as shown in Figure 38.

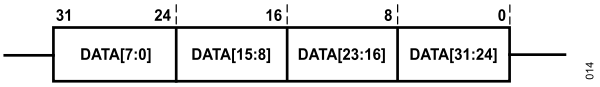

Figure 38. ADE9178 Data/Response SPI Frame Format

The command header is also a 32-bit field with 24th bit indicates if the command is read or write. The format for the write and read command header is shown in Figure 39 and Figure 40, respectively.

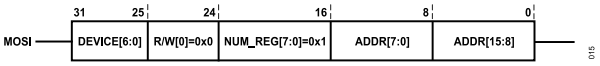

Figure 39. Write Command Header

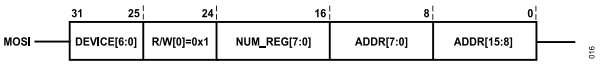

Figure 40. Read Command Header

Table 10. Command Header Details

Field	Description
ADDR	Address of registers, which need to be accessed.
R/W	1: Read. 0: Write.
Device	0: ADE9178. 1: ADC0 − ADC connected to ADC_MISO pin of the ADE9178. 2: ADC1 − ADC connected to ADC_MOSI pin of ADC1. 3: ADC2 − ADC connected to ADC_MOSI pin of ADC2. 4: ADC3 − ADC connected to ADC_MOSI pin of ADC3. 5: All ADCs.
NUM Registers	Number of registers to be read. The ADE9178 sends those many registers starting from the address in the command header. Note that this must be 1 for write commands. If the device field of the command is not ADE9178 (0) , NUM_REGISTER field is ignored and always two 8-bit registers are returned as response. For more details, see the ADC SPI section.

In case of error, 4 bytes status code is sent as response for read and write command.

Table 11 shows the status codes that return.

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Table 11. Status Code Description

Error Code	Failure Reason	Relevant Commands	Command Purpose	ERROR_STATUS Bit	Solution
0x1	Register address not present.	Read/Write ADE9178 Register		N/A[1]	For more details on the register, see the Register Summary: ADE9178 section. Use macros in ade9178.h for address.
0x2	Invalid device.	Read/Write ADE9178/ADC Register		N/A[1]	Verify that the device field is correct.
0x3	Write to more than one register at a time is not supported.	Write ADE9178 Register		N/A[1]	Make NUM_REGISTERS = 1 for write command.
0x4	Register is a read only register. Note that this error is applicable only when device field is ADE9178. Read only check is not done for ADC devices.	Write ADE9178 Register		N/A[1]	For more details on the registers read/write access, see the Register Summary: ADE9178 section.
0x5	Provided BAUD_RATE field of WFS_CONFIG register is not sufficient to stream all channels that are enabled in WFS_CONFIG.	Write ADE9178 Register		N/A[1]	Update BAUD_RATE. For more details on minimum baud rate, see the Waveform Streaming section.
0x6	Configuration Lock is enabled.	Write ADE9178 Register		N/A[1]	Unlock configuration registers by writing 0 to CONFIG_LOCK register.
0x7	Slots configured in the ADC_REDIRECTx register is not supported.	ADC_REDIRECTx	ADC Datapath Redirection	N/A[1]	Verify that the value written to the register is correct.
0x8	Command failed to execute.	ADC_CONTROL = 0x2	Initialize ADC	ADC_INIT_ERROR	Retry the command.
		Read/Write ADC Register		N/A[1]	If ADE9178 is reset while ADC_RUN = 1, then subsequent ADC read/writes may return the COMMAND_FAILED code even though the ADC read/write is successful. It is recommended to reinitialize the ADCs after ADE9178 reset.
	Number of ADCs configured is incorrect.	ADC_CONFIG	Configure number of ADCs	N/A[1]	Check if the number of ADCs being configured is between 1 and 4.
0x9	ADCs are not initialized.	ADC_CONTROL = 0x1	Start ADC data capture	N/A[1]	Verify that ADC initialization is done by writing 2 to ADC_CONTROL.
		ADC_CONTROL = 0x5	Synchronize ADC	N/A[1]	Verify that ADC initialization is done by writing 2 to ADC_CONTROL.
0xA	Issue in SPI communication between Host MCU and ADE9178.	Read/Write ADE9178 Register		N/A[1]	Check CRC header values. Reset ADE9178 if error persists.
0xB	Synchronization already in progress and has not yet complete.	ADC_CONTROL = 0x5	Synchronize ADCs	N/A[1]	Synchronization is already issued. Wait for it to complete.
		Read/Write ADC Register		N/A[1]	Synchronization is already issued. Wait for it to complete.

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Table 11. Status Code Description (Continued)

Error Code	Failure Reason	Relevant Commands	Command Purpose	ERROR_STATUS Bit	Solution
N/A[1]	Issue in SPI data transmission.	Read/Write ADE9178 Register		HOST_SPI_RUNTIME_ERROR	Retry the command. Reset ADE9178 if the error persists.
N/A[1]	Issue in UART communication.	WFS		UART_RUNTIME_ERROR	Reset ADE9178 if the error persists.

[1] N/A means not applicable.

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Support for Reading and Writing ADC Registers

The ADE9178 provides support for reading and writing ADC registers by configuring the device field of the command. If the device is a nonzero value less than 5, the read or write command is sent to corresponding ADC. If the device field is 5, the same command is sent to all ADCs in the daisy chain. ADC reads return two 8-bit values, the value at the address in the command header and the value at the consecutive address.

See Table 10 to relate ADC number to physical ADC channel, for example, ADC1 relates to the ADC that is connected to the ADC_MISO pin of the ADE9178.

For single ADC write, the protocol is the same as shown in Figure 34 except the register value in the Command Header and the Register Value is stored in the lower 8 bits of the 32-bit register (upper 24 bits are 0 padded). For multiple ADC write, it is important to note that the same register value is written to all ADCs and depending on how many ADCs are connected to ADE9178 the response size changes.

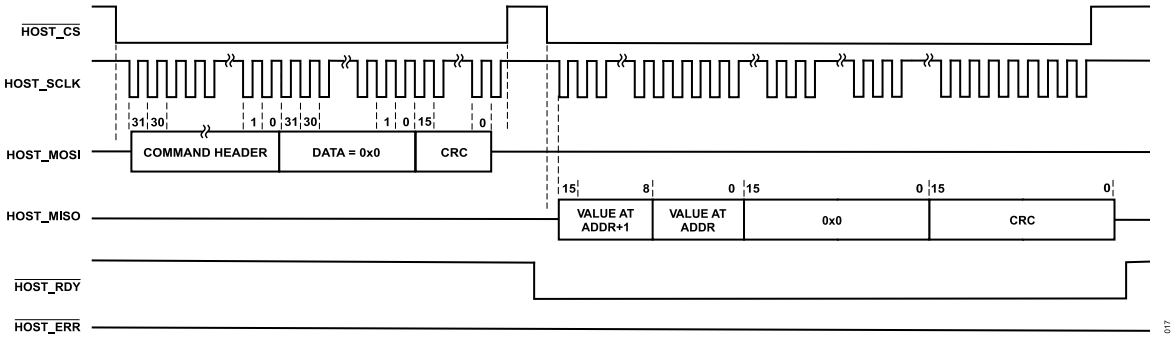

Figure 41. Protocol to Read ADC Registers Individually

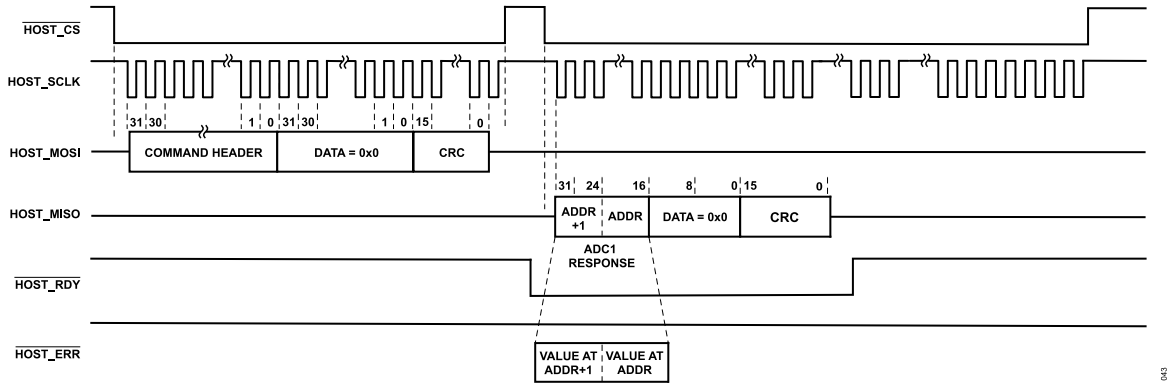

Figure 42. Protocol to Read ADC Registers Simultaneously (NUM_ADC = 0x1)

THEORY OF OPERATION

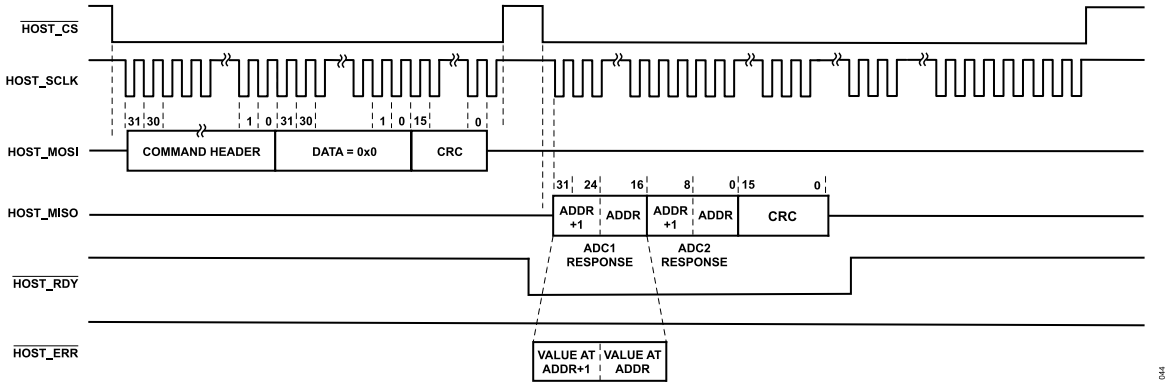

Figure 43. Protocol to Read ADC Registers Simultaneously (NUM_ADC = 0x2)

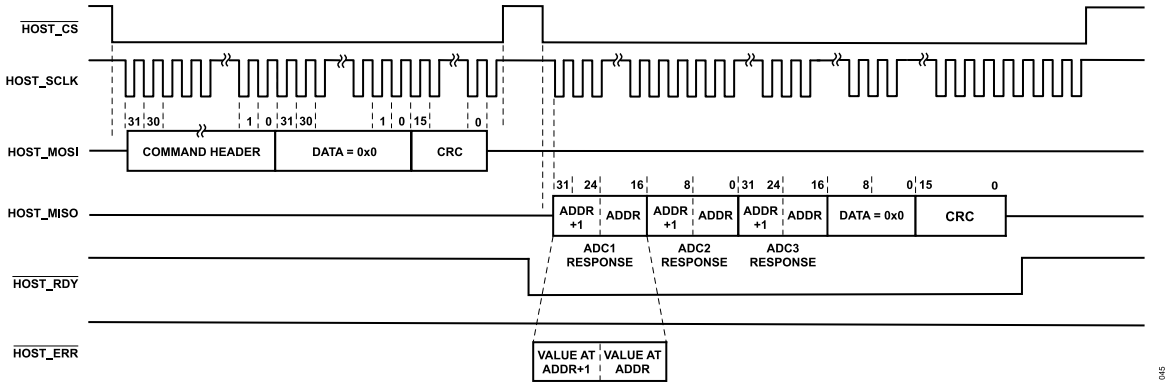

Figure 44. Protocol to Read ADC Registers Simultaneously (NUM_ADC = 0x3)

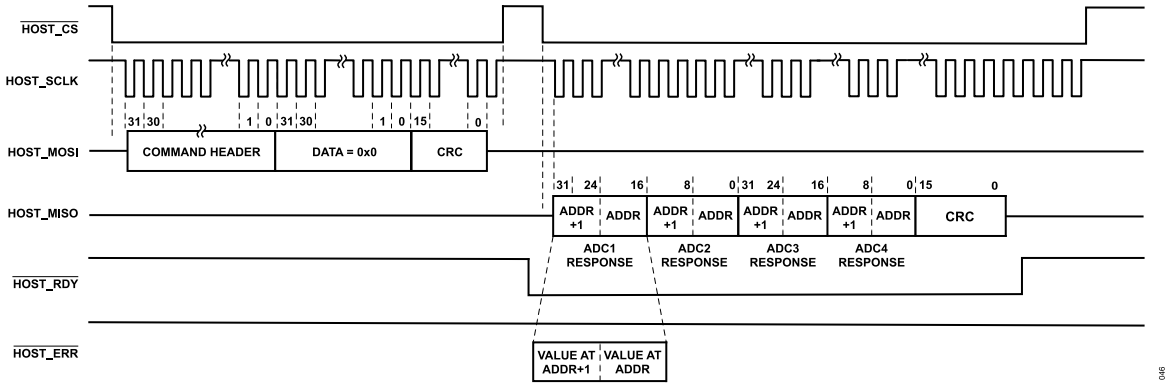

Figure 45. Protocol to Read ADC Registers Simultaneously (NUM_ADC = 0x4)

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Host SPI Protocol CRC

The ADE9178 SPI port uses CRC to verify the integrity of the data received and sent over the SPI. CRC-16-CCITT algorithm with initial value 0xFFFF is used for this purpose.

The CRC of the command field (COMMAND_HEADER + DATA) is calculated and compared against the CRC field of the command. If there is a CRC mismatch, command is not executed, HOST_ERR pin is raised, and status code 0xA (for more details, see Table 11) is returned. By default the CRC check is enabled and can be disabled by writing CRC_DIS bit of CONFIG0. For that purpose, use the following command fields:

- Command Header = 0x0001AE00
- Register Value = 0x20000180
- CRC = 0x26BE

Note that the SPI command frame size is fixed and application should send 2 dummy bytes as CRC even if CRC check is disabled for the command. The 16-bit CRC of the response is appended at the end of every response. There is no option to disable this but application can ignore the CRC if there is no need to verify the integrity of the response.

CRC of Configuration Registers

The configuration register CRC feature monitors many register values. It also optionally includes 15 register sets that are individually selectable in the CRC_OPTEN register. The result is stored in the CRC_RSLT register. If any of the monitored registers change value, the CRC_RSLT changes as well, and the CRC_CHG bit in the STATUS1 register is set; this can also be configured to generate an interrupt on $\overline{\text{IRQ1}}$. For more details, see CRC_OPTEN in the Register Details: ADE9178 section.

Configuration Lock

To prevent accidental overwriting of configuration registers, a provision to lock writing of configuration registers is provided. The user can write 0x1 to the CONFIG_LOCK register to lock the ability to write to the configuration registers. When the lock is enabled, all writes to configuration registers other than CONFIG_LOCK throw an error. The configuration register write can be unlocked by writing 0x0 to the CONFIG_LOCK register.

Burst Register Read

The ADE9178 supports burst reading of up to 256 registers by using the NUM_REGISTERS field in the SPI write command header (for more details, see the Host SPI section). There are five address ranges supported by the ADE9178, which are shown in Table 12.

Table 12. Burst Read Address Ranges

Name	Address Range (Inclusive)
Config registers	0x0 to 0xDD
Output registers	0x200 to 0x295
Status registers	0x400 to 0x40B
Output registers grouped by function	0x600 to 0x630
Output registers grouped by phase	0x631 to 0x661

For each address space, wrap-around happens if start address and NUM_REGISTERS combination gives an address greater than last address in that range. For example, if application issues a read with 0x290 as ADDRESS and NUM_REGISTERS as 10, then the returned registers are 0x290, 0x291, 0x292, 0x293, 0x294, 0x295, 0x200, 0x201, 0x202, and 0x203.

There are some address gaps in the register map, which are not documented and untested. Burst read works as if it is a normal register but the value is undefined.

Clear-on-Read Registers

The energy registers can be configured to be clear-on-read (for more details, see the Energy Calculation section) and peak registers are always clear-on-read. If burst access is issued for such registers, registers are cleared just before initiating the SPI traction for response. For example, addresses of IPEAK, VPEAK, and AUXPEAK are 0x285, 0x286, and 0x287, respectively. If a read is issued with ADDRESS 0x284 and NUM_REGISTERS as 4, all three peak registers are cleared before sending the values of registers from 0x284 to 0x287.

Note that the exact time of clearing the register is not defined. It can vary between the time the command reaches the ADE9178 and the HOST_RDY pin is asserted. Even if the transaction is aborted or the response is corrupted for clear-on-register register reads, the register is cleared and there is no way to retrieve the data.

FULL-SCALE CODES AND CONVERSION EQUATIONS

The ADE9178 calculates various parameters on the input channels and provides output as 32-bit registers in fixed point format. It can be easily converted to physical units such as amperes, volts, and watt. It is required to have knowledge of what is the input voltage and current that gives full-scale ADC input and what are the output registers given by the ADE9178 for such input. Signals corresponding to full-scale input in physical units are referred as X_{FS}, where, X_{FS} can be either I_{FS}, V_{FS_T}, or AUX_{FS} based on whether channels are current, voltage, or auxiliary, respectively. These parameters are choices made during system design and it is assumed that the application developers are already aware of it. Table 13 summarizes the ADE9178 register values when full-scale inputs are provided at ADC inputs. These are referred as X_{FS_CODES}, where X can vary based on type of the register.

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Table 13. Terminology and Full-Scale Codes

Notation	Description	Value	Applicable Registers
I_{FS}	RMS Current in amperes (A_{RMS}), which gives full-scale signal at ADC input. This is the current that gives full scale at the ADC current (IP) inputs of ±31.25 mV peak to peak.	Depends on system parameters. For more details, see the example system configuration. Depends on shunt resistor size.	
V_{FS_T}	Theoretical full-scale RMS voltage in volts (V_{RMS}), which gives full-scale input at ADC input. This is the voltage that gives full scale at the ADC voltage (V1P) inputs of ±1 V peak to peak.	Depends on system parameters. Depends on resistor-divider ratio.	
AUX_{FS}	Signal value (RMS) in appropriate units, which gives full-scale value at ADC input. The units can be either voltage or current. This is the voltage/current that gives full scale at the auxiliary ADC input. ±1 V peak to peak for V1P/V2P inputs and ±31.25 mV peak to peak for IP input, which depends on the ADC Mux settings.	Depends on system parameters.	
RMS_{FS_CODES}	RMS output register value when full-scale input is applied to the ADC input.	107310840	xRMS, xRMSONE, xRMSHALF, xDIP, xSWELL, xPEAK
POW_{FS_CODES}	Power output register value when full-scale voltage and current of same phase is applied at the ADC input.	85829040	xWATT, xVA
PCF_{FS_CODES}	Phase compensation filter (PCF) output for waveform streaming.	6706531	
M	Meter constant (impls/kWHr), which defines the frequency of the CF pulse output.	System Configuration. Supported between 100 and 10000.	

The format for configuration registers for each feature are given along with description of appropriate features are shown in the following sections. To convert output registers to physical quantities, use the following equations shown in Table 14.

Table 14. Conversion Equations

Purpose	Equation		Unit	Applicable registers
RMS related output calculation	$\left(\frac{X_{FS}}{RMS_{FS\_CODES}}\right) \times X$	(1)	X_{RMS}	Where, X = xRMS, xRMSONE, xRMSHALF, xDIP, xSWELL, xPEAK
Power calculation	$\left(\frac{I_{FS} \times V_{FS\_T}}{POW_{FS\_CODES}}\right) \times X$	(2)	watt, VA	Where, X = xWATT, xVA
Energy calculation	$\left[\frac{I_{FS} \times V_{FS\_T}}{POW_{FS\_CODES}}\right] \times \left[\frac{(X_{HI} \ll 13) + X_{LO}}{4000}\right]$	(3)	watt × seconds	Where, X_{HI} = xWATTHR_xx_HI or xVAHR_HI X_{LO} = xWATTHR_xx_LO or xVAHR_LO
Power factor	$xPF \times 2^{-27}$			APF, BPF, and CPF
Period calculation	$\frac{xPERIOD + 1}{4000 \times 2^{16}}$	(4)	seconds	xPERIOD, PEN_PERIOD
Angle calculation	$2\pi\frac{ANGL\_X\_Y \times 256}{xPERIOD + 1} - 2\pi$	(5)	radians	ANGL_X_Y, where, X and Y are phase voltage or currents. For example, ANGL_AV_BV or ANGL_BI_CI

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Worked Examples

This section gives example calculations for the above conversion equations with the following system parameters.

System Parameters:

- $V_{NOMINAL}$ = 220 V_{RMS}
- $I_{NOMINAL}$ = 10 A_{RMS}
- Line Frequency = 50 Hz
- Shunt Resistor = 500 µΩ
- Voltage Divider
  - R1 = 990 kΩ
  - R2 = 1 kΩ
  - Divider Ratio = 0.001

$$Theoretical\ Full\text{-}Scale\ Voltage = V_{FS\_T} = \left(\frac{V_{ADC\_FS}}{Divider\_Ratio}\right) \div \sqrt{2} = \left(\frac{1}{0.001}\right) \div \sqrt{2} = 707 V_{RMS} \quad (6)$$

$$Maximum\ \ Input\ \ Voltage\ \left(Pseudo\ Differential\right) = V_{MAX} = \left(\frac{V_{ADC\_FS\_PSEUDO}}{Divider\_Ratio}\right) \div \sqrt{2} = \left(\frac{0.5}{0.001}\right) \div \sqrt{2} = 353.5 V_{RMS} \quad (7)$$

Note that the ADE91xx has two different full-scale voltages, ±1 V peak to peak for fully differential and ±0.5 V peak to peak for pseudo differential (for more details, refer to the *Signal Voltage Range Between the IP and IM, V1P and V1M, and V2P and V2M Pins* section in the ADE91xx data sheet). The full-scale codes defined in the Table 13 table are related to the fully differential setup of the ADC (±1 V peak to peak), therefore, any calculation that includes full-scale codes must use V_{FS_T} calculated above. Note that do not use the pseudo differential full-scale voltage as this leads to incorrect conversions.

As in most applications, the voltage is measured using a resistor-divider ladder, the ADC is being used with a pseudo differential input rather than a fully differential input. This means that the max voltage allowed into the voltage ADC input is ±0.5 V peak to peak, therefore the max voltage that can be applied to the input of the potential divider is $V_{FS\_T}/2$ = 353.5 V_{RMS}. Any voltage above this throws the clipping and measurement errors.

$$Full\text{-}Scale\ Current = I_{FS} = \left(\frac{I_{ADC\_FS}}{Shunt\_Resistance}\right) \div \sqrt{2} = \left(\frac{0.03125}{500 \times 10^{-6}}\right) \div \sqrt{2} = 44.188\, A_{RMS} \quad (8)$$

RMS Output Calculation:

If AIRMS = 24285092 decimal, then:

$$AIRMS_{CONVERTED} = \frac{I_{FS}}{RMS_{FS\_CODES}} \times AIRMS = \frac{44.188}{107310840} \times 24285092 = 10.00\, A_{RMS} \quad (9)$$

If AVRMS = 33394314 decimal, then:

$$AVRMS_{CONVERTED} = \frac{V_{FS\_T}}{RMS_{FS\_CODES}} \times AVRMS = \frac{707}{107310840} \times 33394314 = 220.013 V_{RMS} \quad (10)$$

Power Calculation:

If AWATT = 6044931 decimal, then:

$$AWATT_{CONVERTED} = \frac{I_{FS} \times V_{FS\_T}}{POW_{FS\_CODES}} \times AWATT = \frac{44.188 \times 707}{85829040} \times 6044931 = 2200.295 Watts \quad (11)$$

If AVA = 6038115 decimal, then:

$$AVA_{CONVERTED} = \frac{I_{FS} \times V_{FS\_T}}{POW_{FS\_CODES}} \times AVA = \frac{44.188 \times 707}{85829040} \times 6038115 = 2197.814 VA \quad (12)$$

Energy Calculation:

If AWATTHR_POS_HI = 2950618 decimal and AWATTHR_POS_LO = 7367 decimal, then:

$$Energy = \frac{I_{FS} \times V_{FS\_T}}{POW_{FS\_CODES}} \times \frac{(X_{HI} \ll 13) + X_{LO}}{4000} = \frac{44.188 \times 707}{85829040} \times \frac{(2950618 \ll 13) + 7367}{4000} = 2199.54\, Watt\ Seconds \quad (13)$$

If AVAHR_HI = 2950549 decimal and AVAHR_LO = 7354 decimal, then:

$$Energy = \frac{I_{FS} \times V_{FS\_T}}{POW_{FS\_CODES}} \times \frac{(X_{HI} \ll 13) + X_{LO}}{4000} = \frac{44.188 \times 707}{85829040} \times \frac{(2950549 \ll 13) + 7354}{4000} = 2199.49\, Watt\ Seconds \quad (14)$$

Period Calculation:

If APERIOD = 5242710 decimal, then:

$$APERIOD_{CONVERTED} = \frac{APERIOD + 1}{4000 \times 2^{16}} = \frac{5242710 + 1}{4000 \times 2^{16}} = 19.9994\, ms = 50.0015\, Hz \quad (15)$$

Angle Calculation:

If ANGL_AV_BV = 6826 decimal and APERIOD = 5242738 decimal, then:

$$Angle = 2\pi \frac{ANGL_{XY} \times 256}{xPERIOD + 1} - 2\pi = 2\pi \frac{6826 \times 256}{5242738 + 1} - 2\pi = -4.189 radians = -240.012\, degrees \quad (16)$$

Therefore, phase B voltage is lagging phase A voltage by 240.012°.

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Power-Factor (PF) Calculation:

If APF = 67114928 decimal, then:

$$APF_{CONVERTED} = APF \times 2^{-27} = 67114928 \times 2^{-27} = 0.50005 \quad (17)$$

To determine if the PF is leading or lagging, find the angle between voltage and current (ANGL_xV_xI) by using the **Angle Calculation** shown in this section. If the angle lies between 0° and −180°, then the PF is lagging. If the angle lies between −180° and −360°, then the PF is leading.

For more details, refer to the **Conversion equation** tab in the Calibration and Conversion excel for calculators, available on the product webpage.

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ADE9178 DATA PROCESSING FLOW

This section explains the processing done on the ADC data received before calculating various parameters.

Current-Channel Data Processing Path

The ADE9178 has three current channels. The datapaths for the AI, BI, and CI current channels is shown in Figure 46. Write to the ICONSEL bit in the CONFIG0 register to calculate BI = −AI − CI. This setting can help to save the cost of a current sensor in some 3-wire delta configurations. Waveform data can be streamed to the Host MCU directly from the ADC samples or from after the PCF. WF_SRC[6:5] bits in the WFS_CONFIG register configures which data is streamed.

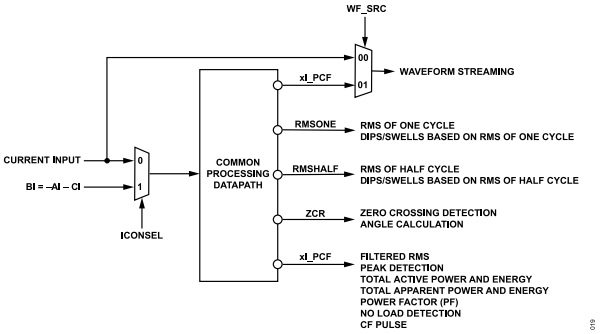

Figure 46. Current-Channel Datapath

Voltage-Channel Data Processing Path

The ADE9178 has three voltage channels. The datapaths for the AV, BV, and CV voltage channels is shown in Figure 47. VCONSEL[2:0] field of CONFIG0 register can be used to configure the channels for different meter configurations such as Wye and Delta. Same as the current channel, WF_SRC[6:5] bits in the WFS_CONFIG register can be used to configure which data is streamed to the Host MCU.

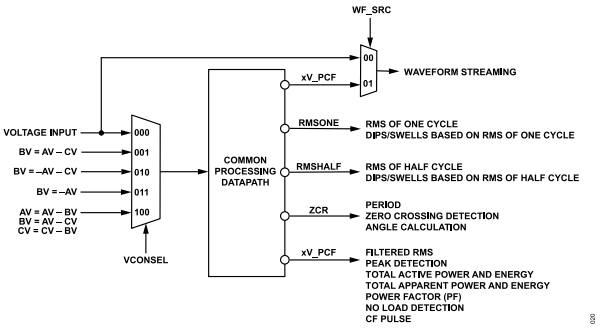

Figure 47. Voltage-Channel Datapath

Auxiliary-Channel Data Processing Path

The ADE9178 supports six auxiliary channels. This can be used for various other measurements including neutral current measurements or additional voltages. The datapath for auxiliary channels are shown in Figure 48. Same as the current and voltage channel, WF_SRC[6:5] bits in the WFS_CONFIG register can be used to configure which data is streamed to the Host MCU.

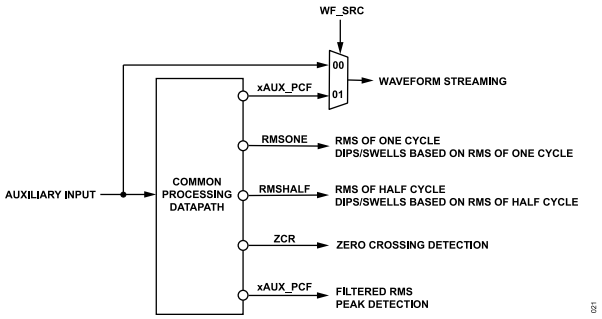

Figure 48. Auxiliary-Channel Datapath

Common-Data Processing Path

Figure 49 shows the common datapath.

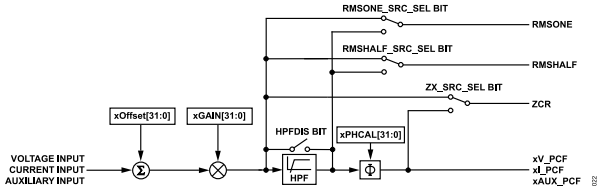

Figure 49. Common Datapath

Gain and Offset Compensation

All channels support gain and offset compensation. Separate registers are provided for each channel

$$xINP = \left(xINP_0 + xOS\right) \times \left(1 + \frac{xGAIN}{2^{27}}\right) \quad (18)$$

where, $xINP_0$ is the initial input value before applying gain and offset calibration.

Note that xOS is typically not used for AC metering applications.

For worked examples, see the Calibration Method section.

Calibration Registers Clamp Values

Table 15 shows the range of adjustment for each calibration register. Any value that is outside of the ranges given in Table 15 is clamped to the maximum or minimum value.

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Table 15. Calibration Registers Clamp Values

Feature	Registers[1]	Range (Register Values)	Range(Real Units)
Channel Gain	xVGAIN, xIGAIN, and AUXyGAIN	−402653184 to 134217728	±2 (Gain)
Channel Offset	xVOS, xIOS, and AUXyOS	±8388608	±8388608 (Codes)
RMS Offset	xVRMSOS, xIRMSOS, AUXyRMSOS, xVRMSONEOS, xIRMSONEOS, AUXyRMSONEOS, xVRMSHALFOS, xIRMSHALFOS, AUXyRMSHALFOS, ISUMRMSOS, VSUMRMSONEOS, and VxyRMSONEOS	±2147483648	±2147483648 (Codes). For more details, see the Root Mean Square (RMS) Measurement section.
Power Gain	xPGAIN	−402653184 to 134217728	±2 (Gain)
Power Offset	xWATTOS	±134217728	±134217728 (Codes)
Phase Calibration	xVPHCAL, xIPHCAL, AUXy, and PHCAL	±134217728	±4.5 degrees at 50 Hz, ±5.4 degrees at 60 Hz

[1] Where, x = A, B, or C, y = 0, 1, 2, 3, 4, or 5, and xy = AB, BC, and AC.

High-Pass Filter (HPF)

The HPF is provided on all the channels to remove DC offsets for accurate RMS and energy measurements. It is enabled by default with a corner frequency is 0.625 Hz. To disable the HPF, set the HPFDIS bit in the CONFIG0 register. The corner frequency is configured with the HPF_CRN bits in the CONFIG0 register.

Table 16. HPF Corner Gain with 50 Hz Input Signal

HPF_CRN[1]	$f_{-3\ dB}$ Hz	HPF_GAIN	Settling Time to 1% for DC Step (sec)	Settling Time to 0.1% for DC Step (Sec)
0	38.7	0.797027686	0.0178	0.0268
1	19.6	0.940985831	0.0363	0.0544
2	9.90	0.987253714	0.0731	0.1097
3	4.97	0.997976919	0.1468	0.2202
4	2.49	0.999733627	0.2942	0.4412
5	1.25	0.999685117	0.5889	0.8833
6 (Default)	0.625	0.999428699	1.1784	1.7675
7	0.313	0.99924257	2.3573	3.5359

[1] It is recommended to leave HPF_CRN as default. If HPF_CRN is changed, then a recalibration is required.

Phase Compensation

xPHCAL register is provided to compensate phase errors. By default, all channels are delayed by one sample (4.5°). It is recommended to keep the voltage channel xVPHCAL as default value (0) to keep angle between voltages of different phases same. Use the Equation 19 to calculate the xPHCAL value for a given phase correction (ϕ)° angle for current with respect to its voltage.

$$xPHCAL = \frac{\sin(\phi - \omega) + \sin(\omega)}{\sin(2\omega - \phi)} \times 2^{27}, \quad where, \omega = 2\pi \times f_{LINE} \times \frac{1}{4000} \tag{19}$$

Zero Crossing and RMS Source Selection

The output of common processing block goes to feature calculations. As shown in Figure 49, additional bits are provided to choose the sources to the following inputs:

- One-Cycle RMS Input: RMSONE_SRC_SEL bit of CONFIG0 register can be used to configure whether this should be before or after HPF.
- Half-cycle RMS Input: RMSHALF_SRC_SEL bit of CONFIG0 register can be used to configure whether this should be before or after HPF.
- Zero-Crossing Input: ZX_SRC_SEL bit of CONFIG0 register selects whether data used in the zero-crossing detection comes before HPF or after phase compensation.
- Phase Compensation Output: This goes to power and energy calculations.

Note that the bits RMS_ONE_SRC_SEL, RMS_HALF_SRC_SEL, ZX_SRC_SEL, and HPFDIS are common for all channels.

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POWER AND ENERGY MEASUREMENTS

Power Calculation

Total Active Power

The ADE9178 computes total active power on up to 3-phases. The measurement is equal to the sum of active power of all fundamental and harmonic components of the voltages and currents.

The total active power on each phase is calculated by first multiplying the xI_PCF and xV_PCF waveforms. Then the result is low-pass filtered, unless the DISAPLPF bit in the CONFIG0 register is equal to 1. Finally, the xPGAIN is applied to perform a gain correction and the xWATTOS value is applied to correct the watt offset. The active power calculations, one for each channel (AWATT, BWATT, and CWATT), are calculated internally at a 4 kHz rate but the output registers are updated at a 1 kHz rate. The complete datapath is shown in Figure 50.

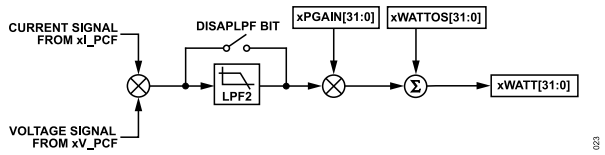

Figure 50. Total Active Power Datapath

The low-pass filter (LPF), LPF2, extracts the total active power, which attenuates harmonics of a 50 Hz or 60 Hz fundamental by 114 dB so that, at full scale, the variation in the low-pass filtered active power is very small, ±0.0002%. Enable the LPF2 (DISAPLPF = 0) for normal operation. Disable LPF2 (by setting DISAPLPF to 1) in the CONFIG0 register to obtain instantaneous total active power. DISAPLPF is 0 at reset.

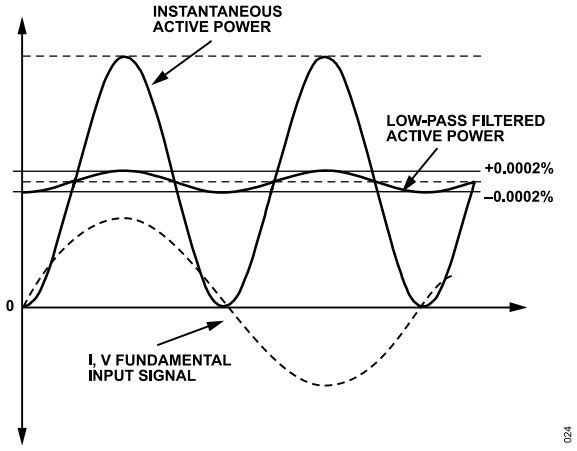

Figure 51. LPF Diagram

The total active power measurements can be calibrated by gain and offset. Equation 20 indicates how the gain and offset calibration registers modify the results in the corresponding power registers:

$$xWATT = \left(1 + \frac{xPGAIN}{2^{27}}\right) \times xWATT_0 + xWATTOS \quad (20)$$

where, $xWATT_0$ is the initial xWATT register value (decimal) before gain and offset calibration. For the worked example, see the Power Gain Calibration section.

The xWSIGN bits in the PHSIGN register indicate the sign of the active power value. Bits [3:1] (REVAPC, REVAPB, and REVAPA) in the STATUS0 register are set when a sign change occurs in the active power measurement.

PWR_SETTLE[17:16] bits in the CONFIG0 register configure the time for the power measurements to settle before starting the energy and CF accumulators. Timer starts when ADC_RUN bit of ADC_CONTROL register is set to 1, then waits the time configured in PWR_SETTLE register, then starts power calculations.

Table 17. Total Active Power Settling Time for 50 Hz Input

	Total Active Power Settling Time (Sec)	
Configuration	**FS = 99%**	**FS = 99.9%**
HPF On, LPF2 On	1.0581	1.41304
HPF On, LPF2 Off	0.23525	0.79525

Total Apparent Power

The ADE9178 computes total apparent power on up to 3-phases. Apparent power is calculated by multiplying the current RMS measurement (xIRMS), by the corresponding voltage RMS (xVRMS), and then applying a gain correction (xPGAIN). The result is stored in the xVA register, which is calculated internally at a 4 kHz rate but the output register is updated at a 1 kHz rate. Note that the offset of the total apparent power calculation is performed by calibrating the xIRMS and xVRMS measurements (using the xIRMSOS and xVRMSOS registers), and there is no specific offset compensation register for the apparent power signal processing.

The ADE9178 offers a register (VNOM) that contains a default RMS value. If the VNOMx_EN bits in the CONFIG0 register are set, VNOM RMS is multiplied with xIRMS to calculate xVA.

To calculate VNOM register value, use the following formula:

$$VNOM = \frac{V \times RMS_{FS\_CODES}}{V_{FS\_T}} \quad (21)$$

where, V is the required nominal voltage, RMS_{FS_CODES} is the RMS output value when full-scale input is applied to the ADC input, and V_{FS_T} is the voltage that gives full scale at the ADC voltage input (system specific).

For example, if the required nominal voltage is 230 V and V_{FS_T} is 707 V, VNOM is calculated as:

$$VNOM = \frac{230 \times 107310840}{707} = 34910174\,decimal = 0{\times}214AFDE$$

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Note that the fully-differential V_{FS_T} is used for this calculation. See the Worked Examples section on how to calculate V_{FS_T} for the system.

The complete apparent power signal processing datapath is shown in Figure 52.

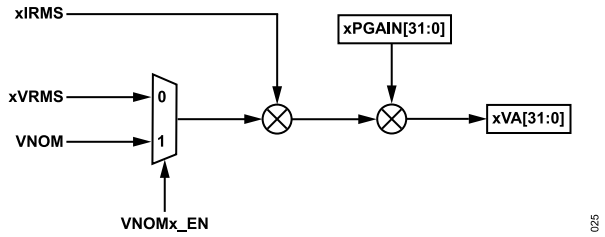

Figure 52. Total Apparent Power Path

Table 18. Total Apparent Power Settling Time with 50 Hz Input

	Total Apparent Power Settling Time (Sec)	
Configuration	**FS = 99%**	**FS = 99.9%**
HPF On, LPF On	1.05754	1.41282

Energy Calculation

The energy path consists of an internal accumulator updating at 4 kHz rate, to perform summation of power outputs. The accumulation is carried out for either a user-defined time duration or number of half-line cycles based upon the EGY_TMR_MODE bit configured in the EP_CFG register. It is recommended to use time-based accumulation mode (for more details, see Table 30). The time or half-line cycles is set in the EGY_TIME register. Set the EGY_PWR_EN bit in EP_CFG register to enable energy accumulation.

After EGY_TIME + 1 ms or EGY_TIME + 1 half-line cycle (depending on EGY_TMR_MODE), the EGYRDY bit is set in the STATUS0 register, and the energy output registers are updated. Note that in the time accumulation mode, four samples of power are produced every 1 ms so the expected output codes in the energy register for a full-scale input signal is POW_{FS_CODES} × 4 × (EGY_TIME + 1). For line-cycle accumulation mode, the expected output codes in the energy register for a full-scale input signal is POW_{FS_CODES} × 4 × (EGY_TIME + 1) × (half_line cycle/1 ms). This is due to power being calculated internally at a 4 kHz rate. The data from the internal energy accumulator is either added or latched to the output register depending on the EGY_LD_ACCUM bit setting in the EP_CFG register. The user can configure automatic resetting the energy output register after reading them using the RD_RST_EN bit in the EP_CFG register. Figure 53 shows an overview of energy accumulation. Three separate accumulators are provided for positive, negative, and signed accumulation. Even though the Figure 53 shows only accumulation of AWATT, there are similar separate accumulators for other active energy channels (BWATT and CWATT). Apparent energy channels (AVA, BVA, and CVA) only have positive accumulators. Energy is not accumulated if no load is detected.

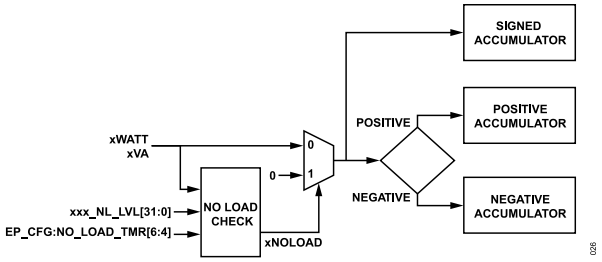

Figure 53. No Load and Sign Check

where, x is the phase (A, B, or C) and xxx is either ACT or APP, which depends on if the calculated energy is active or apparent.

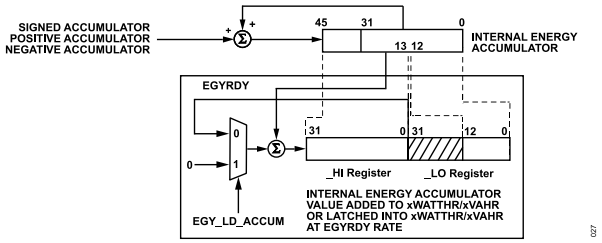

Figure 54. Energy Accumulation Flow

In half-line cycle accumulation mode, the energy is accumulated over an integer number of half-line cycles and is synchronized to one of the voltage channels zero crossings decided by the ZX_SEL bits in the ZX_LP_SEL register. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation and allows the energy to be accumulated accurately over a shorter time. This mode greatly simplifies the energy calibration and significantly reduces the time required to calibrate the meter.

Note that with full-scale inputs, the internal and output energy registers overflows in 51.242 sec of samples. Hence, EGY_TIME register value must be set to value lower than 5124d for half-line cycle accumulation and lower than 51241d in time accumulation mode to prevent overflowing of the output registers.

Each energy output register is 45-bits wide, split between two registers: a register containing the 32 MSB, xHR_xx_HI or xHR_HI , and a register containing the 13 LSB, xHR_xx_LO or xHR_LO (where, x = xWATT or xVA and xx = SIGNED, POS or NEG, for example, AWATTHR_POS_HI or AVAHR_HI). The lower 13 bits of energy output are stored in the xHR_LO register.

For example, if the accumulated energy value is 0x0456789ABCDE, then xHR_xx_HI or xHR_HI stores 0x22B3C4D5 and xHR_xx_LO or xHR_LO stores 0x1CDE.

In some installations, it is not required to accumulate energy at very high precision. In such cases, only the xHR_xx_HI or xHR_HI register can be read and can ignore the value in xHR_xx_LO or XHR_LO register.

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To check how to calculate the energy register value, see the Worked Examples section.

Total Active Energy

For each phase, there are three types of active energy outputs available: positive energy, negative energy and signed energy. The registers available for active energy are xWATTHR_SIGNED_HI and xWATTHR_SIGNED_LO, xWATTHR_POS_HI and xWATTHR_POS_LO, and xWATTHR_NEG_HI and xWATTHR_NEG_LO to store signed, positive and negative energy outputs, respectively.

Total Apparent Energy

For each phase, there is one positively accumulated apparent energy output (xVAHR_HI and xVAHR_LO) exists.

No Load Detection

No load detection prevents energy accumulation due to noise when the input currents are below a given meter start current. To determine if a no load condition is present, the ADE9178 evaluates if the accumulated energy is below a user-defined threshold over a user-defined time period, which is done on a per phase and per energy channel basis. The NOLOAD_TMR[2:0] bits in the EP_CFG register determine whether to evaluate the no load condition over 64 samples to 4096 samples, 64/4 ksps = 16 ms to 1024 ms, as shown in Table 19 . No load detection is enabled by default, over the minimum time of 64/4 ksps = 16 ms. No load detection is disabled when the NOLOAD_TMR[2:0] bits in the EP_CFG are equal to 111 (binary). No load accumulation is always done in absolute accumulation mode. For more details, see Figure 53.

Note, for more details on a known bug with no load feature, see Table 30.

Table 19. No Load Detection Table

NOLOAD_TMR	Samples to Evaluate in No Load Condition	Time That No Load Detection is Evaluated (ms)
0	64	16
1	128	32
2	256	64
3	512	128
4	1024	256
5	2048	512
6	4096	1024
7	No load disabled	No load disabled

The user-defined no load thresholds can be written into the ACT_NL_LVL and APP_NL_LVL registers to sets the no load threshold for the total active energy and total apparent energy, respectively. The configured threshold is directly compared against the accumulated power to decide no load detection. For example, to configure a no load threshold of 0.1% of full-scale active power accumulated for 64 samples, ACT_NL_LVL must be configured to (POW_{FS_CODES} × 0.001 × 64).

No load status of active and apparent energy are indicated by using the bits WATTNLOAD and VANLOAD of STATUS0/STATUS1 register, respectively. The user can enable an interrupt to occur when the no load status changes, either going into or out of no load. The PHNOLOAD register indicates whether each phase of energy is in no load.

Figure 55 shows what happens when the xWATT, low-pass filtered active power value goes above the user-configured no load threshold and then back down below it again. The same concept applies to apparent energy values as well.

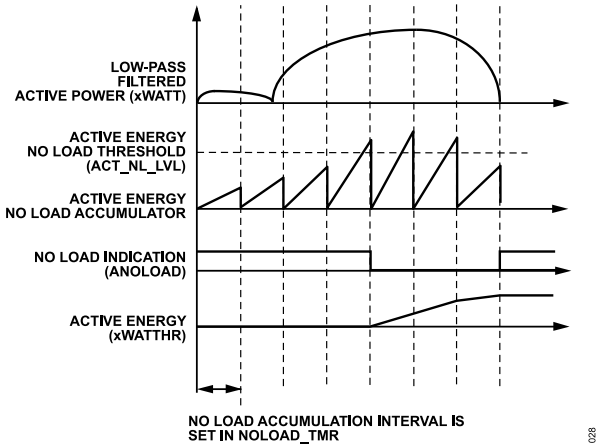

Figure 55. No Load Behavior

Power Factor (PF) Calculation

The total active power and total apparent power are accumulated over 1 sec. Then, the power factor on each phase is calculated by the following equation:

$$xPF = \frac{xWATT\ accumulated\ over\ 1\ sec}{xVA\ accumulated\ over\ 1\ sec} \quad (22)$$

The accumulation is a signed accumulation. The sign of the xPF calculation follows the sign of xWATT. The PF results is stored in 5.27 fixed point format. The highest PF value is 0x07FF_FFFF, which corresponds to a PF of 1. The PF of −1 is stored as 0xF800_0000. To determine the PF from the xPF register value, use this equation:

$$Power\ Factor\ (PF) = xPF \times 2^{-27} \quad (23)$$

Note that the value in xPF register should be treated as a 2's complement number.

To determine if the PF is leading or lagging, find the angle between voltage and current (ANGL_xV_xI) by using the **Angle Calculation** shown in the Full-Scale Codes And Conversion Equations section.

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CF Pulse Generation

Many electricity meters are required to provide a pulse output that is proportional to the energy being accumulated, with a given pulse per kWh meter constant. The ADE9178 includes two pulse outputs that are proportional to the energy accumulation.

A block diagram of the CFx pulse generation and apparent datapath is shown in Figure 56 and Figure 57, respectively. The ACCMODE[8:7] bits in the CFx_CONFIG register decides the CF accumulation mode (signed, positive, or negative accumulation for active power and signed or positive accumulation only for apparent power). The PHASESEL[6:4] bits in the CFx_CONFIG register determines which phases to include for CF accumulation. The PWRSEL[3:1] bits in the CFx_CONFIG register decides whether active power or apparent power is used for CF accumulation. If the application wants to clear CF accumulator, it can be done using the ACC_CLEAR[10] bit in the CFx_CONFIG register. The CF pulses are generated when accumulated value from previous CF pulse exceeds CFx_THR × 2^8.

The low-pulse width of CF pulse can be controlled by CF_LTMR (in µs), for example, CF_LTMR = 50000 decimal sets the low-pulse width to 50 ms register as per Table 20. If WIDTHSEL is set to 1, the maximum active low-pulse width is 80 ms (CF_LTMR = 80000 decimal = 0x13880). Note that the CF_LTMR must be set ≥ 0x1 and ≤ 0x13880.

Note that for the best CF performance, CF frequency must be read from the falling edge of the signal.

Table 20. WIDTHSEL Configuration

WIDTHSEL	Active Low-Pulse Width for Low Frequencies (<6.25 Hz)	Active Low-Pulse Width for High Frequencies (>6.25 Hz)	Behavior when Entering No Load
0	80 ms	50% of period	If CFx is low, finish current pulse, return high
1	CF_LTMR (in µs)	50% of period	

CFx_THR register can be used to control the frequency of the pulses. The ADE9178 issues a pulse whenever accumulated energy from previous CF pulse crosses (CFx_THR × 256). To generate M impulses per kWHr, use the following formula for setting the threshold:

$$CFx\_THR = \frac{1000 \times 60 \times 60 \times POW_{FS\_CODES} \times 4000}{M \times I_{FS} \times V_{FS\_T} \times 256} \quad (24)$$

where, M is the required impulses per kWHr at full-scale inputs, I_{FS} is full-scale current in amperes RMS, and V_{FS_T} is full-scale voltage in volts RMS. Note that the fully-differential V_{FS_T} is used for this calculation. See the Worked Examples section on how to calculate V_{FS_T} for the system. POW_{FS_CODES} is the full-scale power code and can be obtained from full-scale code documentation.

The expected frequency of CF pulse at full-scale input can be calculated as:

$$CF(Hz) = \frac{POW_{FS\_CODES} \times 4000}{CFx\_THR \times 256} \quad (25)$$

Note that the maximum recommended CF frequency of ADE9178 is 500 Hz. So minimum value of CF_X_THR should be more than:

$$CFx\_THR = \frac{POW_{FS\_CODES} \times 4000}{500 \times 256} = \frac{85829040 \times 4000}{500 \times 256} = 2682157\ decimal \quad (26)$$

for single-phase accumulation and more than assuming FS inputs.

$$CFx\_THR = \frac{POW_{FS\_CODES} \times 4000}{500 \times 256} \times 3 = \frac{85829040 \times 4000}{500 \times 256} \times 3 = 8046472\ decimal \quad (27)$$

for 3-phase accumulation assuming FS inputs.

CFx_THR is an unsigned value. For signed, positive, and negative accumulation, the absolute value of the internal accumulation is compared to the CFx_THR.

The SUMxSIGN bits in the PHSIGN register indicate whether the sum of the energy that goes into the last CFx pulse is positive or negative. Bits [5:4] (REVPSUM2 and REVPSUM1) in the STATUS0 register are set when CFx polarity changed sign. For example, if the last CFx pulse is positive active energy and the next CFx pulse is negative active energy, then REVPSUMx bit is set. This bit is updated when the CFx pin goes from high to low.

Example:

System Parameters:

- V_{FS_T} = 707 V_{RMS}
- I_{FS} = 44.188 A_{RMS}
- M = 1000 impls/kWHr

$$CFx\_THR = \frac{1000 \times 60 \times 60 \times 85829040 \times 4000}{1000 \times 44.188 \times 707 \times 256} = 154537194\ decimal \quad (28)$$

$$CF(Hz) = \frac{85829040 \times 4000}{154537194 \times 256} \times 3 = 26.034\ Hz \quad (29)$$

with all 3-phases active.

Therefore, if $V_{NOMINAL}$ = 230 V_{RMS} and $I_{NOMINAL}$= 10 A_{RMS} (3-phase), expected CF pulse output is 1.9167 Hz.

For more details, refer to the **CF Pulse Setup Tab** in the Calibration and Conversion excel for a CFx_THR calculator, available on the product webpage.

THEORY OF OPERATION

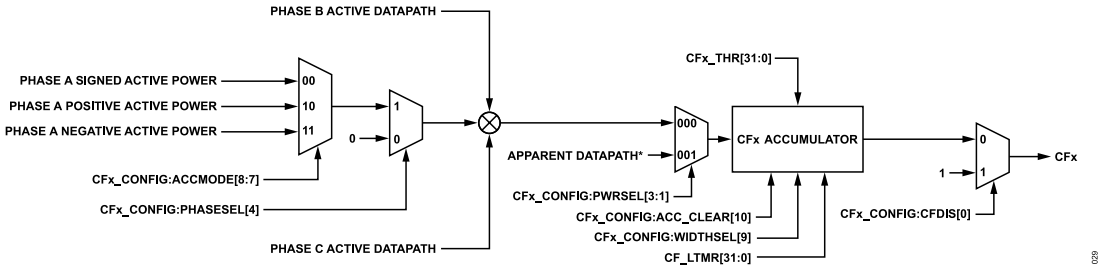

Figure 56. CF Pulse Active Datapath

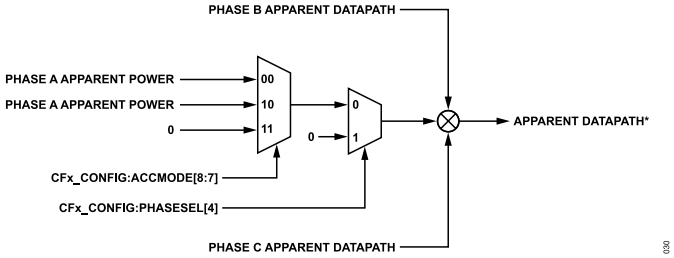

Figure 57. Apparent Datapath

THEORY OF OPERATION

ALL CHANNEL MEASUREMENTS

This section explains the measurements that are done for all 12 channels.

Root Mean Square (RMS) Measurement

The ADE9178 supports three types of RMS measurements:

1. Filtered RMS
2. One-cycle RMS
3. Half-cycle RMS

Each type of RMS is calculated for all the input channels and separate offset registers are provided for each of these for calibration purpose. Offsets for filtered RMS, RMS of one and half cycle can be specified in xRMSOS, xRMSONEOS, and xRMSHALFOS registers, respectively. Note that the offset is applied in the squared domain as shown in Figure 58 and the following equation:

$$xRMS = \sqrt{xRMS_0^{\,2} + \left(2^{15} \times xRMSOS\right)} \quad (30)$$

where, $xRMS_0$ is the initial xRMS value before offset calibration.

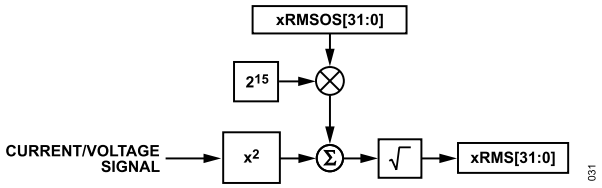

Figure 58. Common RMS Datapath

The number of samples accumulated and averaged varies with the RMS type and is explained in subsequent sections. There is no gain registers separately for RMS calibrations and the application is expected to use signal gain xxGAIN for gain adjustments.

RMS of One Cycle

This feature calculates RMS over every period of input signal. One-cycle RMS measurements of all channels are done over the same time interval and update at the same time as indicated by the RMSONERDY bit in the STATUS0 register. The output is stored in xRMSONE register and is updated every cycle. The LP_SEL bits in the ZX_LP_SEL register select which voltage channel line period value to be used in the one-cycle RMS measurement. Alternatively, the user can set the number of samples used in the calculation by setting the UPERIOD_SEL bit in CONFIG0, where the user-configured USER_PERIOD register is used instead of the selected line period value. USER_PERIOD is specified in Q16 fixed point format as period in number of samples. Note that the USER_PERIOD is not coerced to 50/60 Hz period (based on SELFREQ configuration) if the given value is outside the recommended 40 Hz to 70 Hz range.

For example, if the application wants USER_PERIOD to be 30 ms, USER_PERIOD configures as 0.030 × 4000 × 2^{16} = 7864320 decimal = 0x780000. The RMSONE_SRC_SEL bit in CONFIG0 register decides which waveform input samples should be used for one-cycle RMS measurement. If the bit is set to 1, it indicates that the ADC samples before the HPF are to be used. If the bit is set to 0, then samples obtained after the HPF are used for calculation. For more details, see Figure 49. Since the HPF has a significant settling time associated with it, it is recommended to use the data from before the HPF for the fastest response time (RMSONE_SRC_SEL = 0x1). It is recommended to configure CONFIG0:PERIOD_AVG_CFG[4:3] to 0x2 to average the period over 16 samples. This reduces the period jitter.

RMS of Half Cycle

This feature calculates RMS and updates xRMSHALF registers over every half period of signal. Note that this behavior is different from the ADE9000, where RMS is calculated over one cycle but updated every half cycle. xRMSHALF registers only updates when zero crossings are present, therefore if zero crossing disappear then the value in xRMSHALF register is at the last known value. The RMSHALF_SRC_SEL bit in CONFIG0 (for more details, see Figure 49) register decides which waveform input samples used for half-cycle RMS measurement are to be taken before or after the HPF filter (for the fastest response time, set RMSHALF_SRC_SEL = 0x1). It is recommended to configure CONFIG0:PERIOD_AVG_CFG[4:3] to 0x2 to average the period over 16 samples. This reduces the period jitter. There are two modes of operation. Each channel has a separate configuration bit in RMSHALF_CONFIG register to choose between the two modes. If the bit is set to 0, then the RMS of half-cycle measurement is synchronized to the zero crossing of corresponding channel. This means that the ZX bit for a particular channel in STATUS0 gets set after the xRMSHALF registers are updated.

If the bit is set to 1, then the user can specify half period in USER_PERIOD_HALF register, which is used for measurement. In this case, the output is not synchronized with zero crossings. This mode can be used when measuring non periodic signals. USER_PERIOD_HALF is specified in Q16 fixed point format as period in number of samples same as USER_PERIOD for one-cycle RMS. Note that the USER_PERIOD_HALF is not coerced to 50/60 Hz period (based on SELFREQ configuration) if the given value is outside the recommended 40 Hz to 70 Hz range. For example, if the application wants to set 30 ms, USER_PERIOD_HALF configures as 0.030 × 4000 × 2^{16} = 7864320 decimal = 0x780000.

Filtered RMS

The ADE9178 offers filter-based RMS updated every 1 kSPS. The output of filtered RMS is available in xRMS registers. The settling time for this RMS measurement is approximately 580 ms for both 50 Hz and 60 Hz input signals. Filtered RMS has a bandwidth of 1.61 kHz.

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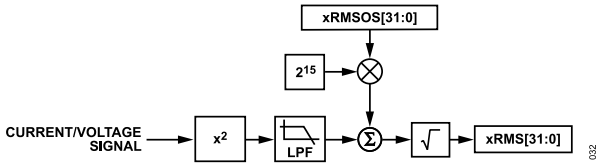

Figure 59. Filtered RMS Datapath

Table 21. Filtered RMS Settling Time with 50 Hz Input

	Filtered RMS Settling Time (Sec)	
Configuration	**FS = 99%**	**FS = 99.9%**
HPF On, LPF On	0.95654	1.44245

Zero-Crossing Detection

The ADE9178 offers zero-crossing detection on all ADC input signals. Each channel is associated with a ZX bit in STATUS0 and STATUS1 registers, which are set when zero crossing is detected on that channel. However, ZX output from the ADE9178 has very high jitter and hence is not intended for external use. A user are expected to use zero-crossing detection output from the ADC if high accuracy is required.

The ZX_SRC_SEL in the CONFIG0 register select whether data going into the zero-crossing detection circuit comes before or after the HPF and phase compensation (for more details, see Figure 49). By default, the xPCF waveforms after the HPF are used for zero-crossing detection. The zero-crossing circuit is the time base for line period, angle, RMS half measurements, and energy accumulation using line-cycle accumulation mode. Note, it is not recommended to use line-cycle accumulation mode (for more details, see Table 30).

Note that the HPF has settling times given in Table 16. Thus, for a fast response, it is recommended to set ZX_SRC_SEL to look for a zero crossing before the HPF. However, if the HPF is disabled with HPFDIS = 1 or if ZX_SRC_SEL = 1. Note that a DC offset on the input may cause the time between negative to positive and positive to negative zero crossings to change, which indicates that the ZX detection does not have a 50% duty cycle.

The input signals are passed through a first sequence low pass with corner frequency of 85 Hz to remove harmonics.

The LPF settling time is 51 samples, 51/4 kSPS, which results in 12.75 ms. Figure 60 shows the delay between the detected zero-crossing signal and the input. Note that there is a 3.5 ms to 4.3 ms delay between the input signal zero crossing and the ZX zero-crossing indication, with a 50 Hz input signal. Zero crossings are generated on both negative to positive and positive to negative transitions.

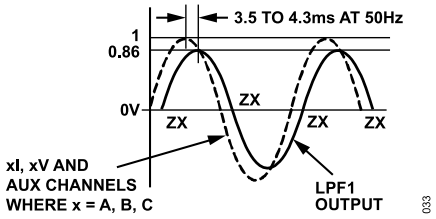

Figure 60. Zero-Crossing Timing

To provide protection from noise for zero-crossing events used for period calculation, zero-crossing events are not generated for voltage channels if the absolute value of the ZX LPF filter output signal is smaller than the threshold ZXTHRSH. Additionally, on all ADC channels, to prevent false zero crossings after a zero crossing is generated, 1 ms must elapse before the next zero crossing can be output. Calculate the zero-crossing threshold, ZXTHRSH, from the following equation:

$$ZXTHRSH = \frac{PCF_{FS\_CODES} \times LPF_{ATTENUATION}}{x} \quad (31)$$

where, $LPF_{ATTENUATION}$ = 0.86 at 50 Hz and 0.81 at 60 Hz. x is the fraction of full scale for which the zero crossing is blocked.

For example, for a 50 Hz input, it is required to block zero-crossing detection for samples 100× lower than full- scale PCF output. Then:

$$ZXTHRSH = \frac{6706531 \times 0.86}{100} = 57676d \quad (32)$$

Zero-Crossing Timeout

The zero-crossing timeout feature alerts the user if a zero-crossing event is not generated after a user- configured amount of time. This feature is available only on the voltage channels. If a zero crossing is not detected after (ZXTOUT+1) ms, the corresponding ZXTOx bit in the STATUS1 register is set. For example, if ZXTOUT is equal to 1000, and if a zero crossing is not detected on phase A for 1001 ms, then ZXTOAV bit is set in the STATUS1 register.

Combined Voltage Zero Crossing

Apart from zero-crossing input signal, the ADE9178 provides zero crossing of a combined signal from AV. BV, and CV. The combined signal is formed as (AV + BV − CV)/2. This zero crossing, ZX_COMB, is stable even if one or more phases drops out.

Zero-Crossing Use in Other Functions

The following features are dependent on zero-crossing detection. The behavior of each feature when zero crossing is absent is given in Table 22.

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Table 22. Zero-Crossing Use in Other Functions

Function Using Zero Crossing	ZX Transition Used	Corresponding STATUSx Register Bits	Selecting Which Phase to Use for Measurement	Effect if ZX Does Not Occur
ZX Indication in STATUS0 Register[1]	Negative to positive and positive to negative	ZXAI, ZXBI, ZXCI, ZXAV, ZXBV, ZXCV, ZXAUX0, ZXAUX1, ZXAUX2, ZXAUX3, ZXAUX4, ZXAUX5, and ZXCOMB of STATUS0 and STATUS1 registers	N/A[2]	ZXx bit is latched in STATUS1. If cleared, it is not set again. ZXx interrupt does not occur.
Zero-Crossing Timeout	Negative to positive and positive to negative	ZXTOAV, ZXTOBV, and ZXTOCV of STATUS0 and STATUS1 registers	N/A[2]	Zero-crossing timeout is indicated by the ZXTOAV, ZXTOBV, or ZXTOCV bit in the STATUS0 register and an interrupt can be enabled to occur.
Phase-Sequence Error Detection	Negative to positive only	SEQERR of STATUS0 and STATUS1 registers	N/A[2]	If one to two ZX events are missing, SEQERR is generated. If all ZX are missing then SEQERR bit is not set.
Energy Accumulation	Negative to positive and positive to negative	N/A[2]	ZX_LP_SEL:ZX_SEL[1:0] selects the zero-crossing output used for line-cycle energy accumulation and ZX output pin.	Line-cycle accumulation does not update. Note, it is not recommended to use line-cycle accumulation mode (for more details, see Table 30).
Line Period Measurement	Negative to positive only	N/A[2]	N/A[2]	Coerced to default value: 0x0050_0000 if ACCMODE.SELFREQ = 0, for a 50 Hz network, 0x0042_AAAA if ACCMODE.SELFREQ = 1, for a 60 Hz network.
RMSONE, DIPONE, SWELLONE	Negative to positive only	STATUS2 register	ZX_LP_SEL:LP_SEL[3:2] selects the phase voltage line period used as the basis for these calculations.	If the selected line period is invalid because zero crossings are not detected or the calculation results in something outside a 40 Hz to 70 Hz range, the line period used for the calculation is coerced to the default line period: 0x0050_0000 if ACCMODE:SELFREQ = 0, for a 50 Hz network, 0x0042_AAAA if ACCMODE:SELFREQ = 1, for a 60 Hz network. This line period is used to calculate RMSONE and associated events.
RMSHALF, DIPHALF, SWELLHALF	Negative to positive and positive to negative	STATUS3 register	N/A[2]	If bits are set to 1 in the RMSHALF_CONFIG register then the corresponding RMSHALF register value is calculated based on the user-configured half line-cycle period register (USER_PERIOD_HALF). Otherwise, if zero crossing is not detected, the corresponding RMSHALF register value is not updated. DIPHALF and SWELLHALF is not detected in such cases.
Angle Measurements	Negative to positive only	N/A[2]	N/A[2]	Does not update, keeps last value.

[1] The ZX output from ADE9178 has very high jitter, hence it is not intended for external use.

[2] N/A means not applicable.

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Peak Detection

The ADE9178 records the peak value measured on the current, voltage, and auxiliary channels, from the xPCF waveforms. The VPEAKSEL[2:0], IPEAKSEL[2:0], and AUXPEAKSEL[5:0] bits in the PEAK_CONFIG register allow the user to select which channels to monitor for peak detection.

The IPEAK register stores the peak current value in IPEAKVAL[23:0] and indicates which phase(s) currents reached the value in the IPPHASE[2:0] bits. Similarly, VPEAKVAL and VPPHASE bits of VPEAK register and AUXPEAKVAL and AUXPHASE bits in AUXPEAK registers provides similar information for voltage and auxiliary channels, respectively.

Note that the range of the PEAK output is clamped to ±8388607 codes.

Dip and Swells

Dip indicates that if the RMS of input signal reaches below a specified threshold for a user-configured number of cycles. Conversely, swell indicates that if the RMS of input signal reaches above a threshold for a specified number of cycles. The ADE9178 supports dip/swell detection on RMSONE and RMSHALF outputs for all ADC channels.

The corresponding xRMSHALF or xRMSONE is compared against the configured xDIPHALF_LVL or xDIPONE_LVL. If the consecutive RMS values are less than the level for configured number of xDIPHALF_CYC (register unit in half-line cycles) or xDIPONE_CYC (register value units in one-line cycles), then the corresponding smallest dip RMS value is updated in xDIPONE or xDIPHALF registers (same register format as all RMS output registers). Each channel is associated with separate LVL and CYC registers. For example, if the application wants to flag DIP if the AVRMSONE reaches below 20% of the full scale for five-line cycles, then AVDIPONE_LVL register must be configured as RMS_{FS_CODE} × 0.2 = 107310840 × 0.2 = 21462168 decimal and AVDIPONE_CYC must be set to 5 decimal. Note that if 0 or 1 is written to the CYC register, the dip/swell flag is set after one cycle.

Similarly, for swell detection, corresponding xRMSHALF or xRMSONE is compared against the configured xSWELLHALF_LVL or xSWELLONE_LVL. If the consecutive RMS values are greater than the level for configured number of xSWELLHALF_CYC or xSWELLONE_CYC, then maximum RMS values is updated in the xSWELLONE or xSWELLHALF registers. Each channel is associated with separate LVL and CYC registers.

Status of RMSONE dips/swells is provided in STATUS2 register and status of RMSHALF dips/swells is provided in STATUS3 register. If DIP_SWELL_x_IRQ_MODE bit in CONFIG0 register is set, then bit in STATUS registers is set only when entering or exiting the dip or swell condition. Otherwise by default, the bit is set continuously after every xDIPx_CYC or xSWELLX_CYC cycles.

$\overline{IRQ2}$/$\overline{IRQ3}$ outputs can be enabled by setting the appropriate bit in the MASK2/MASK3 registers to generate interrupts for these flags.

Figure 61 and Figure 62 show the expected behavior for both continuous and enter and exit IRQ modes. In both examples, the CYC register is set to 0x2.

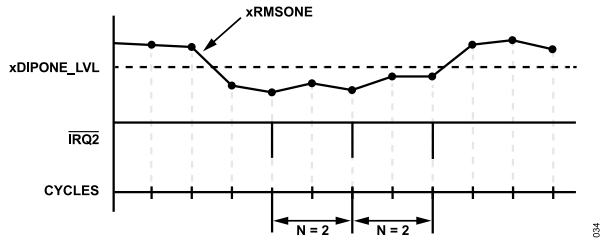

Figure 61. Continuous IRQ Mode

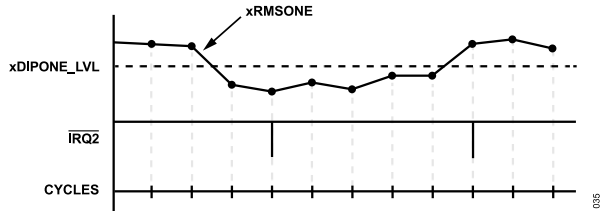

Figure 62. Enter and Exit IRQ Mode

Angle Measurement

The ADE9178 measures angles between voltage signals, current signals, and angle between voltage and current signals. Note that angle measurement is not available for auxiliary channels. It is measured as the time between negative to positive zero crossings of corresponding signals as shown in Figure 63 and Figure 64.

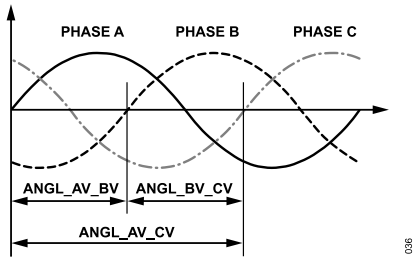

Figure 63. Angle between Voltages

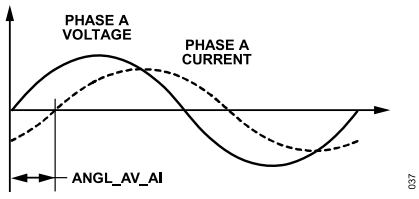

Figure 64. Angle between Voltage and Current

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The output is given as three registers ANGL_AV_BV, ANGL_AV_CV, and ANGL_BV_CV for voltage, three registers ANGL_AI_BI, ANGL_AI_CI, and ANGL_BI_CI for current and another three registers ANGL_AV_AI, ANGL_BV_BI, and ANGL_CV_CI angle between voltage and current of corresponding phases. All angle registers only update when zero crossings are present. Therefore, if the two relevant phases of a register drop out, then both zero crossings disappear, and the value in the angle register remains at the last known value. If only one of the two relevant phases drop out, then the angle register continues to update but the value increases indefinitely. This is due to the nature in which angles are calculated in the ADE9178. Angles are calculated from time between zero crossings, so if one phase zero crossing is not present, then the time between zero crossings increases indefinitely.

To ensure the angle results are valid, monitor the relevant RMS of One Cycle registers on each phase (voltage and current). If the RMSONE registers for a particular phase drops out, ignore any angle output registers related to that phase.

Use the following equation to convert the register to angle in radians:

$$Angle\left(rad\right) = 2\pi\frac{\text{ANGL}_{XY} \times 256}{\text{xPERIOD} + 1} - 2\pi \quad (33)$$

For example, for ANGL_AV_BV this equation gives the angle by which phase B voltage lags phase A voltage expressed as a negative value. All values are between 0 and −2π.

In Equation 33, xPERIOD corresponds to the period of selected channels. There is no period register available for current output and corresponding voltage period values can be used for angle calculation. If the frequency of the signal is known, the following formula can also be used to convert angle registers to radians:

$$Angle\left(rad\right) = 2\pi\frac{\text{ANGL}_{XY} \times f_{LINE}}{4000 \times 2^{8}} - 2\pi \quad (34)$$

For more details, see the Worked Examples section and refer to the Calibration and Conversion excel for the calculator, available on the product webpage.

MEASUREMENTS ONLY FOR VOLTAGE CHANNELS

Line Period Calculation

The ADE9178 calculates period using zero crossings on voltage channels and combined voltage channels described in the Zero-Crossing Detection section. The line period, t_L can be calculated from the xPERIOD register according to the following equation:

$$t_L = \frac{xPERIOD + 1}{4000 \times 2^{16}} \quad (35)$$

If the calculated period value is outside the range of 40 Hz to 70 Hz, or if the negative to positive zero crossings for that phase are not detected, the xPERIOD register is coerced to correspond to 50 Hz or 60 Hz, according to the setting of the SELFREQ bit in the CONFIG0 register. With SELFREQ = 0 for a 50 Hz network, xPERIOD register is coerced to 0x0050 0000. If SELFREQ = 1, which indicates a 60 Hz network, the xPERIOD register is coerced to 0x0042 AAAA. PERIOD_AVG_CFG bits in CONFIG0 register configure the level of averaging performed on the period measurement. It is recommended to configure CONFIG0:PERIOD_AVG_CFG[4:3] to 0x2 to average the period over 16 samples. This reduces the period jitter.

Phase-Sequence Error Detection

The ADE9178 monitors the zero crossings of the voltage signals and raises sequence error if they are not in expected sequence. If SEQ_CYC is set to 0 or 1, the ADE9178 flags sequence error after 1 zero crossing errors. If SEQ_CYC is set to more than 1, the ADE9178 flags sequence error only after getting SEQ_CYC consecutive zero-crossing errors.

After applying VCONSEL, the expected sequence of voltage signals for a 3-phase system is shown in Figure 65.

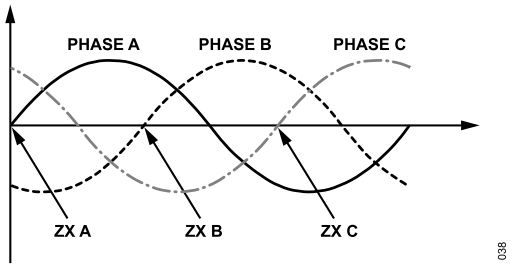

Figure 65. Regular Succession of Zero-Crossing Events: Phase A, Phase B, and Phase C

Figure 66 shows a sequence with phase-sequence error.

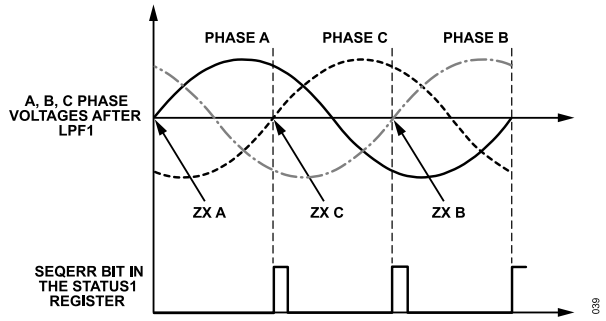

Figure 66. SEQERR Bit Set to 1 When Phase A Voltage is Followed by Phase C Voltage

Note that phase-sequence error also happens if one of the voltage channels are missing as shown in Figure 67.

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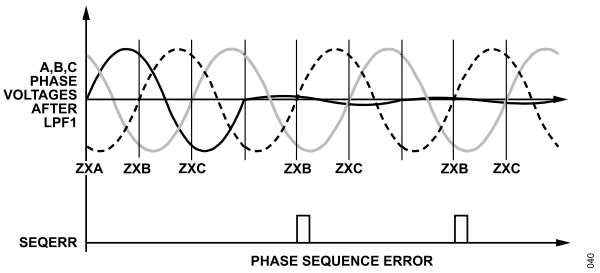

Figure 67. 4-Wire WYE, 4-Wire Delta Phase-Sequence Error from a Phase Voltage Dropping below ZXTHRSH with SEQ_CYC = 1

MEASUREMENTS ONLY FOR CURRENT CHANNELS

Neutral Current Mismatch

The ADE9178 calculates the RMS of the sum of AI + BI + CI sample by sample and stores the result in the ISUMRMS register. The ISUMRMSOS register allows offset calibration of this measurement. The scaling is the same as for the other xIRMS and xIRMSOS registers. Additionally, any one of the six auxiliary ADC path can be selected by configuring the ISUM_AUXSEL bits in CONFIG0 register to be used for neutral current sensing. This channel can be either added or subtracted from the sum of phase channels by configuring ISUM_CFG bits in CONFIG0 register.

In some cases, the application requires to get an interrupt if the RMS of the sum of current channels exceeds a threshold. This threshold value can be set in the ISUMLVL register. ISUMMISMTCH bit of STATUS0 is set when ISUMRMS exceeds ISUMLVL.

To calculate ISUMLVL, use the following formula:

$$ISUMLVL = \left(\frac{I_{NOM}}{I_{FS}}\right) \times (\%\,of\ nominal) \times (RMS_{FS\_CODES}) \quad (36)$$

where, I_{NOM} is the nominal current, I_{FS} is the current that gives full scale at the ADC current input (system specific), % of nominal is the required percentage of nominal for ISUMLVL, and RMS_{FS_CODES} is the RMS output value when full-scale input is applied to the ADC input.

For example, if I_{NOM} is 10 A, I_{FS} is 44.188 A, and the required ISUMLVL is 5% of I_{NOM}, ISUMLVL is calculated as:

$$ISUMLVL = \left(\frac{10}{44.188}\right) \times (0.05) \times (107310840) = 1214253\ decimal = 0x12872D$$

PEN FAULT DETECTION

This feature is designed to detect PEN faults according to the BS7671:2018 Amendment 1:2020 standard.

The ADE9178 provides additional RMSONE calculation and dip/swell detection on certain channels to enable easy PEN fault detection. 3-channels are used for PEN fault detection, PEN_CHANA, PEN_CHANB, and PEN_CHANC. The PEN channels can be configured using the PEN_CHANSELA, PEN_CHANSELB, and PEN_CHANSELC bits in the PEN_CONFIG register. The PEN channels can be any of the 12 ADC channels AV, BV, CV, AI, BI, CI, AUX0, AUX1, AUX2, AUX3, AUX4, and AUX5. CONFIG0:RMSONE_SRC_SEL selects samples either before or after the HPF.

RMS of PEN Fault Channels

Four additional one-cycle RMS values (same as RMS of One Cycle section) are calculated on the following signals:

1. VSUMRMSONE = (PEN_CHANA + PEN_CHANB + PEN_CHANC)/3
2. VABRMSONE = PEN_CHANA − PEN_CHANB
3. VACRMSONE = PEN_CHANA − PEN_CHANC
4. VBCRMSONE = PEN_CHANB − PEN_CHANC

RMSONE_SRC_SEL bit in the CONFIG0 register decides and selects samples either before or after the HPF. Period is calculated for any one of the selected PEN channels based on PEN_LP_SEL bits in the PEN_CONFIG and is stored in the PEN_PERIOD register (for formula to convert to seconds, see Table 14). This period value is used for the PEN channel RMS measurements. Separate RMS offset calibration registers are also provided for each of PEN channel (VSUMRMSONEOS, VABRMSONEOS, VACRMSONEOS, and VBCRMSONEOS). The PEN channel RMS offset register format is the same as the other RMS offset registers (xxRMSOS).

For example, if PEN_CONFIG is set up in the following configuration:

PEN_CHANSELA = 0000 = AV data processing path

PEN_CHANSELB = 0010 = BV data processing path

PEN_CHANSELC = 0100 = CV data processing path

PEN_LP_SEL = 11 = Combined PEN channels (AV + BV − CV)/2

Then the PEN fault output registers is calculated as follows:

VSUMRMSONE = (AV + BV + CV)/3

VABRMSONE = AV − BV

VACRMSONE = AV − CV

VBCRMSONE = BV − CV

PEN_PERIOD = Period of combined PEN channels

Dips and Swells on PEN Fault Channels

Swells can be detected based on VSUMRMSONE value while both dips and swells can be detected on the 3-phase to phase voltage RMS values (VABRMSONE, VACRMSONE, and VBCRMSONE). Separate dip/swell levels and cycle configuration registers (VxxDI-

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PONE_LVL/VxxSWELLONE_LVL and VxxDIPONE_CYC/VxxSWELLONE_CYC, for more details, see the Dip and Swells section) are provided for each of the four PEN fault channels. Four status bits (VSUMSWELLONE, VABSWELLONE, VACSWELLONE, and VBCSWELLONE) are provided for swells and three status bits (VABDIPONE, VACDIPONE, and VBCDIPONE) are provided for dips in the STATUS2 register, which if required can be configured to generate interrupts on $\overline{IRQ2}$ (for more details, see the Dip and Swells section).

WAVEFORM STREAMING

The ADE9178 streams the waveform samples through universal asynchronous receiver-transmitter (UART) interface. The baud rate can be configured using the BAUD_RATE[4:1] bits in the WFS_CONFIG register. The ADE9178 supports waveform streaming of either raw ADC samples or samples after phase compensation filter using the WF_SRC[6:5] bits in the WFS_CONFIG register (setting to 00 streams raw ADC values and 01 streams the samples after the phase compensation filter). The sampling rate of the samples streamed is 4 kHz.

Samples of different channels are transmitted in interleaved format as follows in Table 23.

The individual channels can be enabled or disabled by setting the corresponding x_WFS_EN bits in the WFS_CONFIG register. For example, to stream AV and AI data only, set the AV_WFS_EN[7] and AI_WFS_EN[8] bits to 1 in the WFS_CONFIG register. If a channel is disabled, the samples corresponding to that channel are not transmitted and is occupied by subsequent channel. For example, if only AV, BV, and CV are enabled, samples are streamed as follows in Table 24.

The baud rate required for transmission varies with number of channels enabled. It is recommended to use the 3072 kbps, the highest baud rate supported for waveform streaming. A baud rate of at least 3072000 is required to stream all channels together. Samples may drop if the baud rate is below the minimum requirement. If the baud rate is less than required baud rate when writing WFS_CONFIG register, error pin is asserted.

Each sample is sent as a 32-bit integer with upper 24 bits indicating the sample value and lower 8 bits indicating the corresponding channel. This means the full range of samples is ±8388607. If extreme gain and offset values are applied, then the waveform saturates to the max and min value. This channel id can be used to synchronize various channels. For example, if the number of enabled channels is 12, then to synchronize the starting of the capture to 0th channel, do the following steps:

1. Skip the bytes from UART till 0x0 is encountered.
2. Once 0x0 is received at the Nth byte, check if N + 4th byte is 0x1, N + 8th byte is 0x2, and N + 12th byte is 0x3. If not, then go back to step 1.

The lowest byte of each 32-bit word is sent first through UART.

Table 25 summarizes the minimum baud rate requirement to stream the waveform samples.

Table 23. Transmission Format

AV	AI	BV	BI	CV	CI	AUX0	AUX1	AUX2	AUX3	AUX4	AUX5

Table 24. Transmission Format with Only AV, BV, and CV are Enabled

AV	BV	CV	AV	BV	CV

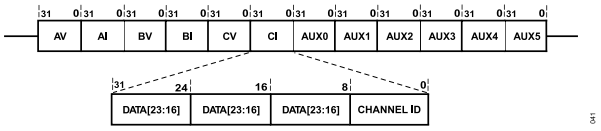

Figure 68. Waveform Streaming UART Transmission Format

Table 25. Minimum Baud Rate Requirements

Channels Enabled	Minimum Baud Rate
12	3072000
11	2048000
10	2048000
9	2048000
8	1536000
7	1536000
6	1536000
5	1024000
4	1024000
3	1024000
2	512000
1	256000

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OUTPUT REGISTER UPDATE RATES

Most of the ADE9178 output registers are updated every 1 ms interval (1 kHz rate). Table 26 summarizes the list of registers that are not updated at the 1 kHz rate.

Table 26. Update Rates

Register Name	Description	Update Rate	Status Bits
xxRMSONE	One-cycle RMS registers	Line period	RMSONERDY (STATUS0/1)
xxRMSHALF	Half-cycle RMS registers	2 × line period	ZXxx(STATUS0/1)
xWATTHR_POS_LO/HI, xWATTHR_NEG_LO/HI, xWATTHR_SIGNED_LO/HI xVAHR_LO/HI	Active/apparent energy registers	Depends on EGY_TMR_MODE bit of EP_CFG	EGYRDY (STATUS0/1)
xPF	Power factor	1 Hz	PF_RDY (STATUS0/1)
xxDIPHALF	Minimum RMSHALF during a half-cycle dip event	2 × line period, but updated only when DIPHALF is detected	xxDIPHALF (STATUS3)
xxDIPONE	Minimum RMSONE during a one-cycle dip event	Line period but updated only when DIPONE is detected	xxDIPONE (STATUS2)
xxSWELLHALF	Maximum RMSHALF during a half-cycle swell event	2 × line period, but updated only when SWELLHALF is detected	xxSWELLHALF (STATUS3)
xxSWELLONE	Maximum RMSONE during a one-cycle swell event	Line period but updated only when SWELLONE is detected	xxSWELLONE (STATUS2)

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INTERRUPTS AND STATUS OUTPUTS

The ADE9178 provides five 32-bit registers STATUS0, STATUS1, STATUS2, STATUS3, and ERROR_STATUS to indicate various events/errors in the system. There are corresponding MASK0, MASK1, MASK2, MASK3, and ERROR_MASK registers, which can be used to map a particular event to one of the interrupt pins IRQ0, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, or $\overline{\text{IRQ3}}$. These pins go low when an enabled interrupt occurs and stays low until the event is acknowledged by writing 1 to the corresponding bit in the STATUS register.

Note that STATUS0 and STATUS1 contains exactly same events except the 14th bit. STATUS0 14th bit is for RSTDONE (nonmaskable) and STATUS1 14th bit is for ERROR (bit enabled by default in the MASK1 register). Two registers are provided to allow mapping to $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ for these events.

As there is no dedicated IRQ pin associated with the ERROR_STATUS register, bit 14 of the STATUS1 register (ERROR) is used to map any error bits in the ERROR_STATUS register to the $\overline{\text{IRQ1}}$ pin. If an error occurs the STATUS1 ERROR bit is asserted only if the corresponding bit is set in the ERROR_MASK register. STATUS1 bit 14 (ERROR) is masked to $\overline{\text{IRQ1}}$ by default. Read the ERROR_STATUS register to determine the cause of the interrupt.

For example, if a user wants to generate an interrupt on $\overline{\text{IRQ1}}$ whenever ADC_RUNTIME_ERROR is detected from ERROR_STATUS, set bit 3 in the ERROR_MASK register. Bit 14 of STATUS1 is logical OR of the ERROR_STATUS bits set in ERROR_MASK.

The ADE91xx ADCs have 3 status registers (ADC_STATUS0, ADC_STATUS1, and ADC_STATUS2). These status registers are mapped to a corresponding bit in the ERROR_STATUS register of the ADE9178. For example, ADC_STATUS0 of ADC0 is mapped to the ADC0_STATUS0 bit in the ERROR_STATUS register. As multiple bits in the ADC_STATUSx register are mapped to a single bit in the ERROR_STATUS register of the ADE9178, select bits in the ADC_STATUSx register are logic OR. The bits that are logic OR in each ADC_STATUS register is as follows: ADC_STATUS0[0:5], ADC_STATUS1[1:3], and ADC_STATUS2[0:6]. For example, if any bits are set in ADC_STATUS1 register of ADC2, the corresponding ADC2_STATUS1 bit is set in the ERROR_STATUS register of the ADE9178.

If a bit is set in the ERROR_STATUS register, the corresponding ADC_STATUSx register can be read to understand what caused the error. To clear the errors, write 1 to the corresponding bits in the ERROR_STATUS register and the ADC_STATUSx register. If the ADC_STATUSx register is not cleared, the bit in ERROR_STATUS register re-asserts.

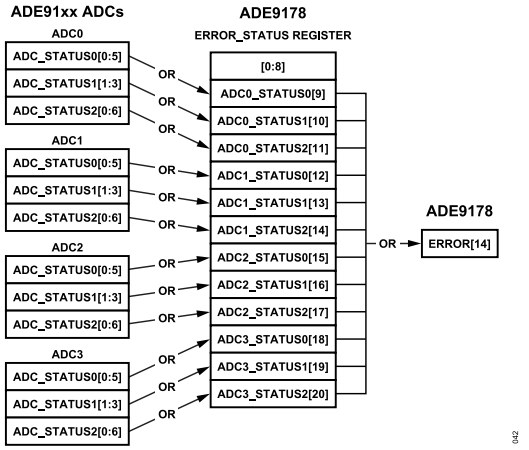

Figure 69. ADC_STATUSX to ERROR_STATUS Register Mapping

ERROR_STATUS Register Table

Table 27 describes what each bit means in the register, how to debug during project development and how to handle if the error appears while in the field.

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Table 27. ERROR_STATUS Register Table

ERROR_STATUS Bit	Description	Possible Cause of Issue	How to Debug during Development	How to Handle in the Field
ADC_INIT_ERROR[0]	Error occurred in ADC initialization.	**1.** ADC SPI signal integrity issue. **2.** Error in ADCs.	**1.** Check signal integrity of SPI connections between the ADE9178 and ADCs. **2.** See the Quick Start section and ensure that ADC related parameters are configured properly. **3.** Read STATUS registers of ADCs to check if any error bits are set. **4.** Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.	**1.** Read STATUS registers of ADCs to check if any error bits are set. **2.** Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.
ERROR0[1]	Internal Error Occurred.		Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.	Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.
ERROR1[2]	Internal Error Occurred.		Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.	Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.
ERROR2[3]	Internal Error Occurred.		Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.	Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.
ERROR3[4]	Internal Error Occurred.		Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.	Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.
ERROR4[5]	Internal Error Occurred.		Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.	Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.
ADC_CRC_ERROR[6]	ADC SPI CRC Error Occurs.	ADC SPI CRC errors are detected on the samples read from the ADCs.	**1.** Check signal integrity of SPI connections between the ADE9178 and ADCs. **2.** Ensure that the ADC related registers are configured correctly as per the Quick Start section. **3.** Read STATUS registers of ADCs to check if any error bits are set. **4.** If error persists, reset the ADE9178 and ADCs and perform ADC initialization again.	If CRC error occurs, the ADE9178 automatically discards the ADC samples, and previous good samples are used for measurements.
ERROR5[7]	Internal Error Occurred.		Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.	Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.
DREADY_FREQ_ERROR[8]	ADC Data Ready Frequency Error. This bit is set when ADC Data Ready frequency is not 4	ADC DREADY frequency might be configured wrong. ADCs reset while ADC is running.	**1.** Check signal integrity of the DREADY signal. **2.** Reset the ADE9178 and ADCs. Initialize ADCs using	Clear DREADY_FREQ_ERR bit by writing 1 to bit 8 of ERROR_STATUS register. If the bit re-asserts reset the ADE9178

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Table 27. ERROR_STATUS Register Table (Continued)

ERROR_STATUS Bit	Description	Possible Cause of Issue	How to Debug during Development	How to Handle in the Field
	kHz. Metrology stops processing if this bit is set to 1.		ADC_INIT of ADC_CONTROL register after ADE9178 reset.	and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.
ADC0_STATUS0[9]	ADC0 STATUS0. This bit is set when one or more bits of STATUS0 register of ADC0 are set.	One or more bits in STATUS0[0:5] of ADC0 is set.	STATUS0 register of ADC0 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC0_STATUS1[10]	ADC0 STATUS1. This bit is set when one or more bits of STATUS1 register of ADC0 are set.	One or more bits in STATUS1[1:3] of ADC0 is set.	STATUS1 register of ADC0 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC0_STATUS2[11]	ADC0 STATUS2. This bit is set when one or more bits of STATUS2 register of ADC0 are set.	STATUS0[6] of ADC0 is set.	STATUS2 register of ADC0 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC1_STATUS0[12]	ADC1 STATUS0. This bit is set when one or more bits of STATUS0 register of ADC1 are set.	One or more bits in STATUS0[0:5] of ADC1 is set.	STATUS0 register of ADC1 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC1_STATUS1[13]	ADC1 STATUS1. This bit is set when one or more bits of STATUS1 register of ADC1 are set.	One or more bits in STATUS1[1:3] of ADC1 is set.	STATUS1 register of ADC1 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC1_STATUS2[14]	ADC1 STATUS2. This bit is set when one or more bits of STATUS2 register of ADC1 are set.	STATUS0[6] of ADC1 is set.	STATUS2 register of ADC1 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC2_STATUS0[15]	ADC2 STATUS0. This bit is set when one or more bits of STATUS0 register of ADC2 are set.	One or more bits in STATUS0[0:5] of ADC2 is set.	STATUS0 register of ADC2 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC2_STATUS1[16]	ADC2 STATUS1. This bit is set when one or more bits of STATUS1 register of ADC2 are set.	One or more bits in STATUS1[1:3] of ADC2 is set.	STATUS1 register of ADC2 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC2_STATUS2[17]	ADC2 STATUS2. This bit is set when one or more bits of STATUS2 register of ADC2 are set.	STATUS0[6] of ADC2 is set.	STATUS2 register of ADC2 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC3_STATUS0[18]	ADC3 STATUS0. This bit is set when one or more bits of STATUS0 register of ADC3 are set.	One or more bits in STATUS0[0:5] of ADC3 is set.	STATUS0 register of ADC3 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC3_STATUS1[19]	ADC3 STATUS1. This bit is set when one or more bits of STATUS1 register of ADC3 are set.	One or more bits in STATUS1[1:3] of ADC3 is set.	STATUS1 register of ADC3 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ADC3_STATUS2[20]	ADC3 STATUS2. This bit is set when one or more bits of STATUS2 register of ADC3 are set.	STATUS0[6] of ADC3 is set.	STATUS2 register of ADC3 can be read to know which error occurred. For more details and to know more about the register, refer to the *Register Details* section of the ADE91xx data sheet.	
ERROR6[21]	Internal Error Occurred.		Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT	Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT

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Table 27. ERROR_STATUS Register Table (Continued)

ERROR_STATUS Bit	Description	Possible Cause of Issue	How to Debug during Development	How to Handle in the Field
			of ADC_CONTROL register after ADE9178 reset.	of ADC_CONTROL register after ADE9178 reset.
ERROR7[22]	Internal Error Occurred.		Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.	Reset the ADE9178 and ADCs. Initialize ADCs using ADC_INIT of ADC_CONTROL register after ADE9178 reset.

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IRQ Reoccurrence Behavior

Most bits of STATUS0 and STATUS1 (for example, CFx, RMSONERDY, PF_RDY, and ZXx) are associated with an event and these bits are set whenever the corresponding events occur. For certain other bits, the rate at which the bits are set are dependent upon a user-configurable value as shown in Table 28.

Table 28. Reoccurrence Behavior

STATUS0 Bits	Reoccurrence Behavior
EGY_RDY	After every EGY_TIME + 1 ms or EGY_TIME + 1 half-line cycles. Note, it is recommended to use time-based accumulation mode (for more details, see Table 30).
SEQERR	After every SEQ_CYC number of consecutive phase-sequence errors.
ZXTOAV, ZXTOBV, ZXTOCV	After every ZXTOUT + 1 ms.

The IRQ reoccurrence behavior for dips/swells bits in STATUS2/STATUS3 registers depends upon the DIP_SWELL_x_IRQ_MODE configuration bit in CONFIG0 register. When this configuration bit is 0 ,then the STATUS register bit is set only when entering or exiting the dip/swell condition. However, if the configuration bit is set to 1 then the STATUS bits are set periodically after every DIP_CYC/SWELL_CYC cycles for as long as the channel is in dips/swells condition.

POWER MANAGEMENT

Initialising the Chipset

The ADE9178 checks its integrity during boot time. If the check fails pins $\overline{\text{HOST\_RDY}}$ and $\overline{\text{HOST\_ERR}}$ go low together and the ADE9178 enters into a standby mode. A hardware reset is required to take the ADE9178 out of this state. For more details on how to perform a hardware reset, see the Hardware Reset section.

Hardware Reset

The ADE9178 has a dedicated reset pin. Hardware reset occurs when the $\overline{\text{RESET}}$ pin is brought low (default state is weak pull-up) for at least 1.5 µs. During a hardware reset, all the registers are set to their default values. The ADE9178 and ADE91xx reset pins should be connected together as shown in the Test Circuit section.

If ADE9178 is reset due to power cycle or an unexpected external interference, RSTDONE bit of STATUS0 register is set and IRQ0 is raised. The application should follow the full start-up procedure to configure the ADE9178 into the required state. For more details on how to configure the ADE9178, see the Quick Start section.

APPLICATIONS INFORMATION

CALIBRATION METHOD

The system is calibrated at nominal operating voltage and current using an accurate source. The worked out example is shown only for phase A. The calculation remains same for other channels as well. All calibration steps involve providing a known signal to the relevant ADC channels and compare one of the output registers to the expected value of the register.

System Parameters:

- $V_{NOMINAL}$ = 220 V_{RMS}
- $I_{NOMINAL}$ = 10 A_{RMS}
- Line Frequency = 50 Hz
- Shunt Resistor = 500 µΩ
- Voltage Divider
  - R1 = 990 kΩ
  - R2 = 1 kΩ
  - Divider Ratio = 0.001

Theoretical Full-Scale Voltage =

$$V_{FS\_T} = \left(\frac{V_{ADC\_FS}}{Divider\_Ratio}\right) \div \sqrt{2} = \left(\frac{1}{0.001}\right) \div \sqrt{2} = 707 V_{RMS} \quad (37)$$

Note that the fully-differential V_{FS_T} is used for this calculation. See the Worked Examples section on how to calculate V_{FS_T} for the system.

Full-Scale Current =

$$I_{FS} = \left(\frac{I_{ADC\_FS}}{Shunt\_Resistance}\right) \div \sqrt{2} = \left(\frac{0.03125}{500 \times 10^{-6}}\right) \div \sqrt{2} = 44.188\, A_{RMS} \quad (38)$$

Gain Calibration

This section explains how to calculate the xxGAIN register, which affects all output parameters of the ADE9178. RMS values are used to calibrate the gain.

With the nominal voltage and current inputs, read the appropriate RMS register (for example, AIRMS, AVRMS, or AUXRMS). It is recommended to read the RMS values once per zero crossings for 1 sec and average them for better accuracy.

The expected RMS register value for given voltage and current can be calculated as follows:

$$xRMS_{EXPECTED} = \frac{RMS_{FS\_CODES} \times X_{NOMINAL}}{X_{FS}} \quad (39)$$

where, $X_{NOMINAL}$ is the nominal signal applied at the ADC input and X_{FS} is either V_{FS_T}, I_{FS}, or AUX_{FS}.

The xxGAIN register can be calculated from expected and observed RMS register as follows:

$$xxGAIN = \left(\frac{xRMS_{EXPECTED}}{xRMS_{MEASURED}} - 1\right) \times 2^{27} \quad (40)$$

Example

With the given example system parameters, the following equation shows the calculations for AV channel gain:

$$AVRMS_{EXPECTED} = \frac{107310840 \times 220}{707} = 33392341\, decimal \quad (41)$$

If $AVRMS_{MEASURED}$ = 33512088 decimal, then:

$$AVGAIN = \left(\frac{33392341}{33512088} - 1\right) \times 2^{27} = -479595\ decimal = 0 \times FFF8AE96 \quad (42)$$

DC Offset Calibration

All xOS registers must be 0 for AC metrology applications.

RMS Offset Calibration

To calibrate RMS offset register, apply a small signal typically at 2000:1 or less dynamic range to the channel the user is trying to calibrate. It is recommended to keep the other channel as nominal. In this example, to calibrate the current offset, the calibration current is set to 20 mA and the voltage is kept at nominal. Read the RMS values once per zero crossings for 1 sec and average them for better accuracy.

The expected RMS register value for given input can be calculated as follows:

$$xRMS_{EXPECTED} = \frac{RMS_{FS\_CODES} \times X_{REDUCED}}{X_{FS}} \quad (43)$$

where, $X_{REDUCED}$ is the reduced calibration signal applied at the ADC input and X_{FS} is either V_{FS_T}, I_{FS}, or AUX_{FS}.

The xxRMSOS register can be calculated from expected and observed RMS register as follows:

$$xxRMSOS = \left(\frac{xRMS^2_{EXPECTED} - xRMS^2_{MEASURED}}{2^{15}}\right) \quad (44)$$

Example

With the reduced input current to 20 mV, the following equation shows the calculations for AI channel offset:

$$AIRMS_{EXPECTED} = \frac{107310840 \times 0.02}{44.188} = 48570\, decimal \quad (45)$$

If $AIRMS_{MEASURED}$ = 48733 decimal, then:

$$AIRMSOS = \left(\frac{48570^2 - 48733^2}{2^{15}}\right) = -484\ decimal = 0 \times FFFFFE1D \quad (46)$$

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Power Gain Calibration

xPGAIN is the gain calibration register for phase x. The active and apparent powers in each phase have a common gain register.

To configure the ADE9178, do the following steps:

1. Apply nominal voltage and current at power factor = 1.
2. Set EP_CFG = 0x15 and EGY_TIME = 999d (1 sec accumulation).
3. Read the xWATTHR_SIGNED_HI register (throw away first sample).

The expected xWATTHR_SIGNED_HI register value for nominal inputs can be calculated as follows:

$$xWATTHR\_SIGNED\_HI_{EXPECTED} = I_{FSP} \times V_{FS\_TP} \times POW_{FS\_CODES} \times Accumulation\_Time \times 4000 \times 2^{-13} \quad (47)$$

where, I_{FSP} is the nominal current as a fraction of full scale and V_{FS_TP} is the nominal voltage as a fraction of full scale.

The xPGAIN register value can be obtained as follows:

$$xPGAIN = \left(\frac{xWATTHR\_SIGNED\_HI_{EXPECTED}}{xWATTHR\_SIGNED\_HI_{MEASURED}} - 1\right) \times 2^{27} \quad (48)$$

Example

With the given example system parameters, the following equations show the calculations for APGAIN:

$$I_{FSP} = \frac{10}{44.188} = 0.22631 \quad (49)$$

$$V_{FS\_TP} = \frac{220}{707} = 0.31117 \quad (50)$$

$$AWATTHR\_SIGNED\_HI_{EXPECTED} = 0.22631 \times 0.31117 \times 85829040 \times 1 \times 4000 \times 2^{-13} = 2951248 \text{ decimal} \quad (51)$$

If AWATTHR_SIGNED_HI$_{MEASURED}$ = 2846714 decimal, then:

$$APGAIN = \left(\frac{2951248}{2846714} - 1\right) \times 2^{27} = 4928600 \; decimal = 0 \times 4B313D \quad (52)$$

Power Offset Calibration

Like the RMS offset calibration, the power offset calibration is performed with a small current at 5000:1 or less dynamic range. In this example, the offset calibration current is 20 mA and the voltage is 220 V.

To configure the ADE9178, do the following steps:

1. Apply nominal voltage and offset calibration current at power factor = 1.
2. Set EP_CFG = 0x15 and EGY_TIME = 9999d (10 sec accumulation).
3. Read the xWATTHR_SIGNED_HI register (throw away first sample).

The expected xWATTHR_SIGNED_HI register value for nominal inputs can be calculated as follows:

$$xWATTHR\_SIGNED\_HI_{EXPECTED} = I_{FSP} \times V_{FS\_TP} \times POW_{FS\_CODES} \times Accumulation\_Time \times 4000 \times 2^{-13} \quad (53)$$

where, I_{FSP} is the nominal current as a fraction of full scale and V_{FS_TP} is the nominal voltage as a fraction of full scale.

The xWATTOS register value can be obtained as follows:

$$xWATTOS = \frac{xWATTHR\_SIGNED\_HI_{EXPECTED} - xWATTHR\_SIGNED\_HI_{MEASURED}}{Accumulation\_Time \times 4000 \times 2^{-13}} \quad (54)$$

Example

With the given example system parameters, the following equations show the calculations for APGAIN:

$$I_{FSP} = \frac{0.02}{44.188} = 0.00045 \quad (55)$$

$$V_{FS\_TP} = \frac{220}{707} = 0.31117 \quad (56)$$

$$AWATTHR\_SIGNED\_HI_{EXPECTED} = 0.00045 \times 0.31117 \times 85829040 \times 10 \times 4000 \times 2^{-13} = 59025 \, decimal \quad (57)$$

If AWATTHR_SIGNED_HI$_{MEASURED}$ = 58134 decimal, then:

$$AWATTOS = \frac{59025 - 58134}{10 \times 4000 \times 2^{-13}} = 182 \, decimal = 0 \times B6 \quad (58)$$

Phase Calibration

It is recommended to keep the voltage channel xVPHCAL as default value (0). To calculate xIPHCAL, apply a nominal current and voltage at lagging power factor of 0.5, calculate phase error from power factor xPF measured as follows:

$$\phi = \left(\frac{\pi}{3} - \cos^{-1}\left(\frac{xPF_{MEASURED}}{2^{27}}\right)\right) \times -1 \quad (59)$$

The xIPHCAL register can be calculated as follows:

$$xIPHCAL = \frac{\sin(\phi - \omega) + \sin(\omega)}{\sin(2\omega - \phi)} \times 2^{27}, where, \omega = 2\pi \times f_{LINE} \times \frac{1}{4000} \quad (60)$$

APPLICATIONS INFORMATION

Example

If $APF_{MEASURED}$ = 67144872 decimal, then:

$$\phi = \left(\frac{\pi}{3} - \cos^{-1}\left(\frac{67144872}{2^{27}}\right)\right) \times -1 = -0.00031 \quad (61)$$

For 50 Hz signal:

$$\omega = 2\pi \times 50 \times \frac{1}{4000} = 0.07854 \quad (62)$$

$$AIPHCAL = \frac{\sin(-0.00031 - 0.07854) + \sin(0.07854)}{\sin(2 \times 0.07854 - -0.00031)} \times 2^{27} = -264472 \quad decimal = 0 \times FFFBF6E8 \quad (63)$$

QUICK START

This section describes how to setup the ADE9178 and ADE91xx chipset for a 3-phase and 4-wire measurement. To setup, do the following steps:

1. Configure the Host MCU to monitor to $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{HOST\_RDY}$, and $\overline{HOST\_ERR}$ pins of the ADE9178.
2. Issue a hardware reset to ADE9178 and ADCs by toggling corresponding reset pins. For more details, see the Hardware Reset section.
3. The ADE9178 checks the integrity during boot time and both $\overline{HOST\_RDY}$ and $\overline{HOST\_ERR}$ pins go low if the integrity error is detected. If this happens, then toggle the hardware reset pin of the ADE9178. If the error persists, contact support team.
4. Wait for $\overline{IRQ0}$ interrupt from the ADE9178 and:
   a. Read the STATUS0 register and check that the RSTDONE bit is set. Note that the RSTDONE bit is expected to be set for first $\overline{IRQ0}$. Otherwise, there is an internal error and it is recommended to reset the ADE9178.
   b. Clear RSTDONE interrupt by writing 1 to the RSTDONE bit in the STATUS0 register.
5. By default all error interrupts in the ERROR_STATUS register are enabled and $\overline{IRQ1}$ is triggered if there is an error. The details of the error can be obtained by reading ERROR_STATUS register. For more details, see the Interrupts and Status Outputs section.
6. If energy is monitored using the CF outputs, configure the following registers (skip this step if the CF outputs are not used):
   a. Configure the PWRSEL bits in the CFx_CONFIG register to select the energy type to monitor.
   b. Configure the PHASESEL bits in the CFx_CONFIG register to select the phases to include in the CF calculation.
   c. Configure the ACCMODE bits in the CFx_CONFIG register to select the accumulation mode.
   d. Set the CFx_THR register based on the required impulses per kilowatt-hour. For CFx_THR formula, see the CF Pulse Generation section.
   e. Configure the WIDTHSEL bit in the CFx_CONFIG register to set the low-pulse width. For more details, see Table 20.
   f. Enable the CF by clearing the CFDIS bit in the CFx_CONFIG register to 0.
7. If energy is monitored using energy registers, configure the following registers:
   a. Configure the EGY_TMR_MODE bit in the EP_CFG register to select time-based accumulation mode (EGY_TMR_MODE = 0). Set the required samples in the EGY_TIME register (N − 1 ms).
      1. It is recommended to use time-based accumulation mode (for more details, see Table 30).
   b. Configure the EGY_LD_ACCUM bit in the EP_CFG register to add the internal energy register to user energy register on EGYRDY (EGY_LD_ACCUM = 0), or to overwrite the user energy register with the internal energy register value (EGY_LD_ACCUM = 1).
   c. Configure the RD_RST_EN bit in the EP_CFG register to enable reset of user energy registers on read (RD_RST_EN = 1), or to disable reset of user energy registers on read (RD_RST_EN = 0).
   d. Configure the NOLOAD_TMR bits in the EP_CFG register and set the ACT_NL_LVL and APP_NL_LVL level registers to detect no load and prevent energy accumulation of noise. For more details, see the No Load Detection section.
8. The ADE9178 can provide interrupts for a variety of events on the $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, and $\overline{IRQ3}$ pins. The MASK0, MASK1, MASK2, MASK3, or ERROR_MASK and STATUS0, STATUS1, STATUS2, STATUS3, or ERROR_STATUS registers manage the respective interrupt pins. For more details, see the Interrupts and Status Outputs section.
9. Write calibration coefficient registers to the ADE9178. For more details, see the Calibration Method section.
10. Configure ADC related parameters and start the data processing as follows:
    a. Configure number of ADCs connected by writing to the NUM_ADC bits in the ADC_CONFIG register.
    b. Review ADC_REDIRECT1 and ADC_REDIRECT2 default values and update if the channel mapping required is different to default. Note that the ADC_REDIRECT1 and ADC_REDIRECT2 must be updated if the number of ADCs present is different than the default 4. For more details, see Table 8.
    c. Initialize the ADCs by setting ADC_INIT bit in the ADC_CONTROL register to 1 (Auto Clears).
    d. Separately, enable data capture and processing by setting the ADC_RUN bit in the ADC_CONTROL register to 1 (Auto Clears is setting ADC_RUN = 1 fails).

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11. See the following sections to set up other metrology features:
    a. Total Active Power
    b. Total Apparent Power
    c. Line Period Calculation:
        1. It is recommended to configure CONFIG0:PERIOD_AVG_CFG[4:3] to 0x2 to average the period over 16 samples. This reduces the period jitter.
    d. RMS of One Cycle:
        1. It is recommended to configure CONFIG0:RMSONE_SRC_SEL[11] to 0x1 to use data from before the HPF for the fastest response time.
        2. It is recommended to configure CONFIG0:PERIOD_AVG_CFG[4:3] to 0x2 to average the period over 16 samples. This reduces the period jitter.
    e. RMS of Half Cycle:
        1. It is recommended to configure CONFIG0:RMSHALF_SRC_SEL[11] to 0x1 to use data from before the HPF for the fastest response time.
        2. It is recommended to configure CONFIG0:PERIOD_AVG_CFG[4:3] to 0x2 to average the period over 16 samples. This reduces the period jitter.
    f. Peak Detection
    g. Dip and Swells
    h. Phase-Sequence Error Detection
    i. Zero-Crossing Timeout
    j. Neutral Current Mismatch
    k. PEN Fault Detection
    l. Waveform Streaming
12. Enable energy accumulation by setting the EGY_PWR_EN bit in the EP_CFG register to 1.
13. It is recommended to enable CRC check of the configuration registers. For more details, see the CRC of Configuration Registers section.
14. To prevent any changes to the ADE9178 configuration, enable write protection by writing 1 to the CONFIG_LOCK register. For more details, see the Configuration Lock section.
15. After the RUN bit of ADC_CONTROL is set, the output registers update at a frequency shown in Table 26. For more details, see the Output Register Update Rates section.

For more detailed information on how to set up the ADE9178 in an EVSE application, refer to the application note, Using ADE9178 for EV Charger Metrology Solution.

LAYOUT GUIDELINES

For layout guidelines, refer to the application note Using ADE9178 for EV Charger Metrology Solution.

SILICON ANOMALY

This anomaly list describes the known issues with the ADE9178 silicon identified by the version2 register (Address 0x40B) being equal to 0x09FD5D0D.

Table 29. ADE9178 Functionality Issues

Silicon Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	Number of Reported Issues
Version2 = 0x09FD5D0D	ADE9178GTL	Released	Rev. A	1 (err001)

FUNCTIONALITY ISSUES

Table 30. err001: No Load with Line-Cycle Accumulation

	Description
Background	When ADE9178 is in a no load condition (for more details, see No Load Detection section), no energy should be accumulating into the output energy registers.
Issue	When ADE9178 is in a no load condition and ADE9178 is configured for line-cycle accumulation mode (EP_CFG: EGY_TMR_MODE[1] =0x1), some residual energy is accumulated into the output energy registers, which could cause errors over time.
Workaround	Use time based accumulation (EP_CFG: EGY_TMR_MODE[1] =0x0).
Related Issues	None.

REGISTER NUMBER FORMAT

Table 31 shows if the number is signed/unsigned and specifies the valid range for input registers.

Table 31. Register Number Format

Register Group	Relevant Registers	Input/Output Register	Signed/Unsigned	Range	Related Section
Gain Registers	xxGAIN, AUXyGAIN	Input	Signed	0xE8000000 to 0x8000000	Gain Calibration, Power Gain Calibration
Phase Cal Registers	xxPHCAL, AUXyPHCAL	Input	Signed	0xF8000000 to 0x8000000	Phase Calibration
Active Power Offset Registers	xWATTOS	Input	Signed	0xF8000000 to 0x8000000	Power Offset Calibration
No Load Level Registers	xxx_NL_LVL	Input	Unsigned	0x0 to 0x7FFFFFFF	No Load Detection
Channel Offset Registers	xxOS, AUXyOS	Input	Signed	0xFF800000 to 0x800000	Gain and Offset Compensation
RMS Offset Registers	xxRMSOS, xxRMSHALFOS, xxRMSONEOS, AUXyRMSOS, AUXyRMSHALFOS, AUXyRMSONEOS, ISUMRMSOS, VSUMRMSONEOS, VxxRMSONEOS	Input	Signed	0x80000000 to 0x7FFFFFFF	RMS Offset Calibration
CF Threshold	CF1_THR, CF2_THR	Input	Unsigned	0x28ED2D to 0x7FFFFFFF	CF Pulse Generation
Dip/Swell Cycle Registers	xxDIPHALF_CYC, xxDIPONE_CYC, AUXyDIPHALF_CYC, AUXyDIPONE_CYC, xxSWELLHALF_CYC, xxSWELLONE_CYC, AUXySWELLHALF_CYC, AUXySWELLONE_CYC, VSUMSWELLONE_CYC, VxxDIPONE_CYC, VxxSWELLONE_CYC	Input	Unsigned	0x0 to 0xFFFFFFFF	Dip and Swells
Zero-Crossing Timeout	ZXTOUT	Input	Unsigned	0x0 to 0xFFFFFFFF	Zero-Crossing Timeout
Phase-Sequence Error Detection	SEQ_CYC	Input	Unsigned	0x0 to 0xFFFFFFFF	Phase-Sequence Error Detection
Energy Accumulation Time	EGY_TIME	Input	Unsigned	0x0 to 0xFFFFFFFF	Energy Calculation
CF Pulse-Width Configuration	CF_LTMR	Input	Unsigned	0x1 to 0x13880	CF Pulse Generation
Zero-Crossing Threshold	ZXTHRSH	Input	Unsigned	0x0 to 0xFFFFFFFF	Zero-Crossing Detection
User-Configured Period Values	USER_PERIOD, USER_PERIOD_HALF	Input	Unsigned	0x0 to 0xFFFFFFFF	RMS of One Cycle, RMS of Half Cycle
Dip/Swell Level Registers	xxDIPHALF_LVL, xxDIPONE_LVL, AUXyDIPHALF_LVL, AUXyDIPONE_LVL, xxSWELLHALF_LVL, xxSWELLONE_LVL, AUXySWELLHALF_LVL, AUXySWELLONE_LVL, VSUMSWELLONE_LVL, VxxDIPONE_LVL, VxxSWELLONE_LVL	Input	Unsigned	0x0 to 0xFFFFFFFF	Dip and Swells
ISUMRMS Threshold	ISUMLVL	Input	Unsigned	0x0 to 0xFFFFFFFF	Neutral Current Mismatch

REGISTER NUMBER FORMAT

Table 31. Register Number Format (Continued)

Register Group	Relevant Registers	Input/Output Register	Signed/Unsigned	Range	Related Section
Nominal Phase Voltage RMS	VNOM	Input	Unsigned	0x0 to 0xFFFFFFFF	Total Apparent Power
RMS Registers	xxRMS, xxRMSHALF, xxRMSONE, AUXyRMS, AUXyRMSHALF, AUXyRMSONE, ISUMRMS, VSUMRMSONE, VxxRMSONE	Output	Unsigned		Full-Scale Codes And Conversion Equations
Dip/Swell Registers	xxDIPHALF, xxDIPONE, AUXyDIPHALF, AUXyDIPONE, xxSWELLHALF, xxSWELLONE, AUXySWELLHALF, AUXySWELLONE, VSUMSWELLONE, VxxDIPONE, VxxSWELLONE	Output	Unsigned		Dip and Swells
Apparent Power Registers	xVA	Output	Unsigned		Full-Scale Codes And Conversion Equations
Active Power Registers	xWATT	Output	Signed		Full-Scale Codes And Conversion Equations
Power-Factor Registers	xPF	Output	Signed		Full-Scale Codes And Conversion Equations
Energy Registers	xWATTHR_xxxx_xx, xVAHR_xx	Output	Signed		Full-Scale Codes And Conversion Equations
Angle Registers	ANGL_xx_yy	Output	Unsigned		Full-Scale Codes And Conversion Equations
Peak Registers	xPEAK	Output	Unsigned		Peak Detection
Period Registers	PEN_PERIOD, xPERIOD, COM_PERIOD	Output	Unsigned		Line Period Calculation

REGISTER SUMMARY: ADE9178

Table 32. Access Mode Description

Access Mode	Description
R/W	Register has Read and Write access.
R	Register has Read access only.
R/W1C	Register has Read access and Write 1 to clear.

Table 33. ADE9178 Register Summary

Address	Name	Description	Reset	Access
0x000	AVGAIN	Phase A Voltage Gain Adjust.	0x00000000	R/W
0x001	AVOS	Phase A Voltage Channel Offset.	0x00000000	R/W
0x002	AVPHCAL	Phase A Voltage-Phase Correction Factor.	0x00000000	R/W
0x003	AVRMSOS	Phase A Voltage RMS Offset.	0x00000000	R/W
0x004	AVRMSHALFOS	Phase A Voltage Half-Cycle RMS Offset.	0x00000000	R/W
0x005	AVRMSONEOS	Phase A Voltage One-Cycle RMS Offset.	0x00000000	R/W
0x006	AVDIPHALF_LVL	Phase A Voltage RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x007	AVDIPONE_LVL	Phase A Voltage RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x008	AVSWELLHALF_LVL	Phase A Voltage RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x009	AVSWELLONE_LVL	Phase A Voltage RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x00A	AVDIPHALF_CYC	Phase A Voltage RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x00B	AVDIPONE_CYC	Phase A Voltage RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x00C	AVSWELLHALF_CYC	Phase A Voltage RMSHALF Swell Half-Line Cycle Configuration.	0xFFFFFFFF	R/W
0x00D	AVSWELLONE_CYC	Phase A Voltage RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x00E	AIGAIN	Phase A Current Gain Adjust.	0x00000000	R/W
0x00F	AIOS	Phase A Current Channel Offset.	0x00000000	R/W
0x010	AIPHCAL	Phase A Current-Phase Correction Factor.	0x00000000	R/W
0x011	AIRMSOS	Phase A Current RMS Offset.	0x00000000	R/W
0x012	AIRMSHALFOS	Phase A Current Half-Cycle RMS Offset.	0x00000000	R/W
0x013	AIRMSONEOS	Phase A Current One-Cycle RMS Offset.	0x00000000	R/W
0x014	AIDIPHALF_LVL	Phase A Current RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x015	AIDIPONE_LVL	Phase A Current RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x016	AISWELLHALF_LVL	Phase A Current RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x017	AISWELLONE_LVL	Phase A Current RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x018	AIDIPHALF_CYC	Phase A Current RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x019	AIDIPONE_CYC	Phase A Current RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x01A	AISWELLHALF_CYC	Phase A Current RMSHALF Swell Half-Line Cycle Configuration.	0xFFFFFFFF	R/W
0x01B	AISWELLONE_CYC	Phase A Current RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x01C	BVGAIN	Phase B Voltage Gain Adjust.	0x00000000	R/W
0x01D	BVOS	Phase B Voltage Channel Offset.	0x00000000	R/W
0x01E	BVPHCAL	Phase B Voltage-Phase Correction Factor.	0x00000000	R/W
0x01F	BVRMSOS	Phase B Voltage RMS Offset.	0x00000000	R/W
0x020	BVRMSHALFOS	Phase B Voltage Half-Cycle RMS Offset.	0x00000000	R/W
0x021	BVRMSONEOS	Phase B Voltage One-Cycle RMS Offset.	0x00000000	R/W
0x022	BVDIPHALF_LVL	Phase B Voltage RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x023	BVDIPONE_LVL	Phase B Voltage RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x024	BVSWELLHALF_LVL	Phase B Voltage RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x025	BVSWELLONE_LVL	Phase B Voltage RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x026	BVDIPHALF_CYC	Phase B Voltage RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x027	BVDIPONE_CYC	Phase B Voltage RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x028	BVSWELLHALF_CYC	Phase B Voltage RMSHALF Swell Half-Line Cycle Configuration.	0xFFFFFFFF	R/W

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x029	BVSWELLONE_CYC	Phase B Voltage RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x02A	BIGAIN	Phase B Current Gain Adjust.	0x00000000	R/W
0x02B	BIOS	Phase B Current Channel Offset.	0x00000000	R/W
0x02C	BIPHCAL	Phase B Current-Phase Correction Factor.	0x00000000	R/W
0x02D	BIRMSOS	Phase B Current RMS Offset.	0x00000000	R/W
0x02E	BIRMSHALFOS	Phase B Current Half-Cycle RMS Offset.	0x00000000	R/W
0x02F	BIRMSONEOS	Phase B Current One-Cycle RMS Offset.	0x00000000	R/W
0x030	BIDIPHALF_LVL	Phase B Current RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x031	BIDIPONE_LVL	Phase B Current RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x032	BISWELLHALF_LVL	Phase B Current RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x033	BISWELLONE_LVL	Phase B Current RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x034	BIDIPHALF_CYC	Phase B Current RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x035	BIDIPONE_CYC	Phase B Current RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x036	BISWELLHALF_CYC	Phase B Current RMSHALF Swell Half-Line Cycle Configuration.	0xFFFFFFFF	R/W
0x037	BISWELLONE_CYC	Phase B Current RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x038	CVGAIN	Phase C Voltage Gain Adjust.	0x00000000	R/W
0x039	CVOS	Phase C Voltage Channel Offset.	0x00000000	R/W
0x03A	CVPHCAL	Phase C Voltage-Phase Correction Factor.	0x00000000	R/W
0x03B	CVRMSOS	Phase C Voltage RMS Offset.	0x00000000	R/W
0x03C	CVRMSHALFOS	Phase C Voltage Half-Cycle RMS Offset.	0x00000000	R/W
0x03D	CVRMSONEOS	Phase C Voltage One-Cycle RMS Offset.	0x00000000	R/W
0x03E	CVDIPHALF_LVL	Phase C Voltage RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x03F	CVDIPONE_LVL	Phase C Voltage RMSONE Dip-Cycle Given in Line Cycles.	0x00000000	R/W
0x040	CVSWELLHALF_LVL	Phase C Voltage RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x041	CVSWELLONE_LVL	Phase C Voltage RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x042	CVDIPHALF_CYC	Phase C Voltage RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x043	CVDIPONE_CYC	Phase C Voltage RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x044	CVSWELLHALF_CYC	Phase C Voltage RMSHALF Swell Half-Line Cycle Configuration.	0xFFFFFFFF	R/W
0x045	CVSWELLONE_CYC	Phase C Voltage RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x046	CIGAIN	Phase C Current Gain Adjust.	0x00000000	R/W
0x047	CIOS	Phase C Current Channel Offset.	0x00000000	R/W
0x048	CIPHCAL	Phase C Current-Phase Correction Factor.	0x00000000	R/W
0x049	CIRMSOS	Phase C Current RMS Offset.	0x00000000	R/W
0x04A	CIRMSHALFOS	Phase C Current Half-Cycle RMS Offset.	0x00000000	R/W
0x04B	CIRMSONEOS	Phase C Current One-Cycle RMS Offset.	0x00000000	R/W
0x04C	CIDIPHALF_LVL	Phase C Current RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x04D	CIDIPONE_LVL	Phase C Current RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x04E	CISWELLHALF_LVL	Phase C Current RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x04F	CISWELLONE_LVL	Phase C Current RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x050	CIDIPHALF_CYC	Phase C Current RMSHALF Dip Specified in Half-Line Cycles.	0xFFFFFFFF	R/W
0x051	CIDIPONE_CYC	Phase C Current RMSONE Dip Specified in Line Cycles.	0xFFFFFFFF	R/W
0x052	CISWELLHALF_CYC	Phase C Current RMSHALF Swell Specified in Half-Line Cycles.	0xFFFFFFFF	R/W
0x053	CISWELLONE_CYC	Phase C Current RMSONE Swell Specified in Line Cycles.	0xFFFFFFFF	R/W
0x054	AUX0GAIN	Auxiliary 0 Channel Gain Adjust.	0x00000000	R/W
0x055	AUX0OS	Auxiliary 0 Channel Offset.	0x00000000	R/W
0x056	AUX0PHCAL	Auxiliary 0 Channel-Phase Correction Factor.	0x00000000	R/W
0x057	AUX0RMSOS	Auxiliary 0 Channel RMS Offset.	0x00000000	R/W

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x058	AUX0RMSHALFOS	Auxiliary 0 Half-Cycle RMS Offset.	0x00000000	R/W
0x059	AUX0RMSONEOS	Auxiliary 0 One-Cycle RMS Offset.	0x00000000	R/W
0x05A	AUX0DIPHALF_LVL	Auxiliary 0 Channel RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x05B	AUX0DIPONE_LVL	Auxiliary 0 Channel RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x05C	AUX0SWELLHALF_LVL	Auxiliary 0 Channel RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x05D	AUX0SWELLONE_LVL	Auxiliary 0 Channel RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x05E	AUX0DIPHALF_CYC	Auxiliary 0 RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x05F	AUX0DIPONE_CYC	Auxiliary 0 RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x060	AUX0SWELLHALF_CYC	Auxiliary 0 RMSHALF Swell Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x061	AUX0SWELLONE_CYC	Auxiliary 0 RMSHALF Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x062	AUX1GAIN	Auxiliary 1 Channel Gain Adjust.	0x00000000	R/W
0x063	AUX1OS	Auxiliary 1 Channel Offset.	0x00000000	R/W
0x064	AUX1PHCAL	Auxiliary 1 Channel-Phase Correction Factor.	0x00000000	R/W
0x065	AUX1RMSOS	Auxiliary 1 Channel-Filtered RMS Offset.	0x00000000	R/W
0x066	AUX1RMSHALFOS	Auxiliary 1 Channel Half-Cycle RMS Offset.	0x00000000	R/W
0x067	AUX1RMSONEOS	Auxiliary 1 Channel One-Cycle RMS Offset.	0x00000000	R/W
0x068	AUX1DIPHALF_LVL	Auxiliary 1 Channel RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x069	AUX1DIPONE_LVL	Auxiliary 1 Channel RMSONE Dip-Detection Threshold Level	0x00000000	R/W
0x06A	AUX1SWELLHALF_LVL	Auxiliary 1 Channel RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x06B	AUX1SWELLONE_LVL	Auxiliary 1 Channel RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x06C	AUX1DIPHALF_CYC	Auxiliary 1 RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x06D	AUX1DIPONE_CYC	Auxiliary 1 RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x06E	AUX1SWELLHALF_CYC	Auxiliary 1 RMSHALF Swell Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x06F	AUX1SWELLONE_CYC	Auxiliary 1 RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x070	AUX2GAIN	Auxiliary 2 Channel Gain Adjust.	0x00000000	R/W
0x071	AUX2OS	Auxiliary 2 Channel Offset.	0x00000000	R/W
0x072	AUX2PHCAL	Auxiliary 2 Channel-Phase Correction Factor.	0x00000000	R/W
0x073	AUX2RMSOS	Auxiliary 2 Channel-Filtered RMS Offset.	0x00000000	R/W
0x074	AUX2RMSHALFOS	Auxiliary 2 Channel Half-Cycle RMS Offset.	0x00000000	R/W
0x075	AUX2RMSONEOS	Auxiliary 2 Channel One-Cycle RMS Offset.	0x00000000	R/W
0x076	AUX2DIPHALF_LVL	Auxiliary 2 Channel RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x077	AUX2DIPONE_LVL	Auxiliary 2 Channel RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x078	AUX2SWELLHALF_LVL	Auxiliary 2 Channel RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x079	AUX2SWELLONE_LVL	Auxiliary 2 Channel RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x07A	AUX2DIPHALF_CYC	Auxiliary 2 RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x07B	AUX2DIPONE_CYC	Auxiliary 2 RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x07C	AUX2SWELLHALF_CYC	Auxiliary 2 RMSHALF Swell Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x07D	AUX2SWELLONE_CYC	Auxiliary 2 RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x07E	AUX3GAIN	Auxiliary 3 Channel Gain Adjust.	0x00000000	R/W
0x07F	AUX3OS	Auxiliary 3 Channel Offset.	0x00000000	R/W
0x080	AUX3PHCAL	Auxiliary 3 Channel-Phase Correction Factor.	0x00000000	R/W
0x081	AUX3RMSOS	Auxiliary 3 Channel-Filtered RMS Offset.	0x00000000	R/W
0x082	AUX3RMSHALFOS	Auxiliary 3 Channel Half-Cycle RMS Offset.	0x00000000	R/W
0x083	AUX3RMSONEOS	Auxiliary 3 Channel One-Cycle RMS Offset.	0x00000000	R/W
0x084	AUX3DIPHALF_LVL	Auxiliary 3 Channel RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x085	AUX3DIPONE_LVL	Auxiliary 3 Channel RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x086	AUX3SWELLHALF_LVL	Auxiliary 3 Channel RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x087	AUX3SWELLONE_LVL	Auxiliary 3 Channel RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x088	AUX3DIPHALF_CYC	Auxiliary 3 RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x089	AUX3DIPONE_CYC	Auxiliary 3 RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x08A	AUX3SWELLHALF_CYC	Auxiliary 3 RMSHALF Swell Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x08B	AUX3SWELLONE_CYC	Auxiliary 3 RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x08C	AUX4GAIN	Auxiliary 4 Channel Gain Adjust.	0x00000000	R/W
0x08D	AUX4OS	Auxiliary 4 Channel Offset.	0x00000000	R/W
0x08E	AUX4PHCAL	Auxiliary 4 Channel-Phase Correction Factor.	0x00000000	R/W
0x08F	AUX4RMSOS	Auxiliary 4 Channel-Filtered RMS Offset.	0x00000000	R/W
0x090	AUX4RMSHALFOS	Auxiliary 4 Channel Half-Cycle RMS Offset.	0x00000000	R/W
0x091	AUX4RMSONEOS	Auxiliary 4 Channel One-Cycle RMS Offset.	0x00000000	R/W
0x092	AUX4DIPHALF_LVL	Auxiliary 4 Channel RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x093	AUX4DIPONE_LVL	Auxiliary 4 Channel RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x094	AUX4SWELLHALF_LVL	Auxiliary 4 Channel RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x095	AUX4SWELLONE_LVL	Auxiliary 4 Channel RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x096	AUX4DIPHALF_CYC	Auxiliary 4 RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x097	AUX4DIPONE_CYC	Auxiliary 4 RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x098	AUX4SWELLHALF_CYC	Auxiliary 4 RMSHALF Swell Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x099	AUX4SWELLONE_CYC	Auxiliary 4 RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x09A	AUX5GAIN	Auxiliary 5 Channel Gain Adjust.	0x00000000	R/W
0x09B	AUX5OS	Auxiliary 5 Channel Offset.	0x00000000	R/W
0x09C	AUX5PHCAL	Auxiliary 5 Channel-Phase Correction Factor.	0x00000000	R/W
0x09D	AUX5RMSOS	Auxiliary 5 Channel-Filtered RMS Offset.	0x00000000	R/W
0x09E	AUX5RMSHALFOS	Auxiliary 5 Channel Half-Cycle RMS Offset.	0x00000000	R/W
0x09F	AUX5RMSONEOS	Auxiliary 5 Channel One-Cycle RMS Offset.	0x00000000	R/W
0x0A0	AUX5DIPHALF_LVL	Auxiliary 5 Channel RMSHALF Dip-Detection Threshold Level.	0x00000000	R/W
0x0A1	AUX5DIPONE_LVL	Auxiliary 5 RMSONE Dip Specified in Line Cycles.	0x00000000	R/W
0x0A2	AUX5SWELLHALF_LVL	Auxiliary 5 Channel RMSHALF Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x0A3	AUX5SWELLONE_LVL	Auxiliary 5 Channel RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x0A4	AUX5DIPHALF_CYC	Auxiliary 5 RMSHALF Dip Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0A5	AUX5DIPONE_CYC	Auxiliary 5 RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0A6	AUX5SWELLHALF_CYC	Auxiliary 5 RMSHALF Swell Half-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0A7	AUX5SWELLONE_CYC	Auxiliary 5 RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0A8	APGAIN	Phase A Power Gain Adjust.	0x00000000	R/W
0x0A9	AWATTOS	Phase A Total Active-Power Offset Correction.	0x00000000	R/W
0x0AA	BPGAIN	Phase B Power Gain Adjust.	0x00000000	R/W
0x0AB	BWATTOS	Phase B Total Active-Power Offset Correction.	0x00000000	R/W
0x0AC	CPGAIN	Phase C Power Gain Adjust.	0x00000000	R/W
0x0AD	CWATTOS	Phase C Total Active-Power Offset Correction.	0x00000000	R/W
0x0AE	CONFIG0	Configuration Register 0.	0x00000D80	R/W
0x0AF	PEAK_CONFIG	Peak-Detection Configuration Register.	0x00000000	R/W
0x0B0	PEN_CONFIG	PEN Fault-Channel Selection Configuration Register.	0x00003420	R/W
0x0B1	CF1_CONFIG	CF1 Configuration Register.	0x00000001	R/W
0x0B2	CF2_CONFIG	CF2 Configuration Register.	0x00000001	R/W
0x0B3	ISUMRMSOS	Offset Correction for ISUMRMS Calculation.	0x00000000	R/W
0x0B4	ISUMLVL	Threshold to Compare ISUMRMS Against.	0x00000000	R/W
0x0B5	VNOM	Nominal Phase Voltage RMS.	0x00000000	R/W

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x0B6	USER_PERIOD	User-Configured Line Period Value.	0x00500000	R/W
0x0B7	RMSHALF_CONFIG	RMSHALF Mode Selection Configuration.	0x00000000	R/W
0x0B8	USER_PERIOD_HALF	User-Configured Half-Line Cycle Period Value.	0x00280000	R/W
0x0B9	CF1_THR	Energy Threshold for CF1 Pulse Generation.	0x0000FFFF	R/W
0x0BA	CF2_THR	Energy Threshold for CF2 Pulse Generation.	0x0000FFFF	R/W
0x0BB	ZXTOUT	Zero-Crossing Timeout Configuration Register.	0x0000FFFF	R/W
0x0BC	ZXTHRSH	Zero-Crossing Threshold Register.	0x000019EA	R/W
0x0BD	ZX_LP_SEL	Zero-Crossing and Line Period Configuration.	0x0000000F	R/W
0x0BE	SEQ_CYC	Line-Cycles for Phase-Sequence Error Detection.	0x00000001	R/W
0x0BF	ACT_NL_LVL	No Load Threshold in the Active Power Datapath.	0x0000FFFF	R/W
0x0C0	APP_NL_LVL	No Load Threshold in the Apparent Power Datapath.	0x0000FFFF	R/W
0x0C1	EP_CFG	Energy and Power Accumulation Configuration.	0x00000000	R/W
0x0C2	EGY_TIME	Energy Accumulation Update Time Configuration.	0x000000FF	R/W
0x0C3	VSUMRMSONEOS	Offset Correction for VSUMRMS Calculation.	0x00000000	R/W
0x0C4	VSUMSWELLONE_LVL	VSUM RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x0C5	VSUMSWELLONE_CYC	VSUM RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0C6	VABRMSONEOS	Offset Correction for VP2P (AV − BV) RMSONE Calculation.	0x00000000	R/W
0x0C7	VABDIPONE_LVL	VP2P (AV − BV) RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x0C8	VABDIPONE_CYC	VP2P (AV − BV) RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0C9	VABSWELLONE_LVL	VP2P (AV − BV) RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x0CA	VABSWELLONE_CYC	VP2P (AV − BV) RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0CB	VBCRMSONEOS	Offset Correction for VP2P (BV − CV) RMSONE Calculation.	0x00000000	R/W
0x0CC	VBCDIPONE_LVL	VP2P (BV − CV) RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x0CD	VBCDIPONE_CYC	VP2P (BV − CV) RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0CE	VBCSWELLONE_LVL	VP2P (BV − CV) RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x0CF	VBCSWELLONE_CYC	VP2P (BV − CV) RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0D0	VACRMSONEOS	Offset Correction for VP2P (AV − CV) RMSONE Calculation.	0x00000000	R/W
0x0D1	VACDIPONE_LVL	VP2P (AV − CV) RMSONE Dip-Detection Threshold Level.	0x00000000	R/W
0x0D2	VACDIPONE_CYC	VP2P (AV − CV) RMSONE Dip-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0D3	VACSWELLONE_LVL	VP2P (AV − CV) RMSONE Swell-Detection Threshold Level.	0xFFFFFFFF	R/W
0x0D4	VACSWELLONE_CYC	VP2P (AV − CV) RMSONE Swell-Line Cycles Configuration.	0xFFFFFFFF	R/W
0x0D5	CF_LTMR	CF Calibration Pulse-Width Configuration Register.	0x00000000	R/W
0x0D6	WFS_CONFIG	Waveform Streaming Configuration Register.	0x0000000C	R/W
0x0D7	ADC_CONTROL	ADC Control Register.	0x00000000	R/W
0x0D8	ADC_CONFIG	ADC Configuration Register.	0x00000004	R/W
0x0D9	ADC_REDIRECT0	ADC Datapath Redirection Register 0.	0x06431D2A	R/W
0x0DA	ADC_REDIRECT1	ADC Datapath Redirection Register 1.	0x0410150B	R/W
0x0DB	CRC_OPTEN	Configuration Registers CRC Selection.	0x00000000	R/W
0x0DC	CRC_FORCE	Force Configuration Registers CRC Update.	0x00000000	R/W
0x0DD	CONFIG_LOCK	Configuration Lock Register.	0x00000000	R/W
0x200	AVRMS	Phase A Filter Based Voltage RMS.	0x00000000	R
0x201	AVRMSHALF	Phase A Voltage Channel Half-Cycle RMS.	0x00000000	R
0x202	AVRMSONE	Phase A Voltage Channel One-Cycle RMS.	0x00000000	R
0x203	AVDIPHALF	Phase A Voltage Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x204	AVDIPONE	Phase A Voltage Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x205	AVSWELLHALF	Phase A Voltage Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x206	AVSWELLONE	Phase A Voltage Maximum RMSONE for Last Detected Swell.	0x00000000	R

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x207	AIRMS	Phase A Filter Based Current RMS.	0x00000000	R
0x208	AIRMSHALF	Phase A Current Channel Half-Cycle RMS.	0x00000000	R
0x209	AIRMSONE	Phase A Current Channel One-Cycle RMS.	0x00000000	R
0x20A	AIDIPHALF	Phase A Current Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x20B	AIDIPONE	Phase A Current Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x20C	AISWELLHALF	Phase A Current Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x20D	AISWELLONE	Phase A Current Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x20E	BVRMS	Phase B Filter Based Voltage RMS.	0x00000000	R
0x20F	BVRMSHALF	Phase B Voltage Channel Half-Cycle RMS.	0x00000000	R
0x210	BVRMSONE	Phase B Voltage Channel One-Cycle RMS.	0x00000000	R
0x211	BVDIPHALF	Phase B Voltage Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x212	BVDIPONE	Phase B Voltage Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x213	BVSWELLHALF	Phase B Voltage Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x214	BVSWELLONE	Phase B Voltage Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x215	BIRMS	Phase B Filter Based Current RMS.	0x00000000	R
0x216	BIRMSHALF	Phase B Current Channel Half Cycle RMS.	0x00000000	R
0x217	BIRMSONE	Phase B Current Channel One Cycle RMS.	0x00000000	R
0x218	BIDIPHALF	Phase B Current Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x219	BIDIPONE	Phase B Current Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x21A	BISWELLHALF	Phase B Current Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x21B	BISWELLONE	Phase B Current Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x21C	CVRMS	Phase C Filter Based Voltage RMS.	0x00000000	R
0x21D	CVRMSHALF	Phase C Voltage Channel Half-Cycle RMS.	0x00000000	R
0x21E	CVRMSONE	Phase C Voltage Channel One-Cycle RMS.	0x00000000	R
0x21F	CVDIPHALF	Phase C Voltage Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x220	CVDIPONE	Phase C Voltage Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x221	CVSWELLHALF	Phase C Voltage Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x222	CVSWELLONE	Phase C Voltage Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x223	CIRMS	Phase C Filter Based Current RMS.	0x00000000	R
0x224	CIRMSHALF	Phase C Current Channel Half-Cycle RMS.	0x00000000	R
0x225	CIRMSONE	Phase C Current Channel One-Cycle RMS.	0x00000000	R
0x226	CIDIPHALF	Phase C Current Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x227	CIDIPONE	Phase C Current Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x228	CISWELLHALF	Phase C Current Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x229	CISWELLONE	Phase C Current Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x22A	AUX0RMS	Auxiliary 0 Filter Based RMS.	0x00000000	R
0x22B	AUX0RMSHALF	Auxiliary 0 Channel Half-Cycle RMS.	0x00000000	R
0x22C	AUX0RMSONE	Auxiliary 0 Channel One-Cycle RMS.	0x00000000	R
0x22D	AUX0DIPHALF	Auxiliary 0 Channel Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x22E	AUX0DIPONE	Auxiliary 0 Channel Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x22F	AUX0SWELLHALF	Auxiliary 0 Channel Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x230	AUX0SWELLONE	Auxiliary 0 Channel Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x231	AUX1RMS	Auxiliary 1 Channel Filter Based RMS.	0x00000000	R
0x232	AUX1RMSHALF	Auxiliary 1 Channel Half-Cycle RMS.	0x00000000	R
0x233	AUX1RMSONE	Auxiliary 1 Channel One-Cycle RMS.	0x00000000	R
0x234	AUX1DIPHALF	Auxiliary 1 Channel Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x235	AUX1DIPONE	Auxiliary 1 Channel Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x236	AUX1SWELLHALF	Auxiliary 1 Channel Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x237	AUX1SWELLONE	Auxiliary 1 Channel Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x238	AUX2RMS	Auxiliary 2 Channel Filter Based RMS.	0x00000000	R
0x239	AUX2RMSHALF	Auxiliary 2 Channel Half-Cycle RMS.	0x00000000	R
0x23A	AUX2RMSONE	Auxiliary 2 Channel One-Cycle RMS.	0x00000000	R
0x23B	AUX2DIPHALF	Auxiliary 2 Channel Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x23C	AUX2DIPONE	Auxiliary 2 Channel Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x23D	AUX2SWELLHALF	Auxiliary 2 Channel Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x23E	AUX2SWELLONE	Auxiliary 2 Channel Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x23F	AUX3RMS	Auxiliary 3 Channel Filter Based RMS.	0x00000000	R
0x240	AUX3RMSHALF	Auxiliary 3 Channel Half-Cycle RMS.	0x00000000	R
0x241	AUX3RMSONE	Auxiliary 3 Channel One-Cycle RMS.	0x00000000	R
0x242	AUX3DIPHALF	Auxiliary 3 Channel Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x243	AUX3DIPONE	Auxiliary 3 Channel Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x244	AUX3SWELLHALF	Auxiliary 3 Channel Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x245	AUX3SWELLONE	Auxiliary 3 Channel Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x246	AUX4RMS	Auxiliary 4 Channel Filter Based RMS.	0x00000000	R
0x247	AUX4RMSHALF	Auxiliary 4 Channel Half-Cycle RMS.	0x00000000	R
0x248	AUX4RMSONE	Auxiliary 4 Channel One-Cycle RMS.	0x00000000	R
0x249	AUX4DIPHALF	Auxiliary 4 Channel Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x24A	AUX4DIPONE	Auxiliary 4 Channel Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x24B	AUX4SWELLHALF	Auxiliary 4 Channel Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x24C	AUX4SWELLONE	Auxiliary 4 Channel Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x24D	AUX5RMS	Auxiliary 5 Channel Filter Based RMS.	0x00000000	R
0x24E	AUX5RMSHALF	Auxiliary 5 Channel Half-Cycle RMS.	0x00000000	R
0x24F	AUX5RMSONE	Auxiliary 5 Channel One-Cycle RMS.	0x00000000	R
0x250	AUX5DIPHALF	Auxiliary 5 Channel Minimum RMSHALF for Last Detected Dip.	0x007FFFFF	R
0x251	AUX5DIPONE	Auxiliary 5 Channel Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x252	AUX5SWELLHALF	Auxiliary 5 Channel Maximum RMSHALF for Last Detected Swell.	0x00000000	R
0x253	AUX5SWELLONE	Auxiliary 5 Channel Maximum RMSONE for Last Detected Swell.	0x00000000	R
0x254	AWATT	Phase A Low-pass Filtered Total Active Power.	0x00000000	R
0x255	AVA	Phase A Total Apparent Power.	0x00000000	R
0x256	APF	Phase A Power Factor.	0x00000000	R
0x257	AWATTHR_POS_LO	Phase A Accumulated Positive Total Active Energy, LSB.	0x00000000	R
0x258	AWATTHR_POS_HI	Phase A Accumulated Positive Total Active Energy, MSB.	0x00000000	R
0x259	AWATTHR_NEG_LO	Phase A Accumulated Negative Total Active Energy, LSB.	0x00000000	R
0x25A	AWATTHR_NEG_HI	Phase A Accumulated Negative Total Active Energy, MSB.	0x00000000	R
0x25B	AWATTHR_SIGNED_LO	Phase A Accumulated Signed Total Active Energy, LSB.	0x00000000	R
0x25C	AWATTHR_SIGNED_HI	Phase A Accumulated Signed Total Active Energy, MSB.	0x00000000	R
0x25D	AVAHR_LO	Phase A Accumulated Total Apparent Energy, LSB.	0x00000000	R
0x25E	AVAHR_HI	Phase A Accumulated Total Apparent Energy, MSB.	0x00000000	R
0x25F	BWATT	Phase B Low-pass Filtered Total Active Power.	0x00000000	R
0x260	BVA	Phase B Total Apparent Power.	0x00000000	R
0x261	BPF	Phase B Power Factor.	0x00000000	R
0x262	BWATTHR_POS_LO	Phase B Accumulated Positive Total Active Energy, LSB.	0x00000000	R
0x263	BWATTHR_POS_HI	Phase B Accumulated Positive Total Active Energy, MSB.	0x00000000	R
0x264	BWATTHR_NEG_LO	Phase B Accumulated Negative Total Active Energy, LSB.	0x00000000	R

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x265	BWATTHR_NEG_HI	Phase B Accumulated Negative Total Active Energy, MSB.	0x00000000	R
0x266	BWATTHR_SIGNED_LO	Phase B Accumulated Signed Total Active Energy, LSB.	0x00000000	R
0x267	BWATTHR_SIGNED_HI	Phase B Accumulated Signed Total Active Energy, MSB.	0x00000000	R
0x268	BVAHR_LO	Phase B Accumulated Total Apparent Energy, LSB.	0x00000000	R
0x269	BVAHR_HI	Phase B Accumulated Total Apparent Energy, MSB.	0x00000000	R
0x26A	CWATT	Phase C Low-pass Filtered Total Active Power.	0x00000000	R
0x26B	CVA	Phase C Total Apparent Power.	0x00000000	R
0x26C	CPF	Phase C Power Factor.	0x00000000	R
0x26D	CWATTHR_POS_LO	Phase C Accumulated Positive Total Active Energy, LSB.	0x00000000	R
0x26E	CWATTHR_POS_HI	Phase C Accumulated Positive Total Active Energy, MSB.	0x00000000	R
0x26F	CWATTHR_NEG_LO	Phase C Accumulated Negative Total Active Energy, LSB.	0x00000000	R
0x270	CWATTHR_NEG_HI	Phase C Accumulated Negative Total Active Energy, MSB.	0x00000000	R
0x271	CWATTHR_SIGNED_LO	Phase C Accumulated Signed Total Active Energy, LSB.	0x00000000	R
0x272	CWATTHR_SIGNED_HI	Phase C Accumulated Signed Total Active Energy, MSB.	0x00000000	R
0x273	CVAHR_LO	Phase C Accumulated Total Apparent Energy, LSB.	0x00000000	R
0x274	CVAHR_HI	Phase C Accumulated Total Apparent Energy, MSB.	0x00000000	R
0x275	ANGL_AV_BV	Phase A Voltage to Phase B Voltage Angle Register.	0x00000000	R
0x276	ANGL_BV_CV	Phase B Voltage to Phase C Voltage Angle Register.	0x00000000	R
0x277	ANGL_AV_CV	Phase A Voltage to Phase C Voltage Angle Register.	0x00000000	R
0x278	ANGL_AV_AI	Phase A Voltage to Current Angle Register.	0x00000000	R
0x279	ANGL_BV_BI	Phase B Voltage to Current Angle Register.	0x00000000	R
0x27A	ANGL_CV_CI	Phase C Voltage to Current Angle Register.	0x00000000	R
0x27B	ANGL_AI_BI	Phase A Current to Phase B Current Angle Register.	0x00000000	R
0x27C	ANGL_BI_CI	Phase B Current to Phase C Current Angle Register.	0x00000000	R
0x27D	ANGL_AI_CI	Phase A Current to Phase C Current Angle Register.	0x00000000	R
0x27E	ISUMRMS	Filter Based RMS Based on the Sum of Current Channels.	0x00000000	R
0x280	PEN_PERIOD	Period Value Used for PEN Channels RMSONE Calculation.	0x00500000	R
0x281	APERIOD	Line Period on Phase A Voltage.	0x00500000	R
0x282	BPERIOD	Line Period on Phase B Voltage.	0x00500000	R
0x283	CPERIOD	Line Period on Phase C Voltage.	0x00500000	R
0x284	COM_PERIOD	Line Period on Combined Phase A, B, and C Voltages.	0x00500000	R
0x285	IPEAK	Current Peak Register.	0x00000000	R
0x286	VPEAK	Voltage Peak Register.	0x00000000	R
0x287	AUXPEAK	Auxiliary-Channels Peak Register.	0x00000000	R
0x288	PHSIGN	Power Sign Register.	0x00000000	R
0x289	PHNOLOAD	Phase No Load Register.	0x00000000	R
0x28A	VSUMRMSONE	One-Cycle RMS for PEN Fault.	0x00000000	R
0x28B	VSUMSWELLONE	Maximum VSUMRMSONE for Last Detected Swell.	0x007FFFFF	R
0x28C	VABRMSONE	VP2P (AV − BV) One-Cycle RMS.	0x00000000	R
0x28D	VABDIPONE	VP2P (AV − BV) Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x28E	VABSWELLONE	VP2P (AV − BV) Maximum RMSONE for Last Detected Swell.	0x007FFFFF	R
0x28F	VBCRMSONE	VP2P (BV − CV) One-Cycle RMS.	0x00000000	R
0x290	VBCDIPONE	VP2P (BV − CV) Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x291	VBCSWELLONE	VP2P (BV − CV) Maximum RMSONE for Last Detected Swell.	0x007FFFFF	R
0x292	VACRMSONE	VP2P (AV − CV) One-Cycle RMS.	0x00000000	R
0x293	VACDIPONE	VP2P (AV − CV) Minimum RMSONE for Last Detected Dip.	0x007FFFFF	R
0x294	VACSWELLONE	VP2P (AV − CV) Maximum RMSONE for Last Detected Swell.	0x007FFFFF	R

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x295	CRC_RSLT	Configuration Registers CRC Value.	0x00000000	R
0x400	STATUS0	Status Register 0.	0x00000000	R/W
0x401	STATUS1	Status Register 1.	0x00000000	R/W
0x402	STATUS2	Status Register 2.	0x00000000	R/W
0x403	STATUS3	Status Register 3.	0x00000000	R/W
0x404	ERROR_STATUS	Firmware Status Register.	0x00000000	R/W
0x405	MASK0	Interrupt Enable Register 0.	0x00004000	R/W
0x406	MASK1	Interrupt Enable Register 1.	0x00004000	R/W
0x407	MASK2	Interrupt Enable Register 2.	0x00000000	R/W
0x408	MASK3	Interrupt Enable Register 3.	0x00000000	R/W
0x409	ERROR_MASK	Firmware Status Interrupt Enable Register.	0x007FFFFF	R/W
0x40A	VERSION	Version of ADE9178 IC.	0x01000000	R
0x40B	VERSION2	Metrology Algorithm Version.	0x09FD5D0D	R
0x600	AVRMS_1	SPI Burst Read Access by Function. See AVRMS.	0x00000000	R
0x601	BVRMS_1	SPI Burst Read Access by Function. See BVRMS.	0x00000000	R
0x602	CVRMS_1	SPI Burst Read Access by Function. See CVRMS.	0x00000000	R
0x603	AIRMS_1	SPI Burst Read Access by Function. See AIRMS.	0x00000000	R
0x604	BIRMS_1	SPI Burst Read Access by Function. See BIRMS.	0x00000000	R
0x605	CIRMS_1	SPI Burst Read Access by Function. See CIRMS.	0x00000000	R
0x606	AUX0RMS_1	SPI Burst Read Access by Function. See AUX0RMS.	0x00000000	R
0x607	AUX1RMS_1	SPI Burst Read Access by Function. See AUX1RMS.	0x00000000	R
0x608	AUX2RMS_1	SPI Burst Read Access by Function. See AUX2RMS.	0x00000000	R
0x609	AUX3RMS_1	SPI Burst Read Access by Function. See AUX3RMS.	0x00000000	R
0x60A	AUX4RMS_1	SPI Burst Read Access by Function. See AUX4RMS.	0x00000000	R
0x60B	AUX5RMS_1	SPI Burst Read Access by Function. See AUX5RMS.	0x00000000	R
0x60C	AWATT_1	SPI Burst Read Access by Function. See AWATT.	0x00000000	R
0x60D	BWATT_1	SPI Burst Read Access by Function. See BWATT.	0x00000000	R
0x60E	CWATT_1	SPI Burst Read Access by Function. See CWATT.	0x00000000	R
0x60F	AVA_1	SPI Burst Read Access by Function. See AVA.	0x00000000	R
0x610	BVA_1	SPI Burst Read Access by Function. See BVA.	0x00000000	R
0x611	CVA_1	SPI Burst Read Access by Function. See CVA.	0x00000000	R
0x612	APF_1	SPI Burst Read Access by Function. See APF.	0x00000000	R
0x613	BPF_1	SPI Burst Read Access by Function. See BPF.	0x00000000	R
0x614	CPF_1	SPI Burst Read Access by Function. See CPF.	0x00000000	R
0x615	AVRMSONE_1	SPI Burst Read Access by Function. See AVRMSONE.	0x00000000	R
0x616	BVRMSONE_1	SPI Burst Read Access by Function. See BVRMSONE.	0x00000000	R
0x617	CVRMSONE_1	SPI Burst Read Access by Function. See CVRMSONE.	0x00000000	R
0x618	AIRMSONE_1	SPI Burst Read Access by Function. See AIRMSONE.	0x00000000	R
0x619	BIRMSONE_1	SPI Burst Read Access by Function. See BIRMSONE.	0x00000000	R
0x61A	CIRMSONE_1	SPI Burst Read Access by Function. See CIRMSONE.	0x00000000	R
0x61B	AUX0RMSONE_1	SPI Burst Read Access by Function. See AUX0RMSONE.	0x00000000	R
0x61C	AUX1RMSONE_1	SPI Burst Read Access by Function. See AUX1RMSONE.	0x00000000	R
0x61D	AUX2RMSONE_1	SPI Burst Read Access by Function. See AUX2RMSONE.	0x00000000	R
0x61E	AUX3RMSONE_1	SPI Burst Read Access by Function. See AUX3RMSONE.	0x00000000	R
0x61F	AUX4RMSONE_1	SPI Burst Read Access by Function. See AUX4RMSONE.	0x00000000	R
0x620	AUX5RMSONE_1	SPI Burst Read Access by Function. See AUX5RMSONE.	0x00000000	R
0x621	VSUMRMSONE_1	SPI Burst Read Access by Function. See VSUMRMSONE.	0x00000000	R

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x622	VABRMSONE_1	SPI Burst Read Access by Function. See VABRMSONE.	0x00000000	R
0x623	VBCRMSONE_1	SPI Burst Read Access by Function. See VBCRMSONE.	0x00000000	R
0x624	VACRMSONE_1	SPI Burst Read Access by Function. See VACRMSONE.	0x00000000	R
0x625	AVRMSHALF_1	SPI Burst Read Access by Function. See AVRMSHALF.	0x00000000	R
0x626	BVRMSHALF_1	SPI Burst Read Access by Function. See BVRMSHALF.	0x00000000	R
0x627	CVRMSHALF_1	SPI Burst Read Access by Function. See CVRMSHALF.	0x00000000	R
0x628	AIRMSHALF_1	SPI Burst Read Access by Function. See AIRMSHALF.	0x00000000	R
0x629	BIRMSHALF_1	SPI Burst Read Access by Function. See BIRMSHALF.	0x00000000	R
0x62A	CIRMSHALF_1	SPI Burst Read Access by Function. See CIRMSHALF.	0x00000000	R
0x62B	AUX0RMSHALF_1	SPI Burst Read Access by Function. See AUX0RMSHALF.	0x00000000	R
0x62C	AUX1RMSHALF_1	SPI Burst Read Access by Function. See AUX1RMSHALF.	0x00000000	R
0x62D	AUX2RMSHALF_1	SPI Burst Read Access by Function. See AUX2RMSHALF.	0x00000000	R
0x62E	AUX3RMSHALF_1	SPI Burst Read Access by Function. See AUX3RMSHALF.	0x00000000	R
0x62F	AUX4RMSHALF_1	SPI Burst Read Access by Function. See AUX4RMSHALF.	0x00000000	R
0x630	AUX5RMSHALF_1	SPI Burst Read Access by Function. See AUX5RMSHALF.	0x00000000	R
0x631	AVRMS_2	SPI Burst Read Access by Phase. See AVRMS.	0x00000000	R
0x632	AIRMS_2	SPI Burst Read Access by Phase. See AIRMS.	0x00000000	R
0x633	AWATT_2	SPI Burst Read Access by Phase. See AWATT.	0x00000000	R
0x634	AVA_2	SPI Burst Read Access by Phase. See AVA.	0x00000000	R
0x635	APF_2	SPI Burst Read Access by Phase. See APF.	0x00000000	R
0x636	AVRMSONE_2	SPI Burst Read Access by Phase. See AVRMSONE.	0x00000000	R
0x637	AIRMSONE_2	SPI Burst Read Access by Phase. See AIRMSONE.	0x00000000	R
0x638	AVRMSHALF_2	SPI Burst Read Access by Phase. See AVRMSHALF.	0x00000000	R
0x639	AIRMSHALF_2	SPI Burst Read Access by Phase. See AIRMSHALF.	0x00000000	R
0x63A	BVRMS_2	SPI Burst Read Access by Phase. See BVRMS.	0x00000000	R
0x63B	BIRMS_2	SPI Burst Read Access by Phase. See BIRMS.	0x00000000	R
0x63C	BWATT_2	SPI Burst Read Access by Phase. See BWATT.	0x00000000	R
0x63D	BVA_2	SPI Burst Read Access by Phase. See BVA.	0x00000000	R
0x63E	BPF_2	SPI Burst Read Access by Phase. See BPF.	0x00000000	R
0x63F	BVRMSONE_2	SPI Burst Read Access by Phase. See BVRMSONE.	0x00000000	R
0x640	BIRMSONE_2	SPI Burst Read Access by Phase. See BIRMSONE.	0x00000000	R
0x641	BVRMSHALF_2	SPI Burst Read Access by Phase. See BVRMSHALF.	0x00000000	R
0x642	BIRMSHALF_2	SPI Burst Read Access by Phase. See BIRMSHALF.	0x00000000	R
0x643	CVRMS_2	SPI Burst Read Access by Phase. See CVRMS.	0x00000000	R
0x644	CIRMS_2	SPI Burst Read Access by Phase. See CIRMS.	0x00000000	R
0x645	CWATT_2	SPI Burst Read Access by Phase. See CWATT.	0x00000000	R
0x646	CVA_2	SPI Burst Read Access by Phase. See CVA.	0x00000000	R
0x647	CPF_2	SPI Burst Read Access by Phase. See CPF.	0x00000000	R
0x648	CVRMSONE_2	SPI Burst Read Access by Phase. See CVRMSONE.	0x00000000	R
0x649	CIRMSONE_2	SPI Burst Read Access by Phase. See CIRMSONE.	0x00000000	R
0x64A	CVRMSHALF_2	SPI Burst Read Access by Phase. See CVRMSHALF.	0x00000000	R
0x64B	CIRMSHALF_2	SPI Burst Read Access by Phase. See CIRMSHALF.	0x00000000	R
0x64C	AUX0RMS_2	SPI Burst Read Access by Phase. See AUX0RMS.	0x00000000	R
0x64D	AUX0RMSONE_2	SPI Burst Read Access by Phase. See AUX0RMSONE.	0x00000000	R
0x64E	AUX0RMSHALF_2	SPI Burst Read Access by Phase. See AUX0RMSHALF.	0x00000000	R
0x64F	AUX1RMS_2	SPI Burst Read Access by Phase. See AUX1RMS.	0x00000000	R
0x650	AUX1RMSONE_2	SPI Burst Read Access by Phase. See AUX1RMSONE.	0x00000000	R

REGISTER SUMMARY: ADE9178

Table 33. ADE9178 Register Summary (Continued)

Address	Name	Description	Reset	Access
0x651	AUX1RMSHALF_2	SPI Burst Read Access by Phase. See AUX1RMSHALF.	0x00000000	R
0x652	AUX2RMS_2	SPI Burst Read Access by Phase. See AUX2RMS.	0x00000000	R
0x653	AUX2RMSONE_2	SPI Burst Read Access by Phase. See AUX2RMSONE.	0x00000000	R
0x654	AUX2RMSHALF_2	SPI Burst Read Access by Phase. See AUX2RMSHALF.	0x00000000	R
0x655	AUX3RMS_2	SPI Burst Read Access by Phase. See AUX3RMS.	0x00000000	R
0x656	AUX3RMSONE_2	SPI Burst Read Access by Phase. See AUX3RMSONE.	0x00000000	R
0x657	AUX3RMSHALF_2	SPI Burst Read Access by Phase. See AUX3RMSHALF.	0x00000000	R
0x658	AUX4RMS_2	SPI Burst Read Access by Phase. See AUX4RMS.	0x00000000	R
0x659	AUX4RMSONE_2	SPI Burst Read Access by Phase. See AUX4RMSONE.	0x00000000	R
0x65A	AUX4RMSHALF_2	SPI Burst Read Access by Phase. See AUX4RMSHALF.	0x00000000	R
0x65B	AUX5RMS_2	SPI Burst Read Access by Phase. See AUX5RMS.	0x00000000	R
0x65C	AUX5RMSONE_2	SPI Burst Read Access by Phase. See AUX5RMSONE.	0x00000000	R
0x65D	AUX5RMSHALF_2	SPI Burst Read Access by Phase. See AUX5RMSHALF.	0x00000000	R
0x65E	VSUMRMSONE_2	SPI Burst Read Access by Function. See VSUMRMSONE.	0x00000000	R
0x65F	VABRMSONE_2	SPI Burst Read Access by Function. See VABRMSONE.	0x00000000	R
0x660	VBCRMSONE_2	SPI Burst Read Access by Function. See VBCRMSONE.	0x00000000	R
0x661	VACRMSONE_2	SPI Burst Read Access by Function. See VACRMSONE.	0x00000000	R

REGISTER DETAILS: ADE9178

Table 34 shows the registers of the ADE9178 that have bitfields. Additional registers listed in Table 33 table do not have bit fields.

Table 34. ADE9178 Register Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0AE	CONFIG0	[31:30]	RESERVED		Reserved.	0x0	R
		29	CRC_DIS		Disable CRC Check. Set this bit to disable CRC check on Host SPI command.	0x0	R/W
		28	ICONSEL		Phase B Current Calculation Selection. Set this bit to calculate the current flowing through BI from the AI and CI measurements. If this bit is set, BI = −AI − CI.	0x0	R/W
		[27:25]	VCONSEL		3-Wire and 4-Wire Hardware Configuration Selection.	0x0	R/W
				000	4-Wire Wye.		
				001	3-Wire Delta. BV' = AV − CV.		
				010	4-Wire Wye, Non-Blondel Compliant. BV' = −AV − CV.		
				011	4-Wire Wye, Non-Blondel Compliant. BV' = −AV.		
				100	3-Wire Delta. AV' = AV − BV; BV' = AV − CV; CV' = CV − BV.		
		[24:22]	ISUM_AUXSEL		Neutral Channel Selection Configuration for ISUM.	0x0	R/W
				000	Auxiliary 0 Channel Used in ISUM Calculation.		
				001	Auxiliary 1 Channel Used in ISUM Calculation.		
				010	Auxiliary 2 Channel Used in ISUM Calculation.		
				011	Auxiliary 3 Channel Used in ISUM Calculation.		
				100	Auxiliary 4 Channel Used in ISUM Calculation.		
				101	Auxiliary 5 Channel Used in ISUM Calculation.		
		[21:20]	ISUM_CFG		ISUM Calculation Configuration.	0x0	R/W
				00	ISUM = AI_PCF + BI_PCF + CI_PCF. For approximated neutral current RMS calculation.		
				01	ISUM = AI_PCF + BI_PCF + CI_PCF + AUXx_PCF. To determine mismatch between neutral and phase currents.		
				10	ISUM = AI_PCF + BI_PCF + CI_PCF − AUXx_PCF. To determine mismatch between neutral and phase currents.		
		19	DIP_SWELL_ONE_IRQ_MODE		Dip and Swell One-Cycle Interrupt Mode Selection.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0	Continuous Interrupts. Get continuous interrupts after every DIP_CYC/SWELL_CYC cycles.		
				1	Enter and Exit Interrupts. Get one interrupt when entering DIP/SWELL mode and another interrupt when exiting DIP/SWELL mode.		
		18	DIP_SWELL_HALF_IRQ_MODE		Dip and Swell Half-Cycle Interrupt Mode Selection.	0x0	R/W
				0	Continuous Interrupts. Get continuous interrupts after every DIP_CYC/SWELL_CYC cycles.		
				1	Enter and Exit Interrupts. Get one interrupt when entering DIP/SWELL mode and another interrupt when exiting DIP/SWELL mode.		
		[17:16]	PWR_SETTLE		Power Settling Time Selection. These bits configure the time for the power measurements to settle before starting the energy and CF accumulations.	0x0	R/W
				00	Settle for 64 ms.		
				01	Settle for 128 ms.		
				10	Settle for 256 ms.		
				11	Settle for 0 ms.		
		15	VNOMC_EN		Nominal Phase Voltage RMS for Phase C Total Apparent Power. Set this bit to use the nominal phase voltage RMS, VNOM, in the computation of Phase C total apparent power, CVA.	0x0	R/W
		14	VNOMB_EN		Nominal Phase Voltage RMS for Phase B Total Apparent Power. Set this bit to use the nominal phase voltage RMS, VNOM, in the computation of Phase B total apparent power, BVA.	0x0	R/W
		13	VNOMA_EN		Nominal Phase Voltage RMS for Phase A Total Apparent Power. Set this bit to use the nominal phase voltage RMS, VNOM, in the computation of Phase A total apparent power, AVA.	0x0	R/W
		12	ZX_SRC_SEL		Zero-Crossing Source Select. This bit selects whether data going into the zero-crossing detection circuit comes before the HPF or after the PCF.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0	ZX After PCF.		
				1	ZX Before HPF.		
		11	RMSONE_SRC_SEL		RMSONE Sample Source Select. Selects samples to be used for the one-cycle RMS calculation.	0x1	R/W
				0	Samples After HPF Used for RMSONE.		
				1	Samples Before HPF Used for RMSONE.		
		10	RMSHALF_SRC_SEL		Fast RMSHALF Sample Source Select. Selects samples to be used for the half-cycle RMS calculation.	0x1	R/W
				0	Samples After HPF Used for RMSHALF.		
				1	Samples Before HPF Used for RMSHALF.		
		9	DISAPLPF		LPF Active Power Disable. Set this bit to disable the LPF in the total active power datapath.	0x0	R/W
		[8:6]	HPF_CRN		HPF Corner Selection. HPF corner (f3dB) enabled when the HPFDIS bit in the CONFIG0 register is equal to zero.	0x6	R/W
				000	38.695 Hz.		
				001	19.6375 Hz.		
				010	9.895 Hz.		
				011	4.9675 Hz.		
				100	2.49 Hz.		
				101	1.2475 Hz.		
				110	0.625 Hz.		
				111	0.3125 Hz.		
		5	HPFDIS		HPF Disable. Set this bit to disable HPF for all channels.	0x0	R/W
		[4:3]	PERIOD_AVG_CFG		Period Averaging Configuration. Further averaging to reduce period jitter.	0x0	R/W
				00	No Additional Averaging.		
				01	Average by 8.		
				10	Average by 16.		
				11	Average by 32.		
		2	UPERIOD_SEL		User-Line Period Enable. Set this bit to use a user-configured line period, in USER_PERIOD, for RMSONE measurements of all channels. If this bit is clear, the phase voltage line period selected by the LP_SEL[1:0] bits in the ZX_LP_SEL register is used.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	SELFREQ		Line-Cycle Frequency Selection. Use this bit to configure the IC for a 50 Hz or 60 Hz system. This setting is used to define the coerced value in period registers (APERIOD, BPERIOD, CPERIOD, COM_PERIOD) when input is outside the 40 Hz to 70 Hz range. It affects line period and one-cycle RMS measurements.	0x0	R/W
				0	50 Hz.		
				1	60 Hz.		
		0	SWRST		Reserved.	0x0	R/W
0x0AF	PEAK_CONFIG	[31:12]	RESERVED		Reserved.	0x0	R
		[11:6]	AUXPEAKSEL		Peak Detection Phase Selection for Auxiliary Channels. Set bits to select which auxiliary phase(s) are monitored for peak detection. Set PEAKSEL[0] to enable AUX0, PEAKSEL[1] to enable AUX1, PEAKSEL[2] to enable AUX2, and so on.	0x0	R/W
		[5:3]	IPEAKSEL		Peak Detection Phase Selection for Current Channels. Set bits to select which current phase(s) are monitored for peak detection. Set PEAKSEL[0] to enable phase A , PEAKSEL[1] to enable phase B, and PEAKSEL[2] to enable phase C for peak detection.	0x0	R/W
		[2:0]	VPEAKSEL		Peak Detection Phase Selection for Voltage Channels. Set bits to select which voltages phase(s) are monitored for peak detection. Set PEAKSEL[0] to enable phase A , PEAKSEL[1] to enable phase B, and PEAKSEL[2] to enable phase C for peak detection.	0x0	R/W
0x0B0	PEN_CONFIG	[31:14]	RESERVED		Reserved.	0x0	R
		[13:12]	PEN_LP_SEL		Line Period Measurement Selection for PEN Channels. Affects RMSONE measurement for PEN channels.	0x3	R/W
				00	Line Period Measurement from PEN Channel A. Line period measurement from PEN_A voltage channel.		

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				01	Line Period Measurement from PEN Channel B. Line period measurement from PEN_B voltage channel.		
				10	Line Period Measurement from PEN Channel C. Line period measurement from PEN_C voltage channel.		
				11	Line Period Measurement from Combined PEN Channels. Line period measurement on combined PEN channels: (PEN_AV + PEN_BV − PEN_CV)/2.		
		[11:8]	PEN_CHANSELC		Channel C Selection for PEN Fault Detection.	0x4	R/W
				0000	AV Data Processing Path.		
				0001	AI Data Processing Path.		
				0010	BV Data Processing Path.		
				0011	BI Data Processing Path.		
				0100	CV Data Processing Path.		
				0101	CI Data Processing Path.		
				0110	AUX0 Data Processing Path.		
				0111	AUX1 Data Processing Path.		
				1000	AUX2 Data Processing Path.		
				1001	AUX3 Data Processing Path.		
				1010	AUX4 Data Processing Path.		
				1011	AUX5 Data Processing Path.		
		[7:4]	PEN_CHANSELB		Channel B Selection for PEN Fault Detection.	0x2	R/W
				0000	AV Data Processing Path.		
				0001	AI Data Processing Path.		
				0010	BV Data Processing Path.		
				0011	BI Data Processing Path.		
				0100	CV Data Processing Path.		
				0101	CI Data Processing Path.		
				0110	AUX0 Data Processing Path.		
				0111	AUX1 Data Processing Path.		
				1000	AUX2 Data Processing Path.		
				1001	AUX3 Data Processing Path.		
				1010	AUX4 Data Processing Path.		
				1011	AUX5 Data Processing Path.		
		[3:0]	PEN_CHANSELA		Channel A Selection for PEN Fault Detection.	0x0	R/W
				0000	AV Data Processing Path.		
				0001	AI Data Processing Path.		
				0010	BV Data Processing Path.		
				0011	BI Data Processing Path.		
				0100	CV Data Processing Path.		
				0101	CI Data Processing Path.		
				0110	AUX0 Data Processing Path.		

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0111	AUX1 Data Processing Path.		
				1000	AUX2 Data Processing Path.		
				1001	AUX3 Data Processing Path.		
				1010	AUX4 Data Processing Path.		
				1011	AUX5 Data Processing Path.		
0x0B1	CF1_CONFIG	[31:11]	RESERVED		Reserved.	0x0	R
		10	ACC_CLEAR		Clear CF1 Accumulator. Set this bit to clear the accumulation in the digital to frequency converter. Note that this bit automatically clears itself.	0x0	R/W
		9	WIDTHSEL		CF1 Pulse Width Select. If this bit is set, the CF1 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active-low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		[8:7]	ACCMODE		CF1 Accumulation Mode Configuration.	0x0	R/W
				00	Signed Accumulation Mode.		
				10	Positive Accumulation Mode.		
				11	Negative Accumulation Mode.		
		[6:4]	PHASESEL		Phases to Include in CF1 Pulse Output. PHASESEL[0] set to 1 to include phase A in the CF1 outputs calculations. PHASESEL[1] set to 1 to include phase B in the CF1 outputs calculations. PHASESEL[2] set to 1 to include phase C in the CF1 outputs calculations.	0x0	R/W
		[3:1]	PWRSEL		CF1 Energy Output Type. Type of energy output on the CF1 pin. Configure PHASESEL1 in the CF1_CONFIG register to select which phases are included.	0x0	R/W
				000	Total Active Power.		
				001	Total Apparent Power.		
		0	CFDIS		CF1 Output Disable. Set this bit to disable the CF1 output and bring the pin high. Note that when this bit is set, the CF1 bit in STATUS0 is not set when a CF pulse is accumulated in the digital to frequency converter.	0x1	R/W
0x0B2	CF2_CONFIG	[31:11]	RESERVED		Reserved.	0x0	R
		10	ACC_CLEAR		Clear CF2 Accumulator. Set this bit to clear the accumulation in the digital to	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					frequency converter. Note that this bit automatically clears itself.		
		9	WIDTHSEL		CF2 Pulse Width Select. If this bit is set, the CF2 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active-low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		[8:7]	ACCMODE		CF2 Accumulation Mode Configuration.	0x0	R/W
				00	Signed Accumulation Mode.		
				10	Positive Accumulation Mode.		
				11	Negative Accumulation Mode.		
		[6:4]	PHASESEL		Phases to Include in CF2 Pulse Output. PHASESEL[0] set to 1 to include phase A in the CF2 outputs calculations. PHASESEL[1] set to 1 to include phase B in the CF2 outputs calculations. PHASESEL[2] set to 1 to include phase C in the CF2 outputs calculations.	0x0	R/W
		[3:1]	PWRSEL		CF2 Energy Output Type. Type of energy output on the CF2 pin. Configure PHASESEL2 in the CF2_CONFIG register to select which phases are included.	0x0	R/W
				000	Total Active Power.		
				001	Total Apparent Power.		
		0	CFDIS		CF2 Output Disable. Set this bit to disable the CF2 output and bring the pin high. Note that when this bit is set, the CF2 bit in STATUS0 is not set when a CF pulse is accumulated in the digital to frequency converter.	0x1	R/W
0x0B7	RMSHALF_CONFIG	[31:12]	RESERVED		Reserved.	0x0	R
		11	AUX5_RMSHALF_MODE_SEL		AUX5RMSHALF Mode Selection. Set this bit to calculate AUX5RMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of AUX5 channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value.		

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					Synchronize RMSHALF calculation with user-defined half period value.		
		10	AUX4_RMSHALF_MODE_SEL		AUX4RMSHALF Mode Selection. Set this bit to calculate AUX4RMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of AUX4 channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		9	AUX3_RMSHALF_MODE_SEL		AUX3RMSHALF Mode Selection. Set this bit to calculate AUX3RMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of AUX3 channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		8	AUX2_RMSHALF_MODE_SEL		AUX2RMSHALF Mode Selection. Set this bit to calculate AUX2RMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of AUX2 channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		7	AUX1_RMSHALF_MODE_SEL		AUX1RMSHALF Mode Selection. Set this bit to calculate AUX1RMSHALF based on	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					USER_PERIOD_HALF or else synchronize with zero crossings of AUX1 channel.		
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		6	AUX0_RMSHALF_MODE_SEL		AUX0RMSHALF Mode Selection. Set this bit to calculate AUX0RMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of AUX0 channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		5	CI_RMSHALF_MODE_SEL		CIRMSHALF Mode Selection. Set this bit to calculate CIRMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of CI channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		4	CV_RMSHALF_MODE_SEL		CVRMSHALF Mode Selection. Set this bit to calculate CVRMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of CV channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value.		

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					Synchronize RMSHALF calculation with user-defined half period value.		
		3	BI_RMSHALF_MODE_SEL		BIRMSHALF Mode Selection. Set this bit to calculate BIRMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of BI channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		2	BV_RMSHALF_MODE_SEL		BVRMSHALF Mode Selection. Set this bit to calculate BVRMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of BV channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		1	AI_RMSHALF_MODE_SEL		AIRMSHALF Mode Selection. Set this bit to calculate AIRMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of AI channel.	0x0	R/W
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
		0	AV_RMSHALF_MODE_SEL		AVRMSHALF Mode Selection. Set this bit to calculate AVRMSHALF based on USER_PERIOD_HALF or else synchronize with zero crossings of AV channel.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0	Synchronized with Zero Crossing. Synchronize RMSHALF calculation with zero crossings of the channel.		
				1	Synchronized with User-Defined Half Period Value. Synchronize RMSHALF calculation with user-defined half period value.		
0x0BD	ZX_LP_SEL	[31:4]	RESERVED		Reserved.	0x0	R
		[3:2]	LP_SEL		Line Period Measurement Selection. Selects line period measurement used for xRMSONE measurement.	0x3	R/W
				00	Phase A Voltage Channel Period. APERIOD, line period measurement from phase A voltage.		
				01	Phase B Voltage Channel Period. BPERIOD, line period measurement from phase B voltage.		
				10	Phase C Voltage Channel Period. CPERIOD, line period measurement from phase C voltage.		
				11	Combined Voltage Channel Period. COMB_PERIOD, line period measurement on combined voltage signal: (AV + BV − CV)/2.		
		[1:0]	ZX_SEL		Zero-Crossing Signal Selection. Selects channel zero crossings used in line cycle energy accumulation mode.	0x3	R/W
				00	Phase A Voltage Channel Zero Crossings. ZXAV, phase A voltage zero-crossing signal.		
				01	Phase B Voltage Channel Zero Crossings. ZXBV, phase B voltage zero-crossing signal.		
				10	Phase C Voltage Channel Zero Crossings. ZXAC, phase C voltage zero-crossing signal.		
				11	Combined Voltage Channel Zero Crossings. ZXCOMB, zero crossing on combined voltage signal: (AV + BV − CV)/2.		
0x0C1	EP_CFG	[31:7]	RESERVED		Reserved.	0x0	R
		[6:4]	NOLOAD_TMR		No Load Condition Evaluation Window. This register configures how many 4 ksps samples are used to evaluate the no load condition.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				000	Evaluation Over 64 Samples.		
				001	Evaluation Over 128 Samples.		
				010	Evaluation Over 256 Samples.		
				011	Evaluation Over 512 Samples.		
				100	Evaluation Over 1024 Samples.		
				101	Evaluation Over 2048 Samples.		
				110	Evaluation Over 4096 Samples.		
				111	Disable No Load Threshold.		
		3	RD_RST_EN		Energy Register Reset on Read Enable. Set this bit to enable the energy register read with reset feature. If this bit is set, when one of the energy accumulation registers is read, it is reset and begins accumulating energy from zero.	0x0	R/W
		2	EGY_LD_ACCUM		Energy Register Update Mode. If this bit is equal to zero, the internal energy register is added to the user-accessible energy register. If the bit is set, the internal energy register overwrites the user-accessible energy register when the EGYRDY event occurs.	0x0	R/W
		1	EGY_TMR_MODE		Energy Accumulation Mode. This bit determines whether energy is accumulated based on time (in ms) or zero-crossing events configured in the EGY_TIME register.	0x0	R/W
				0	Time Based Accumulation. Accumulate energy for fixed time duration (in ms).		
				1	Zero-Crossing Based Accumulation. Accumulate energy based on the zero crossing selected by the ZX_SEL bits in the ZX_LP_SEL register. Note, it is not recommended to use line-cycle accumulation mode. For more details, see Silicon Anomaly section.		
		0	EGY_PWR_EN		Energy Accumulators Enable. Set this bit to enable the energy accumulator, when the run bit is also set.	0x0	R/W
0x0D6	WFS_CONFIG	[31:19]	RESERVED		Reserved.	0x0	R
		18	AUX5_WFS_EN		Set to Enable Auxiliary 5 Channel Waveform Streaming.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		17	AUX4_WFS_EN		Set to Enable Auxiliary 4 Channel Waveform Streaming.	0x0	R/W
		16	AUX3_WFS_EN		Set to Enable Auxiliary 3 Channel Waveform Streaming.	0x0	R/W
		15	AUX2_WFS_EN		Set to Enable Auxiliary 2 Channel Waveform Streaming.	0x0	R/W
		14	AUX1_WFS_EN		Set to Enable Auxiliary 1 Channel Waveform Streaming.	0x0	R/W
		13	AUX0_WFS_EN		Set to Enable Auxiliary 0 Channel Waveform Streaming.	0x0	R/W
		12	CI_WFS_EN		Set to Enable Phase C Current Waveform Streaming.	0x0	R/W
		11	CV_WFS_EN		Set to Enable Phase C Voltage Waveform Streaming.	0x0	R/W
		10	BI_WFS_EN		Set to Enable Phase B Current Waveform Streaming.	0x0	R/W
		9	BV_WFS_EN		Set to Enable Phase B Voltage Waveform Streaming.	0x0	R/W
		8	AI_WFS_EN		Set to Enable Phase A Current Waveform Streaming.	0x0	R/W
		7	AV_WFS_EN		Set to Enable Phase A Voltage Waveform Streaming.	0x0	R/W
		[6:5]	WF_SRC		Waveform Samples to Send.	0x0	R/W
				00	ADC Samples.		
				01	PCF Output.		
		[4:1]	BAUD_RATE		Baud Rate for Waveform Streaming.	0x6	R/W
				000	256000 Bits/s.		
				001	512000 Bits/s.		
				010	1024000 Bits/s.		
				011	1536000 Bits/s.		
				100	2048000 Bits/s.		
				101	3072000 Bits/s.		
		0	WFS_EN		Enable Waveform Streaming.	0x0	R/W
0x0D7	ADC_CONTROL	[31:3]	RESERVED		Reserved.	0x0	R
		2	ADC_SYNC		Set This Bit to Synchronize the ADCs.	0x0	R/W
		1	ADC_INIT		Set This Bit to Initialize the ADCs. Note that this bit is self-clearing.	0x0	R/W
		0	ADC_RUN		Set This Bit to Start the Measurements.	0x0	R/W
0x0D8	ADC_CONFIG	[31:3]	RESERVED		Reserved.	0x0	R
		[2:0]	NUM_ADC		Number of ADCs Daisy-chained in the System. Set the number of ADCs that are daisy-chained in the system.	0x4	R/W
0x0D9	ADC_REDIRECT0	[31:30]	RESERVED		Reserved.	0x0	R
		[29:25]	CI		ADC CI Channel Data Multiplexing. Selects slot to connect CI channel input.	0x3	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[24:20]	CV		ADC CV Channel Data Multiplexing. Selects slot to connect CV channel input.	0x4	R/W
		[19:15]	BI		ADC BI Channel Data Multiplexing. Selects slot to connect BI channel input.	0x6	R/W
		[14:10]	BV		ADC BV Channel Data Multiplexing. Selects slot to connect BV channel input.	0x7	R/W
		[9:5]	AI		ADC AI Channel Data Multiplexing. Selects slot to connect AI channel input.	0x9	R/W
		[4:0]	AV		ADC AV Channel Data Multiplexing. Selects slot to connect AV channel input.	0xA	R/W
0x0DA	ADC_REDIRECT1	[31:30]	RESERVED		Reserved.	0x0	R
		[29:25]	AUX5		ADC AUX5 Channel Data Multiplexing. Selects slot to connect AUX5 channel input.	0x2	R/W
		[24:20]	AUX4		ADC AUX4 Channel Data Multiplexing. Selects slot to connect AUX4 channel input.	0x1	R/W
		[19:15]	AUX3		ADC AUX3 Channel Data Multiplexing. Selects slot to connect AUX3 channel input.	0x0	R/W
		[14:10]	AUX2		ADC AUX2 Channel Data Multiplexing. Selects slot to connect AUX2 channel input.	0x5	R/W
		[9:5]	AUX1		ADC AUX1 Channel Data Multiplexing. Selects slot to connect AUX1 channel input.	0x8	R/W
		[4:0]	AUX0		ADC AUX0 Channel Data Multiplexing. Selects slot to connect AUX0 channel input.	0xB	R/W
0x0DB	CRC_OPTEN	[31:16]	RESERVED		Reserved.	0x0	R
		15	CRC_ZXLPSEL_EN		CRC ZXLPSEL Enable. Set this bit to include the ZX_LP_SEL register in the configuration register CRC calculation.	0x0	R/W
		14	CRC_ZXTOUT_EN		CRC ZXTOUT_EN Enable. Set this bit to include the ZXTOUT register in the configuration register CRC calculation.	0x0	R/W
		13	CRC_APP_NL_LVL_EN		CRC APP_NL_LVL Enable. Set this bit to include the APP_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		12	CRC_ACT_NL_LVL_EN		CRC ACT_NL_LVL Enable. Set this bit to include the ACT_NL_LVL register in the configuration register CRC calculation.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		11	CRC_SWELLONE_CYC_EN		CRC SWELLONE_CYC Enable. Set this bit to include the xSWELLONE_CYC registers of all ADC channels in the configuration register CRC calculation.	0x0	R/W
		10	CRC_SWELLONE_LVL_EN		CRC SWELLONE_LVL Enable. Set this bit to include the xSWELLONE_LVL registers of all ADC channels in the configuration register CRC calculation.	0x0	R/W
		9	CRC_SWELLHALF_CYC_EN		CRC SWELLHALF_CYC Enable. Set this bit to include the xSWELLHALF_CYC registers of all ADC channels in the configuration register CRC calculation.	0x0	R/W
		8	CRC_SWELLHALF_LVL_EN		CRC SWELLHALF_LVL Enable. Set this bit to include the xSWELLHALF_LVL registers of all ADC channels in the configuration register CRC calculation.	0x0	R/W
		7	CRC_DIPONE_CYC_EN		CRC DIPONE_CYC Enable. Set this bit to include the xDIPONE_CYC registers of all ADC channels in the configuration register CRC calculation.	0x0	R/W
		6	CRC_DIPONE_LVL_EN		CRC DIPONE_LVL Enable. Set this bit to include the xDIPONE_LVL registers of all ADC channels in the configuration register CRC calculation.	0x0	R/W
		5	CRC_DIPHALF_CYC_EN		CRC DIPHALF_CYC Enable. Set this bit to include the xDIPHALF_CYC registers of all ADC channels in the configuration register CRC calculation.	0x0	R/W
		4	CRC_DIPHALF_LVL_EN		CRC DIPHALF_LVL Enable. Set this bit to include the xDIPHALF_LVL registers of all ADC channels in the configuration register CRC calculation.	0x0	R/W
		3	CRC_MASK3_EN		CRC MASK3 Enable. Set this bit to include the MASK3 register in the configuration register CRC calculation.	0x0	R/W
		2	CRC_MASK2_EN		CRC MASK2 Enable. Set this bit to include the MASK2	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					register in the configuration register CRC calculation.		
		1	CRC_MASK1_EN		CRC MASK1 Enable. Set this bit to include the MASK1 register in the configuration register CRC calculation.	0x0	R/W
		0	CRC_MASK0_EN		CRC MASK0 Enable. Set this bit to include the MASK0 register in the configuration register CRC calculation.	0x0	R/W
0x0DC	CRC_FORCE	[31:1]	RESERVED		Reserved.	0x0	R
		0	CRC_FORCE_VAL		Force Configuration Registers CRC Update. Write this bit to force the configuration register CRC calculation to start. When the calculation completes, the CRC_DONE bit is set in the STATUS1 register.	0x0	R/W
0x0DD	CONFIG_LOCK	[31:1]	RESERVED		Reserved.	0x0	R
		0	CONFIG_LOCK_VAL		Configuration Lock Register. When set, CONFIG_LOCK prohibits write access to all configuration and user registers.	0x0	R/W
0x257	AWATTHR_POS_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	AWATTHR_POS_LO_VAL		Phase A Accumulated Positive Total Active Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x259	AWATTHR_NEG_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	AWATTHR_NEG_LO_VAL		Phase A Accumulated Negative Total Active Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x25B	AWATTHR_SIGNED_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	AWATTHR_SIGNED_LO_VAL		Phase A Signed Accumulated Total Active Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x25D	AVAHR_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	AVAHR_LO_VAL		Phase A Accumulated Total Apparent Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x262	BWATTHR_POS_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	BWATTHR_POS_LO_VAL		Phase B Accumulated Positive Total Active Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x264	BWATTHR_NEG_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	BWATTHR_NEG_LO_VAL		Phase B Accumulated Negative Total Active Energy,	0x0	R

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Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					LSB. Stores [12:0] bits out of 45 bits energy output.		
0x266	BWATTHR_SIGNED_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	BWATTHR_SIGNED_LO_VAL		Phase B Signed Accumulated Total Active Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x268	BVAHR_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	BVAHR_LO_VAL		Phase B Accumulated Total Apparent Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x26D	CWATTHR_POS_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	CWATTHR_POS_LO_VAL		Phase C Accumulated Positive Total Active Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x26F	CWATTHR_NEG_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	CWATTHR_NEG_LO_VAL		Phase C Accumulated Negative Total Active Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x271	CWATTHR_SIGNED_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	CWATTHR_SIGNED_LO_VAL		Phase C Signed Accumulated Total Active Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x272	CWATTHR_SIGNED_HI	[31:0]	CWATTHR_SIGNED_HI_VAL		Phase C Signed Accumulated Total Active Energy, MSB. Stores [44:13] bits out of 45 bits energy output.	0x0	R
0x273	CVAHR_LO	[31:13]	RESERVED		Reserved.	0x0	R
		[12:0]	CVAHR_LO_VAL		Phase C Accumulated Total Apparent Energy, LSB. Stores [12:0] bits out of 45 bits energy output.	0x0	R
0x285	IPEAK	[31:27]	RESERVED		Reserved.	0x0	R
		[26:24]	IPPHASE		Current Channel Peak Phase. These bits indicate which phase generated the IPEAKVAL value. Among all the monitored phases for peak detection, phase A current had the highest peak if bit 0 is set, phase B current had the highest peak if bit 1 is set, and phase C current had the highest peak if bit 2 is set.	0x0	R
		[23:0]	IPEAKVAL		Absolute Value of the Peak Current. Stores absolute value of the peak for current channels.	0x0	R
0x286	VPEAK	[31:27]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[26:24]	VPPHASE		Voltage Channel Peak Phase. These bits indicate which phase generated the VPEAKVAL value. Among all the monitored phases for peak detection, phase A voltage had the highest peak if bit 0 is set, phase B voltage had the highest peak if bit 1 is set, and phase C voltage had the highest peak if bit 2 is set.	0x0	R
		[23:0]	VPEAKVAL		Absolute Value of the Peak Voltage. Stores absolute value of the peak for voltage channels.	0x0	R
0x287	AUXPEAK	[31:30]	RESERVED		Reserved.	0x0	R
		[29:24]	AUXPHASE		Auxiliary Channel Peak Phase. These bits indicate which phase generated the AUXPEAKVAL value. Among all the monitored phases for peak detection, AUX0 had the highest peak if bit 0 is set, AUX1 had the highest peak if bit 1 is set, AUX2 had the highest peak if bit 2 is set, and so on.	0x0	R
		[23:0]	AUXPEAKVAL		Absolute Peak Value of the Auxiliary Channels. Stores absolute value of the peak for auxiliary channels.	0x0	R
0x288	PHSIGN	[31:5]	RESERVED		Reserved.	0x0	R
		4	SUM2SIGN		CF2 Last Sum Sign. Sign of the sum of the powers included in the CF2 datapath. The CF2 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		3	SUM1SIGN		CF1 Last Sum Sign. Sign of the sum of the powers included in the CF1 datapath. The CF1 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		2	CWSIGN		Phase C Active Power Sign Bit. Sign of the active power of phase C. The active energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		1	BWSIGN		Phase B Active Power Sign Bit. Sign of the active power of phase B. The active energy is positive if this bit is clear and negative if this bit is set.	0x0	R

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	AWSIGN		Phase A Active Power Sign Bit. Sign of the active power of phase A. The active energy is positive if this bit is clear and negative if this bit is set.	0x0	R
0x289	PHNOLOAD	[31:6]	RESERVED		Reserved.	0x0	R
		5	CVANL		Phase C Total Apparent Energy No Load Status. This bit is set if the phase C total apparent energy is in no load.	0x0	R
		4	CWATTNL		Phase C Total Active Energy No Load Status. This bit is set if the phase C total active energy is in no load.	0x0	R
		3	BVANL		Phase B Total Apparent Energy No Load Status. This bit is set if the phase B total apparent energy is in no load.	0x0	R
		2	BWATTNL		Phase B Total Active Energy No Load Status. This bit is set if the phase B total active energy is in no load.	0x0	R
		1	AVANL		Phase A Total Apparent Energy No Load Status. This bit is set if the phase A total apparent energy is in no load.	0x0	R
		0	AWATTNL		Phase A Total Active Energy No Load Status. This bit is set if the phase A total active energy is in no load.	0x0	R
0x295	CRC_RSLT	[31:16]	RESERVED		Reserved.	0x0	R
		[15:0]	CRC_RSLT_VAL		Configuration Registers CRC Value.	0x0	R
0x400	STATUS0	31	ZXAUX5		Auxiliary 5 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX5 channel.	0x0	R/W1C
		30	ZXAUX4		Auxiliary 4 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX4 channel.	0x0	R/W1C
		29	ZXAUX3		Auxiliary 3 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX3 channel.	0x0	R/W1C
		28	ZXAUX2		Auxiliary 2 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX2 channel.	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		27	ZXAUX1		Auxiliary 1 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX1 channel.	0x0	R/W1C
		26	ZXAUX0		Auxiliary 0 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX0 channel.	0x0	R/W1C
		25	ZXCI		Phase C Current Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase C current channel.	0x0	R/W1C
		24	ZXBI		Phase B Current Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase B current channel.	0x0	R/W1C
		23	ZXAI		Phase A Current Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase A current channel.	0x0	R/W1C
		22	ZXCOMB		Combined Voltage Channels Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the combined signal from AV, BV, and CV.	0x0	R/W1C
		21	ZXCV		Phase C Voltage Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase C voltage channel.	0x0	R/W1C
		20	ZXBV		Phase B Voltage Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase B voltage channel.	0x0	R/W1C
		19	ZXAV		Phase A Voltage Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase A voltage channel.	0x0	R/W1C
		18	ZXTOCV		Phase C Voltage Zero-Crossing Timeout. This bit is set to indicate a zero-crossing timeout on phase C. This means that a zero crossing on the phase C voltage is missing.	0x0	R/W1C
		17	ZXTOBV		Phase B Voltage Zero-Crossing Timeout. This bit is set to indicate a zero-crossing	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					timeout on phase B. This means that a zero crossing on the phase B voltage is missing.		
		16	ZXTOAV		Phase A Voltage Zero-Crossing Timeout. This bit is set to indicate a zero-crossing timeout on phase A. This means that a zero crossing on the Phase A voltage is missing.	0x0	R/W1C
		15	SEQERR		Phase Sequence Error Occurred on Voltage Zero Crossings. This bit is set if zero crossings on three voltage phases does not follow phase A − phase B − phase C sequence.	0x0	R/W1C
		14	RSTDONE		Reset Completed and Ready for SPI Communication. This bit is set to indicate that reset is complete and board is ready for SPI communication.	0x0	R/W1C
		13	CRC_CHG		CRC Changed. This bit is set if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W1C
		12	VANLOAD		Total Apparent Energy No Load Condition Changed. This bit is set when one or more phase of total apparent energy enters or exits the no load condition.	0x0	R/W1C
		11	WATTNLOAD		Total Active Energy No Load Condition Changed. This bit is set when one or more phase of total active energy enters or exits the no load condition.	0x0	R/W1C
		10	ISUMMISMTCH		ISUM RMS Mismatch. This bit is set to indicate a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W1C
		9	PF_RDY		Power Factor Data Ready. This bit is set to indicate that power factor measurements are updated, every 1 sec.	0x0	R/W1C
		8	RMSONERDY		One-Cycle RMS Data Ready. This bit is set when the one-cycle RMS values are updated.	0x0	R/W1C
		7	CF2		CF2 Pulse Issued. This bit is set when a CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W1C
		6	CF1		CF1 Pulse Issued. This bit is set when a CF1 pulse is	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					issued, when the CF1 pin goes from a high to low state.		
		5	REVPSUM2		CF2 Polarity Sign Change. This bit is set to indicate if the CF2 polarity changed sign. See REVPSUM1.	0x0	R/W1C
		4	REVPSUM1		CF1 Polarity Sign Change. This bit is set to indicate if the CF1 polarity changed sign. For example, if the last CF1 pulse was positive active energy and the next CF1 pulse is negative active energy, then REVPSUM1 bit is set. This bit is updated when the CF1 pin goes from high to low.	0x0	R/W1C
		3	REVAPC		Phase C Active Power Sign Change. This bit indicates if the phase C active power has changed sign. See REVAPA.	0x0	R/W1C
		2	REVAPB		Phase B Active Power Sign Change. This bit indicates if the phase B active power has changed sign. See REVAPA.	0x0	R/W1C
		1	REVAPA		Phase A Active Power Sign Change. This bit indicates if the phase A active power has changed sign. This bit is updated when the power values in the xWATT_ACC registers update, after (EGY_TIME + 1) milliseconds or half-line cycles.	0x0	R/W1C
		0	EGYRDY		Energy Data Ready. This bit is set when the accumulated energy values (xWATTHR, xVAHR …) are updated, after (EGY_TIME + 1) milliseconds or half-line cycles, which depends on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W1C
0x401	STATUS1	31	ZXAUX5		Auxiliary 5 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX5 channel.	0x0	R/W1C
		30	ZXAUX4		Auxiliary 4 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX4 channel.	0x0	R/W1C
		29	ZXAUX3		Auxiliary 3 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					is detected on the AUX3 channel.		
		28	ZXAUX2		Auxiliary 2 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX2 channel.	0x0	R/W1C
		27	ZXAUX1		Auxiliary 1 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX1 channel.	0x0	R/W1C
		26	ZXAUX0		Auxiliary 0 Channel Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the AUX0 channel.	0x0	R/W1C
		25	ZXCI		Phase C Current Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase C current channel.	0x0	R/W1C
		24	ZXBI		Phase B Current Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase B current channel.	0x0	R/W1C
		23	ZXAI		Phase A Current Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase A current channel.	0x0	R/W1C
		22	ZXCOMB		Combined Voltage Channels Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the combined signal from AV, BV, and CV.	0x0	R/W1C
		21	ZXCV		Phase C Voltage Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase C voltage channel.	0x0	R/W1C
		20	ZXBV		Phase B Voltage Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase B voltage channel.	0x0	R/W1C
		19	ZXAV		Phase A Voltage Zero Crossing Detected. This bit is set to indicate a zero crossing is detected on the phase A voltage channel.	0x0	R/W1C
		18	ZXTOCV		Phase C Voltage Zero-Crossing Timeout. This bit is	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					set to indicate a zero-crossing timeout on phase C. This means that a zero crossing on the phase C voltage is missing.		
		17	ZXTOBV		Phase B Voltage Zero-Crossing Timeout. This bit is set to indicate a zero-crossing timeout on phase B. This means that a zero crossing on the phase B voltage is missing.	0x0	R/W1C
		16	ZXTOAV		Phase A Voltage Zero-Crossing Timeout. This bit is set to indicate a zero-crossing timeout on phase A. This means that a zero crossing on the phase A voltage is missing.	0x0	R/W1C
		15	SEQERR		Phase Sequence Error Occurred on Voltage Zero Crossings. This bit is set if zero crossings on three voltage phases does not follow phase A − phase B − phase C sequence.	0x0	R/W1C
		14	ERROR		Error Occurred. This bit is set to indicate that error has occurred. To identify the error, check ERROR_STATUS register.	0x0	R/W1C
		13	CRC_CHG		CRC Changed. This bit is set if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W1C
		12	VANLOAD		Total Apparent Energy No Load Condition Changed. This bit is set when one or more phase of total apparent energy enters or exits the no load condition.	0x0	R/W1C
		11	WATTNLOAD		Total Active Energy No Load Condition Changed. This bit is set when one or more phase of total active energy enters or exits the no load condition.	0x0	R/W1C
		10	ISUMMISMTCH		ISUM RMS Mismatch. This bit is set to indicate a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W1C
		9	PF_RDY		Power Factor Data Ready. This bit is set to indicate that power factor measurements are updated, every 1sec.	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		8	RMSONERDY		One-Cycle RMS Data Ready. This bit is set when the one-cycle RMS values are updated.	0x0	R/W1C
		7	CF2		CF2 Pulse Issued. This bit is set when a CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W1C
		6	CF1		CF1 Pulse Issued. This bit is set when a CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W1C
		5	REVPSUM2		CF2 Polarity Sign Change. This bit is set to indicate if the CF2 polarity changed sign. See REVPSUM1.	0x0	R/W1C
		4	REVPSUM1		CF1 Polarity Sign Change. This bit is set to indicate if the CF1 polarity changed sign. For example, if the last CF1 pulse was positive active energy and the next CF1 pulse is negative active energy, then REVPSUM1 bit is set. This bit is updated when the CF1 pin goes from high to low.	0x0	R/W1C
		3	REVAPC		Phase C Active Power Sign Change. This bit indicates if the phase C active power has changed sign. See REVAPA.	0x0	R/W1C
		2	REVAPB		Phase B Active Power Sign Change. This bit indicates if the phase B active power has changed sign. See REVAPA.	0x0	R/W1C
		1	REVAPA		Phase A Active Power Sign Change. This bit indicates if the phase A active power has changed sign. This bit is updated when the power values in the xWATT_ACC registers update, after (EGY_TIME + 1) milliseconds or half-line cycles.	0x0	R/W1C
		0	EGYRDY		Energy Data Ready. This bit is set when the accumulated energy values (xWATTHR, xVAHR ...) are updated, after (EGY_TIME + 1) milliseconds or half-line cycles, which depends on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W1C
0x402	STATUS2	31	RESERVED		Reserved.	0x0	R
		30	VACSWELLONE		VP2P Swell Condition Detected. This bit is set when the VP2P (AV − CV) voltage	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.		
		29	VBCSWELLONE		VP2P Swell Condition Detected. This bit is set when the VP2P (BV − CV) voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		28	VABSWELLONE		VP2P Swell Condition Detected. This bit is set when the VP2P (AV − BV) voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		27	VACDIPONE		VP2P Dip Condition Detected. This bit is set when the VP2P (AV − CV) voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		26	VBCDIPONE		VP2P Dip Condition Detected. This bit is set when the VP2P (BV − CV) voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		25	VABDIPONE		VP2P Dip Condition Detected. This bit is set when the VP2P (AV − BV) voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		24	VSUMSWELLONE		VSUM Swell Condition Detected. This bit is set when the sum of voltage channels is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		23	AUX5SWELLONE		Auxiliary 5 Channel Swell Condition Detected. This bit is set when the AUX5 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		22	AUX4SWELLONE		Auxiliary 4 Channel Swell Condition Detected. This bit is set when the AUX4 channel is in the swell condition and is zero when it is not in a	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					swell condition, as calculated by RMSONE.		
		21	AUX3SWELLONE		Auxiliary 3 Channel Swell Condition Detected. This bit is set when the AUX3 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		20	AUX2SWELLONE		Auxiliary 2 Channel Swell Condition Detected. This bit is set when the AUX2 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		19	AUX1SWELLONE		Auxiliary 1 Channel Swell Condition Detected. This bit is set when the AUX1 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		18	AUX0SWELLONE		Auxiliary 0 Channel Swell Condition Detected. This bit is set when the AUX0 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		17	CISWELLONE		Phase C Current Swell Condition Detected. This bit is set when the phase C current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		16	CVSWELLONE		Phase C Voltage Swell Condition Detected. This bit is set when the phase C voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		15	BISWELLONE		Phase B Current Swell Condition Detected. This bit is set when the phase B current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		14	BVSWELLONE		Phase B Voltage Swell Condition Detected. This bit is set when the phase B voltage is in the swell condition and is zero when it is not in a	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					swell condition, as calculated by RMSONE.		
		13	AISWELLONE		Phase A Current Swell Condition Detected. This bit is set when the phase A current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		12	AVSWELLONE		Phase A Voltage Swell Condition Detected. This bit is set when the phase A voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W1C
		11	AUX5DIPONE		Auxiliary 5 Channel Dip Condition Detected. This bit is set when the AUX5 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		10	AUX4DIPONE		Auxiliary 4 Channel Dip Condition Detected. This bit is set when the AUX4 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		9	AUX3DIPONE		Auxiliary 3 Channel Dip Condition Detected. This bit is set when the AUX3 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		8	AUX2DIPONE		Auxiliary 2 Channel Dip Condition Detected. This bit is set when the AUX2 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		7	AUX1DIPONE		Auxiliary 1 Channel Dip Condition Detected. This bit is set when the AUX1 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		6	AUX0DIPONE		Auxiliary 0 Channel Dip Condition Detected. This bit is set when the AUX0 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		5	CIDIPONE		Phase C Current Dip Condition Detected. This bit is set when the phase C current is in the	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.		
		4	CVDIPONE		Phase C Voltage Dip Condition Detected. This bit is set when the phase C voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		3	BIDIPONE		Phase B Current Dip Condition Detected. This bit is set when the phase B current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		2	BVDIPONE		Phase B Voltage Dip Condition Detected. This bit is set when the phase B voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		1	AIDIPONE		Phase A Current Dip Condition Detected. This bit is set when the phase A current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
		0	AVDIPONE		Phase A Voltage Dip Condition Detected. This bit is set when the phase A voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W1C
0x403	STATUS3	[31:24]	RESERVED		Reserved.	0x0	R
		23	AUX5SWELLHALF		Auxiliary 5 Channel Swell Condition Detected. This bit is set when the AUX5 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		22	AUX4SWELLHALF		Auxiliary 4 Channel Swell Condition Detected. This bit is set when the AUX4 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		21	AUX3SWELLHALF		Auxiliary 3 Channel Swell Condition Detected. This bit is set when the AUX3 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		20	AUX2SWELLHALF		Auxiliary 2 Channel Swell Condition Detected. This bit is set when the AUX2 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		19	AUX1SWELLHALF		Auxiliary 1 Channel Swell Condition Detected. This bit is set when the AUX1 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		18	AUX0SWELLHALF		Auxiliary 0 Channel Swell Condition Detected. This bit is set when the AUX0 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		17	CISWELLHALF		Phase C Current Swell Condition Detected. This bit is set when the phase C current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		16	CVSWELLHALF		Phase C Voltage Swell Condition Detected. This bit is set when the phase C voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		15	BISWELLHALF		Phase B Current Swell Condition Detected. This bit is set when the phase B current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		14	BVSWELLHALF		Phase B Voltage Swell Condition Detected. This bit is set when the phase B voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		13	AISWELLHALF		Phase A Current Swell Condition Detected. This bit is set when the phase A current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		12	AVSWELLHALF		Phase A Voltage Swell Condition Detected. This bit is set when the phase A voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W1C
		11	AUX5DIPHALF		Auxiliary 5 Channel Dip Condition Detected. This bit is set when the AUX5 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		10	AUX4DIPHALF		Auxiliary 4 Channel Dip Condition Detected. This bit is set when the AUX4 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		9	AUX3DIPHALF		Auxiliary 3 Channel Dip Condition Detected. This bit is set when the AUX3 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		8	AUX2DIPHALF		Auxiliary 2 Channel Dip Condition Detected. This bit is set when the AUX2 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		7	AUX1DIPHALF		Auxiliary 1 Channel Dip Condition Detected. This bit is set when the AUX1 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		6	AUX0DIPHALF		Auxiliary 0 Channel Dip Condition Detected. This bit is set when the AUX0 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		5	CIDIPHALF		Phase C Current Dip Condition Detected. This bit is set when the phase C current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		4	CVDIPHALF		Phase C Voltage Dip Condition Detected. This bit is set when the phase C voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	BIDIPHALF		Phase B Current Dip Condition Detected. This bit is set when the phase B current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		2	BVDIPHALF		Phase B Voltage Dip Condition Detected. This bit is set when the phase B voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		1	AIDIPHALF		Phase A Current Dip Condition Detected. This bit is set when the phase A current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
		0	AVDIPHALF		Phase A Voltage Dip Condition Detected. This bit is set when the phase A voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W1C
0x404	ERROR_STATUS	[31:23]	RESERVED		Reserved.	0x0	R
		22	ERROR7		Internal Error. Reset ADE9178 and ADCs.	0x0	R/W1C
		21	ERROR6		Internal Error. Reset ADE9178 and ADCs.	0x0	R/W1C
		20	ADC3_STATUS2		ADC3 STATUS2. This bit is set when one or more bits of STATUS2 register of ADC3 are set.	0x0	R/W1C
		19	ADC3_STATUS1		ADC3 STATUS1. This bit is set when one or more bits of STATUS1 register of ADC3 are set.	0x0	R/W1C
		18	ADC3_STATUS0		ADC3 STATUS0. This bit is set when one or more bits of STATUS0 register of ADC3 are set.	0x0	R/W1C
		17	ADC2_STATUS2		ADC2 STATUS2. This bit is set when one or more bits of STATUS2 register of ADC2 are set.	0x0	R/W1C
		16	ADC2_STATUS1		ADC2 STATUS1. This bit is set when one or more bits of STATUS1 register of ADC2 are set.	0x0	R/W1C
		15	ADC2_STATUS0		ADC2 STATUS0. This bit is set when one or more bits of STATUS0 register of ADC2 are set.	0x0	R/W1C

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		14	ADC1_STATUS2		ADC1 STATUS2. This bit is set when one or more bits of STATUS2 register of ADC1 are set.	0x0	R/W1C
		13	ADC1_STATUS1		ADC1 STATUS1. This bit is set when one or more bits of STATUS1 register of ADC1 are set.	0x0	R/W1C
		12	ADC1_STATUS0		ADC1 STATUS0. This bit is set when one or more bits of STATUS0 register of ADC1 are set.	0x0	R/W1C
		11	ADC0_STATUS2		ADC0 STATUS2. This bit is set when one or more bits of STATUS2 register of ADC0 are set.	0x0	R/W1C
		10	ADC0_STATUS1		ADC0 STATUS1. This bit is set when one or more bits of STATUS1 register of ADC0 are set.	0x0	R/W1C
		9	ADC0_STATUS0		ADC0 STATUS0. This bit is set when one or more bits of STATUS0 register of ADC0 are set.	0x0	R/W1C
		8	DREADY_FREQ_ERROR		ADC Data Ready Frequency Error. This bit is set when ADC Data Ready frequency is not 4 kHz. If the bit is set then new input samples will not be processed and output registers will not be updated.	0x0	R/W1C
		7	ERROR5		Internal Error. Reset ADE9178 and ADCs.	0x0	R/W1C
		6	ADC_CRC_ERROR		ADC CRC Error Occurs. This bit is set when ADC CRC error occurs.	0x0	R/W1C
		5	ERROR4		Internal Error. Reset ADE9178 and ADCs.	0x0	R/W1C
		4	ERROR3		Internal Error. Reset ADE9178 and ADCs.	0x0	R/W1C
		3	ERROR2		Internal Error. Reset ADE9178 and ADCs.	0x0	R/W1C
		2	ERROR1		Internal Error. Reset ADE9178 and ADCs.	0x0	R/W1C
		1	ERROR0		Internal Error. Reset ADE9178 and ADCs.	0x0	R/W1C
		0	ADC_INIT_ERROR		Error Occurs in ADC Initialization. This bit is set when error occurs in ADC initialization.	0x0	R/W1C
0x405	MASK0	31	ZXAUX5		Auxiliary 5 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					when a zero crossing is detected on the AUX5 channel.		
		30	ZXAUX4		Auxiliary 4 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX4 channel.	0x0	R/W
		29	ZXAUX3		Auxiliary 3 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX3 channel.	0x0	R/W
		28	ZXAUX2		Auxiliary 2 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX2 channel.	0x0	R/W
		27	ZXAUX1		Auxiliary 1 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX1 channel.	0x0	R/W
		26	ZXAUX0		Auxiliary 0 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX0 channel.	0x0	R/W
		25	ZXCI		Phase C Current Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase C current channel.	0x0	R/W
		24	ZXBI		Phase B Current Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase B current channel.	0x0	R/W
		23	ZXAI		Phase A Current Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase A current channel.	0x0	R/W
		22	ZXCOMB		Combined Voltage Channels Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the combined signal from AV, BV, and CV.	0x0	R/W
		21	ZXCV		Phase C Voltage Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase C voltage channel.	0x0	R/W
		20	ZXBV		Phase B Voltage Zero Crossing Detected Mask. Set this bit	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					to enable an interrupt when a zero crossing is detected on the phase B voltage channel.		
		19	ZXAV		Phase A Voltage Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase A voltage channel.	0x0	R/W
		18	ZXTOCV		Phase C Voltage Zero-Crossing Timeout Mask. Set this bit to enable an interrupt when there is a zero-crossing timeout on phase C. This means that a zero crossing on the phase C voltage is missing.	0x0	R/W
		17	ZXTOBV		Phase B Voltage Zero-Crossing Timeout Mask. Set this bit to enable an interrupt when there is a zero-crossing timeout on phase B. This means that a zero crossing on the phase B voltage is missing.	0x0	R/W
		16	ZXTOAV		Phase A Voltage Zero-Crossing Timeout Mask. Set this bit to enable an interrupt when there is a zero-crossing timeout on phase A. This means that a zero crossing on the phase A voltage is missing.	0x0	R/W
		15	SEQERR		Phase Sequence Error Occurred on Voltage Zero Crossings. Set this bit to enable an interrupt when zero crossings on three voltage phases does not follow phase A − phase B − phase C sequence.	0x0	R/W
		14	RSTDONE		Reset Completed and Ready for SPI Communication. Set this bit to enable an interrupt when the reset is complete and board is ready for SPI communication.	0x1	R
		13	CRC_CHG		CRC Changed Mask. Set this bit to enable an interrupt if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W
		12	VANLOAD		Total Apparent Energy No Load Condition Changed Mask. Set this bit to enable an interrupt when one or more phase of	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					total apparent energy enters or exits the no load condition.		
		11	WATTNLOAD		Total Active Energy No Load Condition Changed Mask. Set this bit to enable an interrupt when one or more phase of total active energy enters or exits the no load condition.	0x0	R/W
		10	ISUMMISMTCH		ISUM RMS Mismatch Mask. Set this bit to enable an interrupt when there is a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W
		9	PF_RDY		Power Factor Data Ready Mask. Set this bit to enable an interrupt when the power factor measurements are updated, every 1 sec.	0x0	R/W
		8	RMSONERDY		One-Cycle RMS Data Ready Mask. Set this bit to enable an interrupt when the one-cycle RMS values are updated.	0x0	R/W
		7	CF2		CF2 Pulse Issued Mask. Set this bit to enable an interrupt when a CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W
		6	CF1		CF1 Pulse Issued Mask. Set this bit to enable an interrupt when a CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W
		5	REVPSUM2		CF2 Polarity Sign Change Mask. Set this bit to enable an interrupt when the CF2 polarity changed sign.	0x0	R/W
		4	REVPSUM1		CF1 Polarity Sign Change Mask. Set this bit to enable an interrupt when the CF1 polarity changed sign.	0x0	R/W
		3	REVAPC		Phase C Active Power Sign Change Mask. Set this bit to enable an interrupt when the phase C active power has changed sign.	0x0	R/W
		2	REVAPB		Phase B Active Power Sign Change Mask. Set this bit to enable an interrupt when the phase B active power has changed sign.	0x0	R/W
		1	REVAPA		Phase A Active Power Sign Change Mask. Set this bit to enable an interrupt when the	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					phase A active power has changed sign.		
		0	EGYRDY		Energy Data Ready Mask. Set this bit to enable an interrupt when the accumulated energy values (xWATTHR, xAVHR ...) are updated.	0x0	R/W
0x406	MASK1	31	ZXAUX5		Auxiliary 5 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX5 channel.	0x0	R/W
		30	ZXAUX4		Auxiliary 4 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX4 channel.	0x0	R/W
		29	ZXAUX3		Auxiliary 3 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX3 channel.	0x0	R/W
		28	ZXAUX2		Auxiliary 2 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX2 channel.	0x0	R/W
		27	ZXAUX1		Auxiliary 1 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX1 channel.	0x0	R/W
		26	ZXAUX0		Auxiliary 0 Channel Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the AUX0 channel.	0x0	R/W
		25	ZXCI		Phase C Current Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase C current channel.	0x0	R/W
		24	ZXBI		Phase B Current Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase B current channel.	0x0	R/W
		23	ZXAI		Phase A Current Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase A current channel.	0x0	R/W
		22	ZXCOMB		Combined Voltage Channels Zero Crossing Detected Mask. Set this bit to enable an	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					interrupt when a zero crossing is detected on the combined signal from AV, BV, and CV.		
		21	ZXCV		Phase C Voltage Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase C voltage channel.	0x0	R/W
		20	ZXBV		Phase B Voltage Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase B voltage channel.	0x0	R/W
		19	ZXAV		Phase A Voltage Zero Crossing Detected Mask. Set this bit to enable an interrupt when a zero crossing is detected on the phase A voltage channel.	0x0	R/W
		18	ZXTOCV		Phase C Voltage Zero-Crossing Timeout Mask. Set this bit to enable an interrupt when there is a zero-crossing timeout on phase C. This means that a zero crossing on the phase C voltage is missing.	0x0	R/W
		17	ZXTOBV		Phase B Voltage Zero-Crossing Timeout Mask. Set this bit to enable an interrupt when there is a zero-crossing timeout on phase B. This means that a zero crossing on the phase B voltage is missing.	0x0	R/W
		16	ZXTOAV		Phase A Voltage Zero-Crossing Timeout Mask. Set this bit to enable an interrupt when there is a zero-crossing timeout on phase A. This means that a zero crossing on the phase A voltage is missing.	0x0	R/W
		15	SEQERR		Phase Sequence Error Occurred on Voltage Zero Crossings. Set this bit to enable an interrupt when zero crossings on three voltage phases does not follow phase A − phase B − phase C sequence.	0x0	R/W
		14	ERROR		Error Occurred. Set this bit is set to enable an interrupt when error has occurred. To identify the error, check ERROR_STATUS register.	0x1	R/W
		13	CRC_CHG		CRC Changed Mask. Set this bit to enable an interrupt if any of the registers monitored	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.		
		12	VANLOAD		Total Apparent Energy No Load Condition Changed Mask. Set this bit to enable an interrupt when one or more phase of total apparent energy enters or exits the no load condition.	0x0	R/W
		11	WATTNLOAD		Total Active Energy No Load Condition Changed Mask. Set this bit to enable an interrupt when one or more phase of total active energy enters or exits the no load condition.	0x0	R/W
		10	ISUMMISMTCH		ISUM RMS Mismatch Mask. Set this bit to enable an interrupt when there is a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W
		9	PF_RDY		Power Factor Data Ready Mask. Set this bit to enable an interrupt when the power factor measurements update, every 1 sec.	0x0	R/W
		8	RMSONERDY		One-Cycle RMS Data Ready Mask. Set this bit to enable an interrupt when the one cycle RMS values are updated.	0x0	R/W
		7	CF2		CF2 Pulse Issued Mask. Set this bit to enable an interrupt when a CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W
		6	CF1		CF1 Pulse Issued Mask. Set this bit to enable an interrupt when a CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W
		5	REVPSUM2		CF2 Polarity Sign Change Mask. Set this bit to enable an interrupt when the CF2 polarity changed sign.	0x0	R/W
		4	REVPSUM1		CF1 Polarity Sign Change Mask. Set this bit to enable an interrupt when the CF1 polarity changed sign.	0x0	R/W
		3	REVAPC		Phase C Active Power Sign Change Mask. Set this bit to enable an interrupt when the phase C active power has changed sign.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	REVAPB		Phase B Active Power Sign Change Mask. Set this bit to enable an interrupt when the phase B active power has changed sign.	0x0	R/W
		1	REVAPA		Phase A Active Power Sign Change Mask. Set this bit to enable an interrupt when the phase A active power has changed sign.	0x0	R/W
		0	EGYRDY		Energy Data Ready Mask. Set this bit to enable an interrupt when the accumulated energy values (xWATTHR, xAVHR ...) are updated.	0x0	R/W
0x407	MASK2	31	RESERVED		Reserved.	0x0	R
		30	VACSWELLONE		VP2P Swell Condition Detected. Set this bit to enable an interrupt when the VP2P (AV − CV) voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		29	VBCSWELLONE		VP2P Swell Condition Detected. Set this bit to enable an interrupt when the VP2P (BV − CV) voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		28	VABSWELLONE		VP2P Swell Condition Detected. Set this bit to enable an interrupt when the VP2P (AV − BV) voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		27	VACDIPONE		VP2P Dip Condition Detected. Set this bit to enable an interrupt when the VP2P (AV − CV) voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		26	VBCDIPONE		VP2P Dip Condition Detected. Set this bit to enable an interrupt when the VP2P (BV − CV) voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		25	VABDIPONE		VP2P Dip Condition Detected. Set this bit to enable an interrupt when the VP2P (AV − BV) voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		24	VSUMSWELLONE		VSUM Swell Condition Detected. Set this bit to enable an interrupt when the sum of voltage channels is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		23	AUX5SWELLONE		Auxiliary 5 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX5 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		22	AUX4SWELLONE		Auxiliary 4 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX4 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		21	AUX3SWELLONE		Auxiliary 3 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX3 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		20	AUX2SWELLONE		Auxiliary 2 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX2 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		19	AUX1SWELLONE		Auxiliary 1 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX1 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		18	AUX0SWELLONE		Auxiliary 0 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX0 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		17	CISWELLONE		Phase C Current Swell Condition Detected. Set this bit to enable an interrupt when the phase C current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		16	CVSWELLONE		Phase C Voltage Swell Condition Detected. Set this bit to enable an interrupt when the phase C voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		15	BISWELLONE		Phase B Current Swell Condition Detected. Set this bit to enable an interrupt when the phase B current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		14	BVSWELLONE		Phase B Voltage Swell Condition Detected. Set this bit to enable an interrupt when the phase B voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		13	AISWELLONE		Phase A Current Swell Condition Detected. Set this bit to enable an interrupt when the phase A current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		12	AVSWELLONE		Phase A Voltage Swell Condition Detected. Set this bit to enable an interrupt when the phase A voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSONE.	0x0	R/W
		11	AUX5DIPONE		Auxiliary 5 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX5 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		10	AUX4DIPONE		Auxiliary 4 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX4 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		9	AUX3DIPONE		Auxiliary 3 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX3 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		8	AUX2DIPONE		Auxiliary 2 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX2 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		7	AUX1DIPONE		Auxiliary 1 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX1 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		6	AUX0DIPONE		Auxiliary 0 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX0 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		5	CIDIPONE		Phase C Current Dip Condition Detected. Set this bit to enable an interrupt when the Phase C current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		4	CVDIPONE		Phase C Voltage Dip Condition Detected. Set this bit to enable an interrupt when the phase C voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		3	BIDIPONE		Phase B Current Dip Condition Detected. Set this bit to enable an interrupt when the phase B current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		2	BVDIPONE		Phase B Voltage Dip Condition Detected. Set this bit to enable an interrupt when the phase B voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	AIDIPONE		Phase A Current Dip Condition Detected. Set this bit to enable an interrupt when the phase A current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
		0	AVDIPONE		Phase A Voltage Dip Condition Detected. Set this bit to enable an interrupt when the phase A voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSONE.	0x0	R/W
0x408	MASK3	[31:24]	RESERVED		Reserved.	0x0	R
		23	AUX5SWELLHALF		Auxiliary 5 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX5 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		22	AUX4SWELLHALF		Auxiliary 4 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX4 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		21	AUX3SWELLHALF		Auxiliary 3 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX3 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		20	AUX2SWELLHALF		Auxiliary 2 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX2 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		19	AUX1SWELLHALF		Auxiliary 1 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX1 channel is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		18	AUX0SWELLHALF		Auxiliary 0 Channel Swell Condition Detected. Set this bit to enable an interrupt when the AUX0 channel is in the swell condition and is zero when it	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					is not in a swell condition, as calculated by RMSHALF.		
		17	CISWELLHALF		Phase C Current Swell Condition Detected. Set this bit to enable an interrupt when the phase C current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		16	CVSWELLHALF		Phase C Voltage Swell Condition Detected. Set this bit to enable an interrupt when the phase C voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		15	BISWELLHALF		Phase B Current Swell Condition Detected. Set this bit to enable an interrupt when the phase B current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		14	BVSWELLHALF		Phase B Voltage Swell Condition Detected. Set this bit to enable an interrupt when the phase B voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		13	AISWELLHALF		Phase A Current Swell Condition Detected. Set this bit to enable an interrupt when the phase A current is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		12	AVSWELLHALF		Phase A Voltage Swell Condition Detected. Set this bit to enable an interrupt when the phase A voltage is in the swell condition and is zero when it is not in a swell condition, as calculated by RMSHALF.	0x0	R/W
		11	AUX5DIPHALF		Auxiliary 5 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX5 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		10	AUX4DIPHALF		Auxiliary 4 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX4 channel is in the dip condition and is zero when it	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					is not in a dip condition, as calculated by RMSHALF.		
		9	AUX3DIPHALF		Auxiliary 3 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX3 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		8	AUX2DIPHALF		Auxiliary 2 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX2 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		7	AUX1DIPHALF		Auxiliary 1 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX1 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		6	AUX0DIPHALF		Auxiliary 0 Channel Dip Condition Detected. Set this bit to enable an interrupt when the AUX0 channel is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		5	CIDIPHALF		Phase C Current Dip Condition Detected. Set this bit to enable an interrupt when the phase C current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		4	CVDIPHALF		Phase C Voltage Dip Condition Detected. Set this bit to enable an interrupt when the phase C voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		3	BIDIPHALF		Phase B Current Dip Condition Detected. Set this bit to enable an interrupt when the phase B current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		2	BVDIPHALF		Phase B Voltage Dip Condition Detected. Set this bit to enable an interrupt when the phase B voltage is in the dip condition and is zero when it is not in a	0x0	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					dip condition, as calculated by RMSHALF.		
		1	AIDIPHALF		Phase A Current Dip Condition Detected. Set this bit to enable an interrupt when the phase A current is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
		0	AVDIPHALF		Phase A Voltage Dip Condition Detected. Set this bit to enable an interrupt when the phase A voltage is in the dip condition and is zero when it is not in a dip condition, as calculated by RMSHALF.	0x0	R/W
0x409	ERROR_MASK	[31:23]	RESERVED		Reserved.	0x0	R
		22	ERROR7		Error7 Bit Mask. Set this bit to enable an interrupt when an internal error occurs.	0x1	R/W
		21	ERROR6		Error6 Bit Mask. Set this bit to enable an interrupt when an internal error occurs.	0x1	R/W
		20	ADC3_STATUS2		ADC3 STATUS2 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS2 register of ADC3 are set.	0x1	R/W
		19	ADC3_STATUS1		ADC3 STATUS1 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS1 register of ADC3 are set.	0x1	R/W
		18	ADC3_STATUS0		ADC3 STATUS0 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS0 register of ADC3 are set.	0x1	R/W
		17	ADC2_STATUS2		ADC2 STATUS2 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS2 register of ADC2 are set.	0x1	R/W
		16	ADC2_STATUS1		ADC2 STATUS1 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS1 register of ADC2 are set.	0x1	R/W
		15	ADC2_STATUS0		ADC2 STATUS0 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS0 register of ADC2 are set.	0x1	R/W
		14	ADC1_STATUS2		ADC1 STATUS2 Bit Mask. Set this bit to enable an interrupt	0x1	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
					when one or more bits of STATUS2 register of ADC1 are set.		
		13	ADC1_STATUS1		ADC1 STATUS1 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS1 register of ADC1 are set.	0x1	R/W
		12	ADC1_STATUS0		ADC1 STATUS0 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS0 register of ADC1 are set.	0x1	R/W
		11	ADC0_STATUS2		ADC0 STATUS2 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS2 register of ADC0 are set.	0x1	R/W
		10	ADC0_STATUS1		ADC0 STATUS1 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS1 register of ADC0 are set.	0x1	R/W
		9	ADC0_STATUS0		ADC0 STATUS0 Bit Mask. Set this bit to enable an interrupt when one or more bits of STATUS0 register of ADC0 are set.	0x1	R/W
		8	DREADY_FREQ_ERROR		ADC Data Ready Frequency Error Bit Mask. Set this bit to enable an interrupt when ADC Data Ready frequency is not 4KHz.	0x1	R/W
		7	ERROR5		Error5 Bit Mask. Set this bit to enable an interrupt when an internal error occurs.	0x1	R/W
		6	ADC_CRC_ERROR		ADC CRC Error Bit Mask. Set this bit to enable an interrupt when ADC CRC error occurs.	0x1	R/W
		5	ERROR4		Error4 Bit Mask. Set this bit to enable an interrupt when an internal error occurs.	0x1	R/W
		4	ERROR3		Error3 Bit Mask. Set this bit to enable an interrupt when an internal error occurs.	0x1	R/W
		3	ERROR2		Error2 Bit Mask. Set this bit to enable an interrupt when an internal error occurs.	0x1	R/W
		2	ERROR1		Error1 Bit Mask. Set this bit to enable an interrupt when an internal error occurs.	0x1	R/W
		1	ERROR0		Error0 Bit Mask. Set this bit to enable an interrupt when an internal error occurs.	0x1	R/W

REGISTER DETAILS: ADE9178

Table 34. ADE9178 Register Details (Continued)

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	ADC_INIT_ERROR		ADC Initialization Error Bit Mask. Set this bit to enable an interrupt when error occurs in ADC initialization.	0x1	R/W

OUTLINE DIMENSIONS

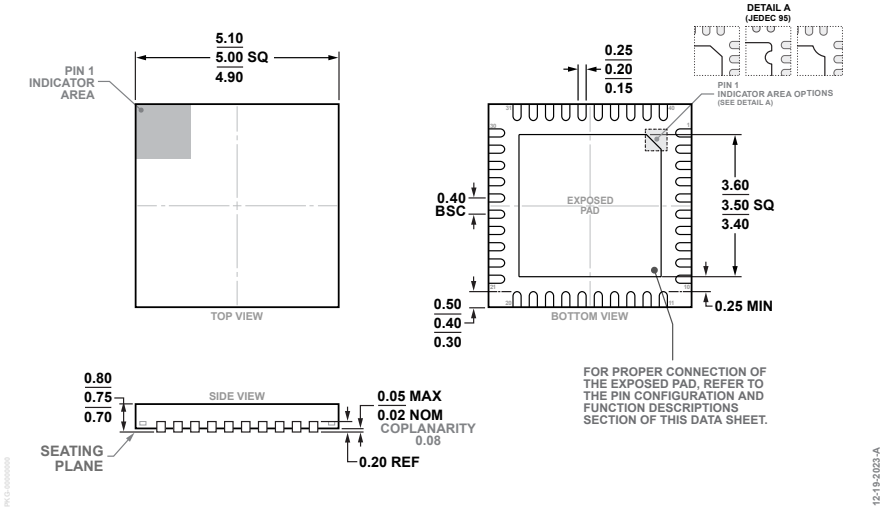

Figure 70. 40-Lead Lead Frame Chip-Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-40-33)
Dimensions Shown in millimeters

Updated: June 12, 2024

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADE9178GTL+T	−40°C to +105°C	40-Lead TQFN-EP Package (5 mm × 5 mm × 0.75 mm)	Reel, 2500	CP-40-33
ADE9178GTL+	−40°C to +105°C	40-Lead TQFN-EP Package (5 mm × 5 mm × 0.75 mm)	Tray, 490	CP-40-33

[1] All models are RoHS-Compliant Part.

[2] T = Tape and reel.

EVALUATION BOARDS

Table 35. Evaluation Boards

Model	Description
ADE9178EVKIT#	Evaluation Kit

LICENSES

For more details, refer to the Software License Agreement on the product webpage.