



NEX81801DA; NEX81802DA

Adaptive Synchronous Rectifier (SR) Controller

Rev. 1 — 30 September 2024

Product data sheet

1. General description

The NEX81801DA and NEX81802DA (NEX81801/2DA) are high performance synchronous rectification controllers used in switching mode power supplies. It supports operation in Discontinuous Conduction Mode (DCM), Continuous Conduction Mode (CCM) and quasi-resonant flyback converters.

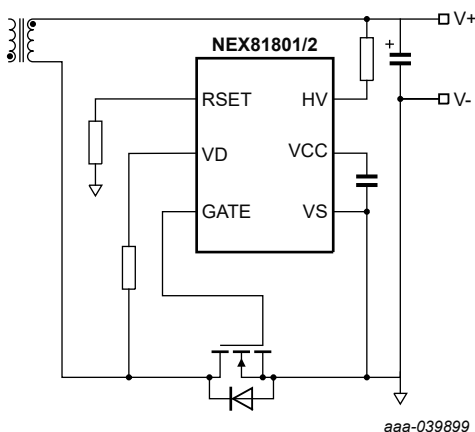
The NEX81801/2DA regulates the forward drop voltage of an external synchronous rectifier (SR) MOSFET in two stages. This allows the SR FET to turn off quickly when the V_{DS} becomes positive.

The externally adjustable turn-on blanking time can effectively prevent the synchronous rectifier from being falsely turned off due to leakage inductance and parasitic parameter oscillation.

The adaptive turn-on detection circuit can prevent the SR from being mistakenly turned on when the V_{DS} DCM oscillation crosses zero during some load conditions. The adaptive turn-on detection circuit also enhances SR conduction efficiency during light load conditions, thereby improving the average efficiency of the power supply across the entire load range.

The synchronous switch can be configured at high-side or low-side output without auxiliary windings or other power sources, because the NEX81801/2DA has a self-supply capability.

The NEX81801/2DA uses TSOT23-6 packaging with low thermal resistance. This can effectively reduce the junction temperature of the chip, making it suitable for high-density power supply design.

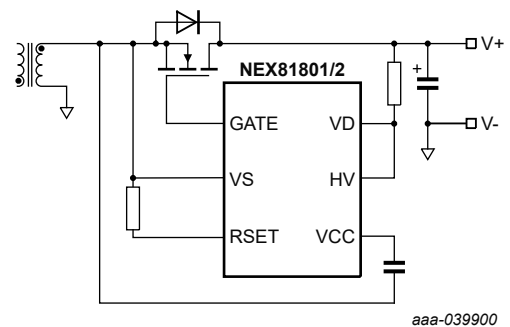


2. Features and benefits

- Supports DCM, CCM, QR operation
- Supports up to 800 kHz switching frequency
- Standard and logic level MOSFET driving capability
- Wide output range down to 0 V with 2-channel VCC supply
- No need for auxiliary winding for high-side or low-side rectification
- Smart proportional gate driver for fast SR turn-off at CCM
- Adjustable turn-on blanking time for increased noise immunity
- Proprietary adaptive turn-on detection prevents SR FET from falsely turning on during DCM operation
- 10 ns typical turn-off propagation delay
- Available in a TSOT23-6 FC package
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C2a exceeds 500 V

3. Applications

- USB PD/QC chargers
- AC/DC adapters for portable devices
- Flyback SMPS with high-efficiency requirements



4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NEX81801DA	-40 °C to +125 °C	TSOT23-6FC	Plastic, surface-mounted package; 6 leads	SOT8061-1
NEX81802DA	-40 °C to +125 °C	TSOT23-6FC	Plastic, surface-mounted package; 6 leads	SOT8061-1

5. Marking

Table 2. Marking code

Type number	Marking code
NEX81801DA	ND3
NEX81802DA	ND4

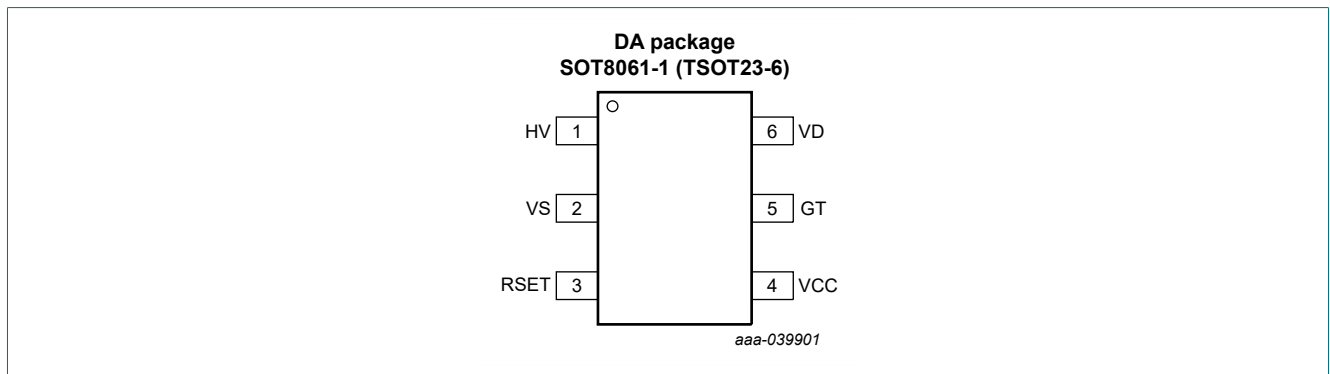
6. Device comparison

Table 3. Device comparison

Type number	Turn on blanking time (C_{SET} not installed)
NEX81801DA	1.0 μ s
NEX81802DA	0.5 μ s

7. Pinning information

7.1. Pinning



7.2. Pin description

Pin		I/O	Description
Name	Number		
HV	1	I	HV linear regulator input
VS	2	-	Ground reference
RSET	3	-	Configuration pin for turn-on detection and t_{on} min setting
VCC	4	-	Internal power supply
GT	5	O	Output to drive MOSFET
VD	6	O	MOSFET drain voltage sense

8. Product specifications

8.1. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VS (ground = 0 V).

[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	+14.0	V
GT	gate driver output		-0.3	+14.0	V
V_D	MOSFET drain voltage sense		-1.0	120	V
HV	HV linear regulator input		-1.0	120	V
RSET	turn-on detection		-0.3	6.5	V
T_{stg}	storage temperature		-55	150	°C
ESD					
V_{ESD}	ESD voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	-2000	+2000	V
		CDM: ANSI/ESDA/JEDEC JS-001 class C2a	-500	+500	V

[1] Stresses beyond those listed here may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 8.3](#). Exposure to these limiting values for extended periods may affect device reliability.

8.2. Thermal characteristics

Table 5. Thermal characteristics

For more information about thermal metrics consult application note.

Symbol	Parameter	package 1	Unit
$R_{\theta JA}$	junction-to-ambient thermal resistance	112	K/W
$R_{\theta JC(BOT)}$	junction-to-case (bottle) thermal resistance	78	K/W

8.3. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to VS (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.3	13.0	V
GT	gate driver output		-0.3	10.0	V
V _D	MOSFET drain voltage sense		-1.0	100	V
HV	HV linear regulator input		-1.0	100	V
RSET	turn-on detection		-0.3	5.0	V
T _J	operation junction temperature		-40	125	°C

8.4. Recommended components

Table 7. Recommended components

Nominal component values, not including derating factors.

Symbol	Parameter	Min	Typical	Max	Unit
C _{VCC}	capacitance on VCC	0.047	0.1	2.2	μF
C _{SET}	capacitance on RSET	-	NC	-	nF
R _{SET}	resistance on RSET	0	36	200	kΩ

8.5. Electrical characteristics

Table 8. Static characteristics

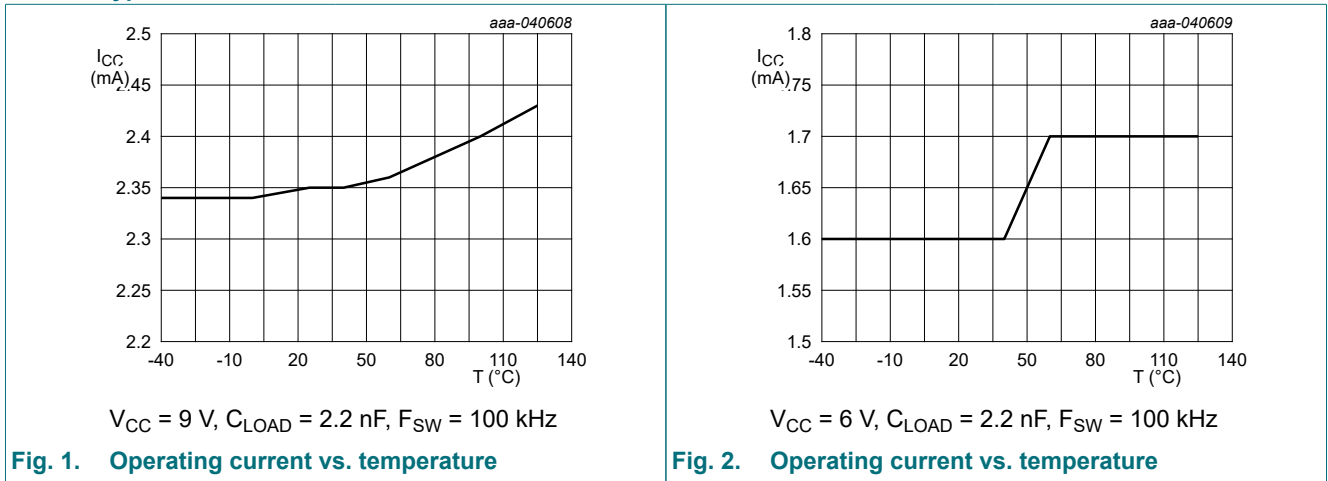
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply management section						
V _{CC_ON}	V _{CC} supply voltage	V _{CC} supply voltage (turn-on)	4.0	4.5	5.0	V
V _{CC_OFF}		V _{CC} supply voltage (turn-off)	3.5	4.0	4.5	V
V _{CC_HYS}	V _{CC_UVLO} hysteresis		-	0.5	-	V
I _{VCC_CHG}	V _{CC} maximum charging current	V _{CC} = 7 V; HV = 20 V	-	70	-	mA
		V _{CC} = 4 V; V _D = 30 V; HV = 0 V	-	40	-	mA
V _{CC_REG}	V _{CC} regulation voltage	V _D = 12 V; HV = 12 V	8	9	10	V
		V _D = 12 V; HV = 3 V	5.5	6	6.5	V
I _{CC}	current consumption	V _{CC} = 9 V; C _{LOAD} = 2.2 nF; F _{sw} = 100 kHz	-	2.3	3	mA
		V _{CC} = 6 V; C _{LOAD} = 2.2 nF; F _{sw} = 100 kHz	-	1.4	1.8	mA
I _{CC_UVLO}	current consumption under UVLO	V _{CC} = UVLO - 0.1 V	-	40	60	μA
Control circuitry section						
V _{REG1}	1st step regulation voltage (V _{DS})		-50	-35	-20	mV
V _{REG2}	2nd step regulation voltage (V _{DS})		-200	-150	-100	mV
V _{th_ON}	turn-on threshold (V _{DS})	V _D falling	-200	-150	-80	mV
V _{th_OFF}	turn-off threshold (V _{DS})	V _D rising	-12	-3	6	mV
t _{d_ON}	turn-on delay	C _{LOAD} = 2.2 nF	-	35	-	ns
t _{d_OFF}	turn-off delay	C _{LOAD} = 2.2 nF	-	20	-	ns

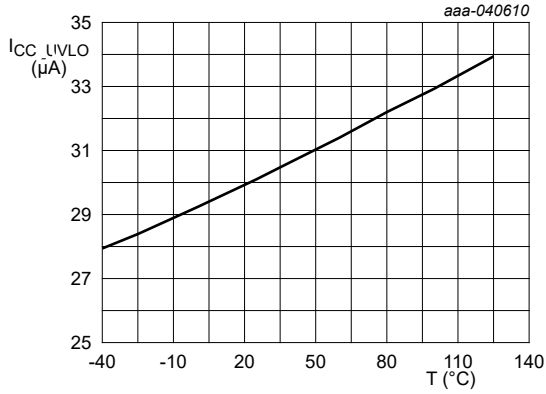
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{d_OFF(prop)}$	turn-off propagation delay	[1]	-	10	-	ns	
t_{b_on}	turn-on blanking time	C_{SET} is not installed	NEX81801DA	-	1.0	-	μ s
			NEX81802DA	-	0.5	-	μ s
		$C_{SET} = 1$ nF	NEX81801DA	-	1.5	-	μ s
			NEX81802DA	-	1.0	-	μ s
		$C_{SET} = 22$ nF	NEX81801DA	-	2.0	-	μ s
NEX81802DA	-	1.5	-	μ s			
V_{b_off}	turn-off blanking threshold (V_{DS})		1.2	1.8	2.4	V	
Gate driver							
V_{GT_L}	V_{GT} (low)	$I_{LOAD} = 10$ mA	-	0.01	0.02	V	
V_{GT_H}	V_{GT} (high)	$I_{LOAD} = 0$ mA	-	V_{CC}	-	V	
I_{GT_PU}	gate driver maximum source current		-	1	-	A	
I_{GT_PD}	gate driver maximum sink current		-	4	-	A	
R_{PU}	pull-up impedance		-	2.8	4.2	Ω	
R_{PD}	pull-down impedance		-	0.4	0.9	Ω	

[1] Guaranteed by characterization and design.

8.6. Typical characteristics

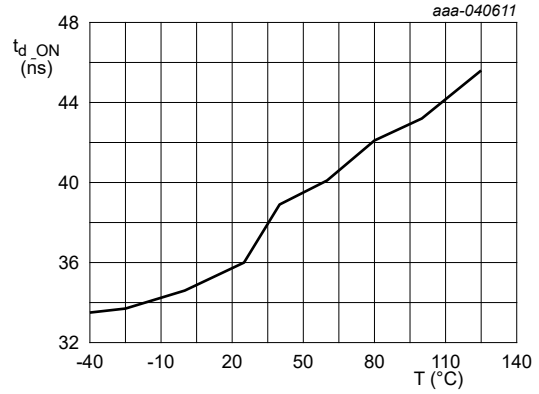
Table 9. Typical characteristics





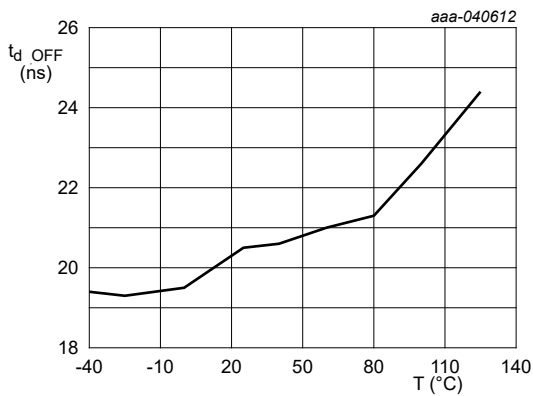
$V_{CC} = 4\ V$

Fig. 3. V_{CC} shutdown current vs. temperature



$V_{CC} = 9\ V, C_{LOAD} = 2.2\ nF$

Fig. 4. Turn-on delay vs. temperature



$V_{CC} = 9\ V, C_{LOAD} = 2.2\ nF$

Fig. 5. Turn-off delay vs. temperature

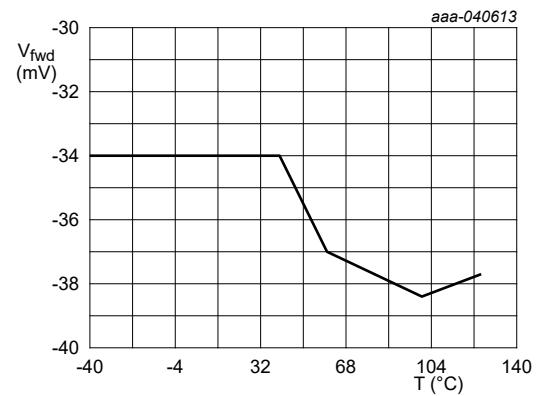


Fig. 6. First step regulation voltage vs. temperature

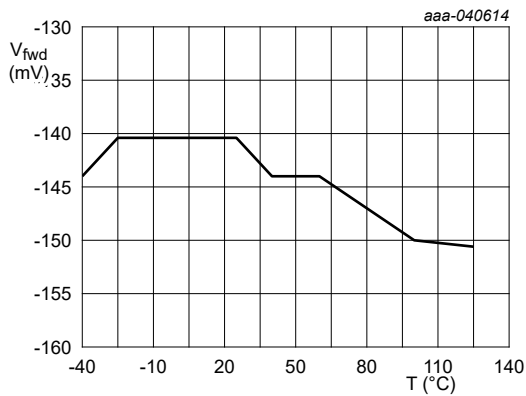
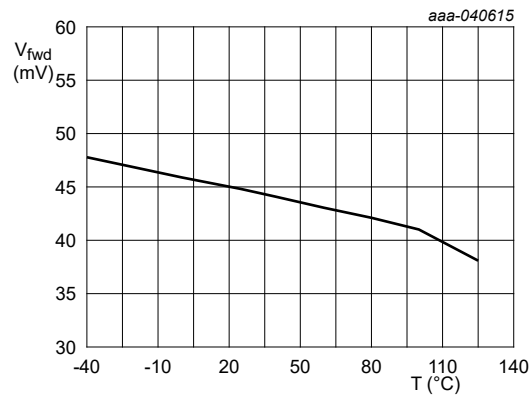
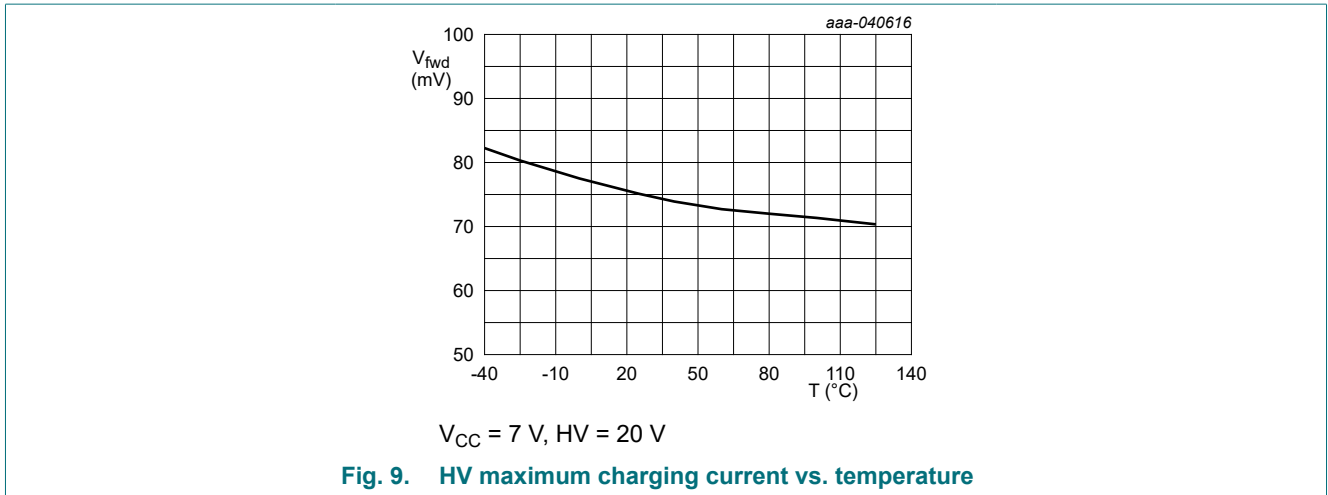


Fig. 7. Second step regulation voltage vs. temperature



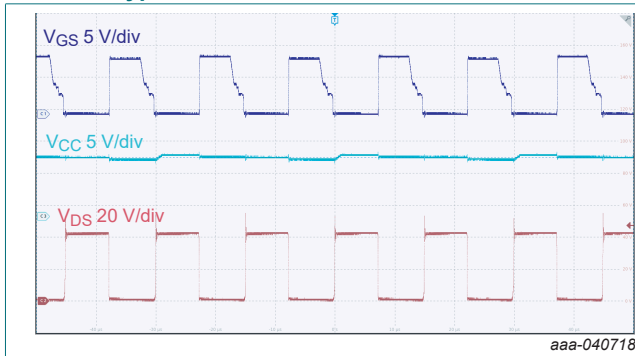
$V_{CC} = 4\ V, V_D = 30\ V$

Fig. 8. V_D maximum charging current vs. temperature



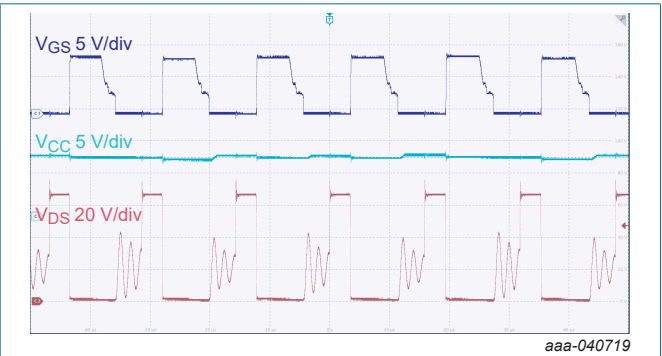
8.7. Typical waveforms

Table 10. Typical waveforms



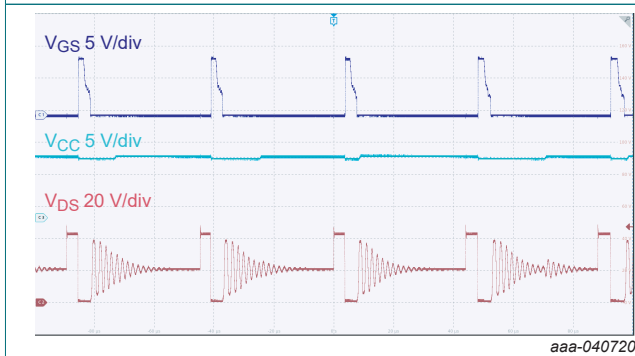
V_{IN} = 110V_{AC}, V_{OUT} = 20 V, I_{OUT} = 3.25 A
High-side, HV connected to VD

Fig. 10. Operation in 65 W flyback application



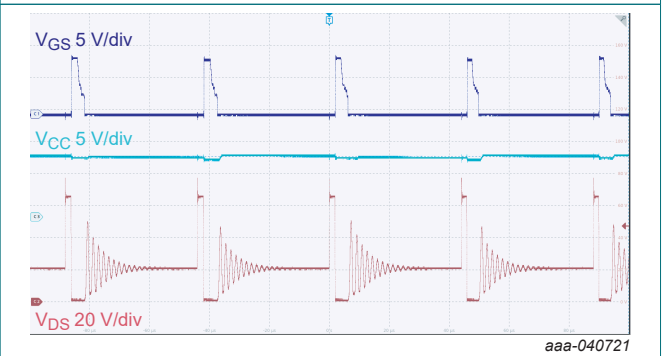
V_{IN} = 230V_{AC}, V_{OUT} = 20 V, I_{OUT} = 3.25 A
High-side, HV connected to VD

Fig. 11. Operation in 65 W flyback application



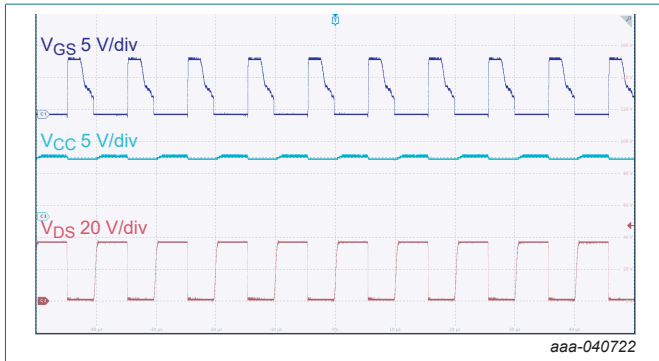
V_{IN} = 110V_{AC}, V_{OUT} = 20 V, I_{OUT} = 0.325 A
High-side, HV connected to VD

Fig. 12. Operation in 65 W flyback application



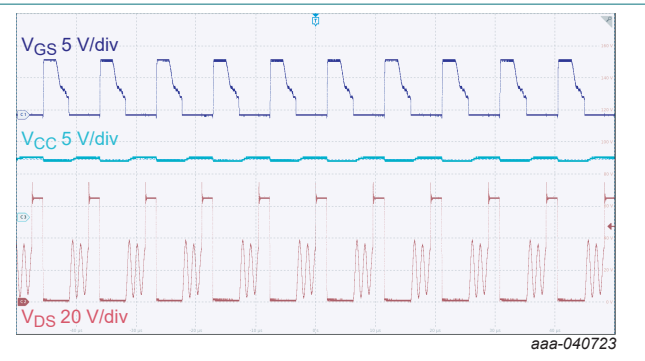
V_{IN} = 230V_{AC}, V_{OUT} = 20 V, I_{OUT} = 0.325 A
High-side, HV connected to VD

Fig. 13. Operation in 65 W flyback application



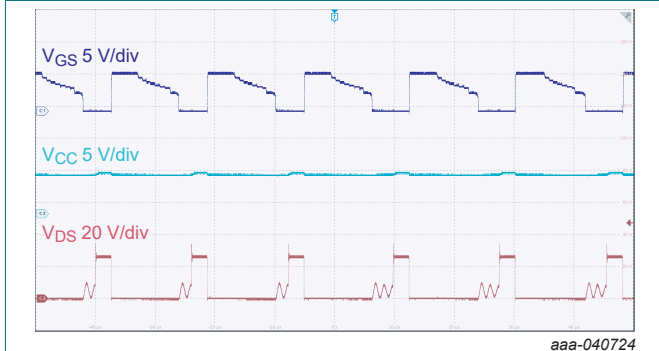
$V_{IN} = 110V_{AC}$, $V_{OUT} = 20V$, $I_{OUT} = 3.25A$
Low-side, HV connected to V+

Fig. 14. Operation in 65 W flyback application



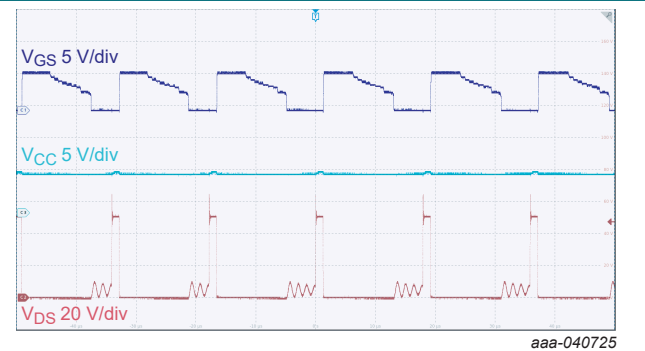
$V_{IN} = 230V_{AC}$, $V_{OUT} = 20V$, $I_{OUT} = 3.25A$
Low-side, HV connected to V+

Fig. 15. Operation in 65 W flyback application



$V_{IN} = 110V_{AC}$, $V_{OUT} = 5V$, $I_{OUT} = 3.25A$
Low-side, HV connected to V+

Fig. 16. Operation in 65 W flyback application



$V_{IN} = 230V_{AC}$, $V_{OUT} = 5V$, $I_{OUT} = 3.25A$
Low-side, HV connected to V+

Fig. 17. Operation in 65 W flyback application

9. Detailed Description

9.1. Overview

The NEX81801/2DA is designed to operate with CCM, critical conduction mode (CrM), and DCM flyback converters. The control circuitry turns on the MOSFET when the voltage on V_{DS} drops below the turn-on threshold V_{th_ON} , and turns off the MOSFET when the V_{DS} rises above the turn-off threshold V_{th_OFF} , which is typically 0 V. The IC supports both high-side and low-side SR applications.

9.2. Functional block diagram

The NEX81801/2DA functional block diagram is shown in [Fig. 18](#):

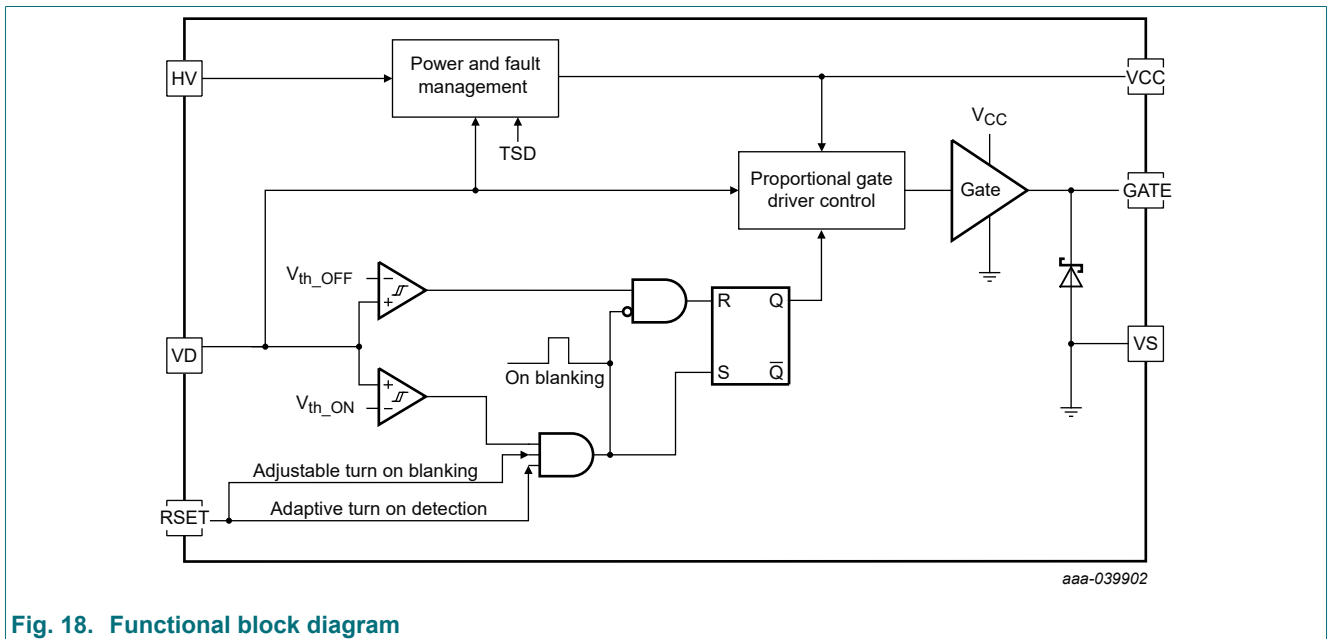


Fig. 18. Functional block diagram

9.3. Feature description

9.3.1. Supply section

When V_{CC} rises above 4.5 V, the NEX81801/2DA is enabled and exits under-voltage lockout (UVLO). When V_{CC} drops below 4.0 V, the IC enters UVLO and stops working. The UVLO hysteresis is 500 mV. A capacitor (typically 100 nF) on VCC can be used to set the startup time.

The capacitor at VCC supplies power for the IC and can be charged by both HV and VD.

If V_{HV} is less than 6.7 V, V_{CC} is regulated to 6 V.

If V_{HV} is between 6.7 V and 9.7 V, V_{CC} is regulated to $V_{HV} - 0.7$ V.

If V_{HV} is higher than 9.7 V, V_{CC} is regulated to 9 V.

9.3.2. Turn-on section

An adaptive turn-on detection circuit monitors the SR MOSFET V_{DS} waveform. Once the waveform meets the turn-on criteria, the SR MOSFET will be turned on after a turn-on delay time. In DCM operation, when the magnetizing inductor current drops to zero, an oscillation waveform can be observed at V_{DS} of SR MOSFET. Sometimes the oscillation may ring below 0 V and cause the SR MOSFET to be turned on by mistake. To prevent this, NEX81801/2DA uses a circuit with an adaptive turn-on mechanism. The shorter the SR turn-off time is, the stricter the requirement is used to turn on SR MOSFET. This prevents the MOSFET from conducting during DCM ringing.

When the circuit operates under light load conditions, the SR will turn off for a longer time, which relaxes the requirements for the SR to be turned on. By this means, the SR MOSFET can be turned on normally and the light load efficiency is improved.

9.3.3. Adjustable turn-on blanking

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on-state lasts for a predetermined length of time. The default turn-on blanking time of NEX81801DA is 1.0 μ s, which is suitable for low-frequency applications. The default turn-on blanking time of NEX81802DA is 0.5 μ s, which is suitable for high-frequency

applications. The turn-on blanking time can be adjusted by adding MLCC (C_{SET}) in parallel with R_{SET} to prevent accidental shutdown in case of excessive inductance on the lead wires of the SR MOSFET and the printed circuit board (PCB), or excessive oscillation between parasitic capacitances and transformer leakage inductance. The relationship between blanking time and C_{SET} is shown in [Table 11](#).

Table 11. NEX81801 t-blanking setting

	C_{SET}	R_{SET} (Ω)	Turn-on blanking time (ns)
NEX81801	not installed	0 Ω to 200 k Ω ; 0 Ω recommended	1.0
	1.0 nF-3.3 nF	0 Ω to 200 k Ω ; 36 k Ω recommended	1.5
	10 nF-27 nF		2.0

Table 12. NEX81802 t-blanking setting

	C_{SET}	R_{SET} (Ω)	Turn-on blanking time (ns)
NEX81802	not installed	0 Ω to 200 k Ω ; 0 Ω recommended	0.5
	1.0 nF-3.3 nF	0 Ω to 200 k Ω ; 36 k Ω recommended	1.0
	10 nF-27 nF		1.5

However, if V_{DS} reaches 1.8 V within the turn-on blanking time, V_{GS} is pulled low immediately.

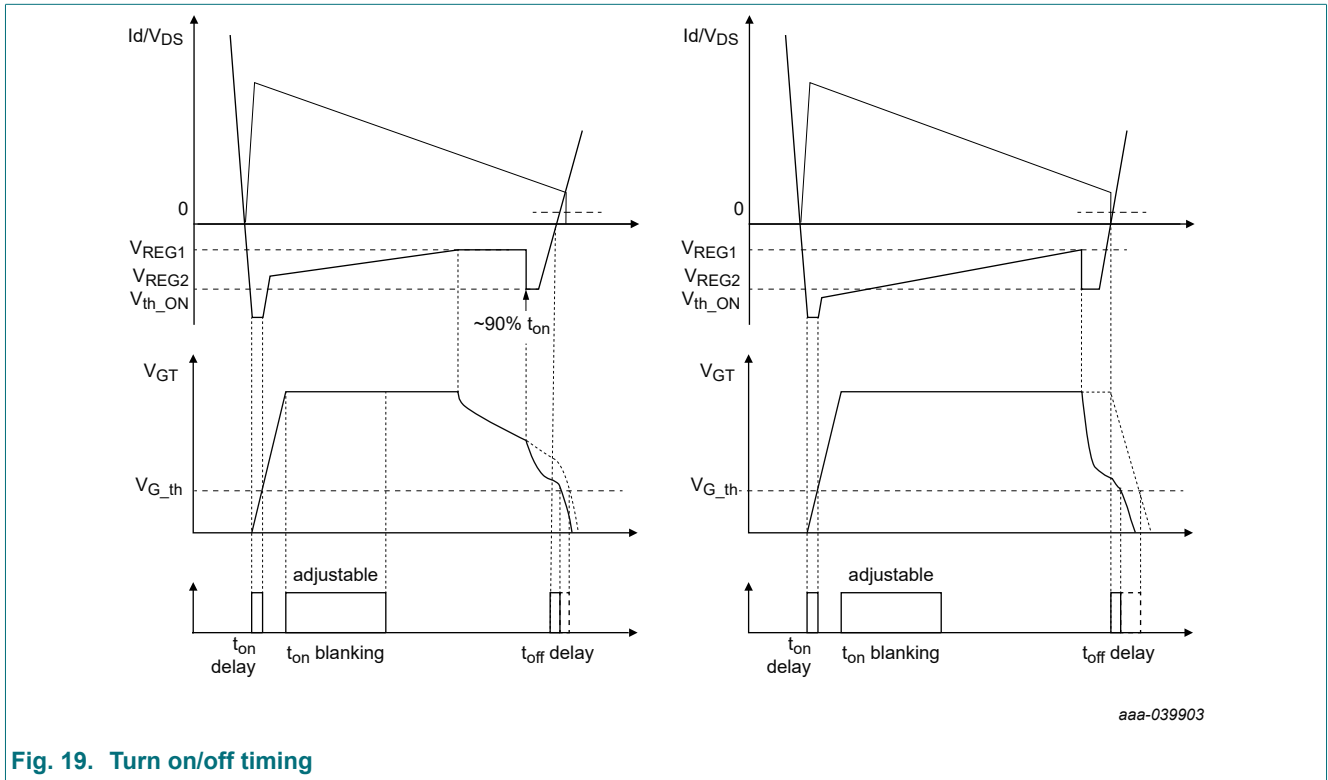


Fig. 19. Turn on/off timing

9.3.4. Conduction section

When V_{DS} rises above the first regulation step (-35mV), the gate voltage of the SR MOSFET will decrease to regulate V_{DS} to this threshold. At 90% t_{on} , NEX81801/2DA further reduces the gate voltage level to adjust V_{DS} to the second adjustment threshold (-150mV). When the V_{DS} turn off threshold is triggered, the SR MOSFET will turn off very quickly because the gate voltage is very close to the gate turn off threshold.

When the circuit operates under deep CCM conditions, or when a high $R_{DS(on)}$ MOSFET is selected, the first regulation threshold may not be triggered, but the circuit still has a chance to trigger to the second regulation threshold, thus still achieving fast turn off speed.

9.3.5. Turn-off section

The turn-off threshold is triggered when V_{DS} rises to 0 mV. Adaptive regulation control pulls the gate driver voltage (V_{GS}) to 0 mV after a very short 10 ns turn-off delay. When V_{GS} is pulled to 0 mV, a turn-off blanking time is applied, during which the gate driver signal is latched off. The turn-off blanking is removed when V_{DS} rises above 1.8 V.

10. Application Information

10.1. Application information

The following section discusses the external components required to complete the power supply design for several input and output voltage options, using the typical applications as a reference.

10.2. Typical system implementation

The NEX81801/2DA can support both high-side and low-side applications.

Fig. 20 shows the typical low-side implementation with standard level MOSFET. In this situation, V_{CC} is regulated to $V_{HV} - 0.7$ V. The maximum value of V_{CC} is 9 V.

Fig. 21 shows the typical low-side implementation with logic level MOSFET; V_{CC} is regulated to 6 V.

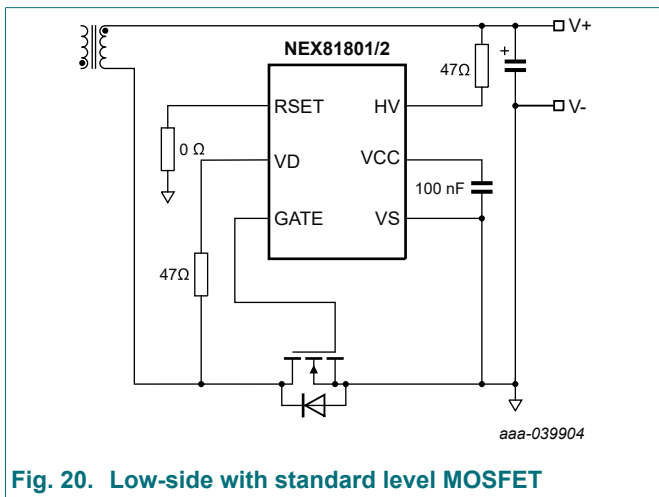


Fig. 20. Low-side with standard level MOSFET

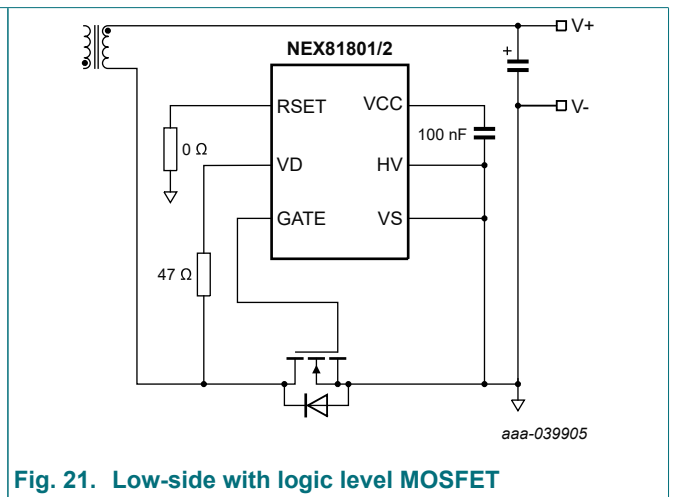


Fig. 21. Low-side with logic level MOSFET

Fig. 22 shows the typical high-side implementation with standard level MOSFET; V_{CC} is regulated to 9 V.

Fig. 23 shows the typical high-side implementation with standard level MOSFET, high voltage output; V_{CC} is regulated to 9 V (suitable for high voltage output applications).

Fig. 24 shows the typical high-side implementation with logic level MOSFET; V_{CC} is regulated to 6 V.

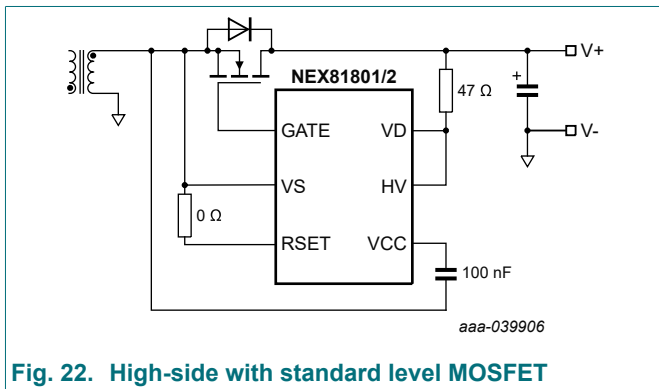


Fig. 22. High-side with standard level MOSFET

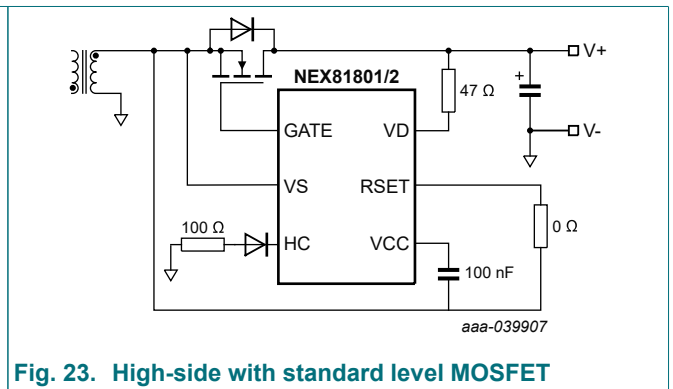


Fig. 23. High-side with standard level MOSFET

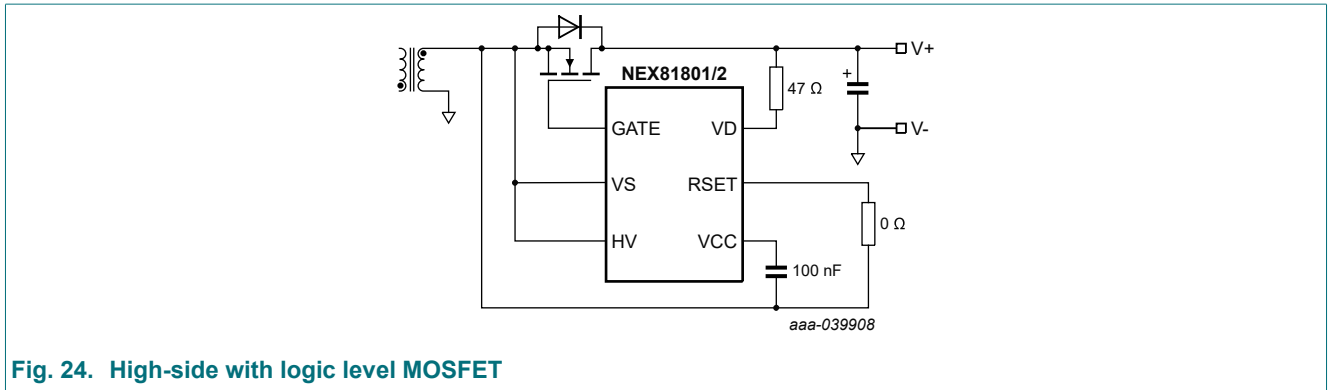


Fig. 24. High-side with logic level MOSFET

10.3. External resistor selection

To prevent high negative voltage on the VD and HV pins from damaging the device, an external resistor needs to be in series to VD and HV. The resistor can also protect the IC from ESD damage. Generally, a resistance between 10-100 Ω is recommended.

The adaptive turn-on mechanism means that RSET can directly short to GND, to better prevent the circuit from misconducting by DCM ringing. The resistance is recommended to be less than 200 k Ω .

10.4. External capacitor selection

Normally, a capacitor with a range of 100 nF to 1 μ F is needed to connect between VCC and GND. Larger VCC capacitance leads to longer start up time and larger V_{DS} spike; 100 nF or 220 nF is recommended as the VCC UVLO hysteresis 500 mV is big enough to cover the larger ripple on V_{CC} .

R_{SET} is recommended to be higher than 30 k Ω if C_{SET} is placed. For C_{SET} values, see [Table 11](#).

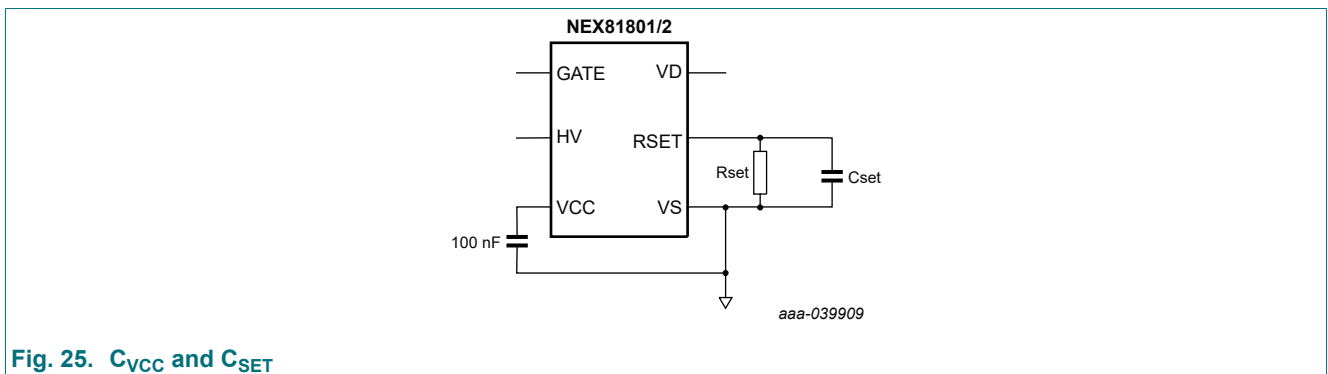


Fig. 25. C_{VCC} and C_{SET}

11. Layout

1. Make the sensing connection (VD/VS) as close as possible to the MOSFET (drain/source).
2. Make the sensing loop as small as possible. Keep the IC out of the power loop to avoid interference between the sensing loop and the power loop.
3. Place a decoupling ceramic capacitor from VCC to GND close to the IC for adequate filtering.
4. Make the gate driver loop as small as possible to minimize the parasitic inductance.
5. Keep the driver signal far away from the VD sensing trace on the layout.

12. Package outline

Plastic, surface-mounted package (TSOT23-6); 6 leads

SOT8061-1

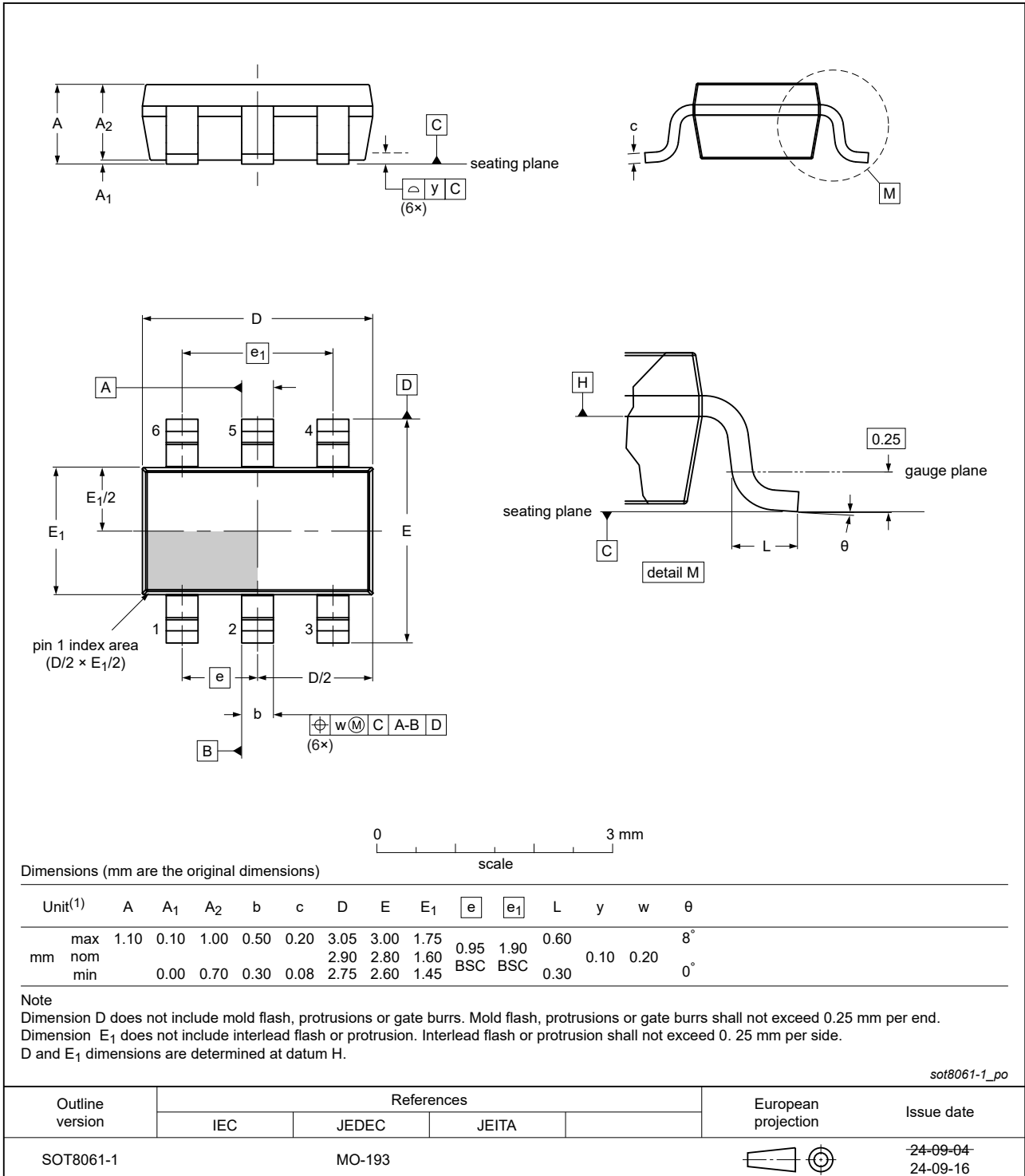


Fig. 26. Package outline SOT8061-1 (TSOT23-6)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
AC	Alternating Current
ANSI	American National Standards Institute
CCM	Continuous Conduction Mode
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CrM	Critical conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
FC	Flip Chip
HBM	Human Body Model
HV	High Voltage
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
QR	Quasi-resonant
SMPS	Switched-Mode Power Supply
SR	Synchronous Rectification
TTL	Transistor-Transistor Logic
USB	Universal Serial Bus
UVLO	Under-Voltage LockOut

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX81801/2DA v.1	20240930	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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