MPQ2179B

6V, 3A, 710kHz, Synchronous Step-Down Converter with PG and SS, AEC-Q100 Qualified

DESCRIPTION

The MPQ2179B is a monolithic, step-down switch-mode converter with built-in internal power MOSFETs. The device achieves up to 3A of continuous output current (I_{OUT}) across a 2.5V to 6V input voltage (V_{IN}) range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.5V.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MPQ2179B is ideal for a wide range of applications, including automotive infotainment systems, clusters, and telematics.

The MPQ2179B requires a minimal number of readily available, standard external components, and is available in an ultra-small QFN-8 (1.5mmx2mm) package.

FEATURES

- Designed for Automotive Applications
  - Wide 2.5V to 6V Operating Input Voltage (V_{IN}) Range
  - Up to 3A Output Current (I_{OUT})
  - Output Adjustable from 0.5V
  - 1% Feedback (FB) Accuracy
  - -40°C to +150°C Operating Junction Temperature (T_J)
  - Available in AEC-Q100 Grade 1
- High Performance for Improved Thermals
  - 65mΩ and 35mΩ Internal Power MOSFETs
- Optimized for EMC and EMI Reduction
  - 710kHz Switching Frequency (f_{SW})
  - Forced Continuous Conduction Mode (FCCM) across the Entire Load Range
  - MeshConnect™ Flip-Chip Package

FEATURES *(continued)*

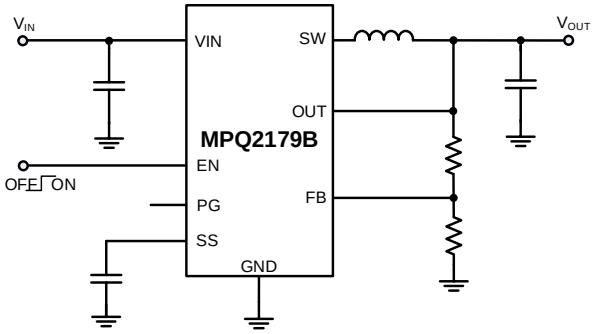
- Optimized for Board Size and BOM
  - Built-in Internal Power MOSFETs
  - Integrated Compensation Network
- Additional Features
  - Enable (EN) for Power Sequencing
  - 100% Duty Cycle
  - Output Discharge
  - Power Good (PG)
  - External Soft Start (SS)
  - Output Over-Voltage Protection (OVP)
  - Short-Circuit Protection (SCP) with Hiccup Mode
  - Available in a QFN-8 (1.5mmx2mm) Package
  - Available in a Wettable Flank Package
- Functional Safety System Design Capable
  - MPSafe™ QM (Documentation Available)

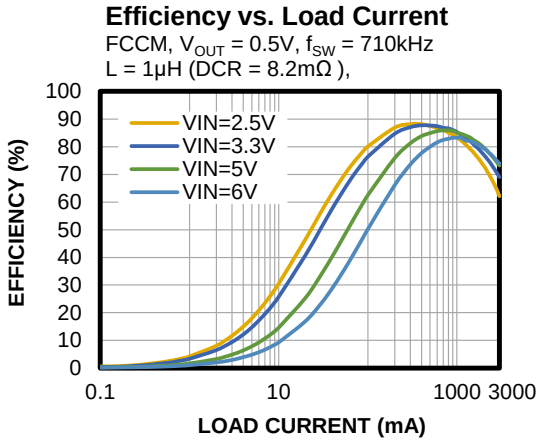
MPSafe™ QM

APPLICATIONS

- Automotive Infotainment Systems
- Camera Modules
- Key Fobs
- Automotive Clusters
- Automotive Telematics
- Industrial Supplies
- Battery-Powered Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2179BGQHE-AEC1***	QFN-8 (1.5mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ2179BGQHE-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

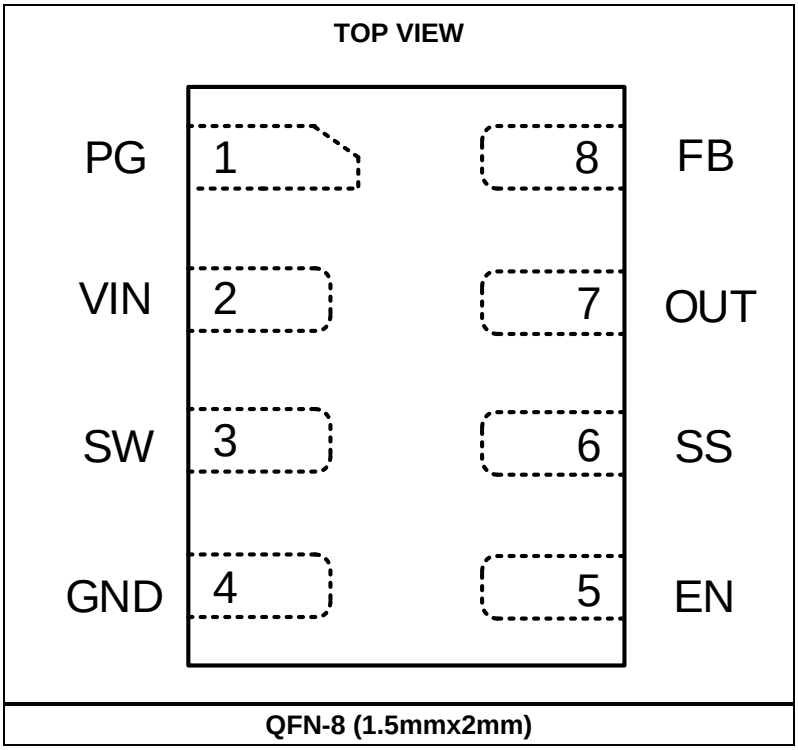
TOP MARKING

$\overline{\text{NX}}$

LL

NX: Product code of MPQ2179BGQHE-AEC1
LL: Lot number

PACKAGE REFERENCE



QFN-8 (1.5mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good indicator.** The PG pin is an open-drain output. Connect PG to a voltage source using an external resistor. PG is pulled high when the feedback (FB) voltage (V_{FB}) exceeds 90% of the reference voltage (V_{REF}). PG is pulled low to GND if V_{FB} drops below 84% of V_{REF}. Float PG if it is not used.
2	VIN	**Input voltage.** The MPQ2179B operates from a 2.5V to 6V input voltage (V_{IN}) range. Use a decoupling capacitor to prevent large voltage spikes from appearing at the input.
3	SW	**Output switching node.** The SW pin is the drain of the internal P-channel high-side MOSFET (HS-FET). Connect an inductor to SW to complete the converter.
4	GND	**Ground.**
5	EN	**Enable control.** Pull the EN pin above the rising threshold (0.9V) to turn the converter on; pull EN below the falling threshold (0.65V) to turn it off. There is an internal 2MΩ resistor connected from the EN pin to ground.
6	SS	**Soft start.** Connect a capacitor from SS to GND to set the soft-stat time (t_{SS}) and avoid start-up inrush current. It is recommended that the soft-start capacitor (C_{SS}) to be ≥6.8nF.
7	OUT	**Output voltage.** The OUT pin is the power rail and input sense for the output voltage (V_{OUT}). Connect the load to this pin. Use an output capacitor to reduce the V_{OUT} ripple (ΔV_{OUT}).
8	FB	**Feedback pin.** An external resistor divider tapped to the FB pin should be connected from the output to GND. V_{FB} is compared to the internal V_{REF} (0.5V) to set the regulation voltage.

ABSOLUTE MAXIMUM RATINGS (1)

SW .....-0.3V (-1.5V for <10ns) to +6.5V (7.5V for <10ns)
All other pins .....-0.3V to +6.5V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2) (6) 2.2W
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (3)
Charged-device model (CDM) .....Class 2b (4)

Recommended Operating Conditions

Input voltage (V_{IN}) .....2.5V to 6V
Output voltage (V_{OUT}).....0.5V to V_{IN} - 0.5V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-8 (1.5mmx2mm)		
JESD51-7 (5).....	130.....	25....°C/W
EVQ2179B-QH-00A (6).....	59.....	14....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from the junction-to-case bottom.
6) Measured on an MPS standard EVB: 6.3cmx6.3cm, 2oz. copper thickness, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from the junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage (V_{IN}) range			2.5		6	V
Under-voltage lockout (UVLO) rising threshold				2.3	2.45	V
UVLO hysteresis				200		mV
Shutdown supply current		V_{EN} = 0V, T_J = 25°C		0.01	1	µA
		V_{EN} = 0V, T_J = -40°C to +125°C (8)			3	µA
		V_{EN} = 0V, T_J = -40°C to +150°C			20	µA
Quiescent supply current		V_{EN} = 2V, V_{FB} = 0.525V, V_{IN} = 3.6V		462.5	652.5	µA
Feedback (FB) voltage	V_{FB}	T_J = 25°C	495	500	505	mV
		T_J = -40°C to +150°C	492.5	500	507.5	mV
FB current	I_{FB}	V_{FB} = 0.525V		50	100	nA
P-channel MOSFET on resistance	$R_{DS(ON)\_P}$	V_{IN} = 5V		65	85	mΩ
N-channel MOSFET on resistance	$R_{DS(ON)\_N}$	V_{IN} = 5V		35	55	mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = 25°C		0	1	µA
		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = -40°C to +125°C (8)			30	µA
Switching frequency	f_{SW}	V_{IN} = 5V, V_{OUT} = 1.2V, continuous conduction mode (CCM)	550	710	850	kHz
Minimum on time (8)	t_{MIN_ON}	V_{IN} = 5V		71		ns
Minimum off time (8)	t_{MIN_OFF}	V_{IN} = 5V		80		ns
P-channel MOSFET peak current limit (I_{LIMIT})			4	5	6	A
N-channel MOSFET valley I_{LIMIT}			1.5	3	4.5	A
Soft-start current	I_{SS}		13.1	15	18.7	µA
Maximum duty cycle				100		%
Power good (PG) under-voltage (UV) rising threshold		FB rising edge	87	90	93	% of V_{REF}
PG UV falling threshold		FB falling edge	80	84	88	% of V_{REF}
PG delay	t_{PGD}	PG rising/falling edge		70		µs
PG sink current capability	V_{PG_SINK}	Sink 1mA			0.4	V
PG logic high voltage	V_{PG_HIGH}	V_{IN} = 5V, V_{FB} = 0.5V	4.9			V
Self-bias PG (7)					0.7	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG leakage current/logic high		5V logic high			100	nA
Enable (EN_ turn-on delay		EN on to SW active		100		µs
EN turn-off delay		EN off to stop switching		11		µs
EN input logic low voltage			0.4	0.65		V
EN input logic high voltage				0.9	1.2	V
EN pull-down resistance				2		MΩ
Output discharge resistance	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		120		Ω
EN input current		V_{EN} = 2V		1.2		µA
		V_{EN} = 0V		0		µA
Output over-voltage protection (OVP) rising threshold	V_{OVP}		111	116	121	% of V_{FB}
Output OVP hysteresis	V_{OVP_HYS}			8		% of V_{FB}
Output OVP delay				2		µs
Low-side MOSFET (LS-FET) I_{LIMIT}		Current flowing from SW to GND		1.2		A
Absolute V_{IN} OVP		After V_{OUT} OVP is enabled		6.1		V
Absolute V_{IN} OVP hysteresis				160		mV
Thermal shutdown (8)				170		°C
Thermal shutdown hysteresis (8)				20		°C

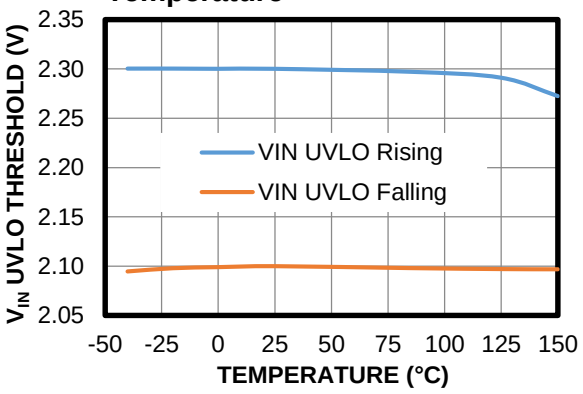
Notes:

7) If V_{IN} = 0V and V_{EN} = 0V, then PG is pulled up between 3V and 6V using a 100kΩ resistor.
8) Guaranteed by design and bench characterization. Not tested in production.

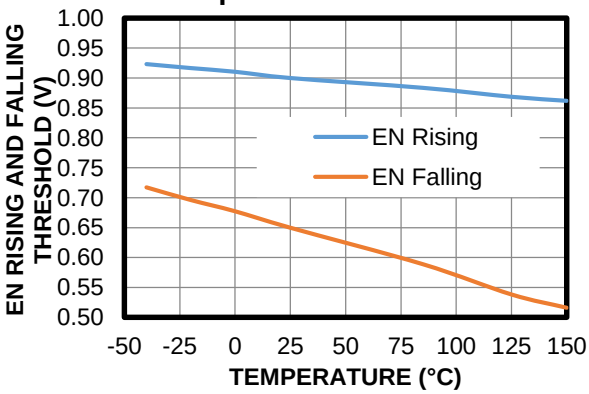
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

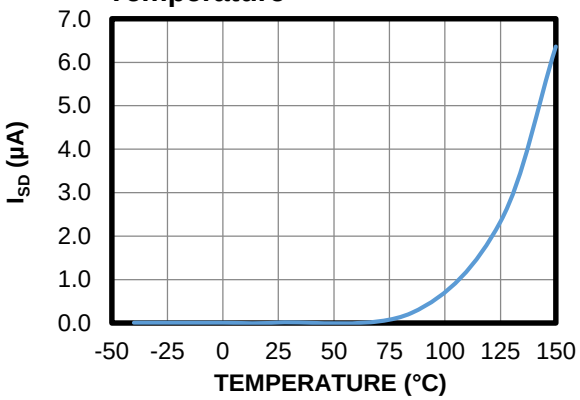
V_{IN} UVLO Threshold vs. Temperature



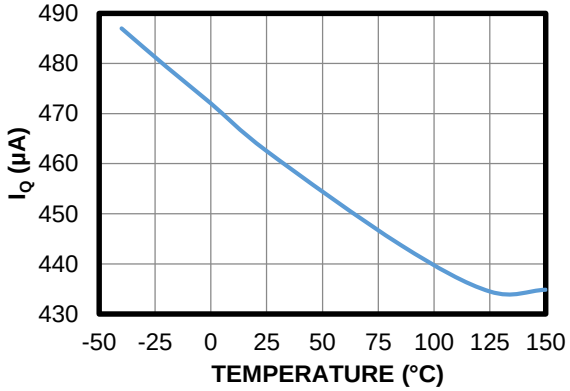
EN Rising and Falling Threshold vs. Temperature



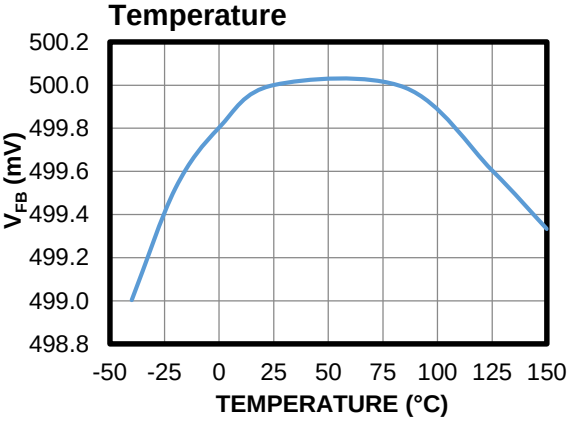
Shutdown Current vs. Temperature



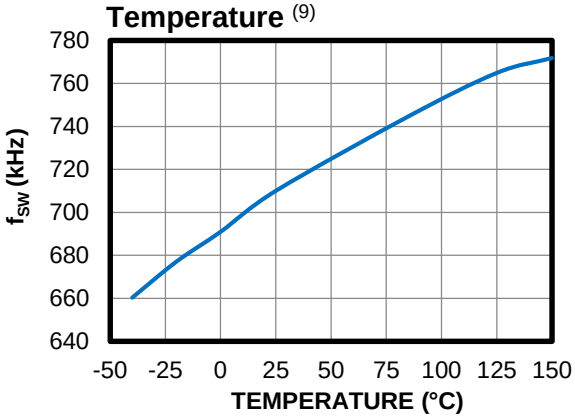
Quiescent Current vs. Temperature



Feedback Voltage vs. Temperature



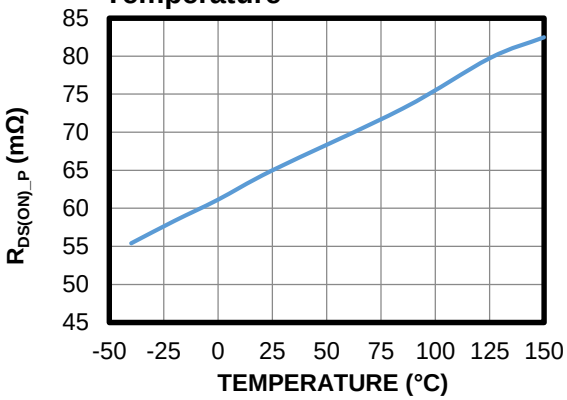
Switching Frequency vs. Temperature (9)



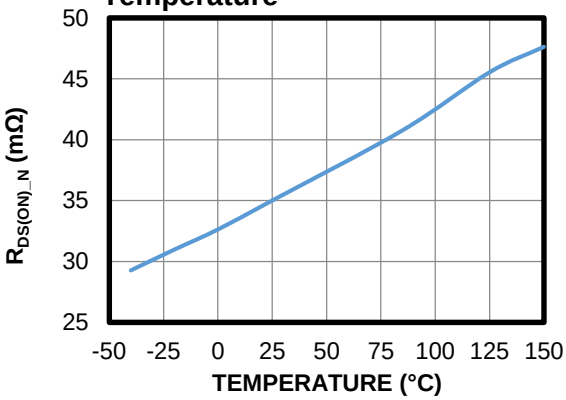
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

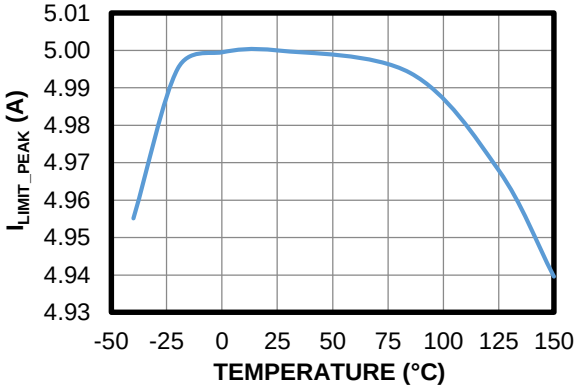
P-Channel MOSFET On Resistance vs. Temperature (9)



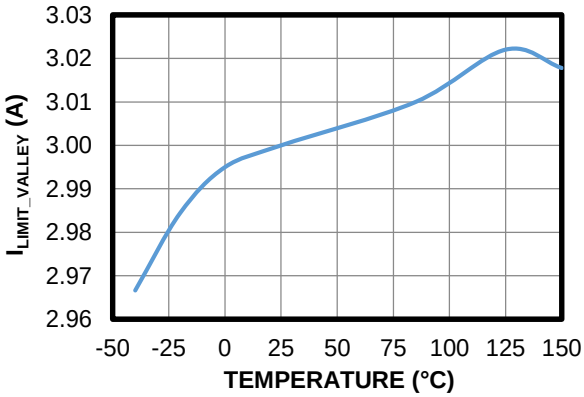
N-Channel MOSFET On Resistance vs. Temperature (9)



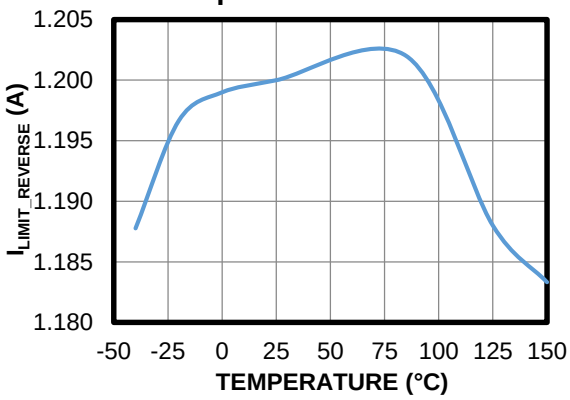
P-Channel MOSFET Peak Current Limit vs. Temperature



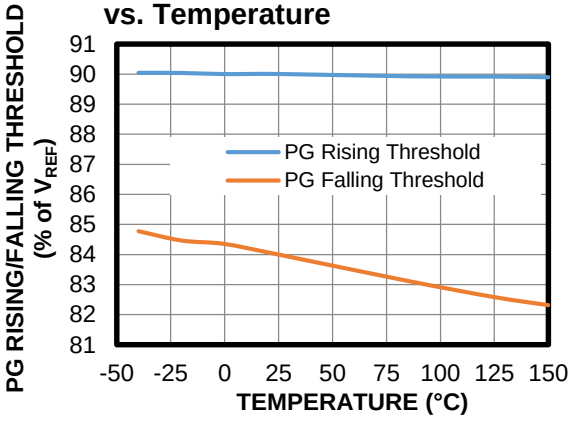
N-Channel MOSFET Valley Current Limit vs. Temperature



Low-Side Reverse Current Limit vs. Temperature



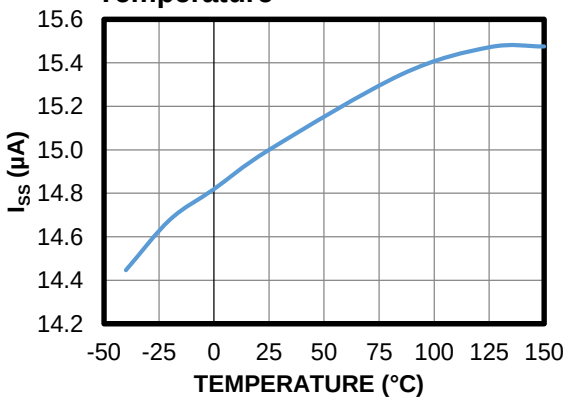
PG Rising and Falling Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

Soft-Start Current vs. Temperature



Note:

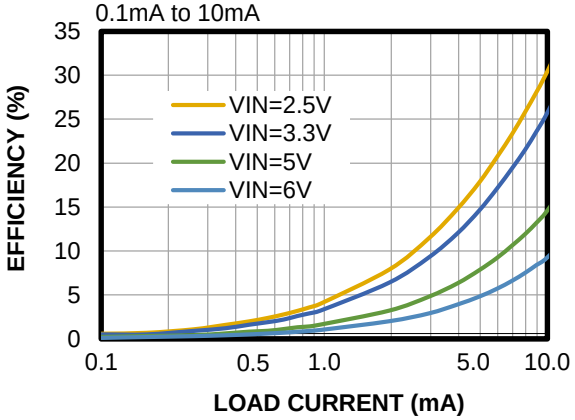
9) This test item is evaluated at V_{IN} = 5V.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 0.5V, L = 1µH, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

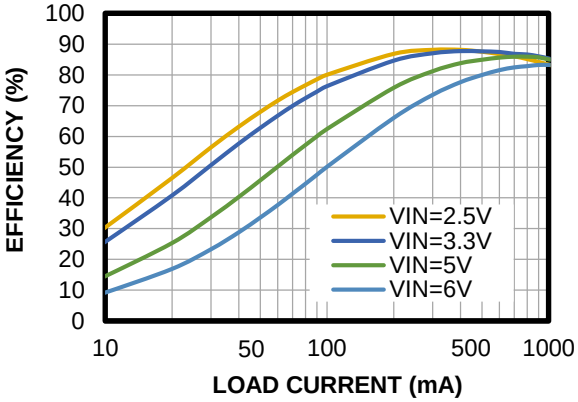
Efficiency vs. Load Current

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ),
0.1mA to 10mA



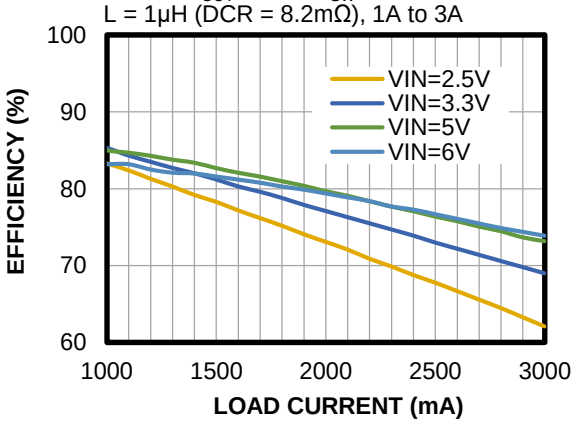
Efficiency vs. Load Current

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ),
10mA to 1000mA



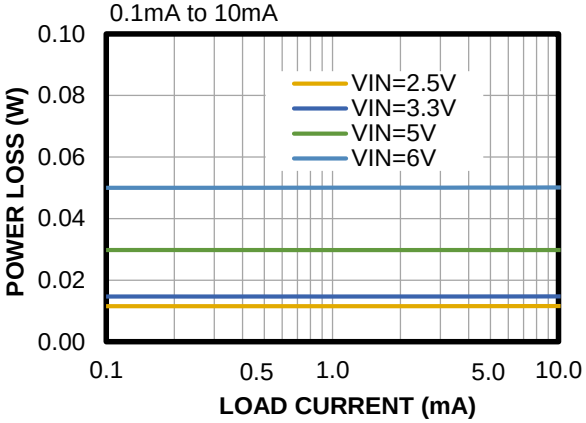
Efficiency vs. Load Current

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ), 1A to 3A



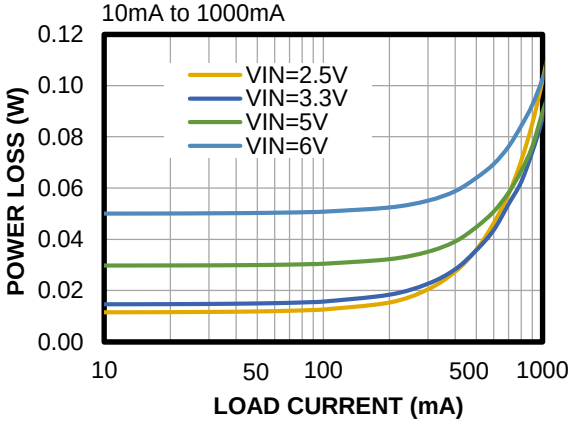
Power Loss vs. Load Current

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ),
0.1mA to 10mA



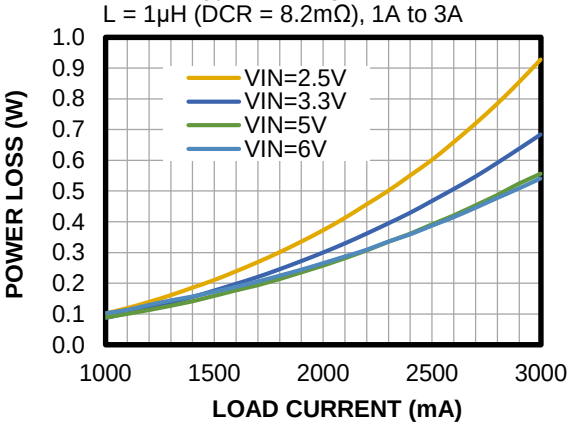
Power Loss vs. Load Current

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ),
10mA to 1000mA



Power Loss vs. Load Current

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ), 1A to 3A

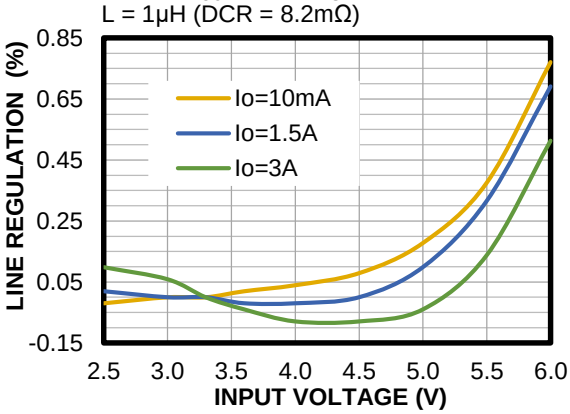


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 0.5V, L = 1µH, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

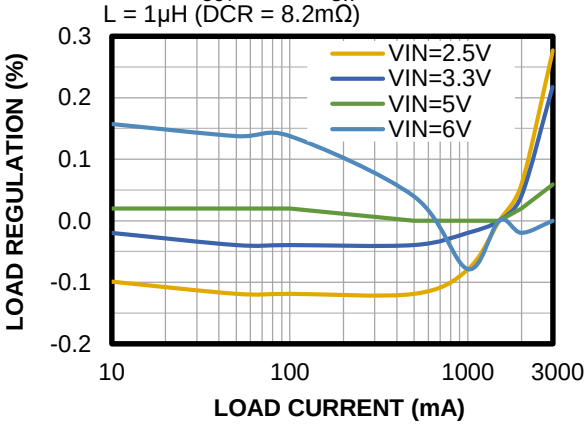
Line Regulation

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ)



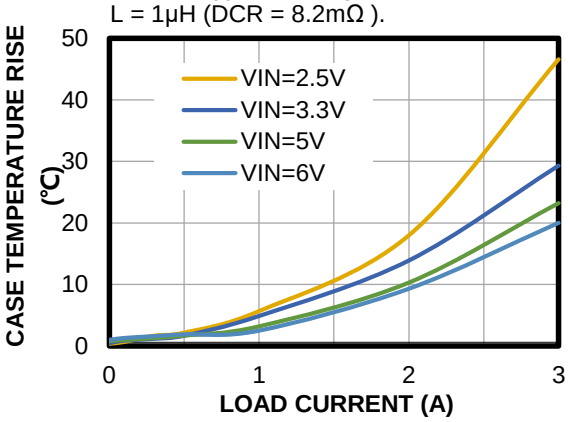
Load Regulation

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ)



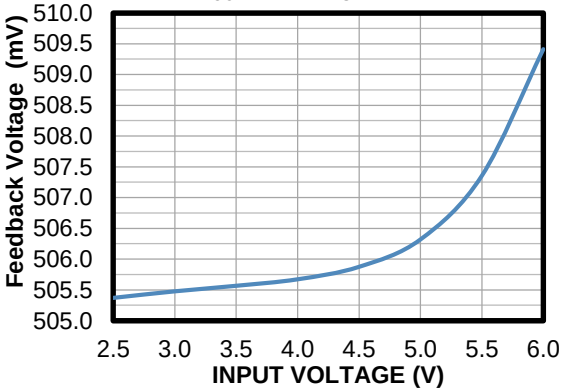
Case Temperature Rise

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz
L = 1µH (DCR = 8.2mΩ).



Feedback Voltage vs. Input Voltage

FCCM, V_{OUT} = 0.5V, f_{SW} = 710kHz

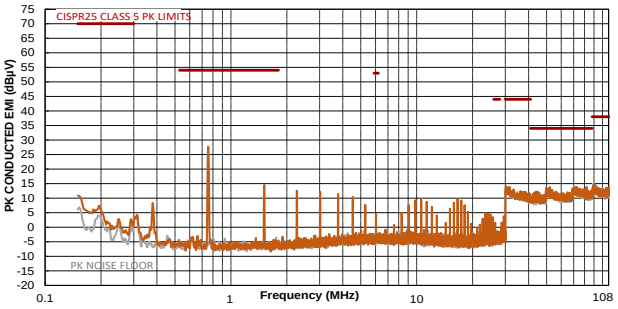


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 0.5V, L = 1µH (10), C_{OUT} = 2 x 22µF, I_{OUT} = 3A, T_A = 25°C, unless otherwise noted. (11)

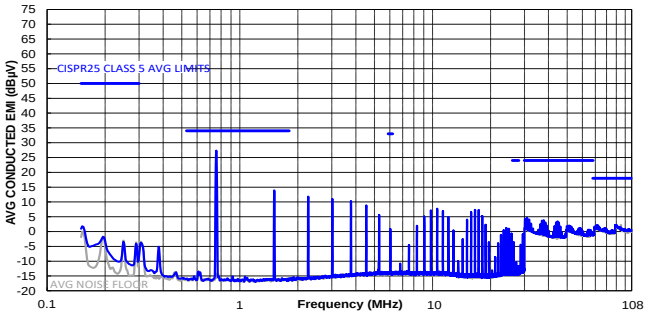
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



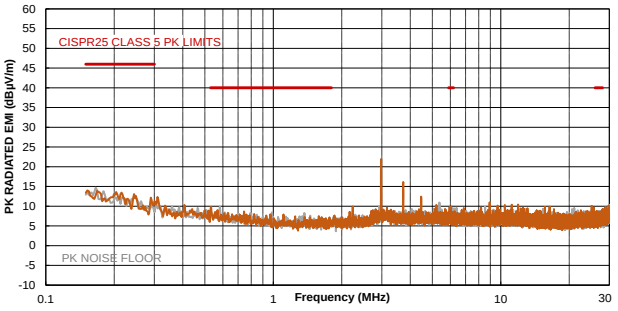
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



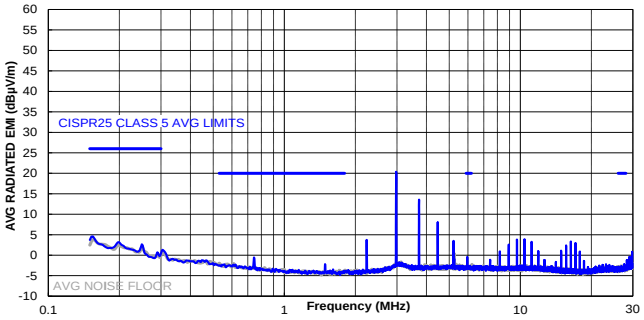
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



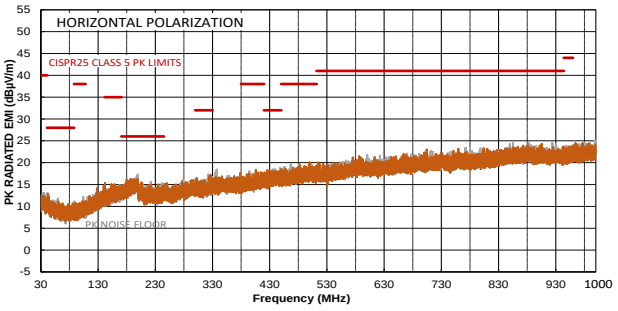
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



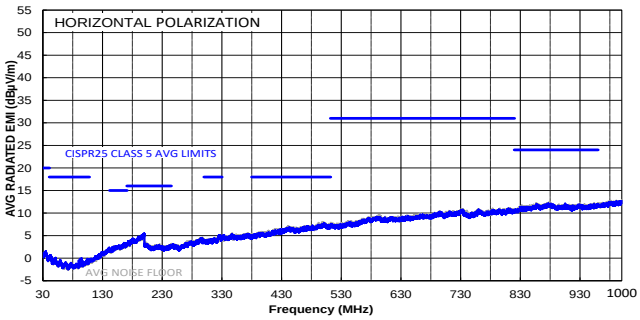
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

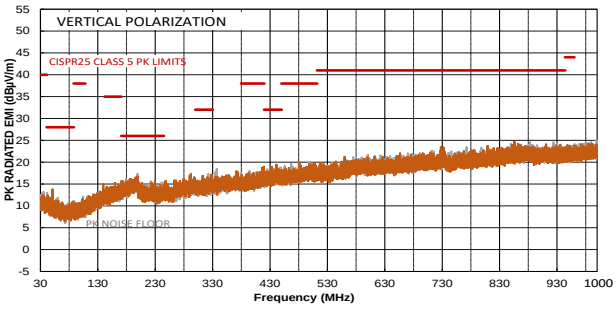


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 0.5V, L = 1µH (10), C_{OUT} = 2 x 22µF, I_{OUT} = 3A, T_A = 25°C, unless otherwise noted. (11)

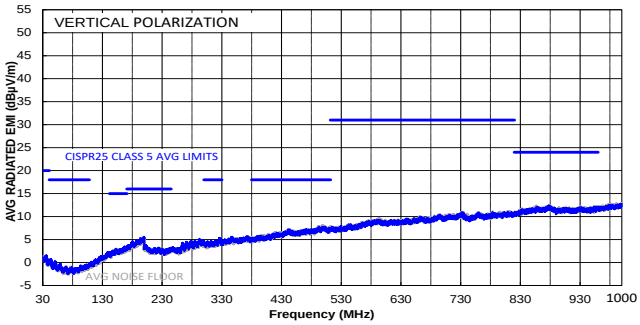
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

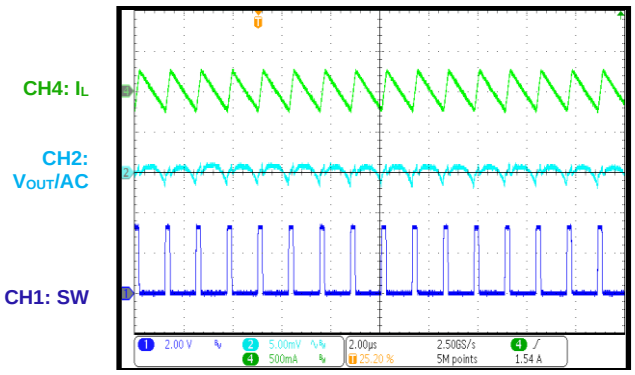
10) Inductor part number: XGL4020-102MEB. DCR = 8.2mΩ.

11) The EMC test results are based on the typical application circuit with EMI filters (see Figure 8 on page 26).

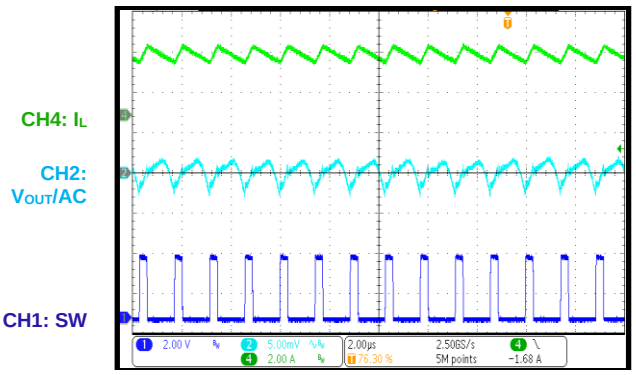
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 0.5V, L = 1µH, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

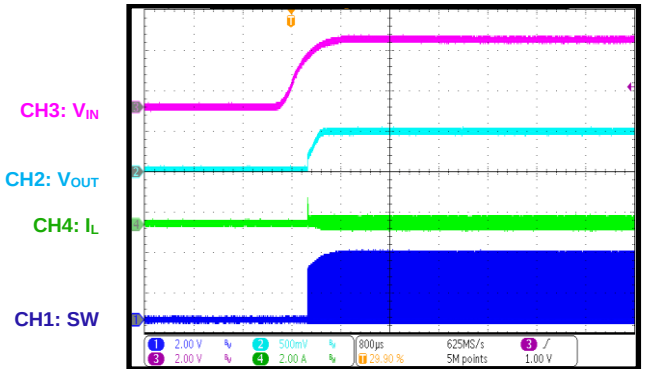
Steady State
I_{OUT} = 0A, FCCM



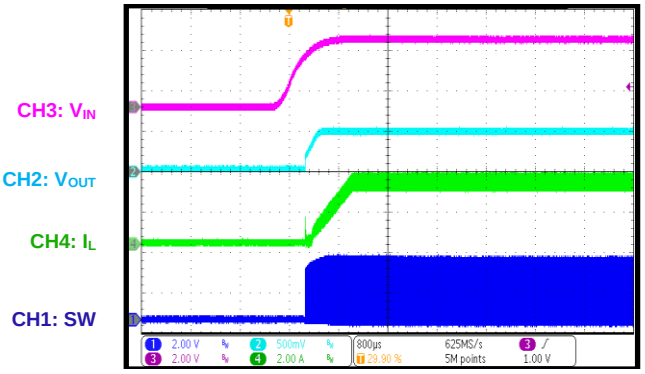
Steady State
I_{OUT} = 3A



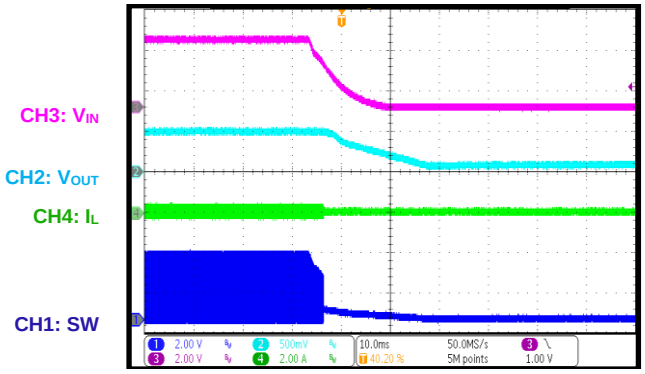
Start-Up through VIN
I_{OUT} = 0A, FCCM



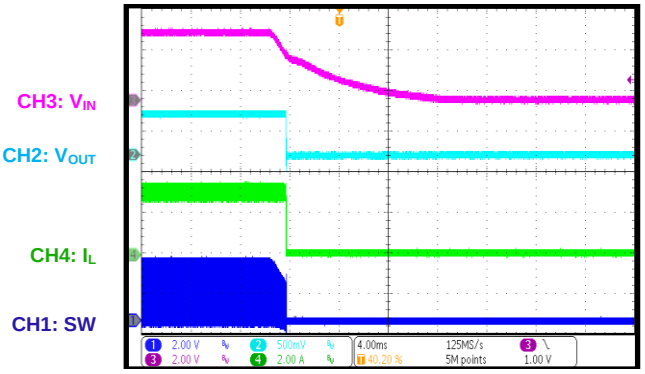
Start-Up through VIN
I_{OUT} = 3A



Shutdown through VIN
I_{OUT} = 0A, FCCM



Shutdown through VIN
I_{OUT} = 3A

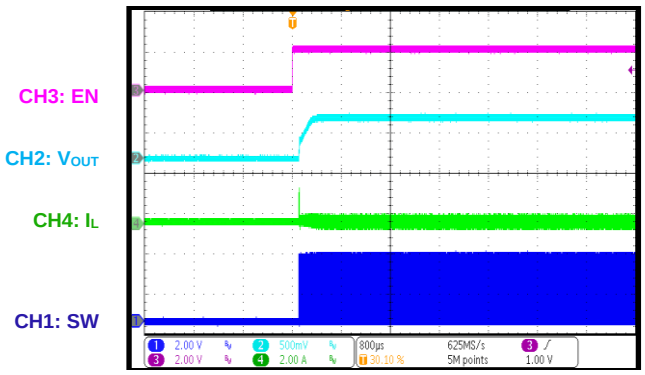


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 0.5V, L = 1µH, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

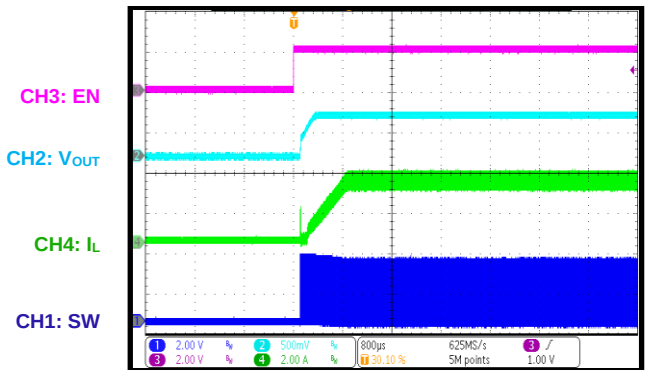
Start-Up through EN

I_{OUT} = 0A, FCCM



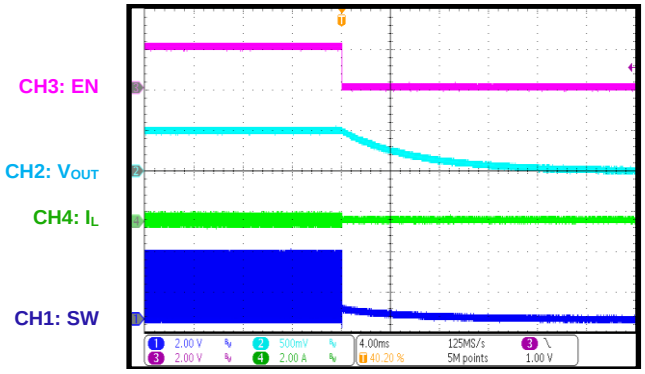
Start-Up through EN

I_{OUT} = 3A



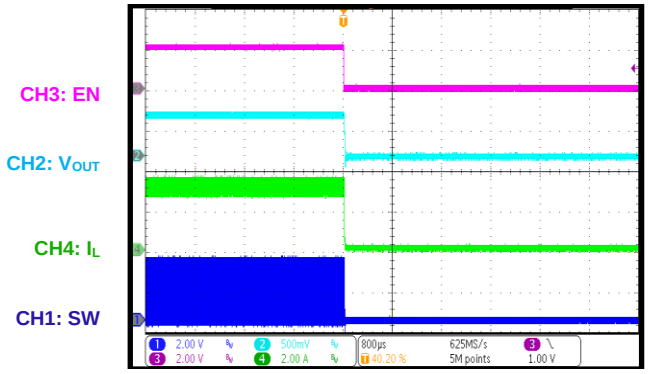
Shutdown through EN

I_{OUT} = 0A, FCCM



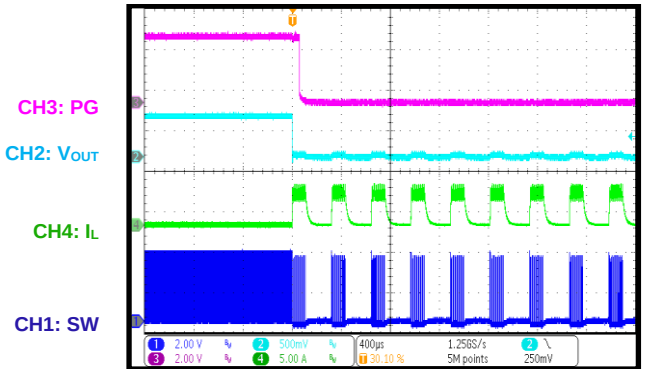
Shutdown through EN

I_{OUT} = 3A



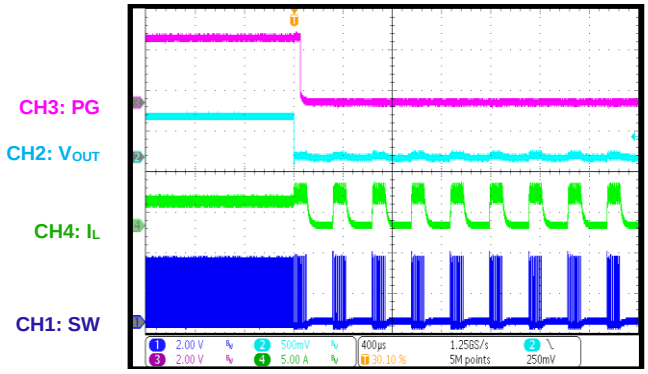
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

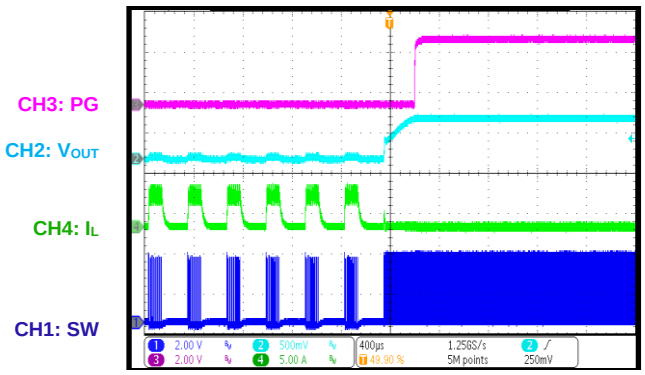
I_{OUT} = 3A



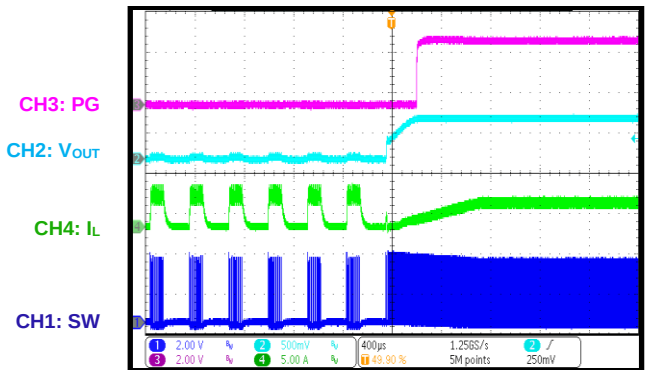
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 0.5V, L = 1µH, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

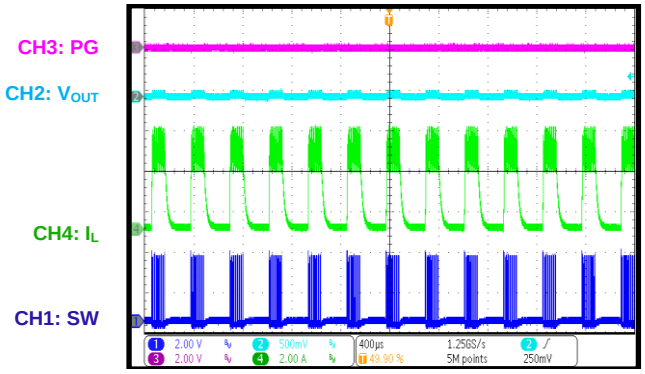
SCP Recovery
I_{OUT} = 0A, FCCM



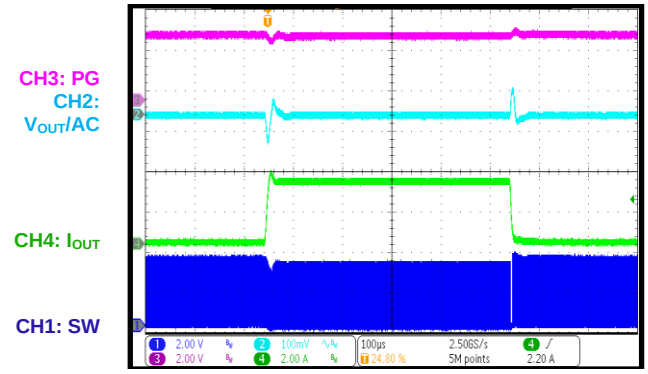
SCP Recovery
I_{OUT} = 3A



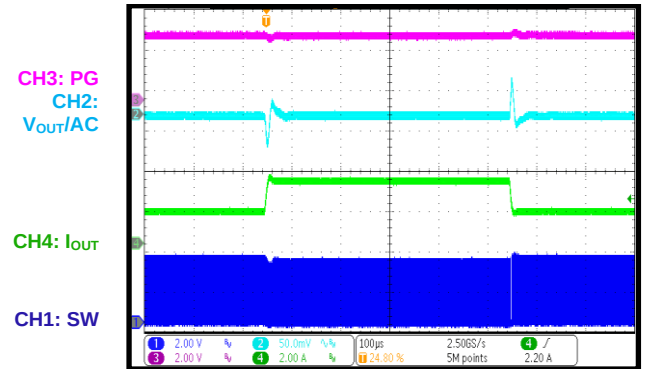
SCP Steady State



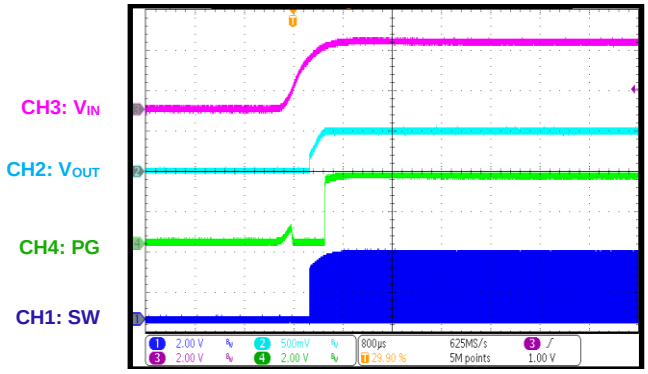
Load Transient
I_{OUT} = 0A to 3A, 1.6A/µs



Load Transient
I_{OUT} = 1.5A to 3A, 1.6A/µs



PG Start-Up through VIN
I_{OUT} = 0A, FCCM

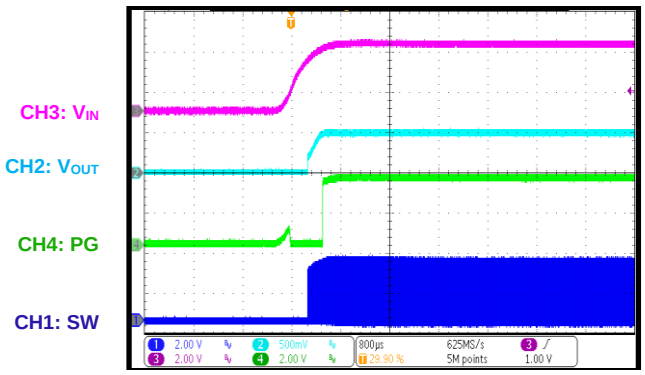


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 0.5V, L = 1µH, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

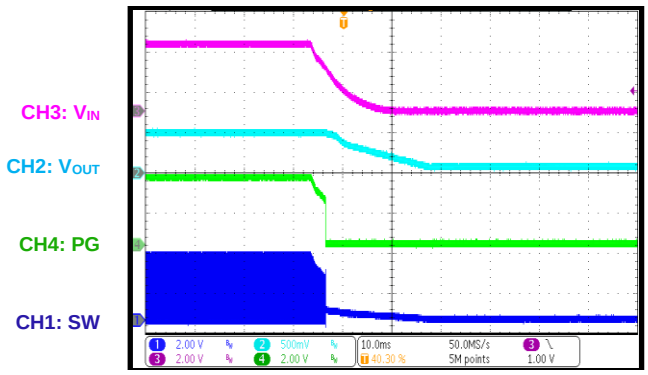
PG Start-Up through VIN

I_{OUT} = 3A



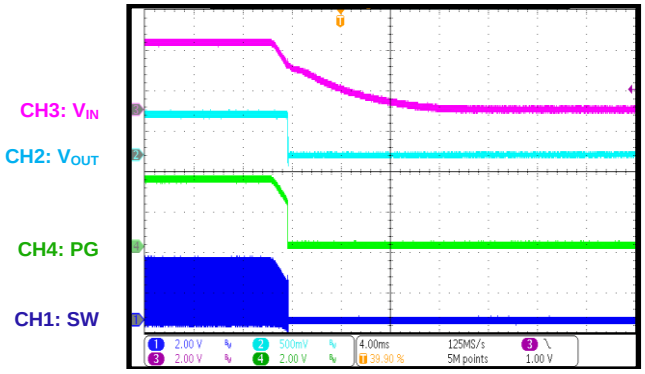
PG Shutdown through VIN

I_{OUT} = 0A, FCCM



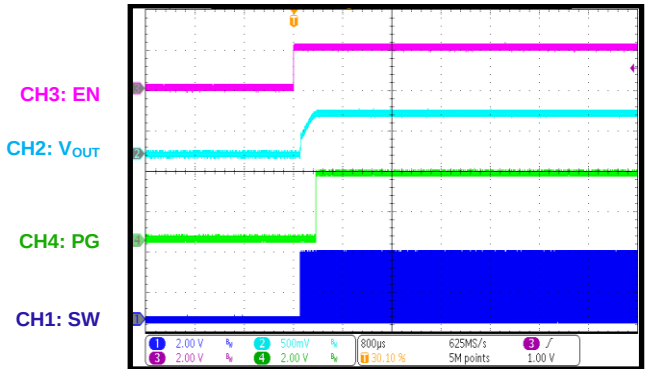
PG Shutdown through VIN

I_{OUT} = 3A



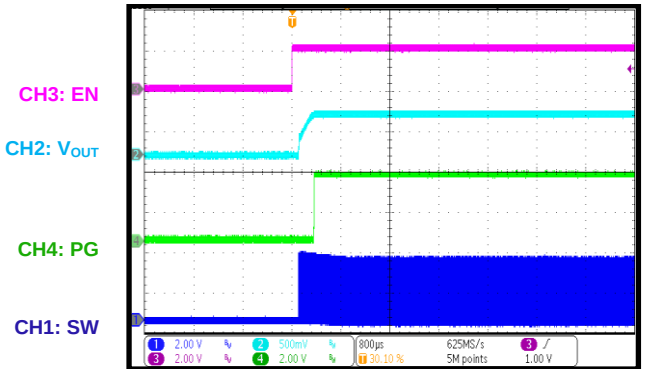
PG Start-Up through EN

I_{OUT} = 0A, FCCM



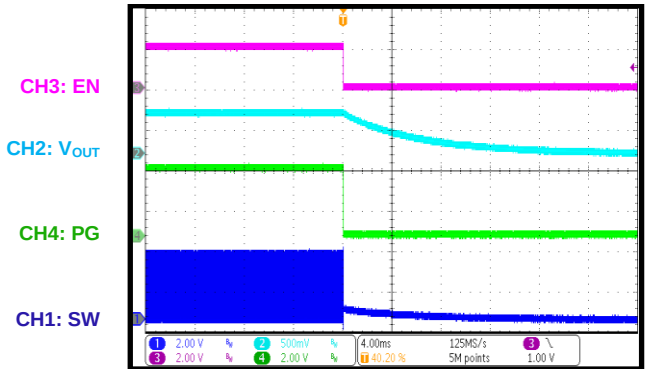
PG Start-Up through EN

I_{OUT} = 3A



PG Shutdown through EN

I_{OUT} = 0A, FCCM

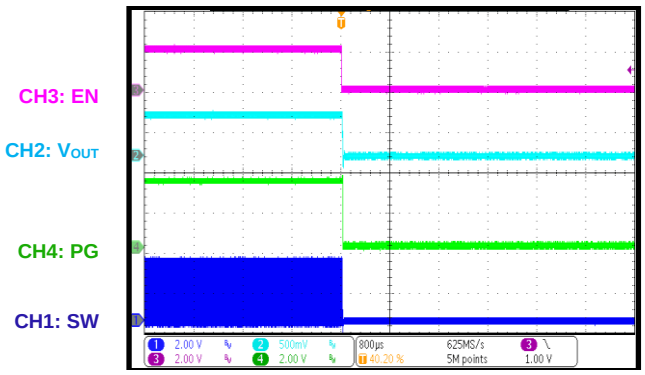


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 0.5V, L = 1µH, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

PG Shutdown through EN

I_{OUT} = 3A



FUNCTIONAL BLOCK DIAGRAM

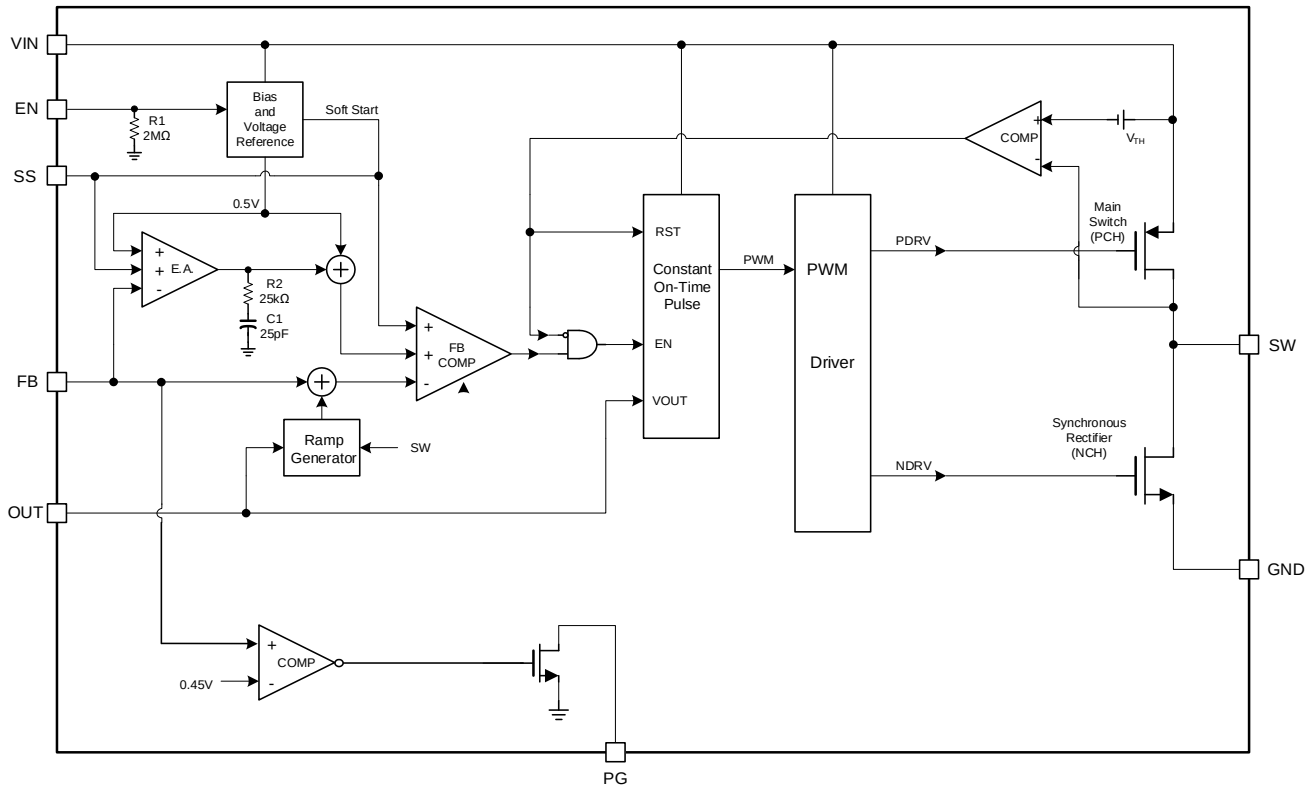


Figure 1: Functional Block Diagram

OPERATION

The MPQ2179B employs constant-on-time (COT) control with input voltage (V_{IN}) feed-forward to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. The device achieves up to 3A of peak output current (I_{OUT}) across the 2.5V to 6V V_{IN} range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.5V. A 100% maximum duty cycle can be reached in dropout.

Constant-On-Time (COT) Control

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers a simpler control loop and faster transient response. To prevent inductor current (I_L) runaway during load transient, the MPQ2179B switching cycles have a fixed minimum off time (t_{OFF_MIN}). The low-side MOSFET (LS-FET) turns on and remains on for at least t_{MIN_OFF}. Then the high-side MOSFET (HS-FET) turns on when the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}). This indicates an insufficient V_{OUT}. V_{IN} feed-forward allows the MPQ2179B to maintain a nearly constant f_{SW} across the input and load ranges. The switching pulse on time (t_{ON}) can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 1400ns \quad (1)$$

To improve frequency stability and reduce V_{OUT} ripple (ΔV_{OUT}), the part operates in forced continuous conduction mode (FCCM).

Enable (EN)

EN is a digital control pin that turns the converter on and off. Pull EN above the rising threshold (0.9V) to turn the converter on; pull EN below the falling threshold (0.65V) to turn it off. Leave EN floating or pull it down to ground to disable the MPQ2179B. There is an internal 2MΩ resistor connected from the EN pin to ground.

Output Discharge

When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET provides a resistive discharge path for the output capacitor (C_{OUT}) between the OUT pin and GND. To block the output discharge path, add an external capacitor between the output and the OUT pin (see the Output Discharge Blocking section on page 24).

Soft Start (SS)

The MPQ2179B has an external soft start (SS) pin that ramps up V_{OUT} at a controlled slew rate to avoid overshoot during start-up. The SS pin's charge current is typically 15μA.

The soft-start time (t_{SS}) is determined by the soft-start capacitor (C_{SS}). t_{SS} can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 0.5V}{I_{SS}(\mu A)} \quad (2)$$

Where C_{SS} is the external soft-start capacitor, and I_{SS} is the internal 15μA soft-start charge current.

It is recommended C_{SS} to be ≥6.8nF.

Peak and Valley Current Limits

Both the P-channel MOSFET (the HS-FET) and the N-channel MOSFET (the LS-FET) have current-limit protection. When I_L reaches the HS-FET's peak current limit (I_{LIMIT}) (typically 5A) during the HS-FET on period, the HS-FET is forced off immediately to prevent the current from rising further. Then the LS-FET turns on and remains on until I_L drops below the LS-FET valley I_{LIMIT} (typically 3.5A). The HS-FET turns on once I_L drops to a sufficiently low threshold. The MPQ2179B remains in hiccup mode until the current drops. This I_{LIMIT} scheme prevents current runaway during overload and short-circuit events.

Short-Circuit Protection (SCP) and Recovery

If the output is shorted to ground, the MPQ2179B initiates short-circuit protection (SCP) once I_L reaches I_{LIMIT}. The device tries to recover with hiccup mode. The IC disables the output power stage and begins discharging the soft-start voltage (V_{SS}). The device restarts with a full soft start (SS) once V_{SS} is fully discharged. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (OVP)

The MPQ2179B monitors a resistor-divided V_{FB} to detect over-voltage (OV) conditions. If V_{FB} exceeds 116% of V_{REF}, the controller enters a dynamic regulation period. During this period, the LS-FET stays on until the LS-FET current drops to -1.2A. This discharges the output and keeps V_{OUT} within the normal range.

If the OV condition remains after this process, the LS-FET turns on after 1.5µs. The device exits this regulation period once V_{FB} drops below 108% of V_{REF}. If dynamic regulation cannot limit V_{OUT}, and a 6.1V V_{IN} is detected, input OVP is triggered, and the MPQ2179B stops switching. The MPQ2179B resumes normal operation once V_{IN} drops below 6V.

Power Good (PG) Indicator

The MPQ2179B has a power good (PG) output to indicate normal operation after t_{SS}. PG is the open drain of an internal MOSFET, which has a maximum $R_{DS(ON)}$ below 400Ω. PG can be connected to VIN or an external voltage source through an external a resistor (e.g. 100kΩ).

Once V_{IN} is applied, the MOSFET turns on and PG is pulled to ground before SS is ready. Once V_{FB} reaches 90% of V_{REF}, PG is pulled high by the external voltage source. When V_{FB} drops to 84% of V_{REF}, the PG voltage (V_{PG}) is pulled to GND to indicate an output failure.

If V_{IN} and EN are not available, and PG is pulled up by an external power supply, PG self-biases and asserts. If a 100kΩ pull-up resistor is used, V_{PG} is below 0.9V.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (V_{OUT}). Select a feedback (FB) resistor (R1) that reduces the V_{OUT} leakage current. Generally, it is recommended for R1 to be between 10kΩ and 100kΩ. R2 can be calculated with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.5} - 1} \quad (3)$$

Figure 2 shows the FB circuit.

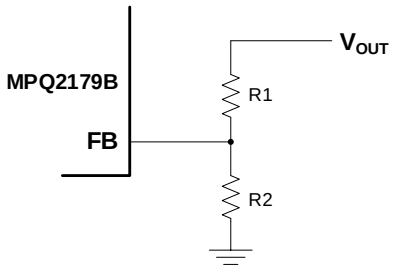


Figure 2: Feedback Network

Table 1 lists the recommended resistances for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
0.5	0 (1%)	NS
1.0	30.9 (1%)	30.9 (1%)
1.2	100 (1%)	71.5 (1%)
1.8	36 (1%)	14 (1%)
2.5	75 (1%)	18.7 (1%)
3.3	68 (1%)	12.1 (1%)

Switching Frequency Scales Down at Low Input Voltages

At heavy loads, the voltage on the HS-FET drops while the on time (t_{ON}) increases, and the duty cycle is extended. If the minimum off time (t_{MIN_OFF}) is reached at a low input voltage (V_{IN}) a heavy load, the switching frequency (f_{SW}) scales down. To maintain a constant f_{SW}, a higher V_{OUT} requires a higher V_{IN} at heavy loads.

V_{IN} while the frequency starts to scale down can be estimated with Equation (4):

$$V_{IN} = \frac{V_{OUT} + R_{DS(ON)\_P} \times I_{OUT}}{1 - \frac{t_{MIN-OFF}}{1400 \times 10^{-9}}} \quad (4)$$

Where the maximum t_{MIN_OFF} is 125ns. (12)

Note:

12) Guaranteed by design and bench characterization. Not tested in production.

Selecting the Inductor

Most applications work best with a 0.47µH to 1.5µH inductor. Select an inductor with a DC resistance below 25mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with magnetic devices can have strong EMI. It is not recommended to use an unshielded power inductor, as they do not provide sufficient magnetic shielding. Shield inductors (e.g. metal alloy inductors or multi-player chip power inductors) are recommended because they effectively reduce magnetic interference.

For most designs, the inductance can be estimated with Equation (5):

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose ΔI_L to be approximately 30% of the maximum load current (I_{LOAD_MAX}). The maximum peak inductor current (I_{L_MAX}) can be calculated with Equation (6):

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply the AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. Higher V_{OUT} may require a 22µF capacitor to increase system stability.

The input capacitor (C1) requires an adequate ripple current rating because it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst case occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose a C1 with an RMS current rating greater than half of I_{LOAD_MAX}.

C1 can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1µF ceramic capacitor, placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Ceramic capacitors are recommended, as well as low-ESR capacitors to limit the V_{OUT} ripple (ΔV_{OUT}). ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (10)$$

Where L_1 is the inductance, and R_{ESR} is the C2 equivalent series resistance (ESR).

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW}, and causes most of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For a 3A load, a 22µF capacitor with a 0805 package (or a larger capacitor) is recommended to reduce ΔV_{OUT} during steady-state operation and load transient. To see the detailed ΔV_{OUT} performance, see the Typical Performance Characteristics section on page 14.

The output capacitance can be smaller for applications with a lower current, or if a larger ΔV_{OUT} is allowed. However, to ensure loop stability, C2 should never be below 10µF, or have a smaller than 1206 package.

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of C2 also affect the stability of the regulation system.

Output Discharge Blocking

If the device is disabled, an internal resistive discharge path between the OUT pin and GND is enabled to discharge C2. The discharge path can be blocked by adding an external capacitor between the output and the OUT pin (see Figure 3).

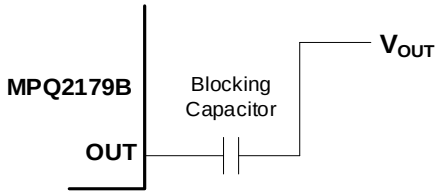


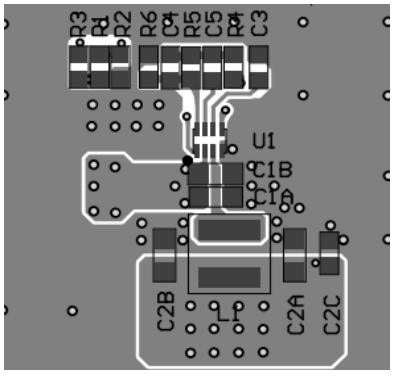
Figure 3: Circuit with VOUT Discharge Blocking

To avoid influencing the loop and load transient, select a ≥10nF blocking capacitor. It is recommended to use a 10nF to 100nF blocking capacitor. A larger blocking capacitance does not have an impact on loop performance; however, it means the capacitor is physically larger, and is typically unnecessary for the best results.

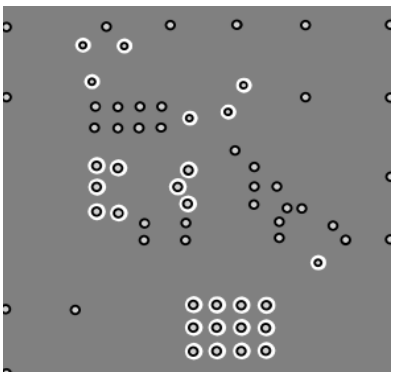
PCB Layout Guidelines

Efficient PCB layout (especially of the switching power supplies) is critical for stable operation. For the high-frequency switching converter, poor layout design can result in poor load or line regulation, as well as stability issues. For the best results, refer to Figure 4 and follow the guidelines below.

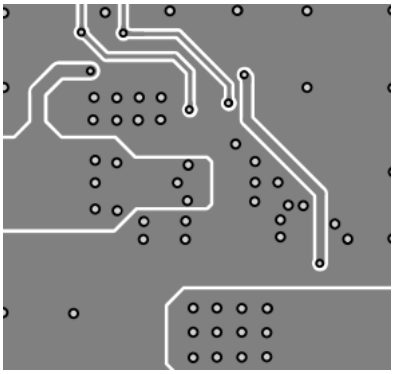
1. Place the high-current paths (GND, VIN, and SW) close to the device using short, direct, and wide traces.
2. Place the input capacitor as close to the VIN and GND pins as possible.
3. Place the GND output capacitor close to the GND pins.
4. Place the external feedback resistors next to the FB pin.
5. Route the switching node (SW) away from the feedback network using a short trace.
6. Route the output voltage sense line away from the power inductor. Make this trace as short as possible. Do not place this line close to the surrounding inductors or SW.



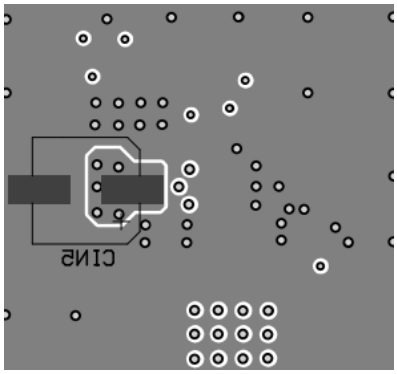
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

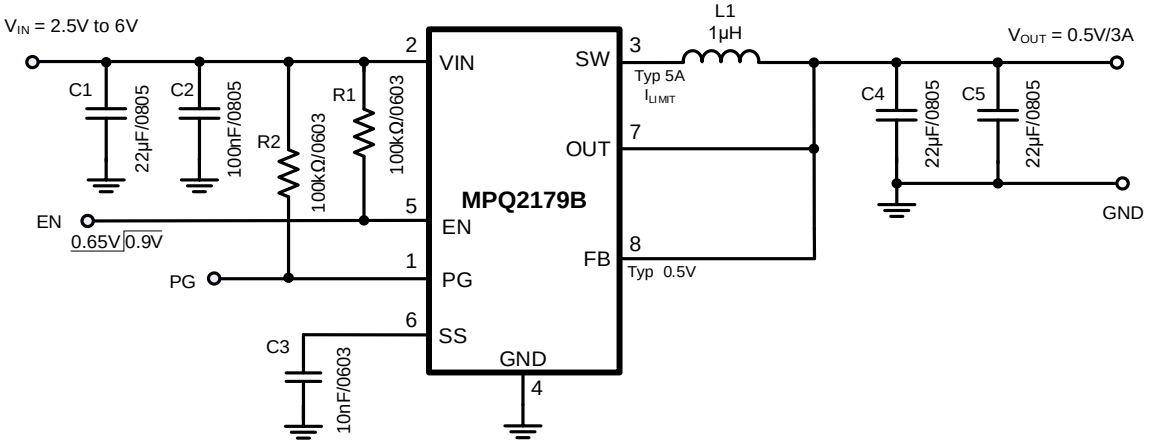


Figure 5: Typical Application Circuit for the Adjustable Output Version (V_{OUT} = 0.5V)

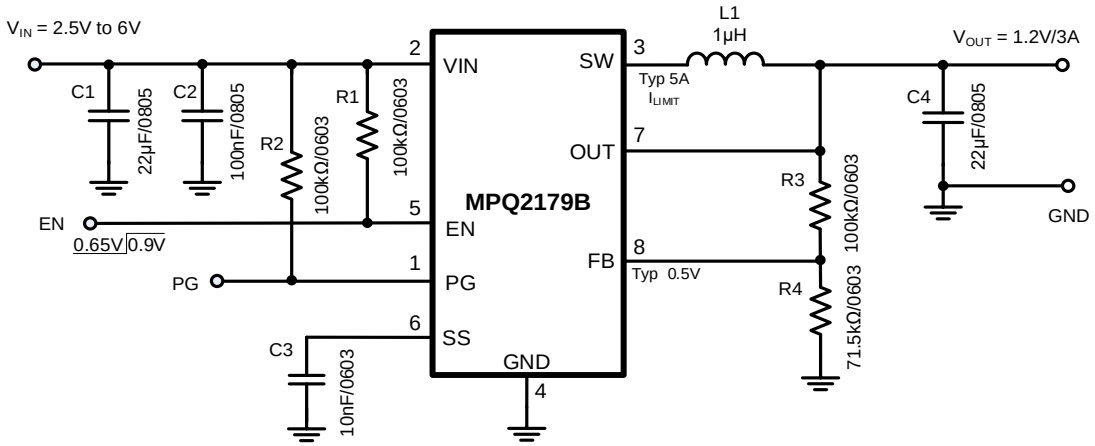


Figure 6: Typical Application Circuit for the Adjustable Output Version (V_{OUT} = 1.2V)

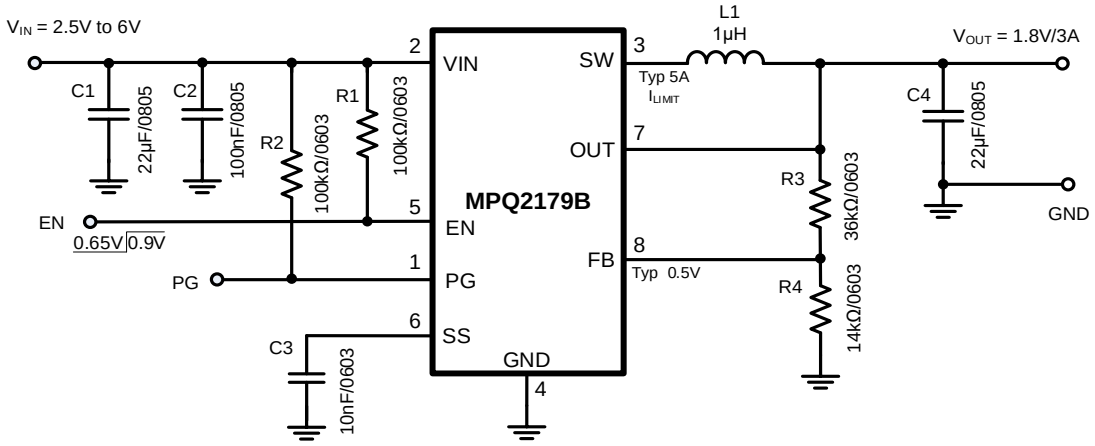


Figure 7: Typical Application Circuit for the Adjustable Output Version (V_{OUT} = 1.8V)

TYPICAL APPLICATION CIRCUITS *(continued)*

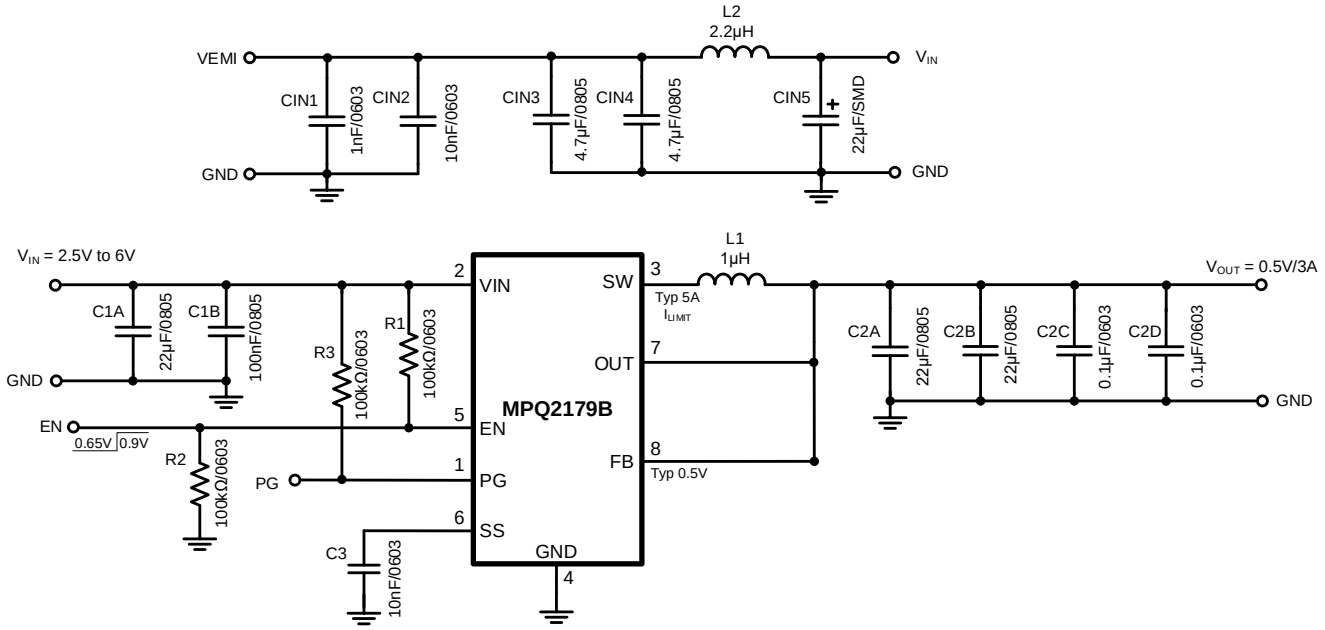
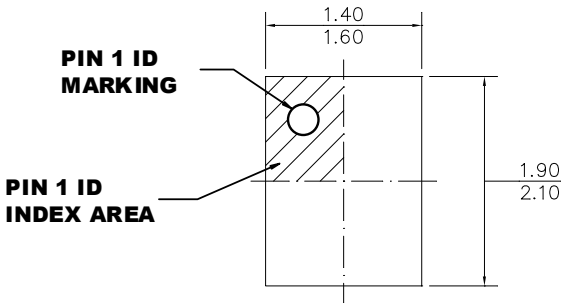


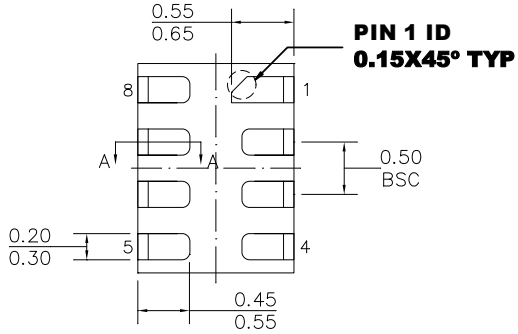
Figure 8: Typical Application Circuit for the Adjustable Output Version with EMI Filter (V_{OUT} = 0.5V)

PACKAGE INFORMATION

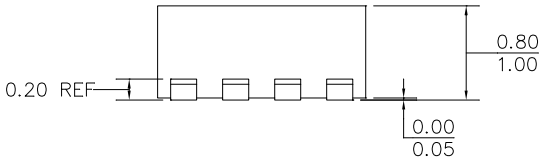
QFN-8 (1.5mmx2mm)
Wettable Flank



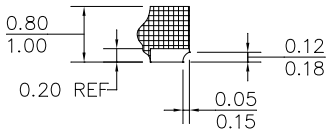
TOP VIEW



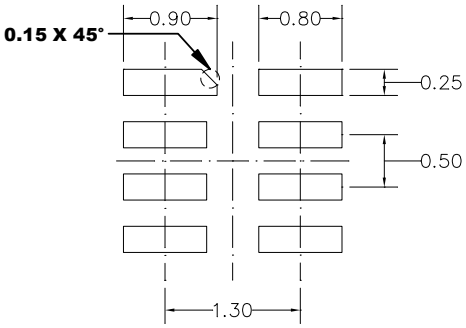
BOTTOM VIEW



SIDE VIEW



SECTION A-A

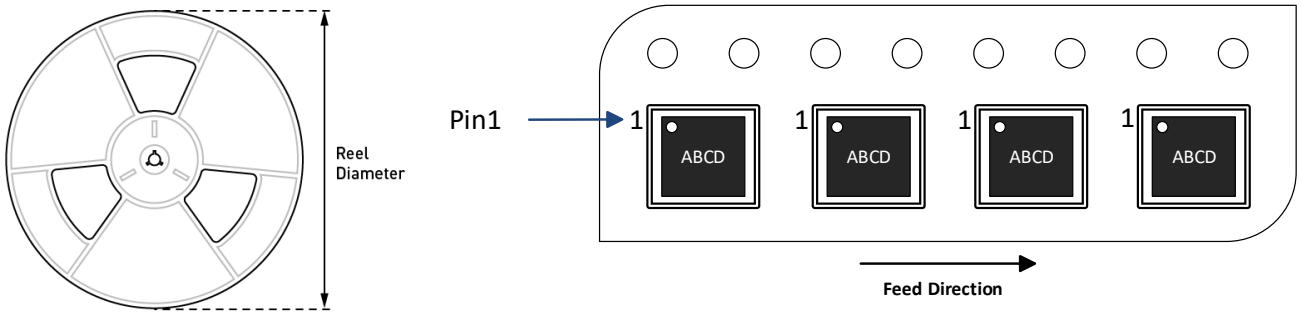


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2179BGQHE-AEC1-Z	QFN-8 (1.5mmx2mm)	5000	N/A	N/A	13in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/14/2023	Initial Release	-