S32M276SFFRD

Reference Design Board for S32M27x CAN MCUs
Hardware User Manual

1 Table of contents

2 Definitions, Acronyms, and Abbreviations

The following list defines the abbreviations used in this document.

BST	Boost
CCM	Counter with CBC MAC (Cipher block chaining message authentication code)
CMOS	Complementary Metal Oxide Semiconductor.
CP	Charge Pump
CPU	Central Processing Unit.
CSPI	Configurable Serial Peripheral Interface.
DDR	Double Data Rate.
DIP	Dual In-line Package.
DPGA	Differential Programmable Gain Amplifier
EEPROM	Electrically Erasable Programmable Read Only Memory.
EPROM	Erasable Programmable Read Only Memory.
FET	Field-Effect Transistor
GCTL	Gate Control
GDU	Gate Driver Unit
GPIO	General Purpose Input/output.
GPO	General Purpose Output.
HG	High-side Gate
HS	High-side Source
HW	Hardware.
HVI	High Voltage Input
HVM	High Voltage Module
I2C	Inter-Integrated Circuit.
I/O	Input/output.
JTAG	Joint Test Access Group.
LED	Light Emitting Diode.
LG	Low-side Gate
LPM	Low-Power Mode
LS	Low-side Source
MB	Megabyte.
MCU	Microcontroller Unit.
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	Memory Stick.
NVRAM	Non-volatile Random-Access Memory.
PCB	Printed Circuit Board.
PHY	Physical interface.
PMC	Power Management Controller
POR	Power-on Reset.
PSRAM	Pseudo Random Access Memory.
PWR	Power.
PWM	Pulse Width Modulation.
RAM	Random Access Memory.
SDRAM	Synchronous Dynamic Random-Access Memory.
TFT	Thin Film Transistor.
UART	Universal Asynchronous Receiver/Transmitter.
USB	Universal Serial Bus.

3 S32M276SFFRD – Block Diagram

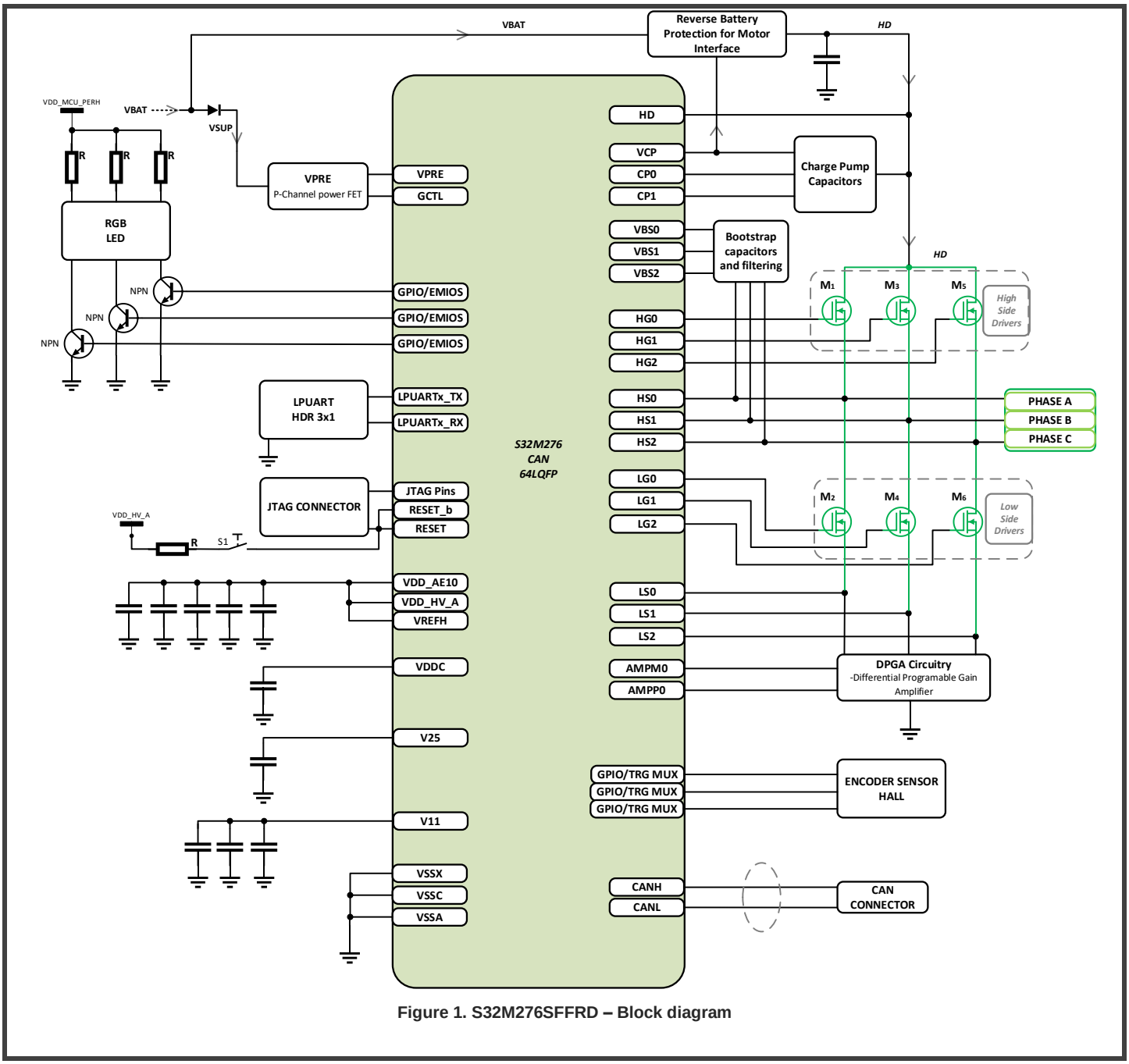


Figure 1. S32M276SFFRD – Block diagram

4 S32M276SFFRD – Features

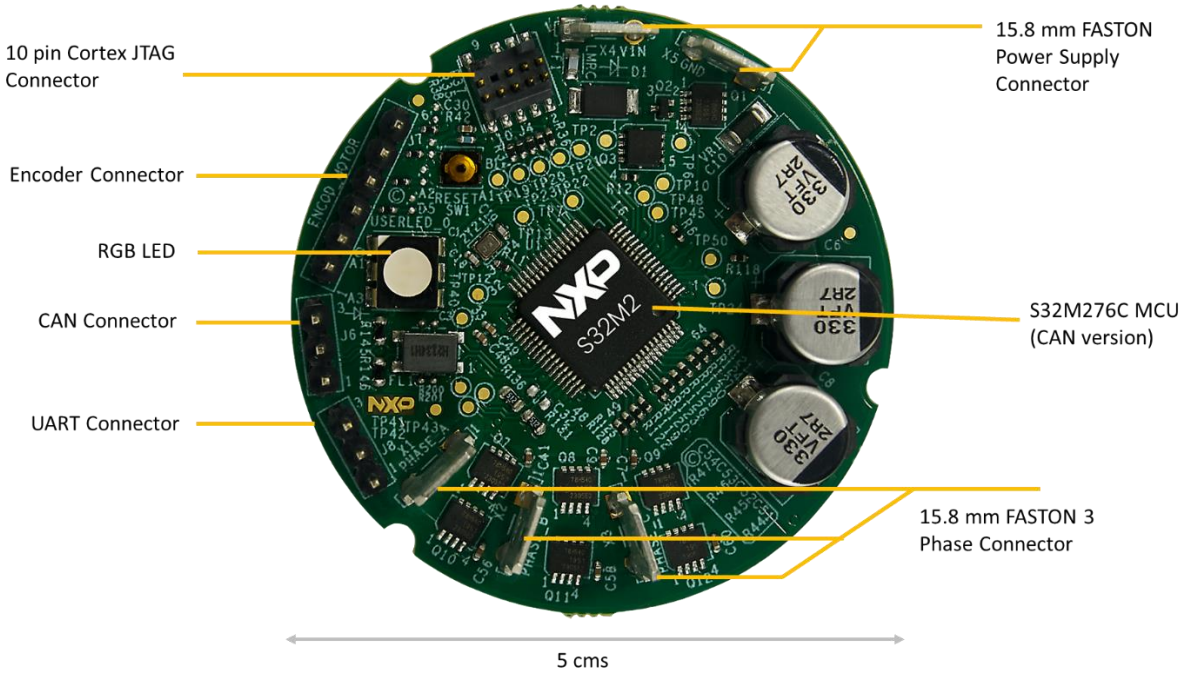


Figure 2. S32M276SFFRD – Features

IMPORTANT
• Before supply the S32M276SFFRD board is used or power is applied, please fully read this user manual. An incorrect configuration in the board may cause a irreparable damage on the component, MCU or entire board.

5 S32M276SFFRD – Default Configuration

Table 1. S32M276SFFRD - Default Configuration

Interface	S32M276SFFRD	Reference / Signal	Default Configuration	Description/Comment
MCU	●	U1	S32M276C MCU	Based on an 120 MHz Arm ® Cortex ® - M7 with single-precision floating-point unit, it has sufficient processing power to support advanced motor control features
MCU Power Supply	●	VSUP_MCU	+12.0V	VSUP_MCU connected to VSUP pin
	●	VPRE_MCU	+6.0V	Generated through an external power FET (gate controlled via GCTL pin)
	●	VDD_MCU	+3.3V	The VDD supplies core, memory, and digital systems inside of the microcontroller(VDD_HV_A). The VDD_AE10 provides voltage to to the microcontroller over the VDD pin.
	●	VDDC_MCU	+5.0V	VDDC is generated by an internal voltage regulator from VPRE, this is the CAN pin supply.
	●	REFH_MCU	VDD_MCU	The VDD_REFH domain is connected to VDD_MCU
	●	V11_MCU	+1.1V	Core and logic voltage supply. This voltage is generated with a low dropout linear voltage regulator.
	●	V25_MCU	+2.5V	Includes a linear regulator that generates a 2.5 V supply from VDD_HV_A.
JTAG	●	J4	Enable	The JTAG interface of the S32M27 MCU is connected through a 10 pin 1.27mm header
UART	●	J3	PTC2	LPUART0_RX
			PTC3	LPUART0_TX
CAN Interface	●	CAN0_OUT	CANH	The S32M276C includes an internal CAN physical interface (PHY) this reduces system components (bill of materials).
			CANL	
User RGB LED	●	D5	PTE16	Red [Active High].
			PTE15	Green [Active High]
			PTD15	Blue [Active High]
Encoder Sensor Hall Connector	●	J7	PTB4	HALL_A
			PTE11	HALL_B
			PTD0	HALL_C
			PTD1	Additional pin in order to have an ADC and TRGMUX access
GDU	●	-	-	The GDU is a pre-driver designed for three-phase motor control applications. A combination of a bootstrap circuit, a charge-pump and a boost converter enables the supply of high-side power MOSFETs of the H-Bridge

6 S32M276SFFRD – Power supply

This reference design requires an external voltage supply of +12V/ 5A. The power management of the S32M276 is done through an internal analog extension die of the SiP, it supplies the internal power needed trough VSUP and VPRE using the aforementioned 12V supply. This further reduces the bill of materials and saves space.

6.1 S32M276SFFRD – Main Power Supply

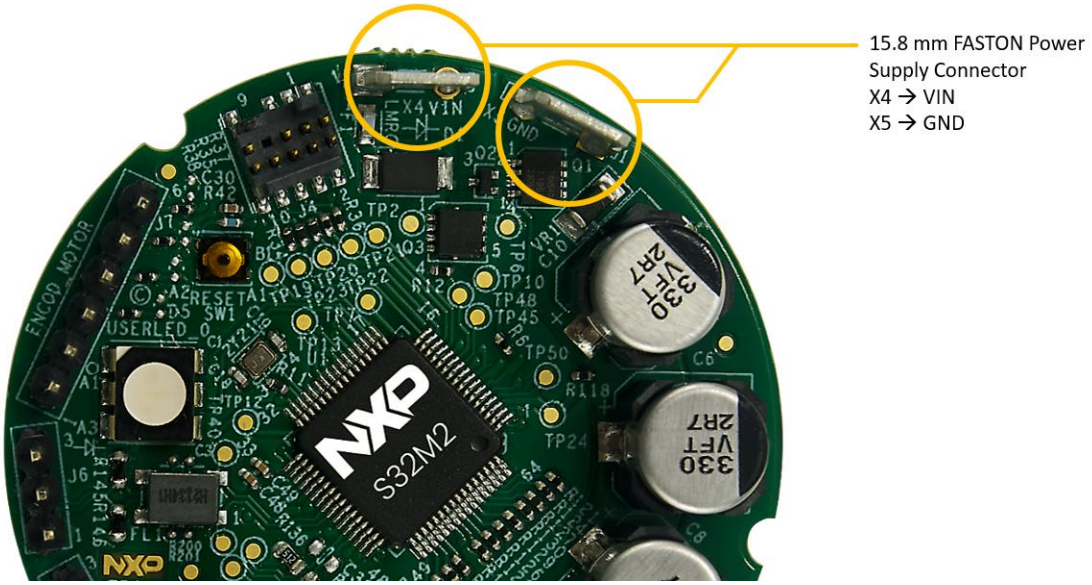


Figure 3. S32M276SFFRD – Main power supply input

Table 2. Main power supply connector

Connector	Circuit/ Interface	Reference	Signal/Connection	Description
	Supply Connectors	X4	VIN	**15.8 mm FASTON Connector – X4 & X5** This connector should be used to connect the power source.
		X5	GND	

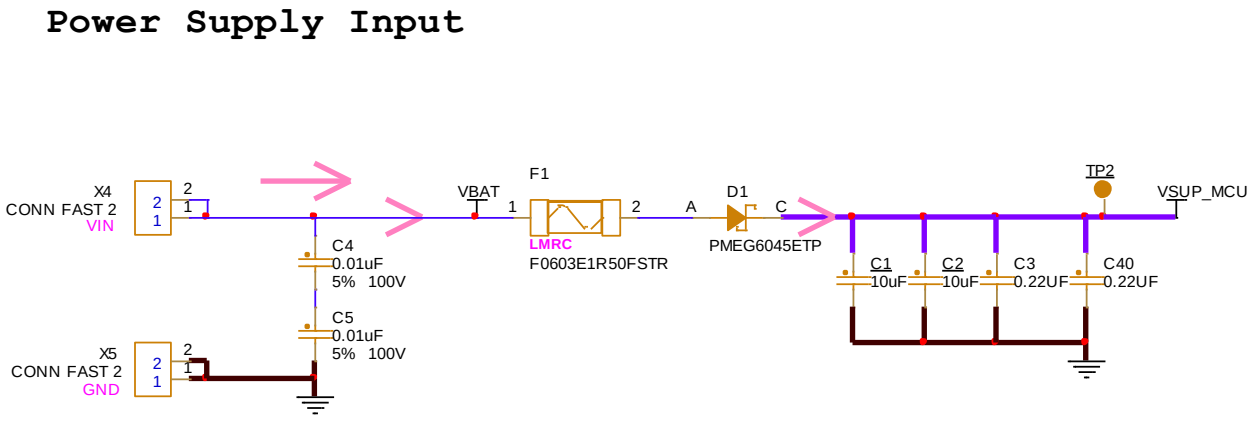


Figure 4. S32M276SFFRD – Power Supply Input

One of the outstanding features of this microcontroller is its ability to supply voltage without the need for an SBC, this is of great convenience in order to reduce the BOM of materials. However, In order to reduce MCU power consumption and minimize potential thermal issues, VPRE is generated using the Gate Control pin to reduce the VSUP voltage to 6 volts and thus supply VPRE pin as shown in the **Figure 5**.

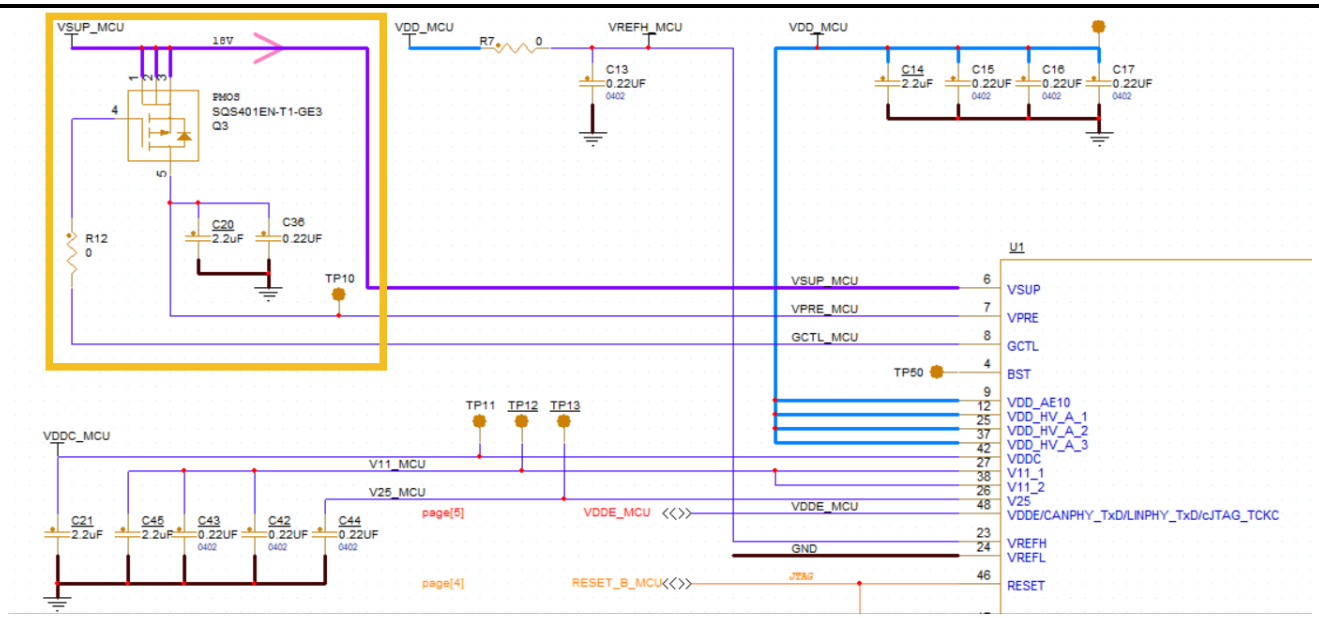


Figure 5. S32M276SFFRD – MCU Power Supply Input VSUP

6.2 S32M276SFFRD – VDD_HV_A

As previously mentioned, the S32M276 is capable of internally regulating the voltage output of the VDD_HV_A_x pins, however it is mandatory to add an external bulk capacitor and one decoupling capacitor for each supply pin, for more details consult the S32M2XX Hardware Design Guidelines. In addition, the VDD_AE10 must be connected with VDD_HV_A pins to a common reference plane on PCB. The values of the decoupling and bulk capacitors are descripted in the **Table 3**

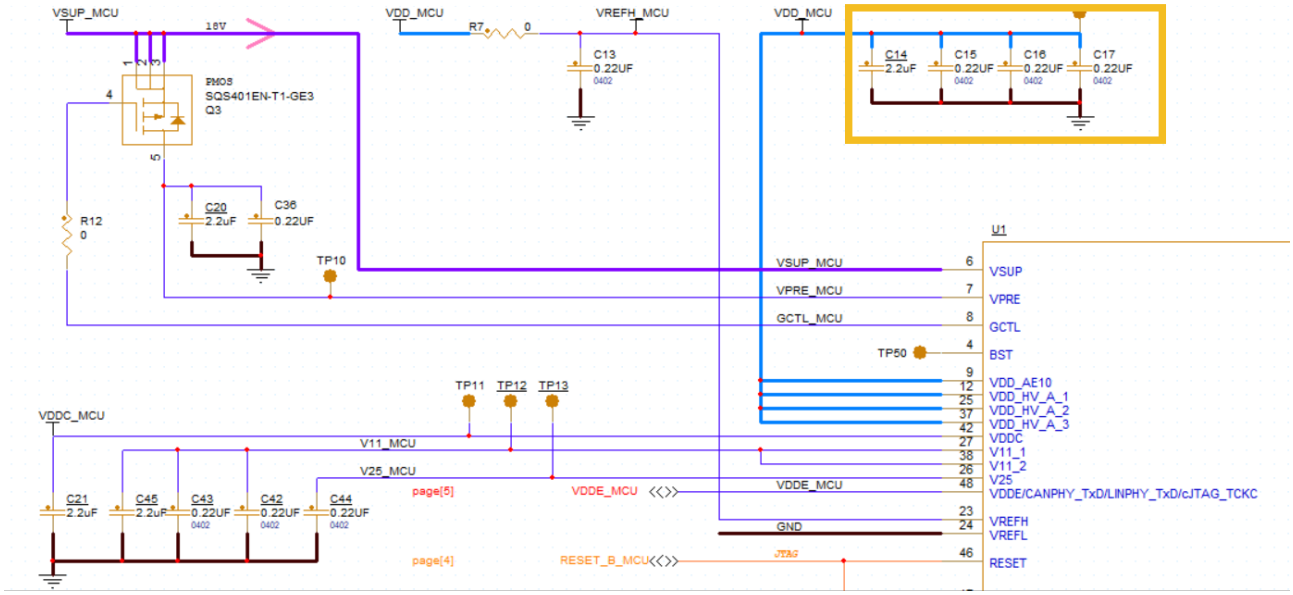


Figure 6. S32M276SFFRD – VDD_HV_A power supply

6.3 S32M276SFFRD – VDDC_MCU

VDDC is CAN supply pin whose voltage is generated by internal voltage regulator from VPRE which can be enabled or disabled to decrease power consumption, this voltage is typically 5V. If configured on, VDDC is automatically turned off in LPM (Low Power Mode) and after wake-up from LPM, VDDC is automatically turned on again. An external bulk capacitor is mandatory.

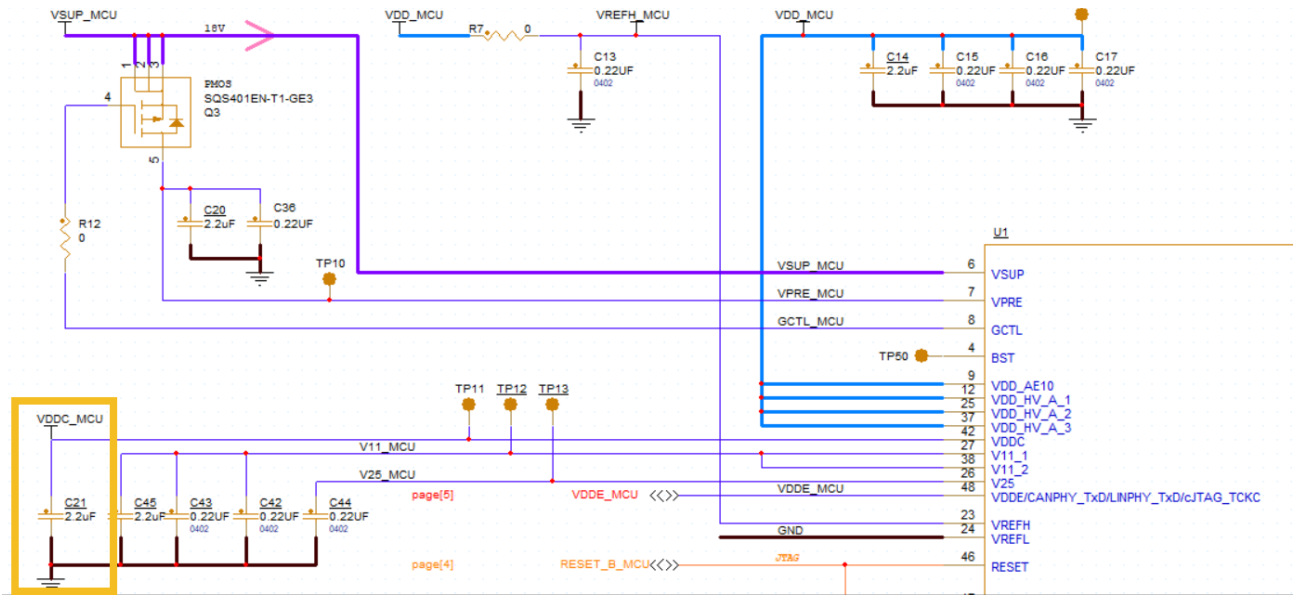


Figure 7. S32M276SFFRD – VDDC_MCU

6.4 S32M276SFFRD – V11

The V11 power pins must be shorted together externally on their voltage domain. Appropriate bulk/bypass and decoupling capacitors should be used to filter noise on the supply. Those pins are the core and logic supply.

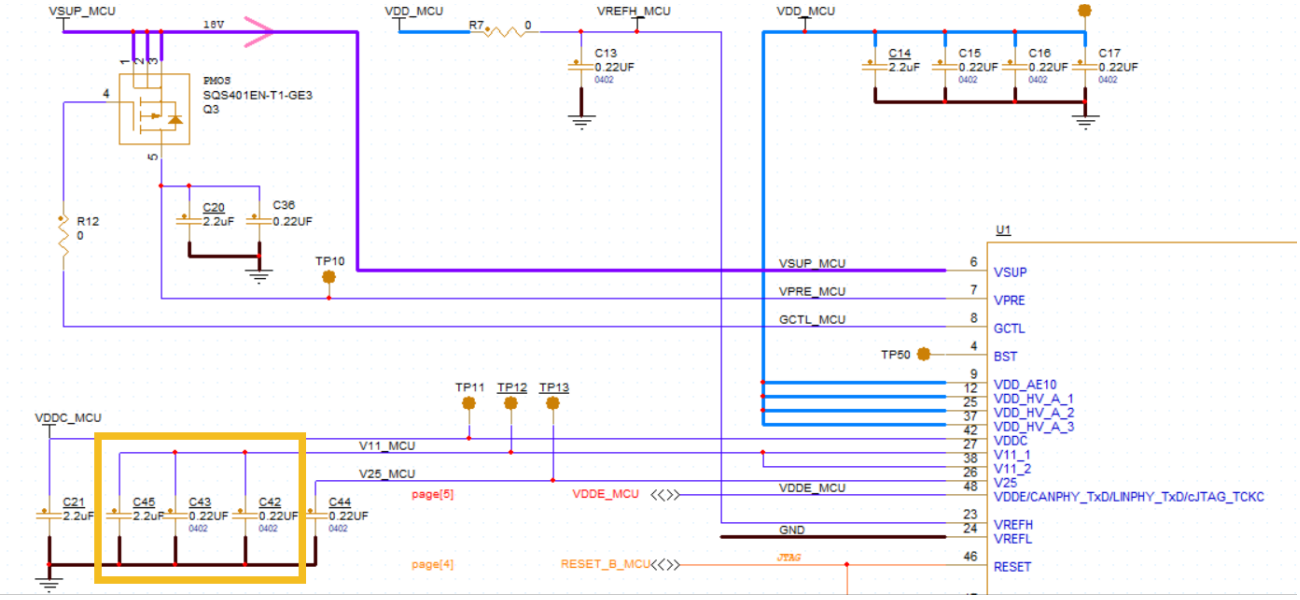


Figure 8. S32M276SFFRD – V11

6.5 S32M276SFFRD – V25

V25 pin supplies the flash memory and (via double bond) the clock modules, this voltage is internally generated from VDD_HV_A.

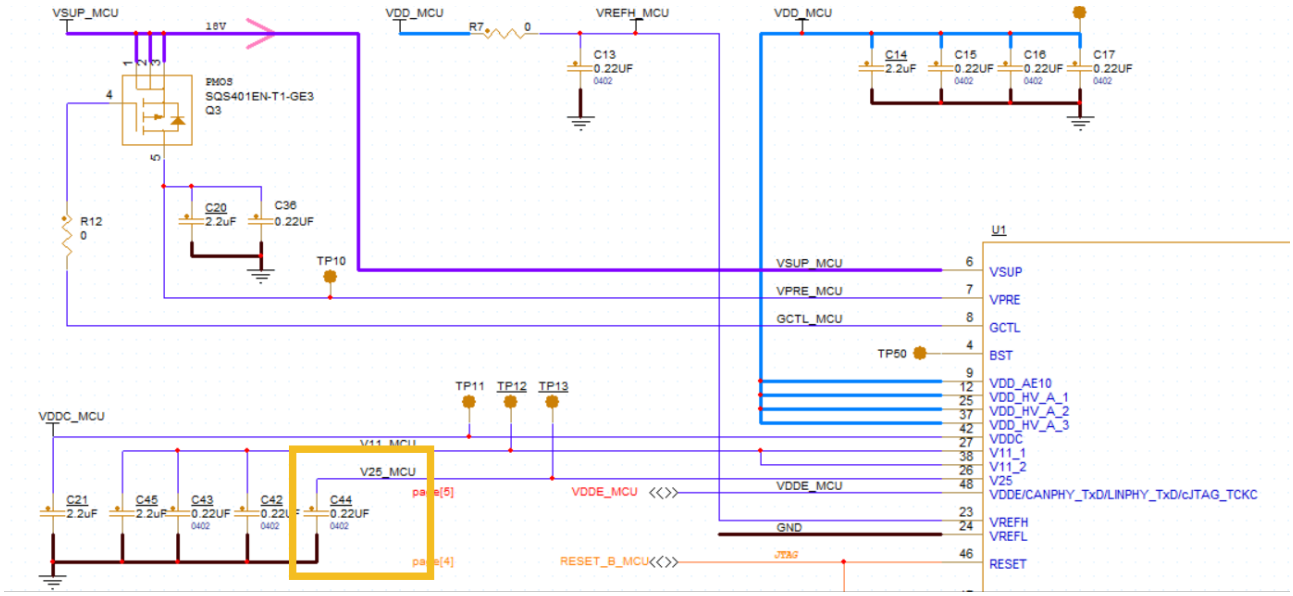


Figure 9. S32M276SFFRD – V25

6.6 S32M276SFFRD – VREFH

The Reference Voltage High (VREFH) should be connected to the same voltage as VDD or may be driven by an external source to a level between the minimum VREFH and the VDDA potential (VDDA + 0.1V and VDD + 0.1 V, or VDD_HV_A + 0.1V).

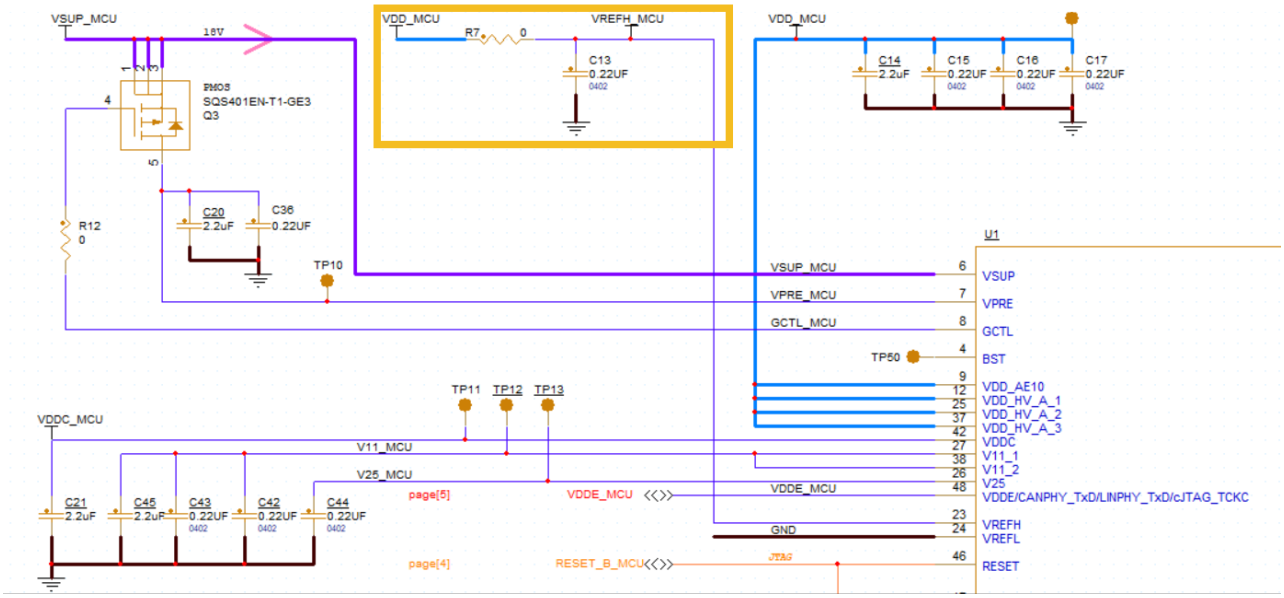


Figure 10. S32M276SFFRD – VREFH

Table 3. Decoupling and bulk capacitors value

Capacitor	Characteristic	Value
Decoupling Capacitor	X7R / X8R Ceramic	100nf - 220nF
Bulk Capacitor	X7R / X8R Ceramic	4.7uF - 2.2uF

7 S32M276SFFRD – Programming and Debug Interface

7.1 S32M276SFFRD – RESET Switch

The RESET switch [SW1] provides an input signal for manual RESET. The S32M276 MCU will drive the RESET signal to reset the board peripherals.

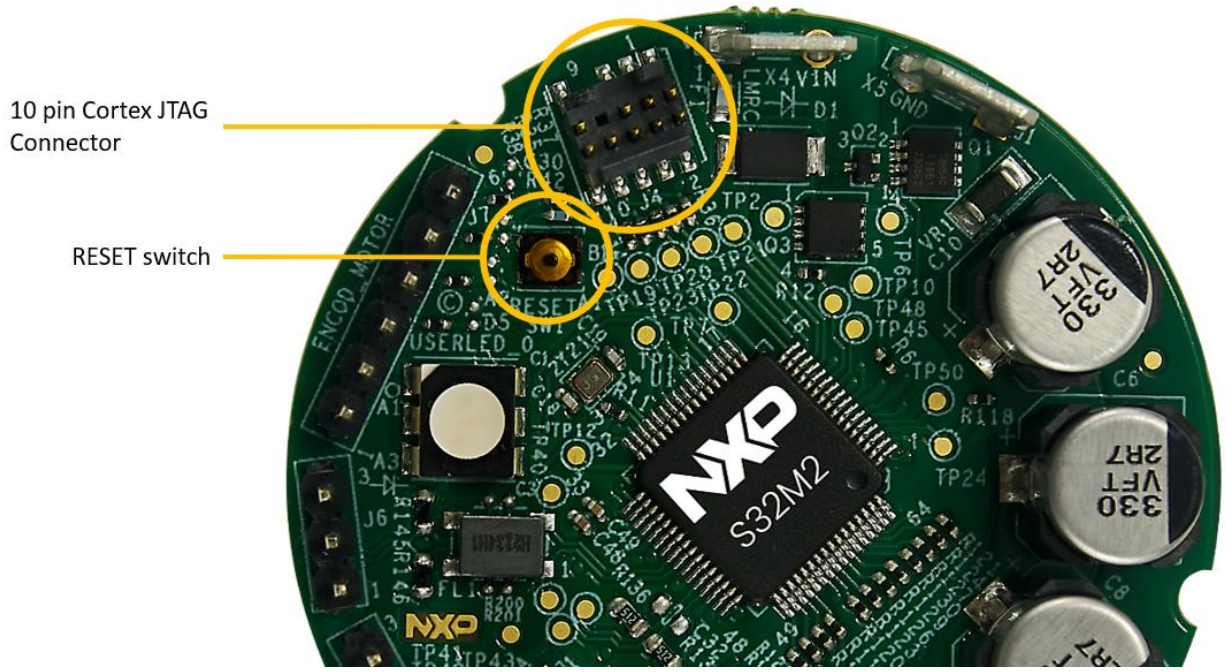


Figure 11. S32M276SFFRD – JTAG connector and RESET Switch

7.2 S32M276SFFRD – JTAG

The S32M276SFFRD incorporates JTAG connectors to program the MCU using a PE Multilink Universal FX Debug Probe which allows the user control the target's execution, read/write registers and memory values, debug code on the processor, and program internal or external FLASH memory devices. In summary It bridges serial and debug communications between an USB host and an embedded target processor.

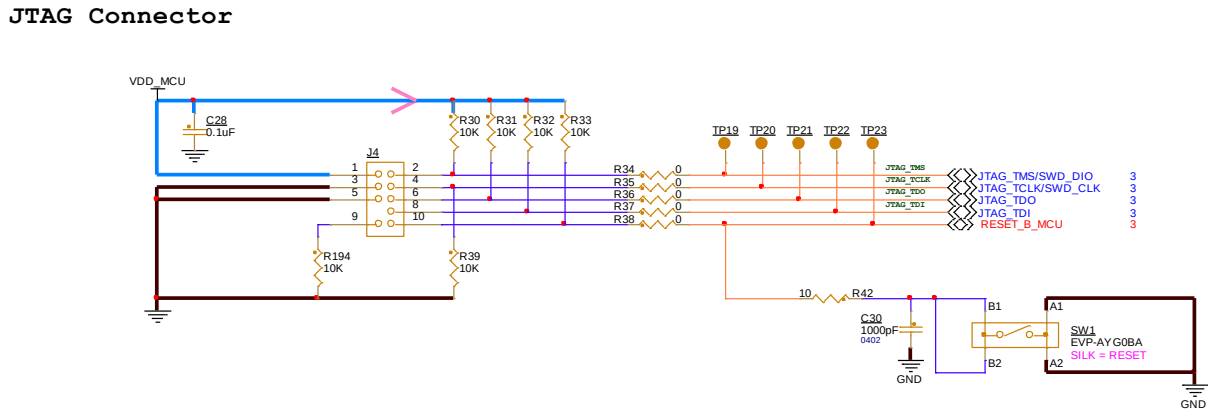
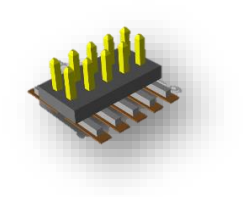


Figure 12. S32M276SFFRD – JTAG

Table 4. Programming and Debug Connectors

Connector		Reference/ Component	Description
10-Pin Cortex Debug		**J4**	This small 10-pin (0.05") connector provides access to SWD, SWV, JTAG, and ETM (4-bit) signals available on a Cortex-M3/M4/M7 device. A 20-pin header (Samtec FTSH-110-01) is specified with dimensions: 0.50" x 0.188" (12.70 mm x 4.78 mm).

8 S32M276SFFRD – LPUART

In order to test the capabilities of the S32M276C on a small PCB board, the J8 connector is routed especially so that the end user can test the UART communication of this MCU and use NXP FreeMaster Tool. To see more details about the pins of this connector consult the **Table 5**.

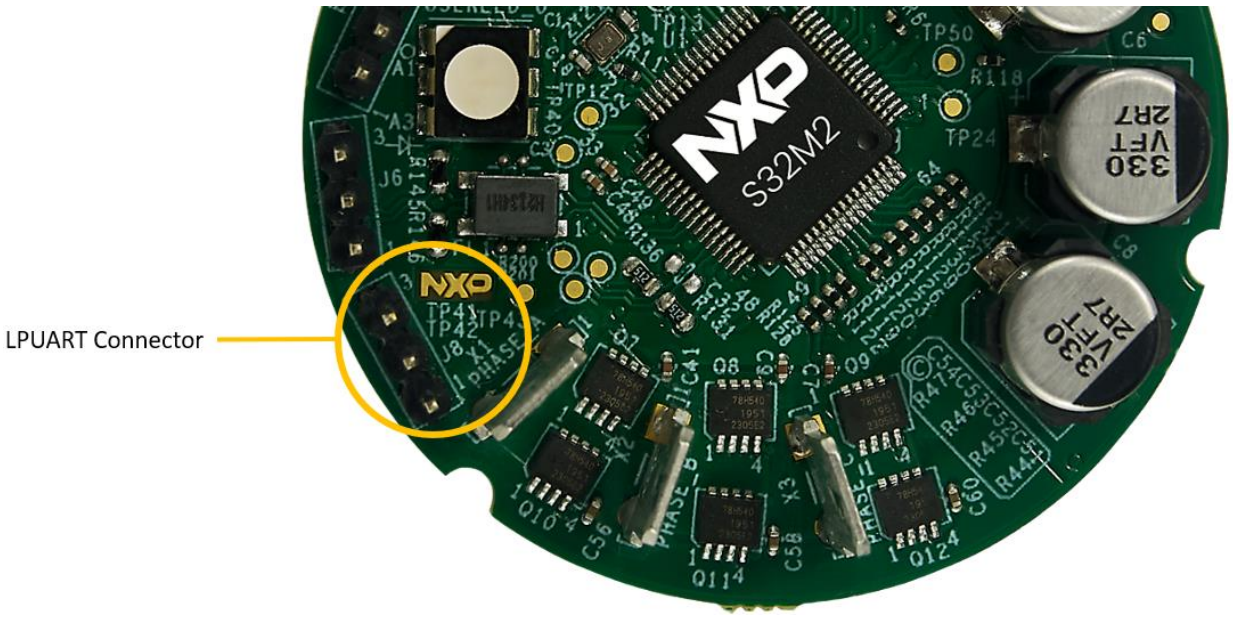


Figure 13. S32M276SFFRD – LPUART Connector

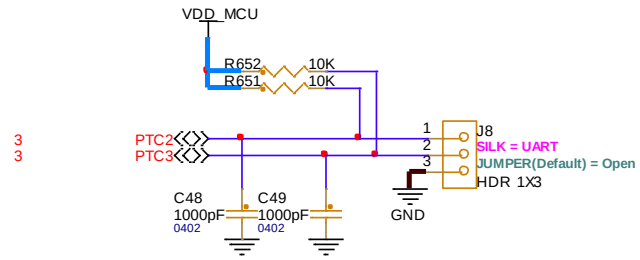
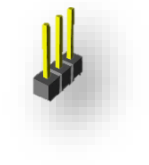


Figure 14. LPUART connection

Table 5. UART Interface – Connector

Connector	Reference	Circuit/ Interface	Pin Number	MCU Port	Interface
	J8	UART	1	PTC2	UART0_RX
			2	PTC3	UART0_TX
			3	NA	GND

9 S32M276SFFRD – CAN Interface

One of the great highlights of this MCU is the ability to integrate a CAN PHY (this due in this reference design are using the CAN variant of the S32M27X) internally in addition to its features described above. This makes schematic and layout as simple as possible due to what is described in the Hardware Design Guidelines and Reference Manual, the user only have to add a few passive components and follow the routing recommendations for the CAN signals.In the following figure is shown the simplicity of the CAN connectivity in the schematic.

Figure 15. S32M276SFFRD – CAN Connector

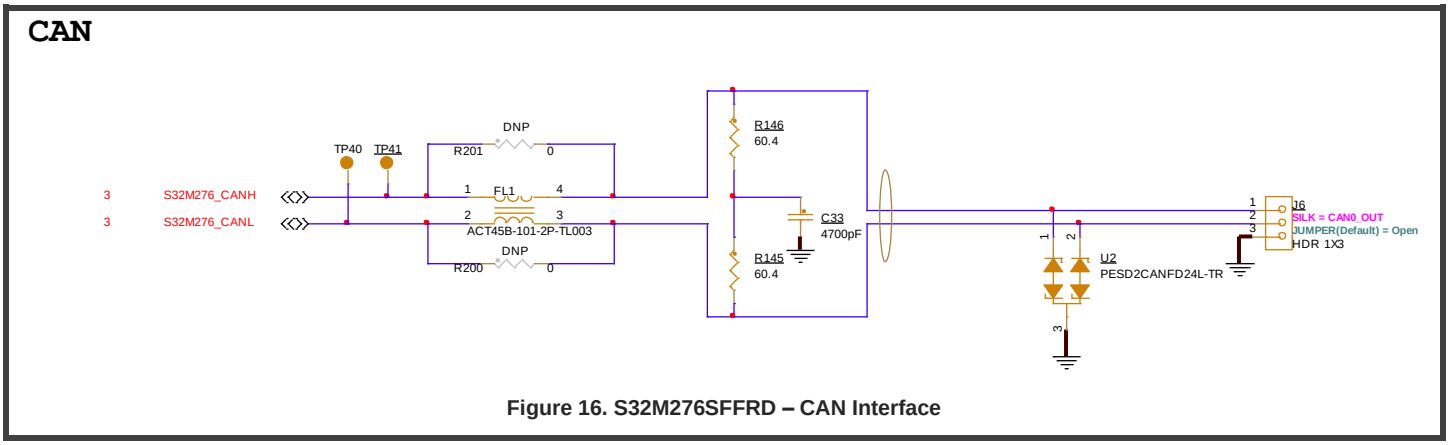
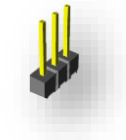


Figure 16. S32M276SFFRD – CAN Interface

Table 6. CAN Interface - Connector

Connector	Reference	Circuit/ Interface	Pin Number	Signal/Connection
	J6	CAN0	1	CANH
			2	CANL
			3	GND

10 S32M276SFFRD – Motor Control Interface

Another feature of the S32M276 MCU is the GDU which provides pre-drivers to control three-phase DC motor via external FETs. In order to support this control, it includes a charge pump and boost converter. The above replace a bootstrap circuit for gate driving.

10.1 S32M276SFFRD – FET pre-driver interface

The GDU contains three gate driver instances. Each instance drives 1 high-side FET (HG) and 1 low-side FET (LG). These high-side and low-side drivers support driving the three phases of a brushless DC motor. The primary function of a driver is to switch a MOSFET from off-state to on-state and vice versa. The pre-driver amplifies the control signals to the required levels to drive the power MOSFET. To guarantee reliable operation, the low-side drivers are supplied by the VLS regulator, while the high-side drivers are supplied directly by the bootstrap circuit over the VBS pins internally.

In the Figure 17 is shown the way half bridge connection to the High Side and Low Side pins of the MCU and in the Figure 18 shows the recommended placement of the MOSFETs for this application.

This reference design board supports 100W three phase BLDC and PMSM motors.

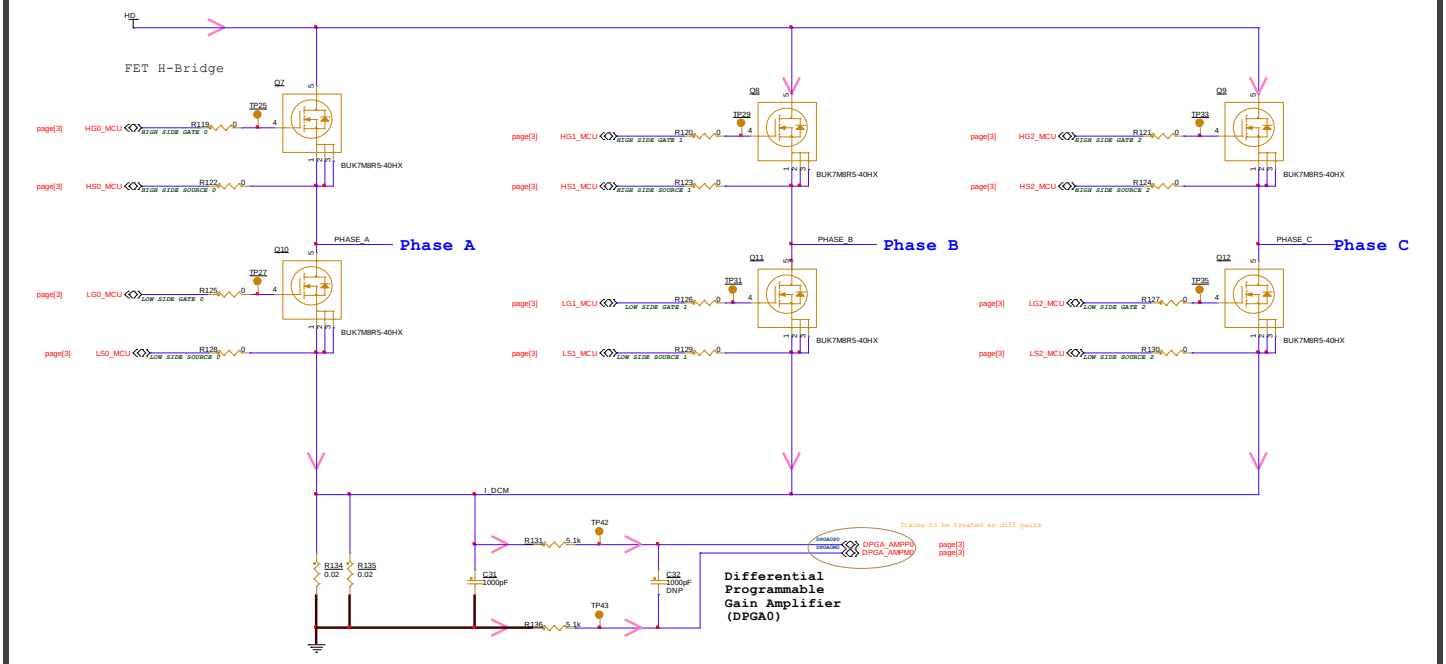


Figure 17. S32M276SFFRD – GDU Interface

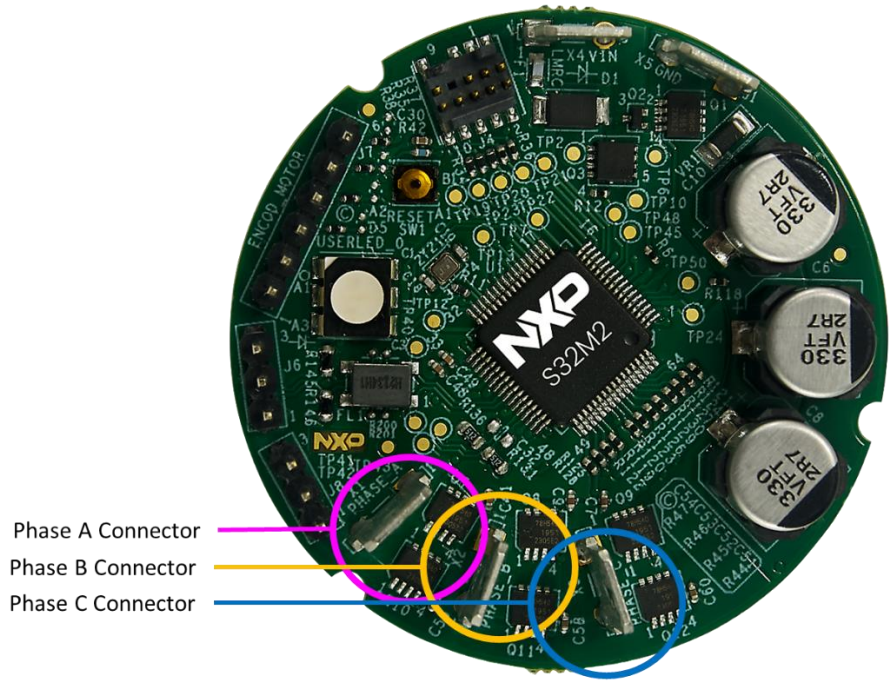
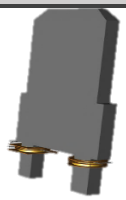


Figure 18. S32M276SFFRD – Phase Connectors

Table 7. Phase Connectors Interface

Connector	Circuit/ Interface	Reference	Signal/Connection
	Phase connectors	X1	PHASE A
		X2	PHASE B
		X3	PHASE C

10.2 S32M276SFFRD – DPGA

A Digital Programmable Gain Amplifier is integrated into the S32M2XX microcontroller for low-side current measurements. The interface consists of one digital programmable current sense amplifier with internal gain settings, blanking time counter and over-currents comparator. It senses voltage drop over the current sense resistor R_{SENSE}.

Additionally using the DPGA we can create a single-shunt motor control application with reduced BOM

- The AMPP0 — Current Sense Amplifier Non-Inverting Input Pin.
- The AMPM0 — Current Sense Amplifier Inverting Input Pin.

DPGA amplifies the voltage drop corresponding to the load current so that it can be measured more precisely than non-amplified signal. The DPGA recommended circuitry for this application is shown in the Figure 19.
For more information about select the R_{SENSE} and the circuitry of the DPGA consult the S32M2XX Hardware Design Guidelines.

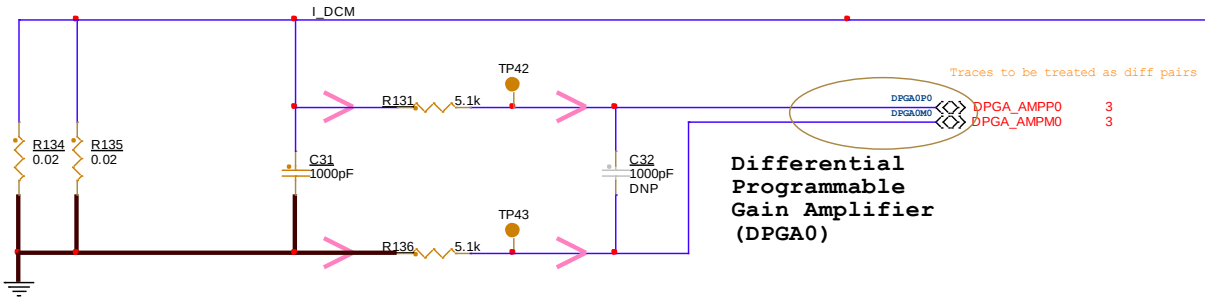


Figure 19. S32M276SFFRD – DPGA

Note: It is highly recommended to use differential pairs at the time the CAD engineer is routing DPGA AMPP0 and DPGA AMPM0 pins, this technique reduces common mode noise by being coupled in this way. Another recommendation to have a better measurement is to avoid signals parallel to this and avoid cross-talk or noise in the signal.

10.3 S32M276SFFRD – Encoder Connector

Another feature that is included in this reference design despite the size of the board is the BLDC motor encoder connector in order to give greater precision to the motor control. In this encoder connector are routed pins with features as EMIOS and EIRQ which are related with the encoder requirements to functionality.

It should be noted that the three main encoder control pins were added a capacitor footprint (0402) in order to fulfill the function of a low pass filter in case the board of the engine encoder has problems with noise in these signals as shown in the Figure 21.

Usually BLDC motors only have 3 encoder signals additionally to the power pins, however an additional pin was added to this connector for the purpose that the user can use this pin (specifically the one corresponding to the PTD1 pin) as an GPIO, ADC, EIRQ or another feature that include this pin and would be used by the user .

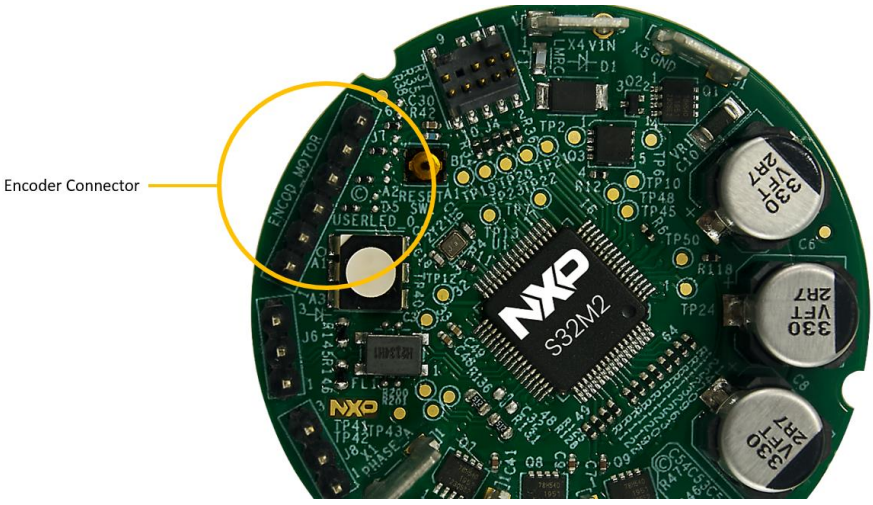


Figure 20. S32M276SFFRD – Encoder connector

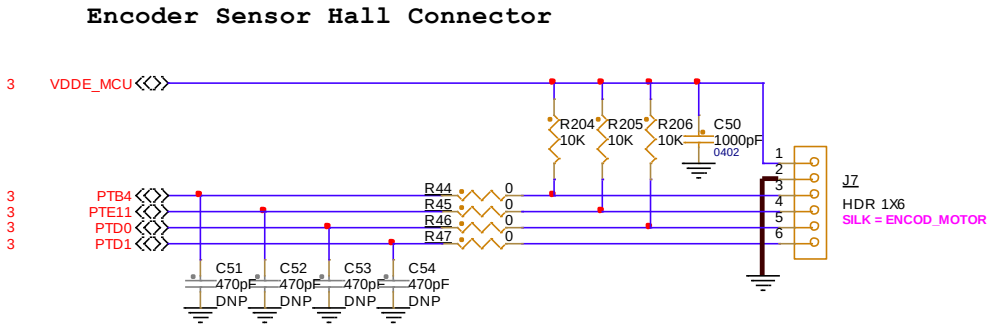


Figure 21. S32M276SFFRD – MCU pins connected to the Encoder connector

Table 8. MCU pins connected to the Encoder connector

Connector	Reference	Circuit/ Interface	Pin Number	Signal / Connection	Pin feature
	J7	Encoder Sensor Hall Connector	1	VDDE_MCU	Encoder +5V external supply
			2	GND	-
			3	PTB4	EMIOS_0_CH_G[4]
			4	PTE11	EMIOS_0_CH_G[1]
			5	PTD0	EMIOS_0_CH_G[2]
			6	PTD1	EMIOS_0_CH_G[3]

11 S32M276SFFRD – User LED RGB

Although this board is a reference design for the motor control application and due of the efficiency of the placement in the board an RGB LED was added in order to indicate an status or just test a code but this depends of the customer application.
The value of the resistor R646, R648 and R650 depends of the VDD_MCU, this voltage reference normally is used at 3.3 volts but if the value of VDD_MCU where modified the value of this resistors should be modified too.

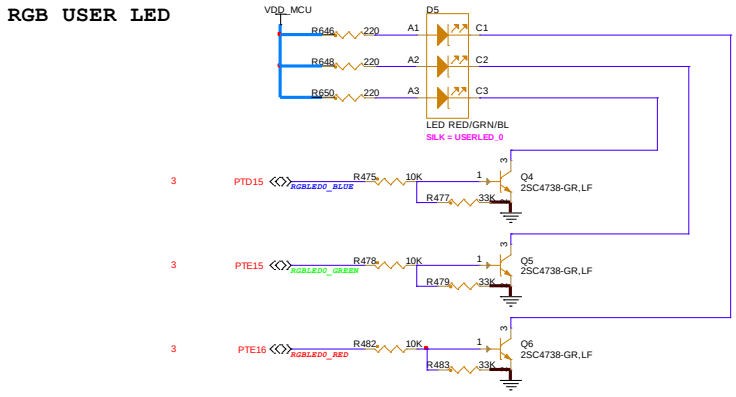


Figure 22. S32M276SFFRD – RGB user LED

Table 9. RGB user LED pins

Reference	Circuit/ Interface	Color	MCU Port connected	Comment
D5	RGB LED	Blue	PTD15	Active High
		Green	PTE15	Active High
		Red	PTE16	Active High

12 S32M276SFFRD – Test points

Certain test-points are added to voltage or critical signals on the board in order to test them in a simple way. Additionally in order to get access to all the pins of the MCU, in the pins that wasn't required for the application a some test points were to enable that pins.

Table 10. S32M276SFFRD – Measurement test points

Test-point	Signal / Connection	Details
TP2	VSUP	Primary supply input to PMC from the supply.
TP6	VBAT Status	Reverse Battery Protection for Motor Interface.
TP7	VDD_MCU	VDD is the supply output that powers the MCU die. It can be configured to be either 3.3V or 5V. It is internally generated from VPRE.
TP10	VPRE signal	Typical 6V and generated from the VSUP.
TP11	VDDC_MCU	Reference voltage to CAN communication.
TP12	V11	Voltage supply for the core 1.1 V.
TP13	V25	Reference design for flash memory.
TP19	JTAG_TMS/SWD_DIO	JTAG TMS connected to the MCU pin17 at PTA4.
TP20	JTAG_TCLK/SWD_CLK	JTAG TCLK connected to the MCU pin15 at PTC4.
TP21	JTAG_TDO	JTAG TDO connected to the MCU pin13 at PTA10.
TP22	JTAG_TDI	JTAG TDI connected to the MCU pin14 at PTC5.
TP23	RESET	RESET input from SW1 to the MCU pin 46 and 16.
TP24	HD_MCU	Test point to get access to the HD pin of the MCU
TP25	HG0_MCU	Test point to get access to the High-Side Gate pin 0
TP27	LG0_MCU	Test point to get access to the Low-Side Gate pin 0
TP29	HG1_MCU	Test point to get access to the High-Side Gate pin 1
TP31	LG1_MCU	Test point to get access to the Low-Side Gate pin 1
TP33	HG2_MCU	Test point to get access to the High-Side Gate pin 2
TP35	LG2_MCU	Test point to get access to the Low-Side Gate pin 2
TP40	S32M276_CANL	Test point to get access to CANL pin
TP41	S32M276_CANH	Test point to get access to CANH pin
TP42	DPGA_AMPP0	Test point to get access to the DPGA AMPM0 pin
TP43	DPGA_AMPM0	Test point to get access to the DPGA AMPP0 pin
TP44	DPGA_AMPOUT	Test point to get access to the DPGA AMPOUT pin
TP45	PTA15	Test point to get access to PTA15 pin of the MCU
TP46	PTB5	Test point to get access to PTB5 pin of the MCU

TP47	PTD16	Test point to get access to PTD16 pin of the MCU
TP48	PTE6	Test point to get access to PTE6 pin of the MCU
TP49	HVI	Test point to get access to HVI pin of the MCU
TP50	BST	Test point to get access to BST pin of the MCU

13 S32M276SFFRD – Revision history

Table 11. Revision History

Document Revision	Date	Board Name	Schematic/ Board Number	Schematic/ Revision	Board Revision	Changes	Author
A	08/2024	S32M276SFFRD	90894	B	A	-	Luis Rico Chávez

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