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SPSA068

Datasheet

Automotive PMIC with BUCK and precise voltage reference for MCU applications

QFN32L Epad
5.0x5.0x1.0 mm

Product status link
SPSA068

Product summary	
Order code	SPSA068
Package	QFN32L
Packing	-
Option	Blank

Features

- AEC-Q100 qualified
- Pre SMPS BUCK regulator, adjustable via NVM to 5.0 V, 3.3 V, 1.2 V at 0.5 A and 1.0 A load current, 0.4/2.4 MHz. Via external resistive divider, it can regulate a voltage between 5 V and 1.2 V.
- Precise voltage reference (1%), adjustable via NVM to 5.0 V, 3.3V, 1.2 V at 20 mA load current
- Standby mode Iq < 5 µA
- Low quiescent current, 50 µA, in low power active mode
- SPI interface with CRC
- Programmable soft start
- Voltage supervisors
- Spread frequency spectrum
- Reset output
- Adjustable window watchdog supervisors
- V_{REF}, tracking of V_{BUCK} in power-up phase
- Short circuit protected outputs and Fault detection pin to microcontroller
- Low external components number
- Thermal warning and thermal shutdown

Description

SPSA068 is a BUCK voltage regulator with a precise voltage reference for MCU applications. All the regulators have internal power switches.

The LPM allows the operation under light-load conditions reducing the quiescent current down to 50 µA typ.

An internal programmable memory allows selecting the main device parameters like output voltages and switching frequencies.

An SPI interface can be used for diagnostics, programming, monitor and external window watchdog.

The device offers a set of features to support applications that need to fulfill functional safety requirements as defined by automotive Safety Integrity Level.

1 Overview

The SPSA068 is a PMIC composed by a synchronous current mode BUCK voltage regulator, with integrated LS and HS power-MOS, and a precise voltage reference. It offers flexibility and ease to use, together with a set of features that make it compliant to the commonly used microcontroller in car passenger applications that require functional safety. The product includes input and output monitors, independent band-gaps, ground loss monitors, digital and analog BIST, FAULT pin.

SPSA068 provides 2 different regulated voltages: there are a battery-compatible regulator with integrated MOS for loads up to 1 A and a 1% accurate reference voltage.

A window watchdog, a reset output and an SPI bus complete the product.

The output voltages can be selected via non-volatile memory cells that should be programmed before using the PMIC, since there is no default programming. The absence of external programming components guarantees precision and safety, since output voltages are not susceptible to variations due to the external environment. It also helps reduce the number of external components. Among programmable parameters there are the output voltages, the switching frequency, the spread spectrum disable, the protection intervention thresholds and the BUCK limiting current.

The device must be programmed at the customer’s production line at first power-up.

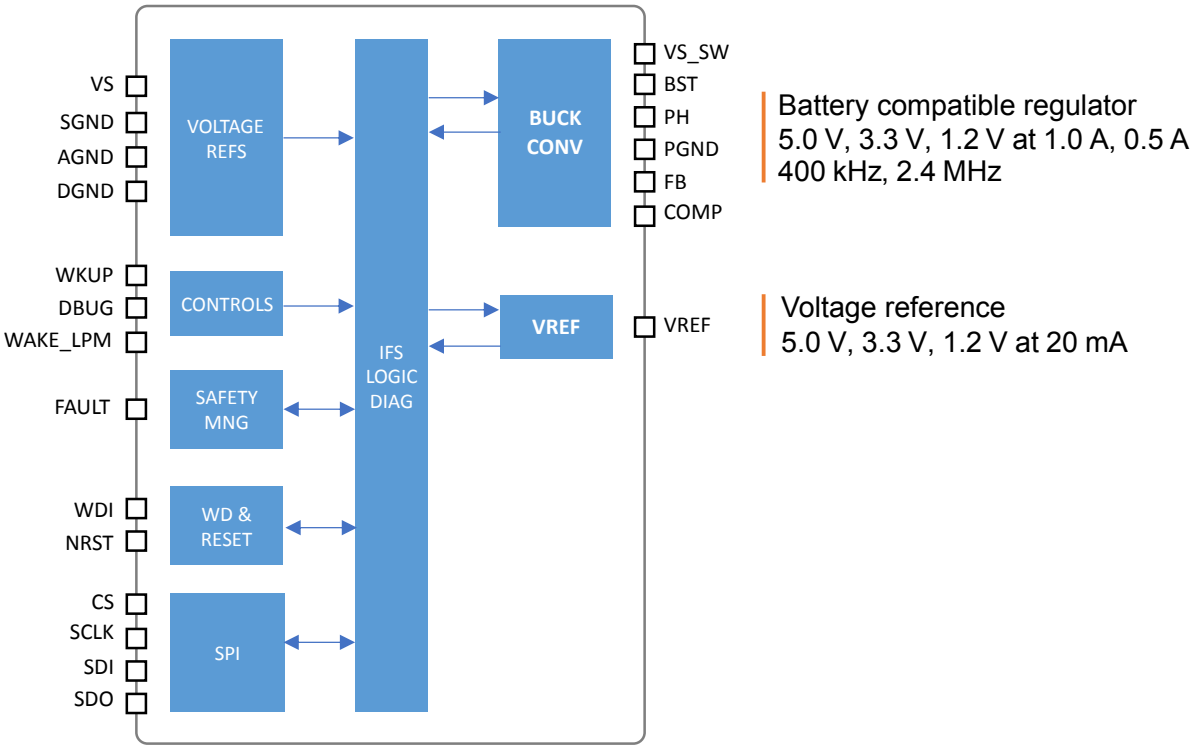
The low power mode allows to supply components at a very optimized quiescent current, down to 50 µA. LPM can be activated by the SPI command and, if not required, it can be disabled by NVM configuration.

An SPI bus is used to program the PMIC and to communicate with the microcontroller. Through the SPI it is possible to provide a watchdog signal and communicate the status of the regulators in case of faults or warnings.

2 Block diagram and pin description

2.1 Block diagram

Figure 1. **Block diagram**



2.2 Pin description

Figure 2. **Pinout (bottom view)**

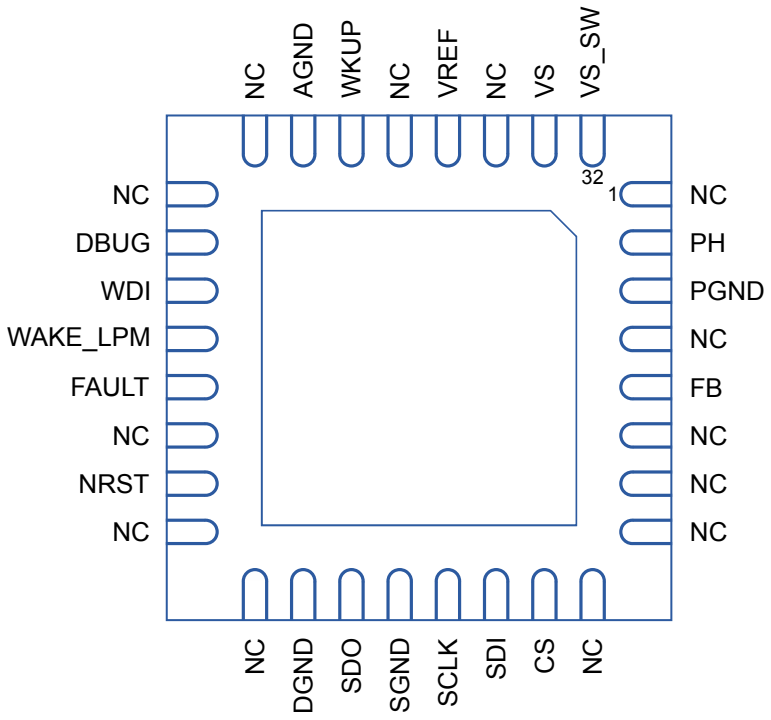


Table 1. **Pin description**

#	Name	Type	Description	Global / Local
1	NO CON	NC	Internally not connected	-
2	PH	O	Switching node BUCK	Local
3	PGND	G	BUCK power ground	Local
4	NO CON	NC	Internally not connected	-
5	FB	I	BUCK regulated voltage output (feedback to internal voltage monitors)	Local
6	NO CON	NC	Internally not connected	-
7	NO CON	NC	Internally not connected	-
8	NO CON	NC	Internally not connected	-
9	NO CON	NC	Internally not connected	-
10	CS	I	SPI: chip select input. Internal current pull-up	Local
11	SDI	I	SPI: serial data input. Internal current pull-down	Local
12	SCLK	I	SPI: serial clock input. Internal current pull-down	Local
13	SGND	G	Signal ground for low noise circuitry	Local
14	SDO	OD	SPI: serial data output	Local
15	DGND	G	Digital ground	Local
16	NO CON	NC	Internally not connected	-
17	NO CON	NC	Internally not connected	-
18	NRST	OD	Reset, negate	Local
19	NO CON	NC	Internally not connected	-

#	Name	Type	Description	Global / Local
20	FAULT	OD	Fault pin detection to MCU	Local
21	WAKE_LPM	I	LPM Wake pin	Local
22	WDI	I	Watchdog input. WDI is trigger input from the MCU. Internal current pull-down	Local
23	DBUG	I	Device debug. Connect to ground when not used	Local
24	NO CON	NC	Internally not connected	-
25	NO CON	NC	Internally not connected	-
26	AGND	G	Analog GND	Local
27	WKUP	I	Wake up input. Internal 200 kΩ pull-down	Global
28	NO CON	NC	Internally not connected	-
29	VREF	O	Accurate reference voltage output	Local
30	NO CON	NC	Internally not connected	-
31	VS	S	Input voltage, battery voltage	Global
32	VS_SW	S	Input voltage for switching regulator (BUCK)	Global

3 Electrical specifications

3.1 Absolute maximum ratings and operating voltage

Table 2. Absolute maximum ratings and operating voltage

Pin name	Absolute maximum rating			Operating voltage		
	Min	Max	Unit	Min	Max	Unit
VS	-0.3	42	V	-0.3	19(1)	V
VS_SW	-0.3	42	V	-0.3	19(1)	V
VREF	-0.3	20(2)	V	-0.3	5.5	V
DGND	-0.3	0.3	V	0	0	V
DEBUG	-0.3	20	V	-0.3	5.5	V
SGND	-0.3	0.3	V	0	0	V
AGND	-0.3	0.3	V	0	0	V
WKUP	-0.3	42	V	-0.3	19	V
FB	-0.3	20(2)	V	-0.3	5.5	V
PGND	-0.3	0.3	V	-0.3	0.3	V
PH	-1	42	V	-1	19	V
WDI	-0.3	20	V	-0.3	5.5	V
CS	-0.3	20	V	-0.3	5.5	V
SDI	-0.3	20	V	-0.3	5.5	V
SCLK	-0.3	20	V	-0.3	5.5	V
SDO	-0.3	20(3)	V	-0.3	5.5	V
NRST	-0.3	20(3)	V	-0.3	5.5	V
FAULT	-0.3	20(3)	V	-0.3	5.5	V
WAKE_LPM	-0.3	20	V	-0.3	5.5	V

1. *In load dump, the PMIC remains active till 32 V.*
2. *Direct short to 20 V is not allowed when the device is in rec mode and fast discharge is enabled, max voltage allowed ≤ 8 V.*
3. *Direct short to 20 V not allowed when pin is asserted, max voltage allowed ≤ 8 V.*

3.2 Thermal data

3.2.1 Thermal resistance

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}a}$	Thermal resistance with device soldered on a 2s2p PCB + vias (according to JEDEC)	32	°C/W
$R_{th\ j\text{-}c}$		2	°C/W
P_{diss}	Target power dissipation at 1 A, 2.4 MHz	1.5	W

3.2.2 Thermal warning and protection

Table 4. Temperature thresholds

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
T_{SD_TH}	Thermal shutdown		160	175	190	°C
T_{SD_hys}	Thermal hysteresis		0.5	4	8	°C
T_{OT_TH}	Over temperature warning		140	155	170	°C
T_{OT_hys}	OT hysteresis		3	7	11	°C
T_{SD_filter}	Thermal filter time		400	500	600	µs
T_J	Junction temperature		-40	-	150	°C
T_{stg}	Storage temperature		-	-	150	°C

3.3 Electrical characteristics

All parameters are tested and guaranteed in the following conditions, unless otherwise noted: Supply voltage according to the operating range of the Table 2; T_J according to operating range of the Table 4.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
General characteristics						
VS	Operating range	BUCK = 3.3 V In case of BUCK = 5 V, the device still operates with VS < 5 V, down to 4 V, but regulated voltage will be equal to BUCK = VS - I_load x RonHS	4.2	14	19	V
VS	Operating range LPM	BUCK = 3.3 V In case of BUCK = 5 V, the device still operates with VS < 5 V, down to 4.5 V, but regulated voltage will be equal to BUCK = VS - I_load x RonHS	4.5	14	19	V
$I_{q\text{-}sm}$	Quiescent current in standby mode on VS pin	All regulators off VS = 14 V, WKUP = GND	-	-	5	µA
$I_{q\text{-}lpmns}$	Quiescent current in low power mode, BUCK not switching, on VS pin	Buck not switching VS = 14 V, WKUP = High	-	25	40	µA
$I_{q\text{-}lpm}$	Quiescent current in low power mode on VS pin	I_{BUCK} = 3.3 V at 80 µA VS = 14 V, WKUP = High	-	50	75	µA
I_{active}	Quiescent current in active power mode on VS pin	All regulators on VS = 14 V, WKUP = High	-	-	12	mA
Supply monitors						
V_{UV}	Undervoltage threshold for VS	Supply decreasing	3.8	-	4.2	V
V_{UV_HYS}	Undervoltage hysteresis		0.05	-	0.2	V
t_{UV_filter}	Undervoltage filter time		-	40	-	µs
V_{NRST_LOW}	NRST pin asserted voltage	I_{RESET} = 1 mA (source current)	0	0.1	0.25	V
T_{NRST}	NRST time assertion		-	500	-	µs

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{FAULT}	FAULT pin asserted voltage	I_{FAULT} = 1 mA	-	0.1	0.25	V
T_{FAULT}	FAULT time toggling after LPM exit		-	500	-	µs
Power on reset						
V_{POR_R}	VS threshold	VS rising	3.1	-	3.8	V
V_{POR_F}	VS threshold	VS falling	2.9	-	3.6	V
Oscillator						
f_{osc_main}	Main oscillator frequency		2.4 - 5%	2.4	2.4 + 5%	MHz
f_{osc_aux}	Aux oscillator frequency		0.4 - 5%	0.4	0.4 + 5%	MHz
BUCK						
Vout_buck5v	Output voltage Output value depends on the input voltage (V_i > V_o)	BUCK_VOUT_SEL<1:0> = 00 V_{in} = 6 to 16 V Load = 0.1 A to 1 A	-2%	5.0	+2%	V
Vout_buck3v3	Output voltage Output value depends on the input voltage (V_i > V_o)	BUCK_VOUT_SEL<1:0> = 01 V_{in} = 6 to 16 V Load = 0.1 A to 1 A	-2%	3.3	+2%	V
Vout_buck1v2	Output voltage Output value depends on the input voltage (V_i > V_o)	BUCK_VOUT_SEL<1:0> = 10 V_{in} = 6 to 16 V Load = 0.1 A to 1 A Frequency 2.4 MHz	-2%	1.2	+2%	V
Vout_buck1v2	Output voltage Output value depends on the input voltage (V_i > V_o)	BUCK_VOUT_SEL<1:0> = 11 V_{in} = 6 to 16 V Load = 0.1 A to 1 A Frequency 400 kHz	-4%	1.2	+4%	V
t_{on_min}	Min Ton internal FET Fast SR	Guaranteed by design BUCK_SLEW_RATE<0> = 1 fast	-	60	-	ns
t_{on_min}	Min Ton internal FET Slow SR	Guaranteed by design BUCK_SLEW_RATE<0> = 0 slow	-	75	-	ns
F_{SW}	Free running frequency	BUCK_FREQ<5> = 0 BUCK_FREQ<5> = 1	-	0.4 2.4	-	MHz
$\Delta V_{LINE\text{-}TRANSIENT}$	Line transient regulation	VS from 6 V to 18 V at 1 V/µs (and vice versa) I_load = 1 A All regulation voltages at 2.4 MHz, 3.3 V and 5 V at 400 kHz C_{load} 40 µF	-6	-	+6	%
$\Delta V_{LINE\text{-}TRANSIENT}$	Line transient regulation	VS from 6 V to 18 V at 1 V/µs (and vice versa) I_load = 1 A 1.2 V at 400 kHz C_{load} 40 µF	-15	-	+15	%
$\Delta V_{LOAD\text{-}TRANSIENT}$	Load transient regulation	I_load from 50 mA to 1 A (and vice versa) at 300 mA/µs	-10	-	+10	%

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
		VS = 14 V 3.3 V and 5 V at 400 kHz and 2.4 MHz C_{load} 40 µF				
$\Delta V_{LOAD-TRANSIENT}$	Load transient regulation	I_load from 50 mA to 1 A (and vice versa) at 300 mA/µs VS = 14 V 1.2 V at 2.4 MHz C_{load} 40 µF	-15	-	+15	%
IL_{IMIT_L}	Peak switching current limitation	BUCK_CURR_LIM<6> = 0 Iload = 1 A	1.6	-	3.4	A
$VREF_{leakage}$	VREF leakage	VS connected Device in standby or sleep	-2	-	+2	µA
IL_{IMIT_L}	Peak switching current limitation	BUCK_CURR_LIM<6> = 1 Iload = 0.5 A	1	-	2.3	A
Ron_{HS}	High side switch on resistance		-	395	-	mΩ
Ron_{LS}	Low side switch on resistance		-	200	-	mΩ
η	Efficiency	Fsw = 2.4 MHz, V_o = 3.3 V Fsw = 2.4 MHz, V_o = 5 V Fsw = 0.4 MHz, V_o = 3.3 V Fsw = 0.4 MHz, V_o = 5 V Iload = 1 A; DCR ≤ 10 mΩ DC ESR ≤ 10 mΩ; V_{in} = 14 V Slow rise and fall time are configured	68 75 85 87	73 80 90 92	-	%
$t_{SOFTSTART\_BUCK}$	Soft start time when start-up	BUCK_SS_CLK_SEL<2> = 1 BUCK_SS_CLK_SEL<2> = 0	-	0.45 1.1	-	ms
F_{spread_BUCK2}	Spread spectrum range	Fsw = 400 kHz Fsw = 2.4 MHz	-3	-	+3	%
$F_{spread\_mod\_2.4}$	Spread spectrum modulation frequency	Fsw = 2.4 MHz	-	9.3	-	kHz
$F_{spread\_mod\_rand\_2.4}$	Spread spectrum random modulation spread	Fsw = 2.4 MHz	-30	-	20	%
$F_{spread\_mod\_400}$	Spread spectrum modulation frequency	Fsw = 400 kHz	-	6.25	-	kHz
$F_{spread\_mod\_rand\_400}$	Spread spectrum random modulation spread	Fsw = 400 kHz	-28	-	+28	%
t_{RT_PH}	Output stage rise time fsw = 400 kHz and 2.4 MHz	BUCK_SLEW_RATE<0> = 0 slow I_load = 500 mA Guaranteed by design	-	12	-	ns
t_{FT_PH}	Output stage fall time fsw = 400 kHz and 2.4 MHz	BUCK_SLEW_RATE<0> = 0 slow I_load = 500 mA Guaranteed by design	-	13	-	ns
t_{RT_PH}	Output stage rise time	BUCK_SLEW_RATE<0> = 1 fast	-	7.5	-	ns

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
	fsw = 400 kHz and 2.4 MHz	I_load = 500 mA Guaranteed by design				
t_{FT_PH}	Output stage fall time fsw = 400 kHz and 2.4 MHz	BUCK_SLEW_RATE<0> = 1 fast I_load = 500 mA Guaranteed by design	-	9	-	ns
Fast_disc	Fast-discharge current of BUCK and VREF	Enabled in REC MODE FB = 5 V	-	12	-	mA
V_{REF}						
V_{out_REF5v}	Output voltage (it depends on input voltage ($V_i > V_o$))	VREF_OUT<10:9> = 00	-1%	5.0	+1%	V
V_{out_REF3v3}	Output voltage (it depends on input voltage ($V_i > V_o$))	VREF_OUT<10:9> = 01	-1%	3.3	+1%	V
V_{out_REF1v2}	Output voltage (it depends on input voltage ($V_i > V_o$))	VREF_OUT<10:9> = 10	-1.5%	1.2	+1.5%	V
I_{load}	Load current range		0	-	20	mA
I_{REF_TOT}	Reference voltage current limit	Ron = 10 Ω	25	50	70	mA
$t_{SOFTSTART\_VREF}$	Soft start time when start-up	BUCK_SS_CLK_SEL<2> = 1 BUCK_SS_CLK_SEL<2> = 0	-	0.45 1.1	-	ms
C_{VREF}	VREF load capacitor	BUCK_SS_CLK_SEL<2> = 1 BUCK_SS_CLK_SEL<2> = 0 In case of Cvref > 1.4 µF (BUCK SOFTSART = 0) or Cvref > 3.5 µF (BUCK SOFTART = 1), the VREF_UV flag may be set at power-up. Flag can be cleared by reading the SPI register	0.22 0.22	-	1.4 3.5	µF
R_{ESR_CVREF}	VREF load capacitor ESR	C_{LOAD} = 220 nF 100 kHz < f < 1 MHz	-	-	100	mΩ
T_{oc_filter}	Filter for over current flag of VREF		-	4	-	ms
WKUP						
V_{WAKE_ON}	Wake pin high threshold	Compatible with 3.3 V	1.25	-	2	V
V_{WAKE_OFF}	Wake pin Low threshold	Compatible with 3.3 V	0.8	-	1.75	V
I_{LEAK_WKUP}	Leakage current	Active mode,WAKE < 20 V	-	-	2	uA
t_{WAKE_filter}	Wake pin filter time		10	25	40	µs
T_{wk_rec1}	Wake up high duration in rec	WAKE_RETRY_TIMER<2:1> = 00	-	10	-	ms
T_{wk_rec2}	Wake up high duration in rec	WAKE_RETRY_TIMER<2:1> = 01	-	20	-	ms
T_{wk_rec3}	Wake up high duration in rec	WAKE_RETRY_TIMER<2:1> = 10	-	30	-	ms
T_{wk_rec4}	Wake up high duration in rec	WAKE_RETRY_TIMER<2:1> = 11	-	40	-	ms

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
GND loss comparator						
V_{GL_TH}	GND loss threshold		0.3	-	0.8	V
t_{GL_filter}	GND loss filter	Filter time before to enable BUCK	-	100	-	µs
V_{PGL_TH}	PGND loss threshold		0.1	-	0.4	V
Power output UV/OV monitor						
$V_{BUCKUV\_H\_0}$	Under voltage threshold at falling edge of output (as % of output). Referred to the BUCK relative value	BUCK_UV_L<3> = 1	88	-	96	%
$V_{BUCKUV\_H\_1}$	Under voltage threshold at falling edge of output (as % of output). Referred to the BUCK relative value	BUCK_UV_L<3> = 0 (default)	84	-	91	%
V_{BUCKUV_HYS}	Hysteresis of BUCK UV		70	-	-	mV
V_{BUCKUV_L}	Deep under voltage threshold at falling edge of output (as % of output). Referred to BUCK relative value		-	-	65	%
V_{BUCKOV_0}	Over voltage threshold at rising edge of output (as % of output). Referred to the BUCK relative value	BUCK_OV_L<4> = 0 (default)	104	-	114	%
V_{BUCKOV_1}	Over voltage threshold at rising edge of output (as % of output). Referred to the BUCK relative value	BUCK_OV_L<4> = 1	109	-	120	%
$t_{UVH\_filter\_BUCK}$	Under voltage threshold filter time		-	40	-	µs
$t_{OV\_filter\_BUCK}$	Over voltage threshold filter time	Overvoltage filter time for SPI flag detection Overvoltage reacts in the loop forcing pulse-skipping	-	500	-	µs
$t_{UV\_filter\_VREF}$	Under voltage threshold filter time		-	20	-	µs
$t_{OV\_filter\_VREF}$	Over voltage threshold filter time		-	20	-	µs
$t_{OV\_filter\_BUCK\_fast}$	Over voltage filter time used for open load diagnosis	BUCK_OL_EN<8> = 1 (open load diagnosis enabled), applicable only during the BUCK start-up phase	-	3	-	µs
$t_{UVL\_filter\_BUCK}$	Buck deep under voltage filter time		-	3	-	µs
V_{REFUV_0}	Under voltage threshold at falling edge of output (as % of output). Referred to the VREF relative value	VREF_UV_L<11> = 0 (default)	87	-	96	%
V_{VREFUV_1}	Under voltage threshold at falling edge of output (as % of output). Referred to the VREF relative value	VREF_UV_L<11> = 1	82	-	91	%

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{REFUV_HYS}	Hysteresis of VREF UV		100	-	-	mV
V_{VREFOV_0}	Over voltage threshold at rising edge of output (as % of output). Referred to the VREF relative value	VREF_OV_L<12> = 0 (default)	104	-	116	%
V_{REFOV_1}	Over voltage threshold at rising edge of output (as % of output). Referred to the VREF relative value	VREF_OV_L<12> = 1	109	-	120	%
$T_{POWER\_ON\_TIMEOUT}$	Power on timeout for BUCK and VREF		-	3	-	ms
Watchdog trigger						
VH_{WDI}	WDI pin threshold high		2.3	-	-	V
VL_{WDI}	WDI pin threshold low		-	-	1	V
T_{LW}	Long open window		160	200	240	ms
R_{WDI_PD}	WDI PD resistance	Active mode	120	200	350	kΩ
T_{EFW1}	Early failure window 1	WDG_TIME_WINDOW<4:3> = 00	-	-	6.4	ms
T_{LFW1}	Late failure window 1	WDG_TIME_WINDOW<4:3> = 00	15.6	-	-	ms
T_{SW1}	Safe window 1	WDG_TIME_WINDOW<4:3> = 00	7.8	-	12.7	ms
T_{EFW2}	Early failure window 2	WDG_TIME_WINDOW<4:3> = 01	-	-	12.7	ms
T_{LFW2}	Late failure window 2	WDG_TIME_WINDOW<4:3> = 01	31.1	-	-	ms
T_{SW2}	Safe window 2	WDG_TIME_WINDOW<4:3> = 01	15.6	-	25.5	ms
T_{EFW3}	Early failure window 3	WDG_TIME_WINDOW<4:3> = 10	-	-	25.5	ms
T_{LFW3}	Late failure window 3	WDG_TIME_WINDOW<4:3> = 10	62.2	-	-	ms
T_{SW3}	Safe window 3	WDG_TIME_WINDOW<4:3> = 10	31.1	-	50.9	ms
T_{EFW4}	Early failure window 4	WDG_TIME_WINDOW<4:3> = 11	-	-	50.9	ms
T_{LFW4}	Late failure window 4	WDG_TIME_WINDOW<4:3> = 11	124.4	-	-	ms
T_{SW4}	Safe window 4	WDG_TIME_WINDOW<4:3> = 11	62.2	-	101.8	ms
T_{DWR}	Delay between WD trigger fault and reset low		-	-	4	µs
LPM parameters						
T_{LPM_EN}	Low power mode enters filter time	Digital filter time	-	5	-	ms
$T_{WAKE\_LPM\_FILT}$	Filter time on WAKE_LPM to exit from LPM	Digital filter time	-	1	-	ms
T_{LPM_DIS}	Low power mode exit delay time	Analog delay + digital wait time from filtered WAKE_LPM = 1 to ACTIVE MODE (FAULT toggle)	-	8	-	ms
T_{PHOLD}	PHOLD timer	Timer starting from WKUP_FILT = 0 before to switch off the device	-	5	-	ms
$V_{WAKELPM\_ON}$	Wake pin high threshold	Compatible with 3.3 V	1.25	-	2	V
$V_{WAKELPM\_OFF}$	Wake pin low threshold	Compatible with 3.3 V	0.8	-	1.75	V
$I_{LEAK\_WAKELPM}$	Leakage current	Active mode,WAKE_LPM < 20 V	-	-	2	µA

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{LPM_24}	Load current in LPM 2.4 MHz	Fsw = 2.4 MHz	0	-	5	mA
I_{LPM_400}	Load current in LPM 400 kHz	Fsw = 400 kHz	0	-	50	mA

3.4 Typical characteristics

Figure 3. Efficiency at 2.4 MHz with V_{bat} at 14 V

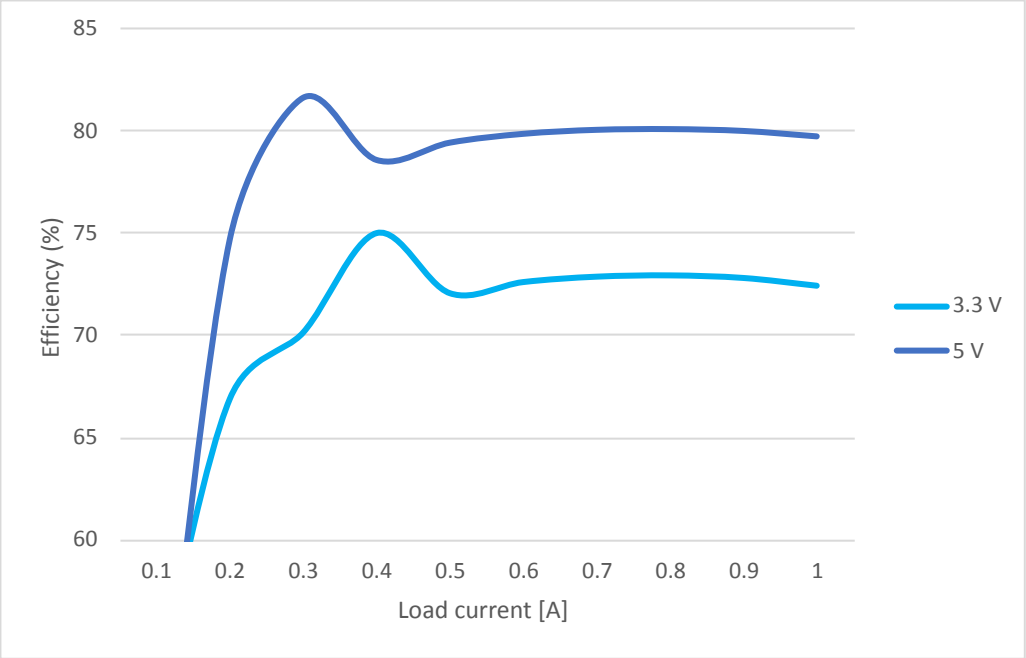
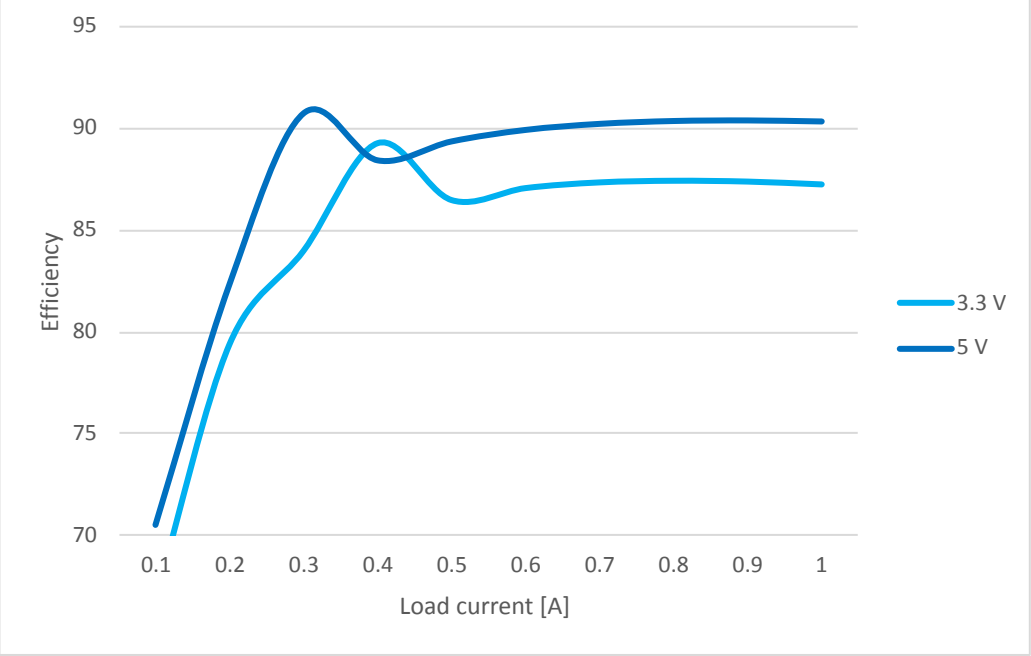


Figure 4. Efficiency at 0.4 MHz with V_{bat} at 14 V



4 Functional description

4.1 Programming by NVM

The device has an internal nonvolatile memory used to program the operating parameters.

Programmable values are:

- BUCK_VOUT_SEL, output values: if ‘00’ is 5 V, if ’01’ is 3.3 V, if ‘10’ is 1.2 V (2 bits)
- BUCK_FREQ, free running frequency: if ‘0’ is 0.4 MHz, if ‘1’ is 2.4 MHz (1 bit)
- BUCK_CURR_LIM, output current limitation: if ‘0’ is 1.0 A, if ‘1’ is 0.5 A (1 bit)
- BUCK_PGND_EN, ground loss detection: if ‘0’ is disabled, if ‘1’ is enabled (1 bit)
- BUCK_OL_EN, open load diagnosis: if ‘0’ is disabled, if ‘1’ is enabled (1 bit)
- BUCK_SS_CLK_SEL, soft start duration: if ‘0’ is 0.45 ms, if ‘1’ is 1.1 ms (1 bit)
- BUCK_UV_L, UV threshold: if’1’ is $V_{BUCKUV\_H\_0}$, if ‘0’ is $V_{BUCKUV\_H\_1}$ (1 bit). In case of 1.2 V configuration, it is mandatory to keep NVM configuration to default ($V_{BUCKUV\_H\_1}$)
- BUCK_OV_L, OV threshold: if ’0’ is V_{BUCKOV_0}, if ‘1’ is V_{BUCKOV_1} (1 bit)
- VREF_OUT, VREF output voltage: if ‘00’ is 5 V, if ’01’ is 3.3 V, if ‘10’ is 1.2 V (2 bits)
- VREF_UV_L, UV threshold: if ’0’ is V_{REFUV_0} if ‘1’ is V_{REFUV_1} (1 bit)
- VREF_OV_L, OV threshold: if ’0’ is V_{REFOV_0} if ‘1’ is V_{REFOV_1} (1 bit)
- Watchdog selection by WDI pin or through SPI (2 bits):
  - If NVM "WDG_SEL" bits are ‘00’ or ‘01’: no watchdog
  - If NVM "WDG_SEL" bits are ‘10’: watchdog by PIN
  - If NVM "WDG_SEL" bits are ‘11’: watchdog by SPI
- Effect of WD failure on FSM. If WDG_REC_EN = 0, in SPI register, and WD_REC_EN = 0, in NVM register, a WD failure asserts NRST but not REC state: the device keeps an active state with all regulators running. If one of these bits is ’1’, NRST is asserted and FSM goes to REC state.
- Effect of BUCK UV/OV failure on FSM. If BUCK_UV_REC_DIS = 1, a BUCK UV fail asserts NRST but not REC state: the device keeps an active state. If BUCK_UV_REC_DIS = 0, a BUCK UV fail asserts NRST and the device goes to REC state. If BUCK_OV_REC_DIS = 1, a BUCK OV fail asserts NRST but not REC state: the device keeps an active state. If BUCK_OV_REC_DIS = 0, a BUCK UV fail asserts NRST and the device goes to REC state.
- Effect of BUCK UV/OV failure on NRST. If BUCK_UV_RST_DIS = 1, a BUCK UV fail does not assert NRST and the device goes to REC state. If BUCK_UV_RST_DIS = 0, a BUCK UV fail asserts NRST and the device goes to REC state. If BUCK_OV_RST_DIS = 1, a BUCK OV fail does not assert NRST and the device goes to REC state. If BUCK_OV_RST_DIS = 0, a BUCK OV fail asserts NRST and the device goes to REC state.
- VREF_POWERUP_DIS chooses if VREF can be disabled or enabled through the SPI
- VREF_DELAY sets the turn on delay after BUCK > BUCK_UV_th: 0 ms, 2.5 ms, 5 ms or 10 ms (2 bits)
- NRST_RELEASE configures the release of NRST after the BUCK crosses its UV threshold or VREF crosses its UV threshold (1 bit) at power-up, with the possibility to add a delay, NRST_DELAY, from 0 ms (no delay) to 2.5 ms, 5 ms or 10 ms (2 bits)
- LPM_MODE_DIS: if ‘0’ the LPM mode is active, if ‘1’ the WAKE_LPM pin is ignored

If the PMIC has never been configured, the device automatically moves to NVM program mode to allow to program the desired configuration for the target application.

Write procedure is protected by CRC and shall be done by SPI interface. NVM PROGRAM operation can be performed only once.

The device embeds a 2 Kbits nonvolatile memory (NVM) where trimming bits are stored to calibrate the device and to configure it. The NVM area can read and written using the control register of SPI. The NVM is internally divided in 16 sectors, each of 128 bit (120 data bit and 8 CRC bit). Two different groups can be distinguished:

- 2 sectors: reserved trimming bits used to calibrate internal voltage and current (ST reserved)
- 1 sector: programmable by the user to configure the device

The MCU can read the configuration bits in NVM_CONF_STATUSx. The MCU can write the user trimming bits using the control register (WRITE_TO_NVM). The data stored in the SPI data register (NVM_CONF_CTRLx) is written inside the trimming registers of the main logic. Then, the user can decide to test the configuration by SPI command (register WRITE_TO_NVM with the command ENTER_SIM_MODE) or to upload the configuration directly inside the NVM (register WRITE_TO_NVM with the command NVM PROGRAM). When the operation is completed, a read operation starts automatically. The whole operation requires about 15 ms.

To simulate the user trimming bits, the procedure at start up is the following:

1. The MCU writes the configuration in NVM_CONF_CTRLx registers (N bits N SPI registers);
2. The MCU writes 0xAAAA (ENTER_SIM_MODE) to enter simulation mode by WRITE_TO_NVM register;
3. The MCU checks the programmed configuration at the end of power-up;
4. The MCU writes 0x5555 (EXIT_SIM_MODE) to exit from simulation mode by WRITE_TO_NVM register and it comes back to PROGRAM MODE.

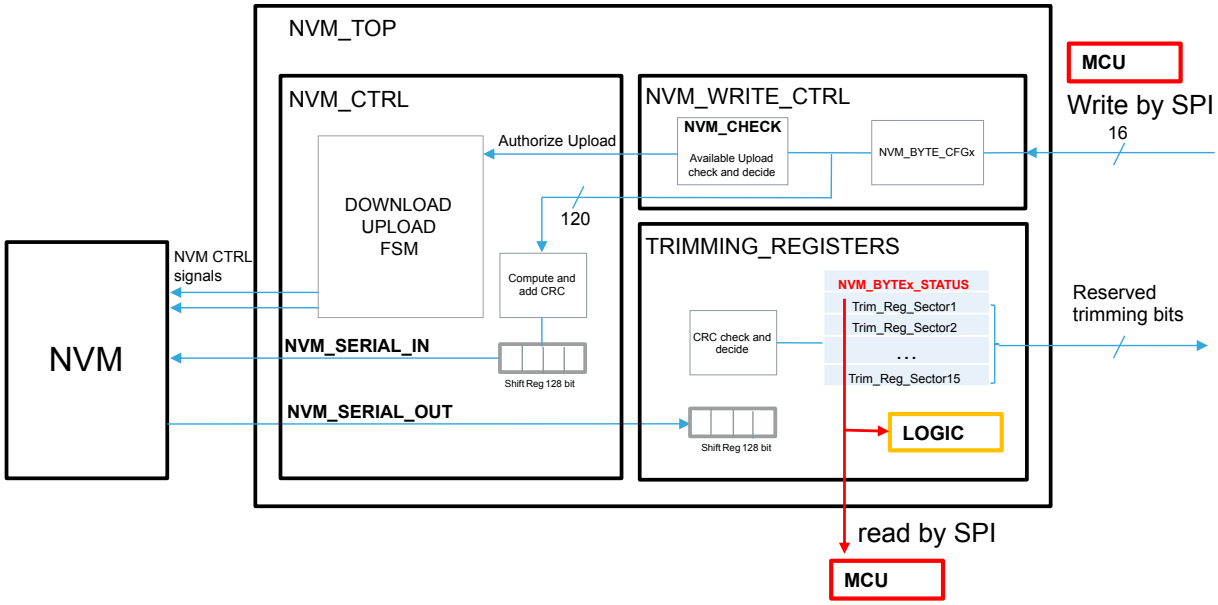
Then, the user can configure again the trimming bits to test another configuration or can perform the NVM WRITE operation. After physical NVM WRITE operation, soft-trimming procedure will not be available.

To perform the NVM write operation, the procedure is the following:

1. The MCU writes the configuration in NVM_CONF_CTRLx registers (N bits N SPI registers);
2. The MCU sends the 0xF0F0 NVM_WRITE_CTRL (WRITE_TO_NVM) command;
3. The FSM validates write operation through CRC check of SPI command and NVM CODE. If the check fails, upload operation is discarded, otherwise upload is authorized;
4. Then the CRC (8 bits) is computed on the whole sector and data is transferred inside.

Then, the NVM_PROGRAM_DONE bit is set to '1'.

Figure 5. NVM block diagram and write procedure



4.2 BUCK

The BUCK regulator operates in constant frequency peak current mode control to reduce the switching noise when the LPM is deactivated. The BUCK is enabled by the WKUP pin signal. The input voltage (VS) is compatible to the car passenger battery level. The switching frequency is set via NVM to 0.4 or 2.4 MHz with the possibility to have a spread spectrum (enabled by default and disabled via SPI). The output current can be programed via NVM to support 1.0 A and 500 mA loads.

The output voltage is programmed with internal memory cells to 3 possible values. 5 V, 3.3 V and 1.2 V. It is suggested to select the 1.2 V when the BUCK is supplied by a preregulated voltage. When configured to regulate 1.2 V, it is possible, with an external resistor divider, to select the desired regulated voltage between 1.2 V and 5 V. The user shall select a proper resistor divider value following the guidelines indicated in the Section 9: Application information. The over current protection is always active. The soft start time can be set via NVM.

The BUCK regulator provides the following diagnostics:

- Monitor of the output voltage by an independent circuit for UV/OV detection with thresholds set via NVM
- Overtemperature detection by a thermal sensor
- Overcurrent detection and limitation on integrated HS and LS MOSFET
- PGND loss detection
- Open load diagnosis during BUCK startup phase and ACTIVE MODE

BUCK fault management:

- If a UV or OV fault occurs, the FAULT pin is asserted low and the corresponding fault bit is set inside the SPI register, where it can be read and cleared. NRST is asserted only if enabled by NVM, otherwise no reset occurs. If configured by NVM, UV or OV faults move the device to the REC state.
- If OT occurs, the power stage is switched OFF when thermal ADC conversion is ready (max 500 µs). The device goes in REC state and restarts when the device is cooled down. The corresponding SPI register bit is set and the FAULT pin is asserted.
- The load overcurrent limitation is a cycle by cycle protection: if the peak current reaches the overcurrent limit, the switcher starts a cycle-by-cycle operation to limit the current until the normal operation is reached. The corresponding fault bit (BUCK_OC_STAT) is set inside the SPI register. When the current is limited, the voltage is lower than the expected value, but the regulator is able to operate normally, also with the fault bit stored. The LS MOS overcurrent detection protects the BUCK against a short to battery fault on PH pin, when BUCK_LS_OC is detected the BUCK regulator goes in high impedance.
- PGND loss detection is able to detect, at power-up, before BUCK startup phase, a ground loss fault on PGND. The corresponding fault bit (PGND_LOSS) is provided by SPI after t_{GL_filter} filter time. If configured by NVM, when the fault is detected at power-up the BUCK regulator is not enabled and the device moves to REC state (safe state). If PGND_LOSS occurs during operation, PGND_LOSS reacts immediately in the loop by forcing the minimum duty cycle, the BUCK continues to operate until the BUCK voltage goes below deep under the voltage threshold: when it happens, the BUCK is disabled and the device moves in a REC state.
- The open load detection is able to detect open FB pin fault, to protect the load (for example MCU) against over voltage events. The open load diagnosis works in a different way depending on the state of the device. During BUCK startup phase, a small pull-up current is provided to the FB pin; if the pin is open, FB goes above the BUCK_OV_L threshold, the digital FSM detects an OV and moves to REC state. During active mode, the pull-up current is disabled to avoid useless current consumption and impact the regulated voltage accuracy; if the FB pin is open, it goes below the BUCK deep under voltage threshold and, thanks to the integrated resistor divider, the digital FSM detects BUCK UV and moves to REC state. Open load diagnosis can be enabled or disabled by NVM bit.

4.3 VREF

SPSA068 includes a 1% precise voltage reference output to supply a system ADC. The output voltage can be selected via NVM cells. This regulator is disabled in LPM.

VREF provides the following diagnostics:

- Monitor of the output voltage by an independent circuit for UV/OV detection
- Overcurrent detection and limitation in case of overload or short to ground

VREF fault management:

- In case of OV, the regulator is turned off, the fault SPI register bit is set and the FAULT pin is asserted low. The power stage is turned on again only after a read and clear cycle.
- In case of UV, the fault SPI bit is set and the FAULT pin is asserted. The rail is not turned off.
- In case of OC, after 4 ms, the SPI register fault bit is set and VREF turns off. The FAULT pin is asserted. VREF turns on again when OC is removed.

4.4 Wake up pin (WKUP)

The maximum voltage this WKUP pin can sustain is limited to 40 V.

A higher voltage compliance level in the application can be achieved by applying an external series resistor between the WKUP pin and the external wake-up signal.

When the device is in STANDBY mode, it can be activated by a voltage above V_{WAKE_ON} threshold, with a minimum duration of t_{WAKE_FILTER}.

The device can be moved to STANDBY mode applying a voltage below V_{WAKE_OFF} threshold, with a minimum pulse width of t_{WAKE_FILTER} and waiting T_{PHOLD} timer. PHOLD timer starts after the detection of t_{WAKE_FILTER}.

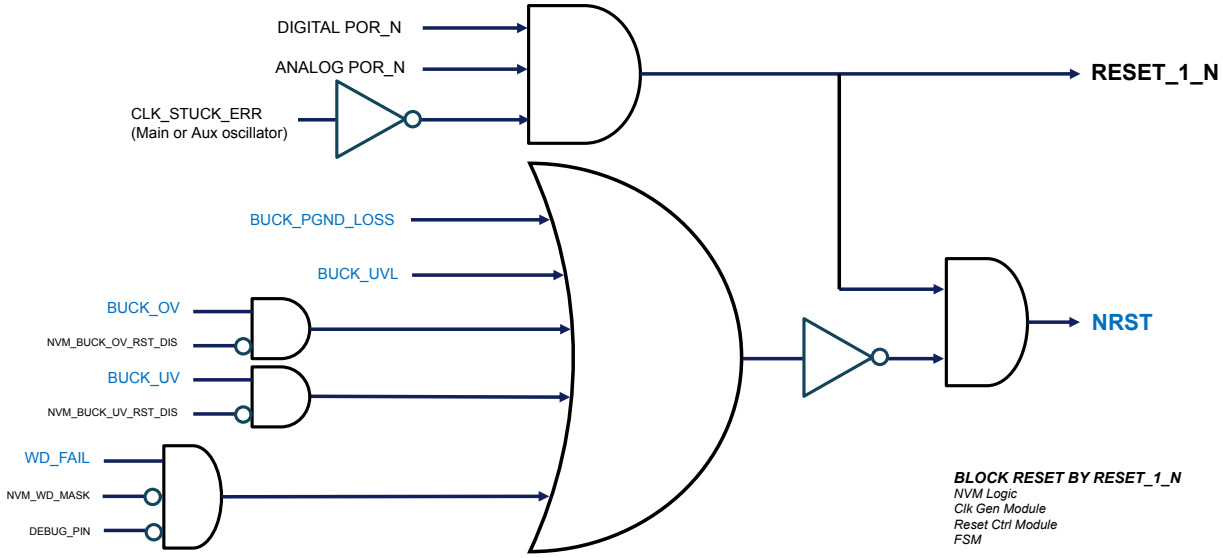
4.5 Reset and fault

In ACTIVE mode, a reset signal is generated by SPSA068 at NRST pin in case of:

- BUCK UV (can be disabled by NVM)
- BUCK OV (can be disabled by NVM)
- PGND loss on BUCK regulator by PGND comparator or BUCKUV_L threshold
- Watchdog failure (can be disabled by NVM)
- CLOCK stuck fault

The minimum pulse of NRST assertion lasts T_{NRST}.

Figure 6. Signal contribution to the reset

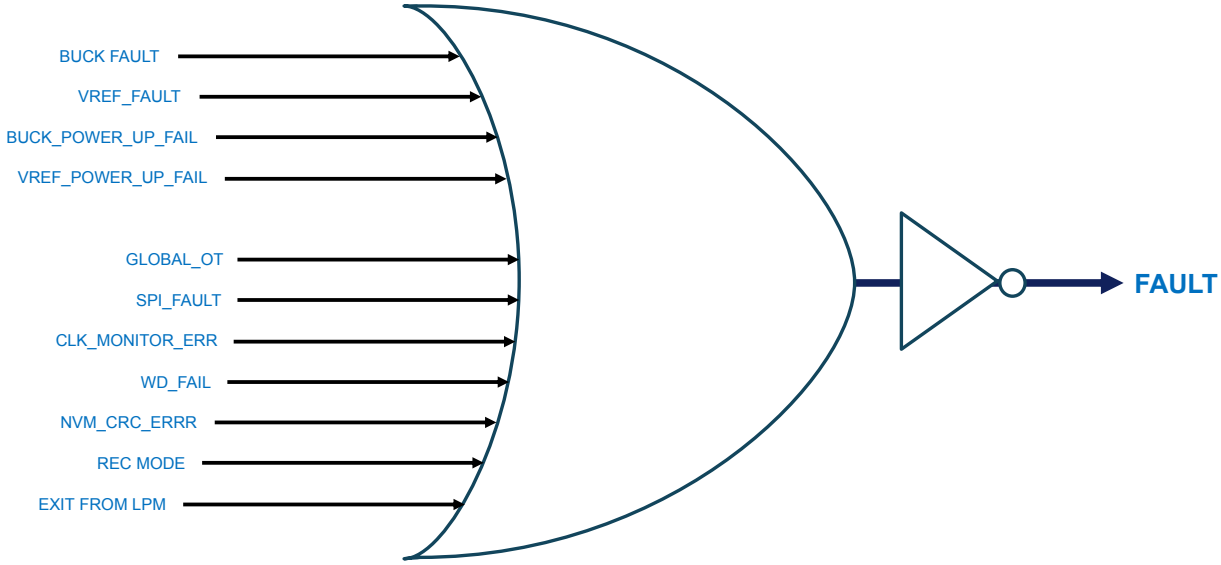


A FAULT signal, active low, is generated when one of the following events occurs:

- BUCK regulator fault
- V_{REF} fault
- OT warning and shutdown
- SPI communication error (CRC)
- Powerup fault. It is an error generated during the power-up phase in case the regulators cannot complete their own power-up phase within $T_{POWER\_ON\_TIMEOUT}$
- Digital bist error
- WD fail
- Clock monitor error
- Device is in REC mode

Furthermore, a FAULT signal is also generated after the LPM exit procedure is completed (toggling of T_{FAULT}).

Figure 7. **Signal contribution to the fault**



4.6 Configurable watchdog and reset

During normal operation, the watchdog monitors the microcontroller within a programmable trigger cycle. When the device is in ACTIVE mode, which means the power-up phase has been correctly performed and NRST signal has been released, the watchdog is started with a timeout (long open window TLW) to allow the microcontroller to run its own setup and then to start the window watchdog by setting an inner signal TRIG = 1. Subsequently, the microcontroller has to serve the watchdog by providing the watchdog trigger bit TRIG within the safe trigger area TSW. The trigger time is configurable by SPI. A correct watchdog trigger signal immediately starts the next cycle. A wrong watchdog trigger causes a watchdog failure.

WDI signal can be ignored, by setting a NVM bit, and SPI can be used as watchdog: in this case, a specific SPI register must be accessed and toggled by SPI within the watchdog window. If the register is not refreshed at the right time, a watchdog failure happens.

A 0 is written to the watchdog register at startup or when the device is reset. Via SPI it is necessary to continue to toggle the bit in the register within the watchdog window.

In case of a watchdog failure, a NRST is always asserted, and the device goes to REC mode or keeps in ACTIVE mode depending on WD_REC_en NVM configuration.

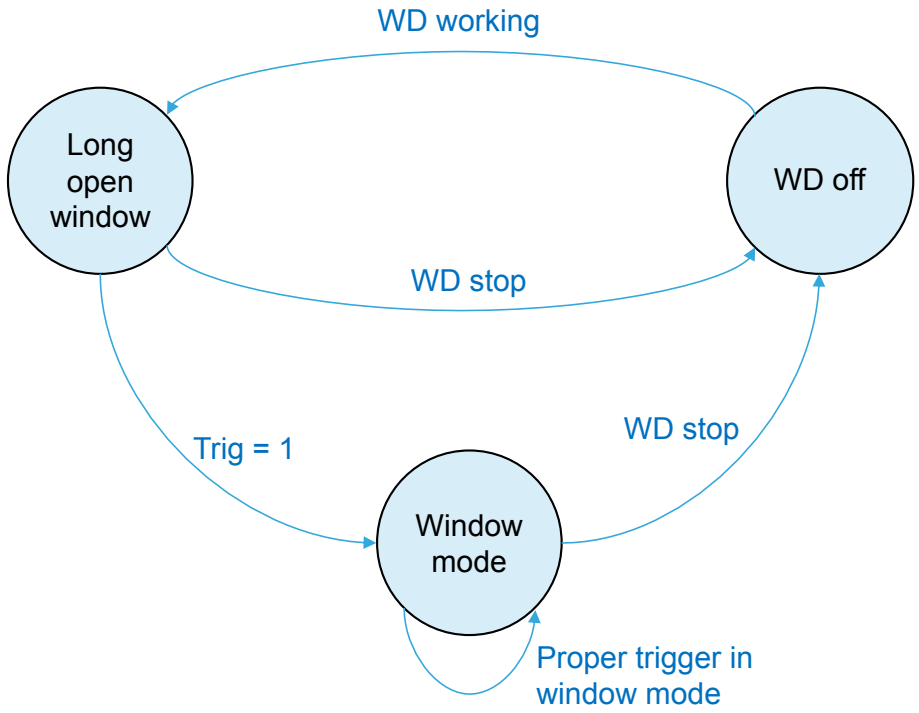
If NVM_WD_REC_en = 1 the device goes to REC mode in case of WD failure, and the WD is not more sensed until the ACTIVE mode is reached again.

If NVM_WD_REC_en = 0, the device keeps the ACTIVE mode in case of WD failure. It remains active in Long open window, but NRST asserts a small pulse (typ 8 µs). If SPI_WD_REC_en = 1, the device behavior is the same as NVM_WD_REC_en = 1, but it expects to receive the WD signal from the SPI.

Configuration with NVM_WD_REC_en = 0 is useful if voltages should be immediately active to initialize the system, regardless of the WD signal.

The following picture illustrates the watchdog behavior. The WD works in ACTIVE mode and if enabled at register level.

Figure 8. **Watchdog behavior**



The watchdog trigger time is configured through the SPI. The change of this time is not limited to the long open window. It can be changed also in "Window mode" state. However, it is suggested to write these bits only during the long window, to avoid watchdog failures. Besides, the first trigger time should be < TLW (160 ms), after that, next trigger should happen between (previous _Trigger_ time + TSW_min) and (previous _Trigger_ time + TSW_max).

Figure 9. **Watchdog timing if WD_REC_en = 1**

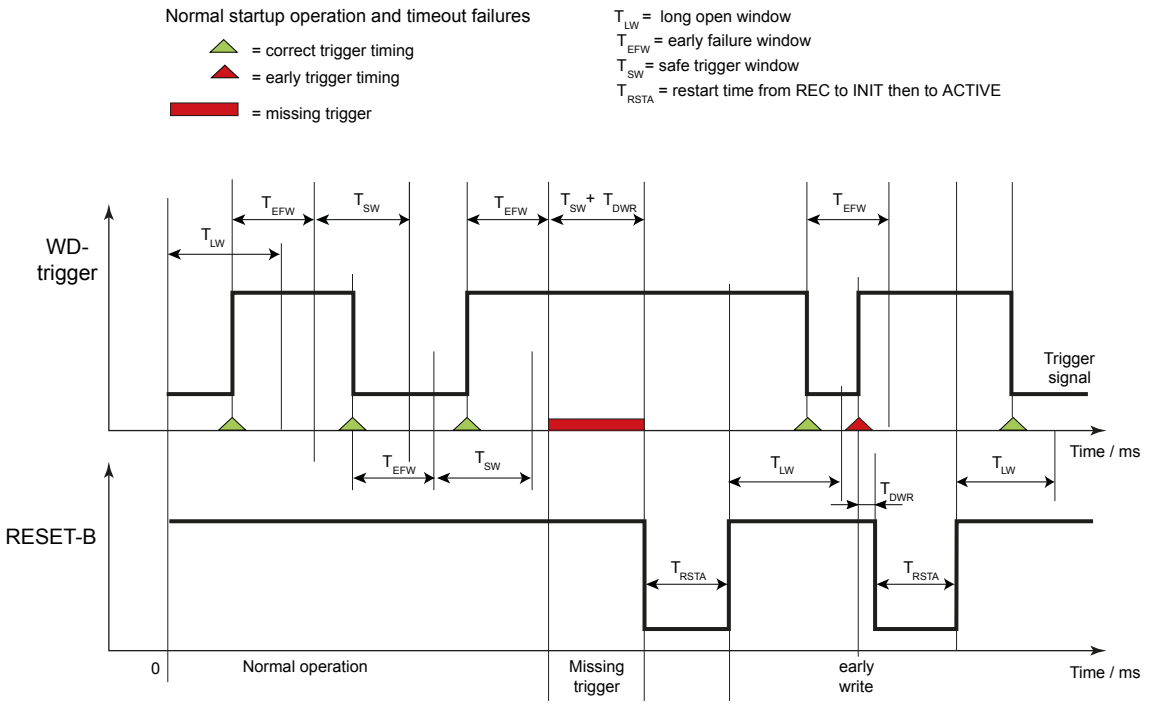


Figure 10. Watchdog timing if WD_REC_en = 0

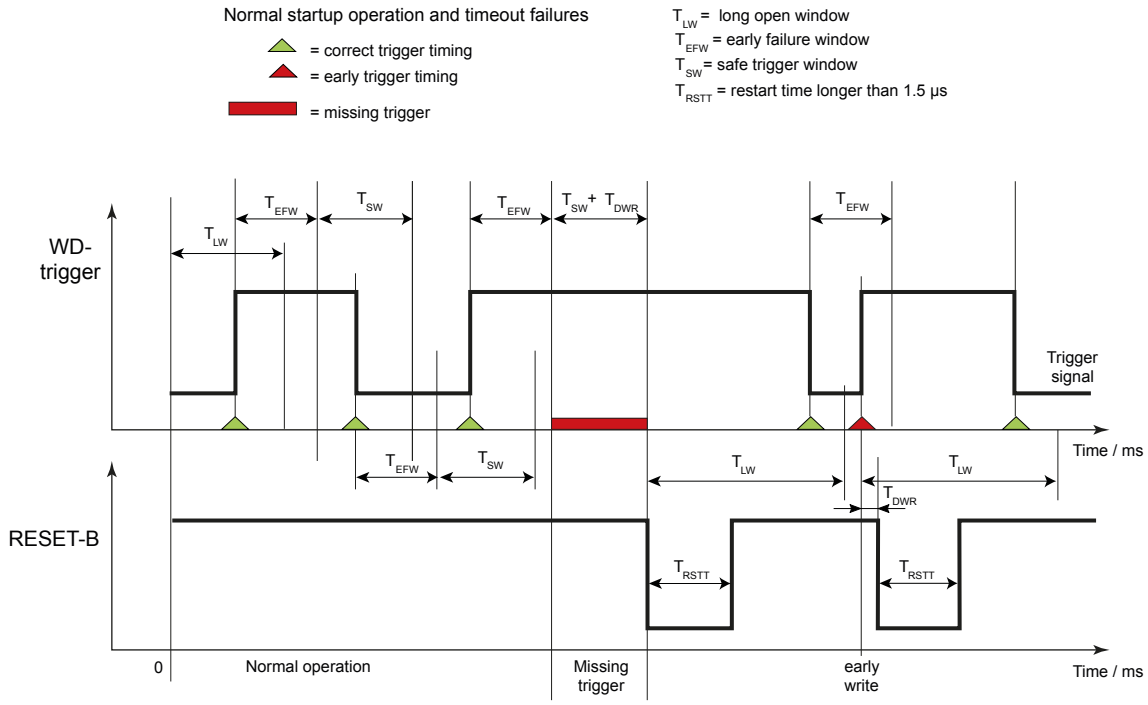
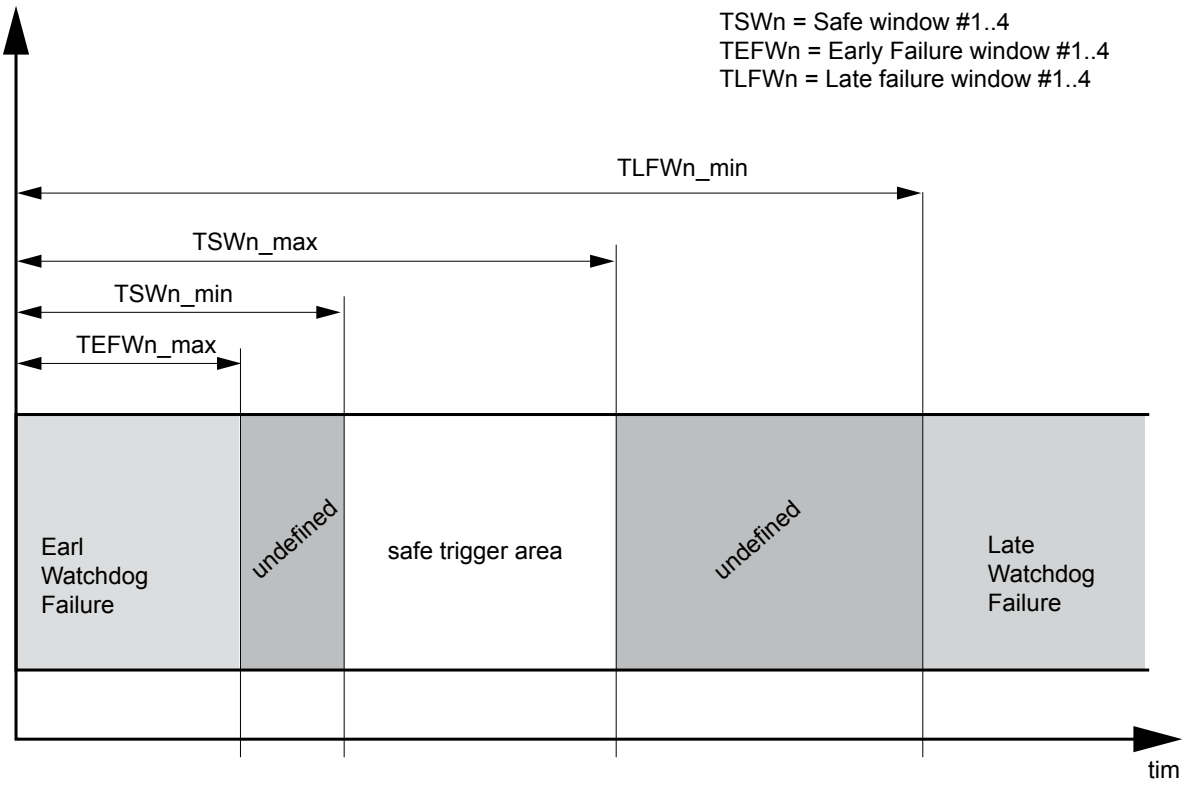


Figure 11. Watchdog early, safe and late window diagram



The WD can be temporarily disabled by keeping the DBUG pin high. This allows software debugging in the development environment.

4.7 Spread spectrum

SPSA068 features a triangular-modulation spread spectrum for 2.4 MHz at the modulation frequency of $F_{spread\_mod\_2.4}$, while for 400 kHz at $F_{spread\_mod\_400}$. The modulation frequency can be fixed or variable according to the SPI configuration: BUCK_SS_MAIN_FIXED_FMODE and BUCK_SS_AUX_FIXED_FMODE. In case of BUCK_SS_MAIN_FIXED_FMODE = '0', the $F_{spread\_mod\_2.4}$ is randomically changed in a range of $F_{spread\_mod\_rand\_2.4}$, while in case of BUCK_SS_AUX_FIXED_FMODE = '0' the $F_{spread\_mod\_400}$ is changed in a range of $F_{spread\_mod\_rand\_400}$, to avoid emissions in the audio band, and it is superposed to a higher frequency modulation of lower amplitude to ensure effectiveness in the whole frequency spectrum. Both spread spectrum's can be independently disabled by SPI.

4.8 Undervoltage and overvoltage (power-good)

Output voltages are monitored: undervoltage and overvoltage information is provided through SPI.

One SPI bit allows to select between two threshold options for each regulator.

The power on timeout for every regulator is a signal that is set to '1' if BUCK or VREF are not switched on after 3 ms. If the timeout expires, the relative power on the timeout is set and the device moves to REC state.

4.9 Temperature control

The PMIC has a thermal sensor with ADC, positioned at the center of the chip to continuously monitor the temperature of the die.

In case the temperature reaches the thermal shutdown threshold, the outputs are shut down and the device moves in REC state.

A temperature warning is signaled by the FAULT pin, written in a register and read out by SPI.

Temperature information is updated every 500 µs and it is coded in the digital domain in unsigned 8 bit word provided into a SPI register.

Temperature is calculated with the following formula:

$$Temperature\,[^{\circ}C] = 1.3706 \times CHIP\_TEMP < 15{:}8 > \; - 77.402 \quad (1)$$

5 SPI format and register mapping

A 32-bit SPI bus is used for bidirectional communication with the microcontroller and for functional and test purpose.

A write operation leads to a modification of the addressed data by the payload if a write access is allowed (for example control register, valid data). A read operation (based on previous communication request) shifts out the data present in the addressed register (out of frame data exchange protocol).

A read and clear operation will lead to a clear of addressed status bits. The bits to be cleared are defined first by payload bits set to 0.

Table 6. SPI DI and SPI DO frames

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DI	RW	ADDRESS								NVM CODE		DATA WRITE																CRC				
DO	SPI ERR	IERR	ADDRESS FDBACK									DATA READ																CRC				

Logic content is reset only by POR activation, once VBAT1 falls below the POR threshold. WD_TWIN is not reset by a reset command (or a WD fail) regardless of 'WD_REC_en' value.

DI stream:

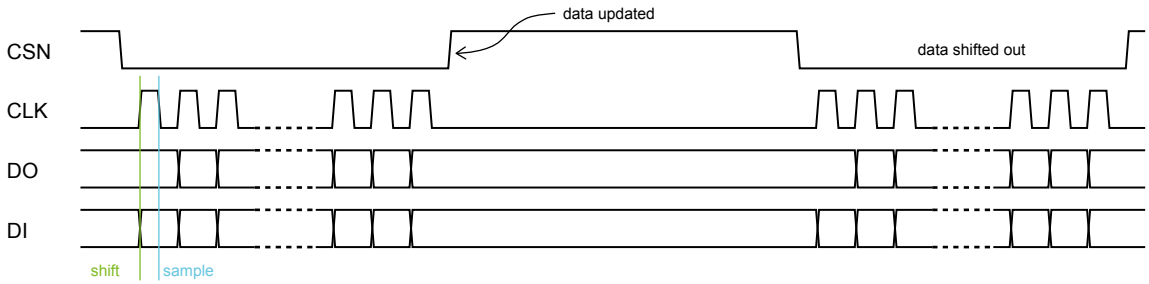
- Bit 31: R/W flag. To select read (0) or write (1) operation
- Bit 30-23: SPI register address
- Bit 22-21: NVM CODE:
  - 00 NVM NOP (NVM code/address error: in case the address field is relative to NVM operation,SPI_ERR is set)
  - 01 NVM SOFT TRIM (NVM code/address error: in case the address field is not relative to NVM operation,SPI_ERR is set)
  - 10 NVM WRITE (NVM code/address error: in case the address field is not relative to NVM operation,SPI_ERR is set)
  - 11 NVM NOP (NVM code/address error: in case the address field is relative to NVM operation,SPI_ERR is set)
- Bit 20-5: Data to be written at a selected address
- Bit 4-0: CRC code

DO stream:

- Bit 31: Previous SPI communication error (frame length error, CRC error, MOSI stuck error, address error, NVM code/address error)
- Bit 30:NRST
- Bit 29: FAULT
- Bit 28:21: SPI register address (related to the previous transmission)
- Bit 20-5: Data read at selected address (related to previous transmission)
- Bit 4-0: CRC code

Note: Bit 29 and bit 30 reflect the current status of NRST pin and FAULT pin. Every time the relevant SPI register is accessed, an internal register will sample the current status of RSTB and FAULT pins, store them, then shift them out on SPI DO frame at the next SPI access.

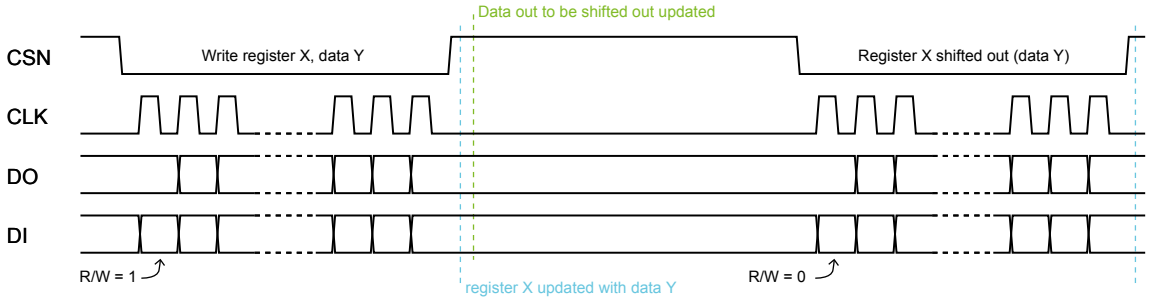
Figure 12. SPI diagram



DO is sampled by the microcontroller on CLK falling edge. DI is sampled by device on CLK falling edge. In case of writing operation selected, internal register is updated at CSN rising edge.

DO is reliable only when the BUCK is active (only in ACTIVE state), otherwise the internal pull-up is not supplied.

Figure 13. SPI protocol diagram



If SPI communication has some errors (no matter to which register), the write in data is discarded. In the next SPI communication, SPI error is communicated.

Table 7. SPI parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VCSNLOW	Input voltage low level	Normal mode	-	-	0.9	V
VCSNHIGH	Input voltage high level	Normal mode	2.3	-	-	V
VCSNHYS	VCSNHIGH - VCSNLOW	Normal mode	0.2	-	-	V
ICSNPU	Internal pull-up resistor	Normal mode	-	800	-	kΩ
Vin L	Input low level		-	-	0.9	V
Vin H	Input high level		2.3	-	-	V
Vin Hyst	Input hysteresis		0.2	0.4	-	V
I in	Pull down current at input	Vin = 1.5 V	3	6.5	10	µA
Cin	Input capacitance at input pins CSN, CLK, DI	Guaranteed by design	-	-	15	pF
fCLK	SPI input frequency at CLK		-	-	1	MHz
tCLK	Clock period		1000	-	-	ns
tCLKH	Clock high time		400	-	-	ns
tCLKL	Clock low time		400	-	-	ns
tset CSN	CSN setup time, CSN low before rising edge of CLK		500	-	-	ns
tset CLK	CLK setup time, CLK high before rising edge of CSN		500	-	-	ns
tset DI	DI setup time		25	-	-	ns

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
thold DI	DI hold time		25	-	-	ns
tCSN_HI_min	Minimum CSN high time (interframe)	Transfer of SPI-command to input register	6	-	-	µs
tr in	Rise time of input signal DI, CLK, CSN		-	-	25	ns
tf in	Fall time of input signal DI, CLK, CSN		-	-	25	ns
VDOL	Output low level	IDO = -4 mA	-	-	0.3	V
IDOLK	Open Drain leakage current	When DO output = High	-5	-	5	µA
CDO	Open Drain input capacitance	Guaranteed by design	-	10	15	pF

Note: The setup and hold timings of the SPI controller have to be considered when selecting the maximum SPI CLK frequency. While the DI signal can switch up to 1 MHz, the DO pin is connected to an open drain structure, therefore the rise and fall times of the DO signal need to be calculated as a function of the pull-up resistor (RDO_PullUp), the capacitive load (CDO_load) and the input high level and input low level thresholds of the SPI controller (see the Figure 14).

Figure 14. SPI controller

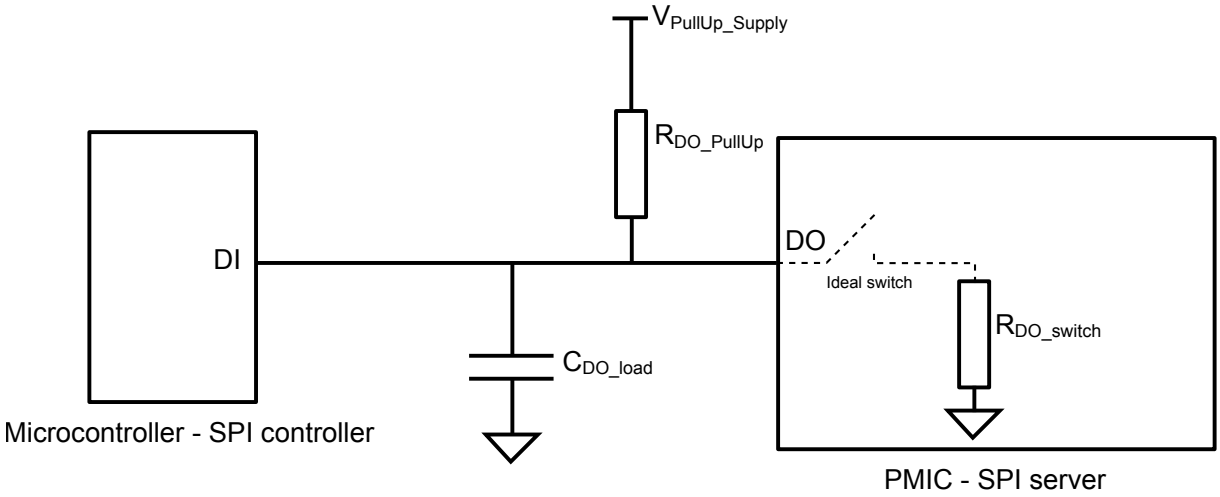
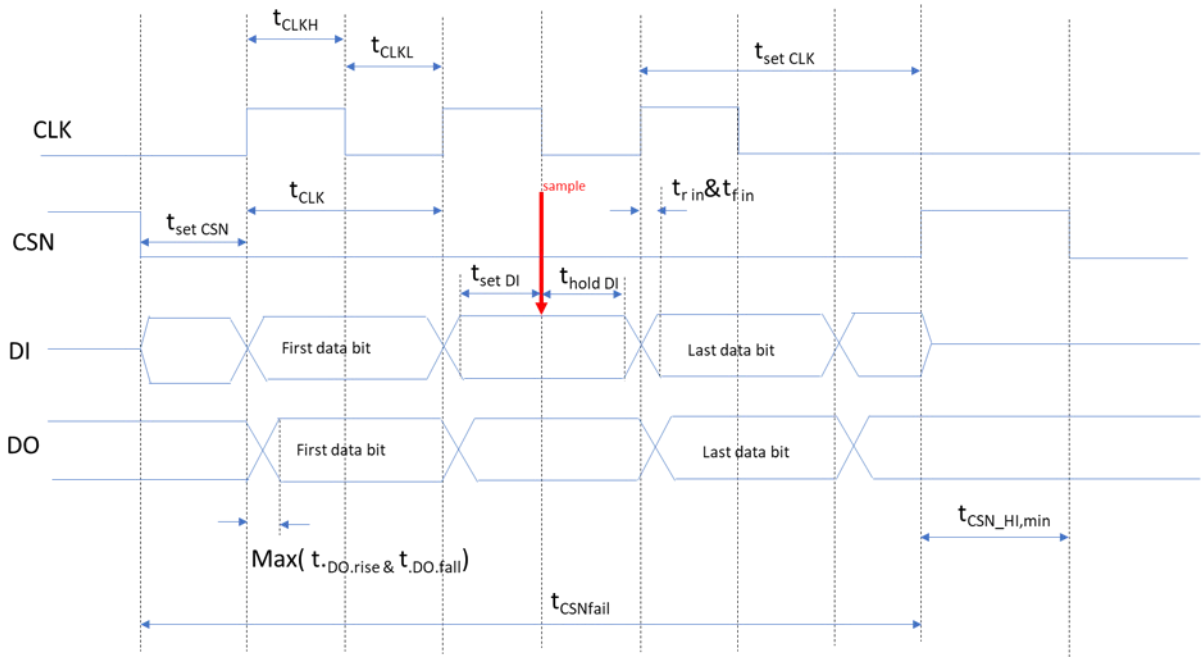


Figure 15. SPI timing diagram



$$t_{DO.fall} = \frac{In\left(\frac{\frac{V_{in.LowLevel.uC\_Port}}{V_{PullUp.Supply}} - \frac{R_{DO.switch}}{R_{DO.Switch} + R_{DO.PullUp}}}{\left(1 - \frac{R_{DO.switch}}{R_{DO.switch} + R_{DO.PullUp}}\right)}\right)}{\frac{1}{R_{DO.PullUp} \times C_{DO.load}} - \frac{1}{R_{DO.switch} \times C_{DO.load}}} \quad (2)$$

$$t_{DO.rise} = -C_{DO.load} \times R_{DO.PullUp} \times In\left(1 - \frac{V_{in.HighLevel.uC\_Port}}{V_{PullUp.Supply}}\right) \quad (3)$$

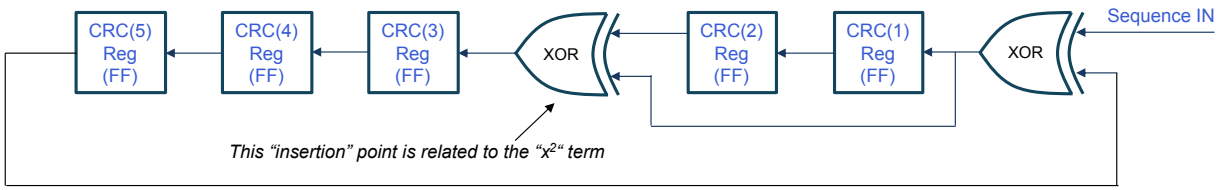
The SPI protocol is defined by frames of 32 bits with 5 bits of CRC (cyclic redundancy check) in both input and output directions. The polynomial calculation implemented is:

$$g(x) = x^5 + x^2 + 1 \quad (4)$$

With INIT value equal to 5'b11111

The "forward" architecture is not a pure polynomial divider. The CRC value of the "input sequence" can be read on the register bits just after the last input sequence's bit has entered the architecture.

Figure 16. SPI CRC "forward" architecture



In "forward" architecture, not only the CRC MSB, but also the Sequence Input enters the injection points

5.1 Register mapping

When registers are not written, their default state is the one shown in the respective map.

Table 8. SPI register mapping

Field name	Type	Value	Reset	Description
CHIPID_TEMP - 0x0				
CHIP_TEMP<15:8>	RO	0x0	POR	Chip temperature
DEVICE_ID<7:0>	RO	0x0	POR	Device identification number
BUCK_VREF_CTRL - 0x1				
RESERVED<15:11>	RO	0x0	POR	RESERVED
NVM_CLK_STOP<10>	RW	0x0	NRST	0: default clock setting 1: gating clock NVM
FAULT_TOGGLE<9:7>	RW	0x0	NRST	101: set fault pin 'low' 110: set fault pin 'high' Others: keep fault pin as original fault output
VREF_DIS<6>	RW	0x0	NRST	1: disabling VREF through SPI (only if VREF is in power-up sequence)
VREF_EN<5>	RW	0x0	NRST	1: enabling VREF through SPI (only if VREF is not in power-up sequence)
BUCK_SPREAD_AUX_EN<4>	RW	0x1	POR	0: spread spectrum disabled 1: spread spectrum aux osc enabled (default)
BUCK_SPREAD_MAIN_EN<3>	RW	0x1	POR	0: spread spectrum disabled 1: spread spectrum main osc enabled (default)
BUCK_SS_AUX_FIXED_FMODE<2>	RW	0x1	POR	0: osc aux spread spectrum random modulation frequency 1: osc aux spread spectrum fixed modulation frequency
BUCK_SS_MAIN_FIXED_FMODE<1>	RW	0x1	POR	0: osc main spread spectrum random modulation frequency 1: osc main spread spectrum fixed modulation frequency
BUCK_SLEW_RATE<0>	RW	0x0	POR	0: slow 16 ns (default) 1: fast 12 ns
POWER_STATUS - 0x2				
RESERVED<15:14>	RO	0x0	POR	-
DGND_LOSS	RLR	0x0	POR	0: no fault (clear on read) 1: Digital gndloss fault
VREF_POWERUP_FAULT	RLR	0x0	POR	0: no fault (clear on read) 1: VREF power-up timeout fault
BUCK_POWERUP_FAULT	RLR	0x0	POR	0: no fault(clear on read) 1: BUCK power-up timeout fault
VS_UV	RLR	0x0	POR	0: no fault (clear on read) 1: VS undervoltage fault
OT_WARN	RLR	0x0	POR	RESERVED
OT_GLOBAL	RLR	0x0	POR	0: no fault (clear on read) 1: OT fault
VREF_OC	RLR	0x0	POR	0: no fault (clear on read) 1: VREF overcurrent fault

Field name	Type	Value	Reset	Description
VREF_OV	RLR	0x0	POR	0: no fault (clear on read) 1: VREF overvoltage fault
VREF_UV	RLR	0x0	POR	0: no fault (clear on read) 1: VREF undervoltage fault
BUCK_OC	RLR	0x0	POR	0: no fault (clear on read) 1: BUCK overcurrent fault
BUCK_GND_LOSS	RLR	0x0	POR	0: no fault (clear on read) 1: BUCK gndloss fault
BUCK_OV	RLR	0x0	POR	0: no fault (clear on read) 1: BUCK overvoltage fault
BUCK_UVH	RLR	0x0	POR	0: no fault (clear on read) 1: BUCK undervoltage 1 fault
BUCK_UVL	RLR	0x0	POR	0: no fault (clear on read) 1: BUCK undervoltage 2 fault
DEVICE_STATUS - 0x3				
FAULT_SELFTEST_ERR	RLR	0x0	POR	0: no fault (clear on read) 1: FAULT seft test fault
WDG_SELFTEST_ERR	RLR	0x0	POR	0: no fault (clear on read) 1: WDG ST fault
NRST_SELFTEST_ERR	RLR	0x0	POR	0: no fault (clear on read) 1: NRST ST fault
OT_SELFTEST_ERR	RLR	0x0	POR	0: no fault (clear on read) 1: OT ST fault
CLK_MON_SELFTEST_ERR	RLR	0x0	POR	0: no fault (clear on read) 1: CLK MON ST fault
CLK_STUCK_ERR	RLR	0x0	POR	0: no fault (clear on read) 1: CLK MAIN STUCK fault
CLK_FREQ_ERR	RLR	0x0	POR	0: no fault (clear on read) 1: CLK MAIN FREQ fault
ABIST_ERR	RO	0x0	POR	0: no fault 1: ABIST fault
NVM_PROGRAM_DONE	RO	0x0	POR	0: NVM is not programmed 1: NVM programmed
NVM_READY	RO	0x0	POR	0: NVM not downloaded 1: NVM downloaded
NVM_USER_CRC_ERR	RO	0x0	POR	0: no crc error in user sector 1: CRC error in user sector
NVM_CRC_ERR	RO	0x0	POR	0: no CRC error 1: CRC error
WDG_ERR_FLAG	RLR	0x0	POR	0: no fault (clear on read) 1: Watchdog fault
FAULT_FLAG	RLR	0x0	POR	0: no fault (clear on read) 1: Fault pin asserted

Field name	Type	Value	Reset	Description
NRST_FLAG	RLR	0x0	POR	0: no fault (clear on read) 1: NRST pin asserted
POR_FLAG	RLR	0x0	POR	0: no POR (clear on read) 1: POR asserted
WDG_CTRL - 0x4				
RESERVED<15:1>	RO	0x0	POR	RESERVED
WDG_CMD	RW	0x0	NRST	0: wdg signal low 1: wdg signal high
WDG_CFG - 0x5				
RESERVED<15:6>	RO	0x0	POR	RESERVED
WDG_REC_EN<5>	RW	0x0	POR	0: disable 1: wdg fault moves device to recovery state
WDG_TIME_WINDOW<4:3>	RW	0x0	POR	Watchdog window timer selection 00: 10 ms 01: 20 ms 10: 40 ms 11: 80 ms
WAKE_RETRY_TIMER<2:1>	RW	0x0	POR	00: 10 ms 01: 20 ms 10: 40 ms 11: 80 ms
WAKE_INF_RETRY_EN<0>	RW	0x0	POR	0: 3 times retry 1: infinite retry
FSM_STATUS - 0x6				
RESERVED<15:12>	RO	0x0	POR	RESERVED
DEBUG_ECHO<11>	RO	0x0	POR	tm pin echo
TM_FSM_STATUS<10:6>	RO	0x0	POR	RESERVED
PROGRAM_VERIFY_ERR<5>	RO	0x0	POR	0: no fault 1: NVM program verify fault
ERASE_VERIFY_ERR<4>	RO	0x0	POR	0: no fault 1: NVM erase verify fault
DEVICE_STATE<3:0>	RO	0x0	POR	FSM state 0010: PROGRAM 0011: RECOVERY 0110: ACTIVE
SPI_STATUS - 0x7				
RESERVED<15:7>	RO	0x0	POR	RESERVED
LPM_ACCESS_ERR<6>	RLR	0x0	POR	0: no fault 1: SPI LPM access code fault
NVM_ACCESS_ERR<5>	RLR	0x0	POR	0: no fault 1: SPI NVM access code fault
FRAME_LONG<4>	RLR	0x0	POR	0: no fault 1: SPI frame long fault

Field name	Type	Value	Reset	Description
FRAME_SHORT<3>	RLR	0x0	POR	0: no fault 1: SPI frame short fault
CRC_ERR<2>	RLR	0x0	POR	0: no fault 1: SPI frame crc fault
FRAME_ERR<1>	RLR	0x0	POR	0: no fault 1: SPI frame generic fault
ADDR_ERR<0>	RLR	0x0	POR	0: no fault 1: SPI frame address fault
LPM_ENTER - 0x8				
LPM_ENTER_CODE<15:0>	WO	0x0	POR	LPM ENTER CODE: 0xA55A
WRITE_TO_NVM (programming section) - 0x9				
NVM_PROGRAM_CODE<15:0>	WO	0x0	POR	ENTER SIM MODE: 0xAAAA EXIT SIM MODE: 0x5555 NVM PROGRAM: 0xF0F0
NVM_CONF_CTRL1 (programming section) - 0xA				
WD_REC_EN<15>	RW	0x0	POR	0: disabled 1: WD moves the device to REC state
WDG_SEL<14:13>	RW	0x0	POR	00: watchdog monitoring disabled 01: watchdog monitoring disabled 10: watchdog by pin 11: watchdog by SPI
VREF_OV_L<12>	RW	0x0	POR	0: OV threshold at V_{REFOV_0} 1: OV threshold at V_{REFOV_1}
VREF_UV_L<11>	RW	0x0	POR	0: UV threshold at V_{REFUV_0} 1: UV threshold at V_{REFUV_1}
VREF_OUT<10:9>	RW	0x0	POR	00: VREF output voltage 5 V 01: VREF output voltage 3.3 V 10: VREF output voltage 1.2 V 11: n/a
BUCK_OL_EN<8>	RW	0x0	POR	0: open load diagnosis disabled 1: open load diagnosis enabled
BUCK_PGND_EN<7>	RW	0x0	POR	0: power ground loss detection disabled 1: power ground loss detection enabled
BUCK_CURR_LIM<6>	RW	0x0	POR	0: output current limitation 1 A 1: output current limitation 0.5 A
BUCK_FREQ<5>	RW	0x0	POR	0: free run frequency 0.4 MHz 1: free run frequency 2.4 MHz
BUCK_OV_L<4>	RW	0x0	POR	0: OV threshold at V_{BUCKOV_0} 1: OV threshold at V_{BUCKOV_1}
BUCK_UV_L<3>	RW	0x0	POR	0: UV threshold at V_{BUCKUV_0} 1: UV threshold at V_{BUCKUV_1}
BUCK_SS_CLK_SEL<2>	RW	0x0	POR	0: soft start duration 1.1 ms

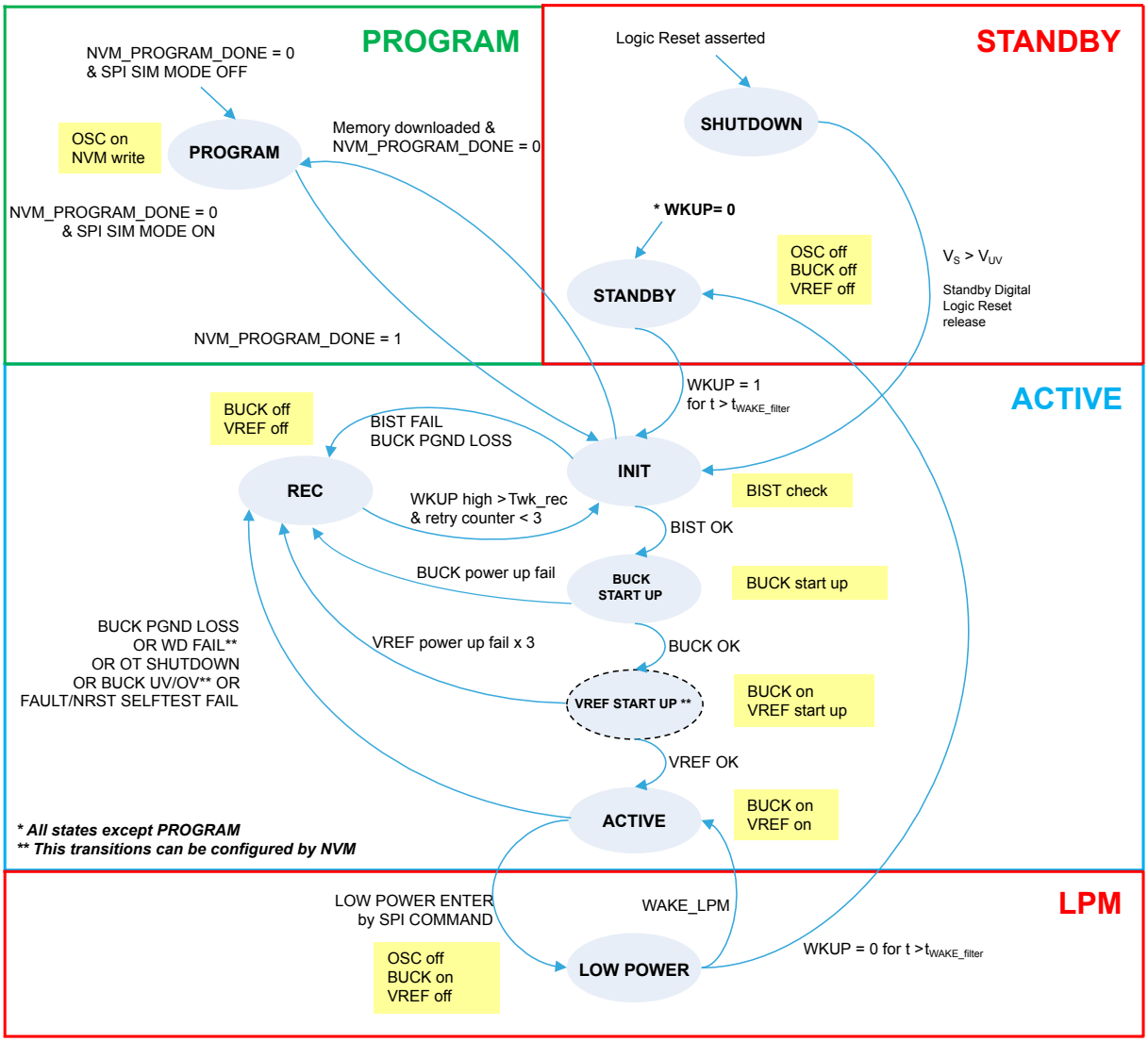
Field name	Type	Value	Reset	Description
				1: soft start duration 0.45 ms
BUCK_VOUT_SEL<1:0>	RW	0x0	POR	00: BUCK output voltage 5 V 01: BUCK output voltage 3.3 V 10: BUCK output voltage 1.2 V 11: n/a
NVM_CONF_CTRL2 (programming section) - 0xB				
RESERVED<15:11>	RO	0x0	POR	RESERVED
LPM_MODE_DIS<10>	RW	0x0	POR	0: LPM enabled 1: LPM disabled
NRST_DELAY<9:8>	RW	0x0	POR	00: no delay 01: 2.5 ms delay 10: 5 ms delay 11: 10 ms delay
NRST_RELEASE<7>	RW	0x0	POR	0: NRST release after VREF 1: NRST release after BUCK
VREF_DELAY<6:5>	RW	0x0	POR	00: no delay 01: 2.5 ms delay 10: 5 ms delay 11: 10 ms delay
VREF_POWERUP_DIS<4>	RW	0x0	POR	0: VREF enable by SPI 1: VREF not manageable by SPI
BUCK_OV_RST_DIS<3>	RW	0x0	POR	0: OV asserts NRST 1: OV does not assert NRST
BUCK_UV_RST_DIS<2>	RW	0x0	POR	0: UV asserts NRST 1: UV does not assert NRST
BUCK_OV_REC_DIS<1>	RW	0x0	POR	0: OV moves to REC state 1: OV does not move to REC
BUCK_UV_REC_DIS<0>	RW	0x0	POR	0: UV moves to REC state 1: UV does not move to REC
NVM_CONF_STATUS1 - 0xC				
WD_REC_EN_READ<15>	RO	0x0	POR	-
WDG_SEL_READ<14:13>	RO	0x0	POR	-
VREF_OV_L_READ<12>	RO	0x0	POR	-
VREF_UV_L_READ<11>	RO	0x0	POR	-
VREF_OUT_READ<10:9>	RO	0x0	POR	-
BUCK_OL_EN_READ<8>	RO	0x0	POR	-
BUCK_PGND_EN_READ<7>	RO	0x0	POR	-
BUCK_CURR_LIM_READ<6>	RO	0x0	POR	-
BUCK_FREQ_READ<5>	RO	0x0	POR	-
BUCK_OV_L_READ<4>	RO	0x0	POR	-
BUCK_UV_L_READ<3>	RO	0x0	POR	-
BUCK_SS_CLK_SEL_READ<2>	RO	0x0	POR	-
BUCK_VOUT_SEL_READ<1:0>	RO	0x0	POR	-

Field name	Type	Value	Reset	Description
NVM_CONF_STATUS2 - 0xD				
RESERVED <15:11>	RO	0x0	POR	-
LPM_MODE_DIS_READ<10>	RO	0x0	POR	-
NRST_DELAY_READ<9:8>	RO	0x0	POR	-
NRST_RELEASE_READ<7>	RO	0x0	POR	-
VREF_DELAY_READ<6:5>	RO	0x0	POR	-
VREF_POWERUP_DIS_READ<4>	RO	0x0	POR	-
BUCK_OV_RST_DIS_READ<3>	RO	0x0	POR	-
BUCK_UV_RST_DIS_READ<2>	RO	0x0	POR	-
BUCK_OV_REC_DIS_READ<1>	RO	0x0	POR	-
BUCK_UV_REC_DIS_READ<0>	RO	0x0	POR	-
SELF_TEST_STATUS - 0xE: RESERVED				
TM_REG - 0xFE: RESERVED				

6 Device operating mode

SPSA068 can work in different operative modes according to input/SPI signals, NVM/SPI settings, fault management and regulators status.

Figure 17. Device operating mode chart



Shutdown mode

In shutdown mode the supply battery VS is not present and all regulators are OFF. A rising edge on VS line triggers a “first switch to battery” procedure. The device is switched-on, and moves to INIT state, where NVM content is downloaded and the NVM check is executed. If the NVM is programmed and WKUP pin remains low, the device moves to standby mode, otherwise it moves to NVM programming mode.

Program mode

In program mode it is possible to both simulate and write the configuration in the NVM through the SPI. It is recommended to simulate the configuration before sending the write command, since after the first write operation it is not possible to modify again the physical values inside the NVM. After performing the soft-trimming (see the Section 4.1: Programming by NVM), it is necessary to send a SPI frame command to enter the simulation mode. The device moves to INIT state and continues the power-up sequence with the selected configurations. After the end of the simulation mode, the SPSA068 goes back in program mode by EXIT_SIM_MODE command. If the user sends the command to physically program the NVM, the NVM is written with the programming bit to ‘1’. After that, the SPSA068 moves to INIT state.

Standby mode

In standby mode, all the regulators are OFF and current consumption is very low, only the standby logic is biased. A low to high transition on WKUP pin moves the IC to INIT mode. If VS falls below POR threshold, the device goes back to shutdown mode.

Standby mode is, by definition, a safe state.

INIT mode

In INIT mode all the functional checks on analog and digital circuitry are performed:

- NVM check: data integrity is verified by CRC check and NVM PROGRAM bit is checked
- Analog BIST on relevant monitor
- Digital BIST(apart FAULT and NRST check)
- Check if VS is ok
- BUCK PGND loss check
- Overtemperature self-test

In case of one of this check fails, the device moves to REC state (FAULT pin kept asserted).

DBIST runs also in ACTIVE state. In case of issues during DBIST, the IC moves to REC mode and the FAULT pin is asserted.

Besides, DBIST includes:

- Clock stuck
- NRST and FAULT assertion and path are checked (only in ACTIVE mode)
- WD logic

If all the checks are completed without any fail, SPSA068 moves to REG_START_UP mode. A transition (high to low) on WKUP moves the state machine back to STANDBY.

BUCK and VREF startup mode

When the device moves to BUCK startup mode, the Buck regulator is turned on. After the BUCK crosses the UV threshold, the device moves to VREF startup mode, where VREF is turned on. If VREF is not part of the power on sequence, now it can be turned on by SPI, if requested.

When the BUCK starts the power-up phase, a power good timer starts, whose duration is typically 3 ms. If BUCK_UV goes low before the timer expires, the device moves to VREF startup, where VREF is turned on after the NVM programmed delay.

We can have two possible scenarios:

- BUCK power-up phase fails, that means BUCK_UV is still ‘1’ after timeout: the device moves to REC phase (VREF kept OFF)
- VREF power-up phase fails: the FAULT pin is asserted and NRST signal is kept low according to NVM configuration. If the VREF power-up phase fails, a retry immediately starts. The retry phase is done three times: if the fail is still present, then the device moves to REC state. While, if VREF is activated in ACTIVE mode by SPI or after exiting from LPM, VREF_UV is masked until $T_{POWER\_ON\_TIMEOUT}$ is expired, otherwise the FAULT pin is asserted.

NRST signal release can be programmed via NVM:

- If only the BUCK is enabled in NVM, it is released after the BUCK is inside the target regulation
- If both the BUCK and the VREG are enabled in NVM, it is released after BUCK and VREF are both inside the target regulation

Moreover, NRST release can be delayed according to POWER_ON_DELAY bits programmed by NVM.

REC mode

When the IC moves from the active to REC state, all regulators switch off at the same time.

In this state, the FAULT pin is asserted and NRST is kept low according to NVM. There are 2 ways to move the device out of REC:

- A transition high to low on WKUP pin moves the IC back to Standby MODE, where the FAULT pin is deasserted.
- If WKUP pin is kept high for a time longer than Twk_rec and the IC goes in REC mode less than a number of times (3 times if WAKE_INF_RETRY_EN = 0, infinite times if WAKE_INF_RETRY_EN = 1), then the device moves from REC to INIT and restarts again.

When the chip enters the REC mode, all the functions of the IC are switched off, only internal regulators and main logic are always enabled. In case the device moves to REC mode due to a fault that disables VREF and BUCK, their voltage are discharged by an internal fast discharge current typical of 12 mA.

REC mode is the “safe state” of the device when WKUP pin is HIGH.

ACTIVE mode

In ACTIVE mode the regulators are ON and the device is controlled by SPI: VREF can be turned on and off via SPI.

If a fault occurs, the device can stays in ACTIVE mode or moves to REC, depending on the kind of fault.

- BUCK UV/OV, if relative NVM bit is set to ‘1’, moves the IC to the REC phase.
- WD failure asserting NRST depends on NVM bit WD_REC_EN: if WD_REC_EN = 1, the PMIC moves to REC phase; if WD_REC_EN = 0, the PMIC keeps in ACTIVE mode.
- OT thermal shutdown moves the IC to REC mode
- BUCK PGND loss and buck open load moves the device to REC mode

WKUP pin is continuously monitored: if the signal goes low after a filtering time, then SPSA068 goes back to standby mode state after the proper power down phase. If WKUP is set to ‘0’, PHOLD timer is activated, and FAULT is asserted.

If WKUP is set to ‘1’ before the timer expires, FAULT pin is deasserted and the device remains ACTIVE. Otherwise, if the PHOLD timer expires, the device is switched off.

LOW POWER mode

The low power mode is enabled by NVM. The low power mode maximizes the efficiency at light-load. The LPM operation satisfies the requirements of the applications directly and constantly connected to the car battery, that have to operate when the engine is off. The typical load when the car is parked is represented by a microcontroller in standby mode with memory content still present (total load is around 10 - 50 µA).

In low power mode only the BUCK is enabled. In LPM the Buck operates with lower and variable frequency depending on the load current.

The LPM is activated by a dedicated SPI command ans deactivated by the WAKE_LPM pin as soon as the microcontroller receives the wake-up command from the system.

If no fault is active, after the LPM entering procedure is received, the device enters the LPM and the NRST pin is kept HIGH (no asserted). In LPM, the NRST pin cannot be asserted by any source.

After the LPM exiting procedure is received, the device moves to ACTIVE mode and the NRST is kept high

The FAULT pin kept high in LPM.

The FAULT pin toggles as soon as device goes back in ACTIVE mode. After the FAULT toggles, the MCU can absorb I_{active} current.

The WKUP pin is continuously monitored.

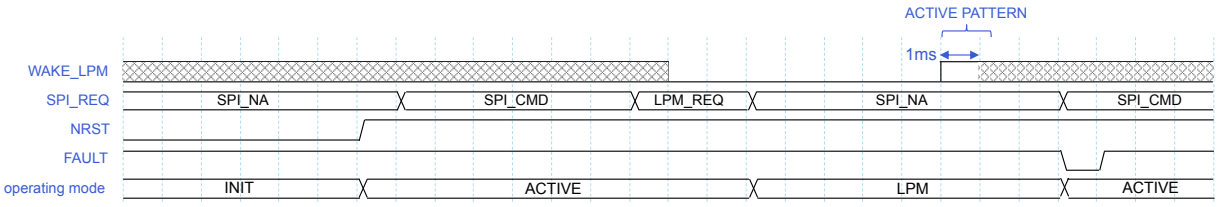
If WKUP is set to '0', after a filtering time (t_{WAKE_filter}) SPSA068 moves to ACTIVE mode.

When WKUP is '0', the PHOLD timer is active, while the FAULT pin remains asserted.

Then, if WKUP is set again to '1' before the timer expires, the FAULT is deasserted and the device remains ACTIVE.

Otherwise, if the PHOLD timer expires, SPSA068 moves to STANDBY mode.

Figure 18. Example of LPM communication

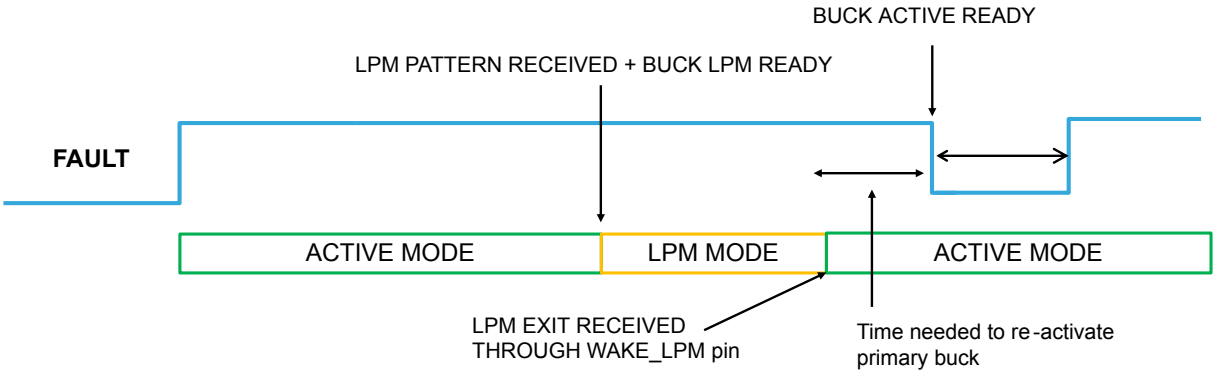


In case of FAULT during the LPM request, LPM entering is aborted.
The device moves to REC state.
In case WAKE_LPM is set high during T_{LPM_EN}, LPM entering is aborted.

WAKE_LPM is ignored in ACTIVE MODE

If WAKE_LPM is already active (set to '1') when the LPM request is done, LPM enter will be aborted.

Figure 19. **FAULT signal behavior**



PIN/STATE	STBY	ACTIVE	LPM
NRST	1	0/1	1
FAULT	1	0/1	1

7 Power-up sequence

The state machine that controls the power on of the BUCK and the VREF is shown in the following figures.

Figure 20. BUCK FSM

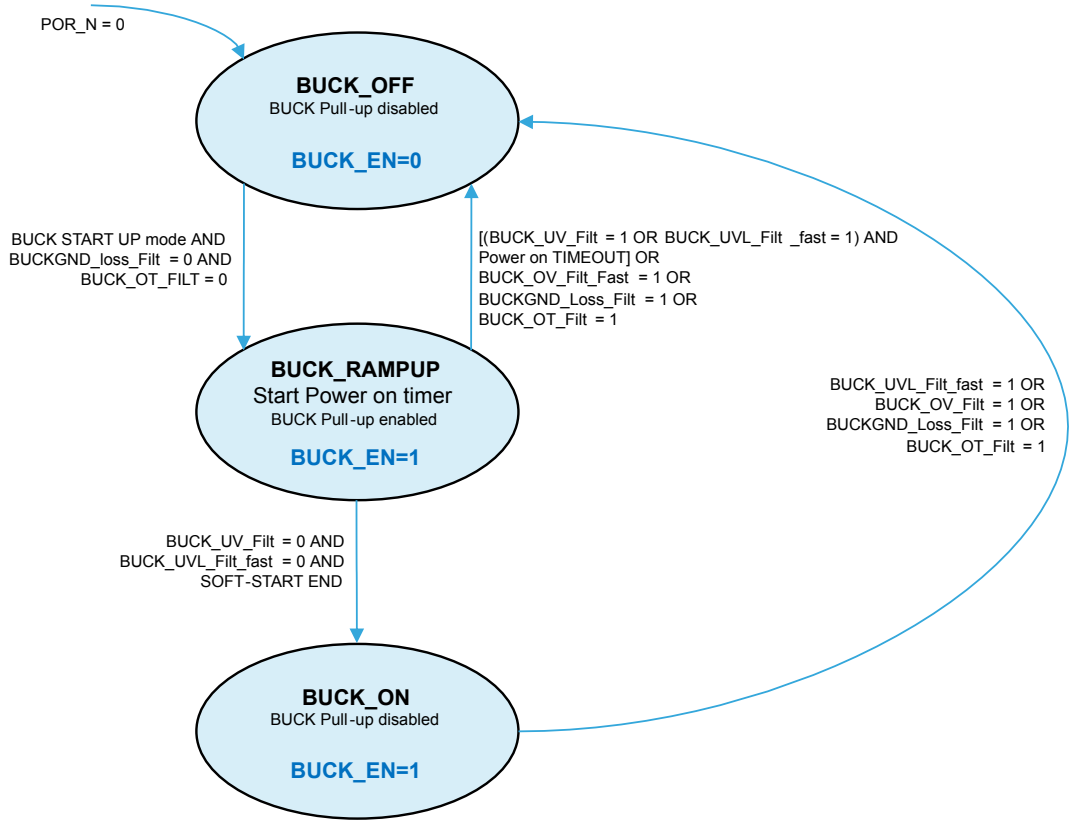
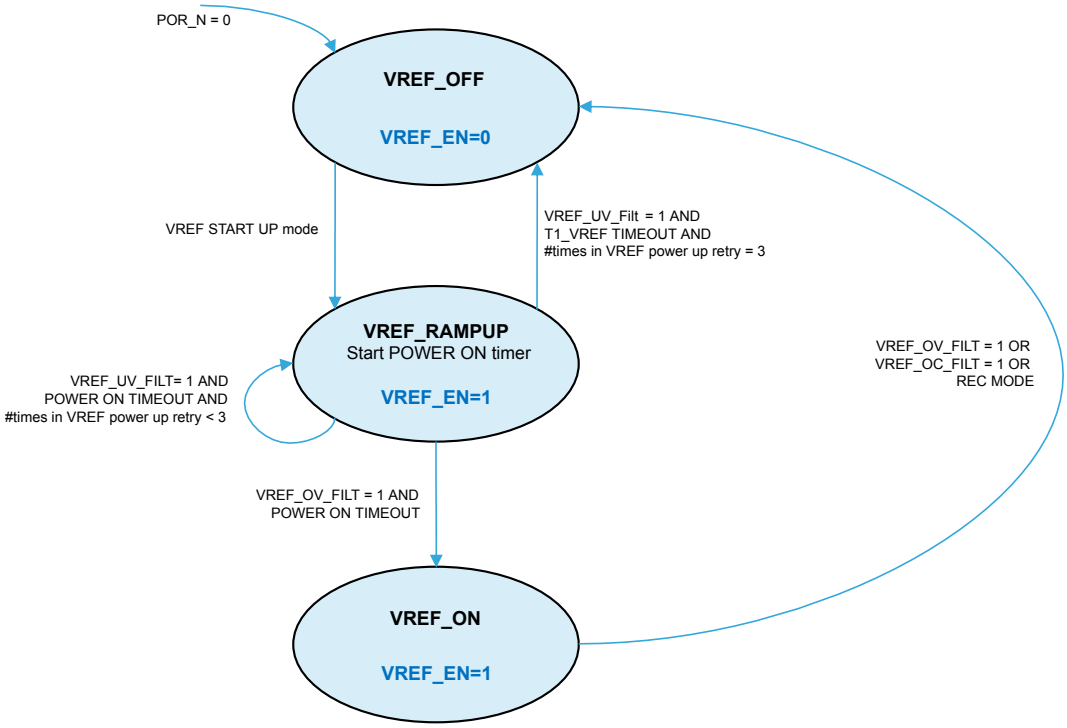


Figure 21. **VREF FSM**



8 Safety concept

8.1 FSR and TSR list

Below table shows Functional Safety Requirements (FSR) and Technical Safety Requirements (TSR)

Table 9. Functional safety requirements

ID	Functional safety requirements	ASIL	Safe state	Fault tolerant time	PMHF
FSR-1	All regulators output voltages must remain within programmed range when NRST and FAULT pins are not asserted	B	REC mode	10 ms	7 FIT
FSR-2	Operation of the voltage regulators is allowed till over temperature limit	B	REC mode	10 ms	15 FIT

Table 10. Technical safety requirements

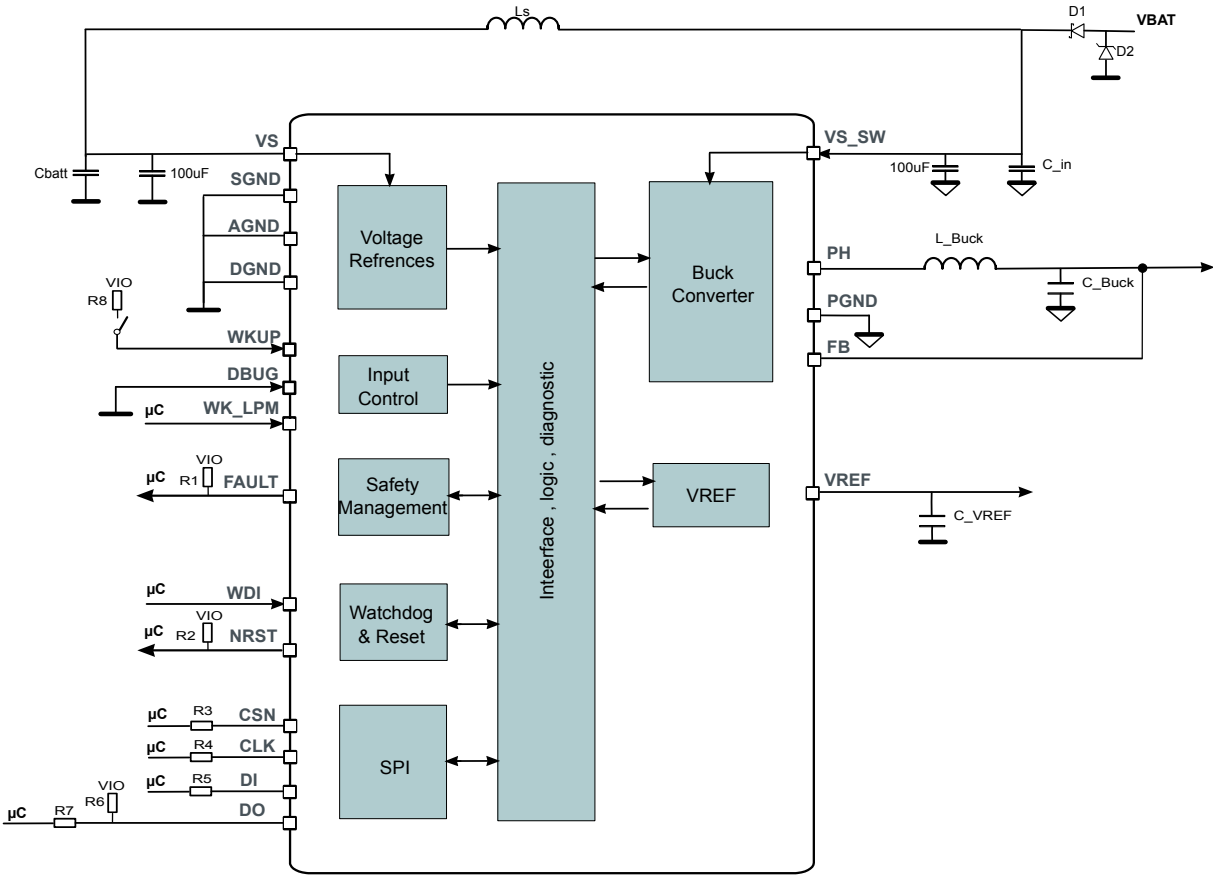
ID	Functional safety requirements	ASIL	Safe state	Fault tolerant time
TSR-1-1	BUCK output voltage must remain within the programmed voltage	B	REC mode(1)	FSR-1
TSR-1-2	VREF output voltage must remain within the programmed voltage	B	REC mode	FSR-1
TSR-1-3	NRST and FAULT pin must be asserted only when requested	B	REC mode	FSR-1
TSR-2-1	Operation of the voltage regulators is allowed till over the temperature limit	B	REC mode	FSR-2

1. *Depending on NVM configuration.*

9 Application information

In the below picture, the SPSA068 typical application circuit is shown. The same application circuit is used for both 400 kHz and 2.4 MHz switching frequencies: only the BUCK inductor must be changed in according to the chosen switching frequency (see the Table 11).

Figure 22. Typical application circuit



Referring to the Figure 22, the Table 11 reports the external components needed for the application

Table 11. External components

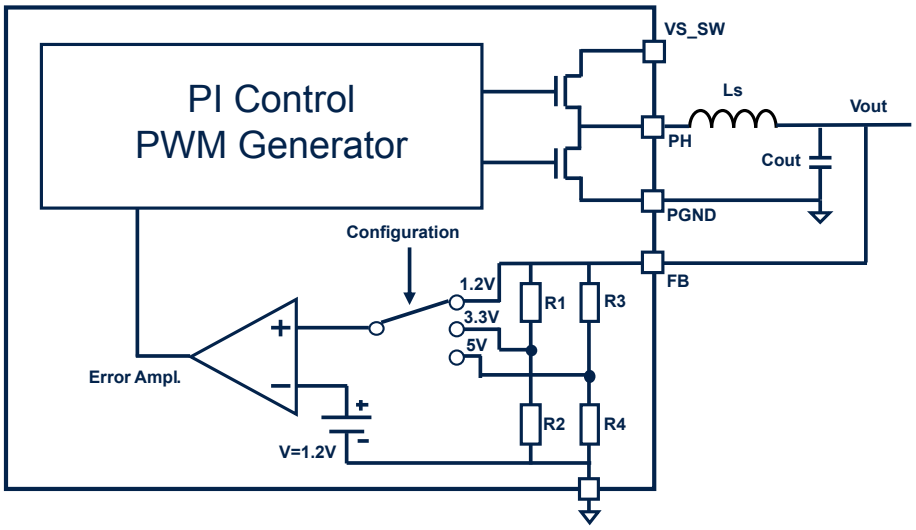
Component	Block/Usage	Typ	Tolerance	Note
D_1, D_2	Reverse battery protection diode	STPS360AF	-	Schottky VRRM = 60 V IF(AV) = 3 A
L_S	Supply filter	15 µH	±20%	Isat > 1 A
C_{batt}	Supply filter	10 µF	±20%	Rated voltage > 40 VDC SMD MLCC, X7R
$C_{\_in}$	Line capacitor	10 µF	±10%	Rated voltage > 40 VDC SMD MLCC, X7R
$L_{\_Buck}$	BUCK inductor	2.2 µH	±20%	Switching freq. = 2.4 MHz Isat > 4 A
		10 µH	±20%	Switching freq. = 400 kHz Isat > 4 A
$C_{\_Buck}$	Output capacitor	10 µF	±10%	Rated voltage = 25 VDC SMD MLCC, X5R
$C_{\_VREF}$	Output capacitor	220 nF	±10%	Rated voltage = 25 VDC SMD MLCC, X5R
R_1	Pull-up resistor on open-drain output pin	3.3 kΩ	±1%	SMD 1/4W
R_2	Pull-up resistor on open-drain output pin	3.3 kΩ	±1%	SMD 1/4W
R_6	Pull-up resistor on open-drain output pin	3.3 kΩ	±1%	SMD 1/4W
R_8	Pull-up resistor on open-drain output pin	3.3 kΩ	±1%	SMD 1/4W
R_3	Protection resistor	0 Ω	5%	SMD 1/4W
R_4	Protection resistor	0 Ω	5%	SMD 1/4W
R_5	Protection resistor	0 Ω	5%	SMD 1/4W
R_7	Protection resistor	0 Ω	5%	SMD 1/4W

9.1 Output voltage definition

SPSA068 converter implements an output voltage “closed loop control” (see the Figure 23).

If the output voltage is configured as 5 V or 3.3 V, the “error amplifier” sense terminal is connected to an internal voltage divider designed to get the assigned output voltage. If 1.2 V is configured, the FB pin is directly connected to the “error amplifier” sense terminal.

Figure 23. Typical application circuit without external resistors



An external voltage divider can be inserted to allow to set output voltage at any value between 1.2 V and 5 V, different from the 3.3 V or 5 V (see the Figure 24). Once the Vout is chosen, the Rx and Ry resistors must be calculated in accordance with:

$$Vfb = Vout \times \frac{R2}{(R1 + R2)} = Vout \times \frac{1}{\left(1 + \frac{Rx}{Ry}\right)} \quad (5)$$

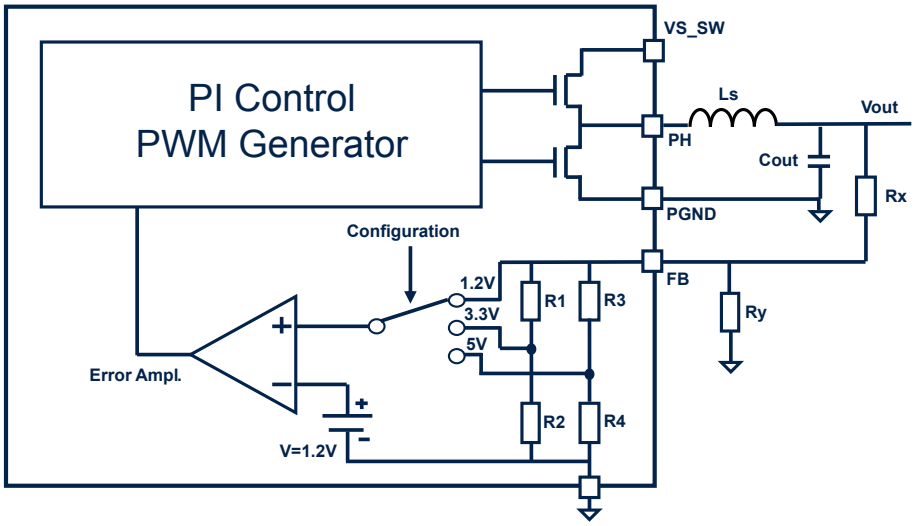
Where Vfb = 1.2 V

So the external resistors ratio is defined as:

$$\frac{Rx}{Ry} = \frac{Vout}{Vfb} - 1 \quad (6)$$

The Rx and Ry values should be selected to reduce the current through the divider.

Figure 24. Typical application circuit with external resistors



10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 QFN32L (5.0x5.0x1.0 mm Epad WETT. FLANKS) package information

Figure 25. QFN32L (5.0x5.0x1.0 mm Epad WETT. FLANKS) package outline

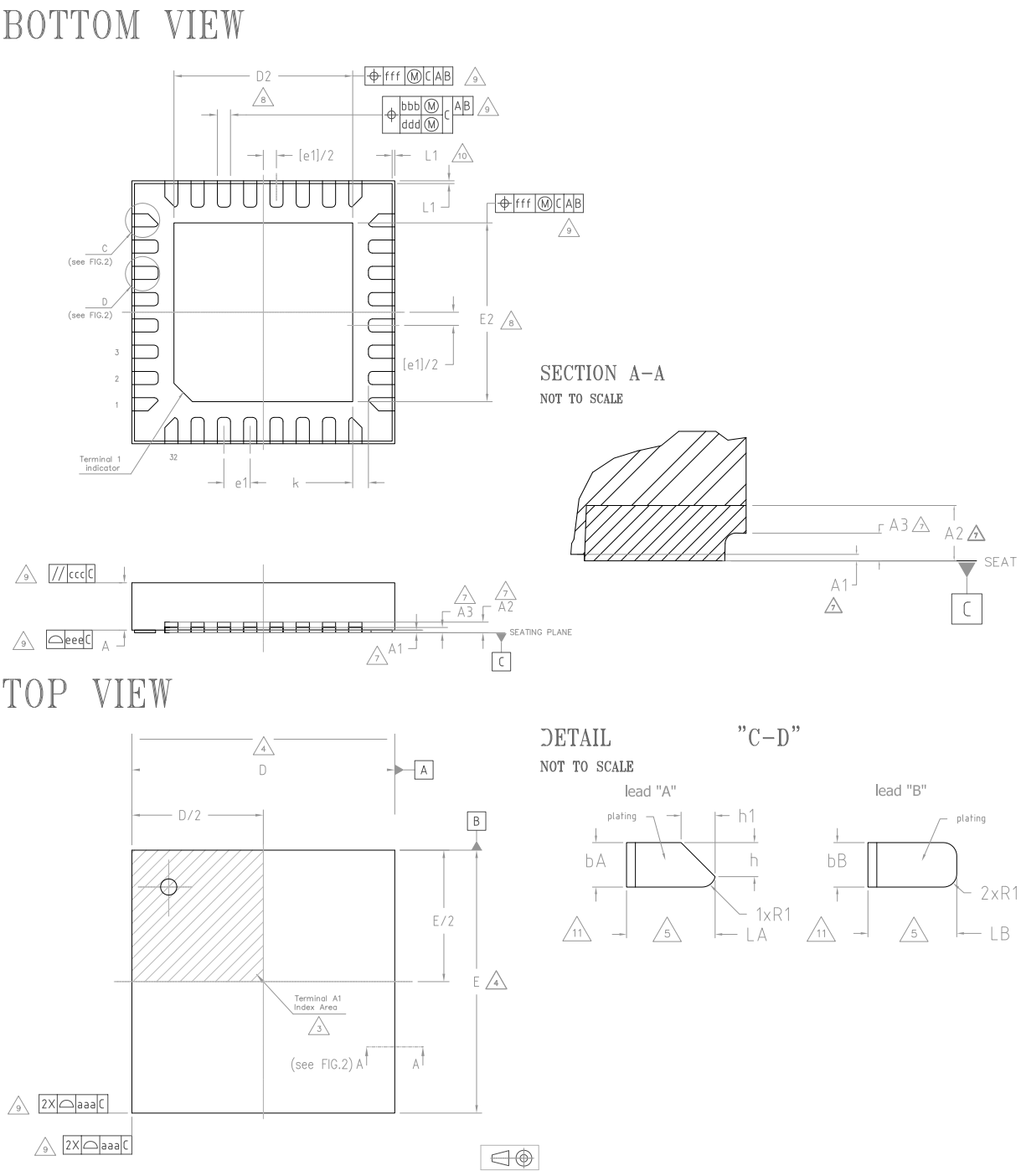


Table 12. **QFN32L (5.0x5.0x1.0 mm Epad WETT. FLANKS) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	-	0.05
A2		0.2 REF	
A3	0.10	-	-
D		5.00 BSC	
D2	3.40	3.50	3.60
E		5.00 BSC	
E2	3.40	3.50	3.60
e1		0.50 BSC	
k	0.20	-	-
L1	-	-	0.050
La	0.40	0.50	0.60
bA	0.20	0.25	0.30
h	-	0.19 REF	-
h1	-	0.19 REF	-
LB	0.45	0.50	0.55
bB	0.20	0.25	0.30
N		32	
R1	-	-	0.10
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Revision history

Table 13. **Document revision history**

Date	Version	Changes
07-Nov-2024	1	Initial release.

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