Innovative Service Around the Globe YAGEO

DATA SHEET

SURFACE MOUNT MULTILAYER CERAMIC CAPACITORS

Automotive grade HiCap
X7R/X7S

4 V TO 100 V
1 µF to 10 µF
RoHS compliant & Halogen Free

YAGEO

Product specification – September 15, 2022 V.1

SCOPE

This specification describes Automotive grade X7R/X7S series chip capacitors with lead-free terminations and used for automotive equipments.

APPLICATIONS

All general purpose applications under normal operation and usage conditions for automotive equipments.

FEATURES

- AEC-Q200 qualified
- MSL class: MSL 1
- AC series soldering is compliant with J-STD-020D
- High component and equipment reliability
- The capacitors are 100% performed by automatic optical inspection prior to taping.

ORDERING INFORMATION - GLOBAL PART NUMBER

All part numbers are identified by the series, size, tolerance, TC material, packing style, voltage, process code, termination and capacitance value.

GLOBAL PART NUMBER

AC xxxx x x xxx x B x xxx
(1) (2) (3) (4) (5) (6) (7)

(1) SIZE – INCH BASED (METRIC)

0201 (0603) / 0402 (1005) / 0603 (1608) / 0805 (2012) / 1206 (3216)/ 1210 (3225) /1812 (4532)

(2) TOLERANCE

J = ±5%
K = ±10%
M= ±20%

Capacitance tolerance ±5% doesn't available for X7R full product range, please contact local sales before order

(3) PACKING STYLE (SEE TABLE. 8 FOR DETAIL)

R = Paper/PE taping reel; Reel 7 inch
K = Blister taping reel; Reel 7 inch
P = Paper/PE taping reel; Reel 13 inch
F = Blister taping reel; Reel 13 inch

(4) TC MATERIAL

X7R : -55 °C to +125 °C (ΔC/C ± 15%)
X7S : -55 °C to +125 °C (ΔC/C ± 22%)

(5) RATED VOLTAGE

4 = 4 V
5 = 6.3 V
6 = 10 V
7 = 16 V
8 = 25 V
G = 35 V
9 = 50 V
0 = 100 V

(6) PROCESS

B = X7R/X7S

(7) CAPACITANCE VALUE

2 significant digits + number of zeros
The 3rd digit signifies the multiplying factor, and letter R is decimal point
Example: 121 = 12 x 10^1 = 120 pF

CONSTRUCTION

The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two end terminations and finally covered with a layer of plated tin (Matte Sn). The terminations are lead-free. A cross section of the structure is shown in Fig.1.

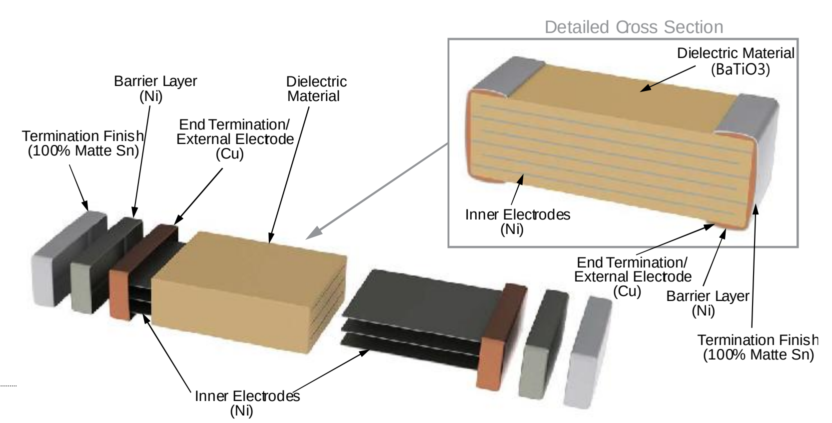


Fig. 1 Surface mounted multilayer ceramic capacitor construction

DIMENSION

Table 1 For outlines see fig. 2

TYPE	L_1 (mm)	W (mm)	T (MM)	L_2 / L_3 (mm)		L_4 (mm)
				min.	max.	min.
0201	0.6 ±0.03	0.3±0.03	0.3±0.03	0.10	0.20	0.20
0402	1.0 ±0.05	0.5 ±0.05	0.5 ±0.05	0.15	0.35	0.30
0603	1.6 ±0.10	0.8 ±0.10	0.8 ±0.10	0.20	0.50	0.60
0805	2.0 ±0.10	1.25 ±0.10	0.6 ±0.10	0.25	0.75	0.70
	2.0 ±0.20	1.25 ±0.20	0.85 ±0.10			
			1.25 ±0.20			
1206	3.2 ±0.15	1.6 ±0.15	0.6 ±0.10	0.25	0.75	1.50
			0.85 ±0.10			
	3.2 ±0.30	1.6 ±0.20	1.15 ± 0.10			
			1.25 ±0.20			
			1.6 ±0.20			
	3.2 ±0.30	1.6 ±0.30	1.6 ±0.30			
1210	3.2 ±0.20	2.5 ±0.20	0.85 ±0.10	0.25	0.75	1.50
	3.2 ±0.30	2.5 ±0.20	1.25 ±0.20			
			1.6 ±0.20			
			2.0 ±0.20			
	3.2 ±0.40	2.5 ±0.30	2.5 ±0.20			
1808	4.5 ±0.40	2.0 ±0.30	1.25 ±0.20	0.25	0.75	2.20
1812	4.5 ±0.40	3.2 ±0.30	0.85 ±0.10	0.25	0.75	2.20
			1.25 ±0.20			
			1.6 ±0.20			

OUTLINES

For dimension see Table 1

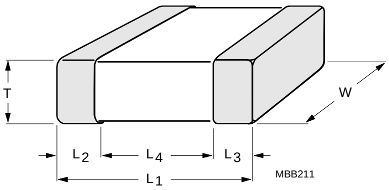


Fig. 2 Surface mounted multilayer ceramic capacitor dimension

CAPACITANCE RANGE & THICKNESS FOR X7R

Table 2 Sizes from 0603 to 0805

CAP.	0603				0805					
	6.3V	10V	16 V	25 V	6.3 V	10 V	16 V	25 V	35 V	50 V
1 µF	0.8±0.1	0.8±0.1	0.8±0.1	0.8±0.1		1.25±0.2	1.25±0.2	1.25±0.2		1.25±0.2
2.2 uF						1.25±0.2	1.25±0.2	1.25±0.2	1.25±0.2	
4.7 uF						1.25±0.2	1.25±0.2			
10 uF					1.25±0.2	1.25±0.2				

Table 3 Sizes 1206

CAP.	1206					
	6.3 V	10V	16V	25V	50 V	100 V
1 µF		1.15±0.10	1.15±0.10	1.60±0.2	1.60±0.2	1.60±0.2
2.2 µF			1.60±0.2	1.60±0.2	1.60±0.2	1.60±0.2
4.7 uF	1.60±0.2	1.60±0.2	1.60±0.2			
10 uF						

Table 4 Sizes 1210 to 1812

CAP.	1210			1812	
	25 V	50V	100 V	50V	100V
1 µF	1.25±0.20	1.25±0.20	2.0±0.2	1.60±0.2	1.60±0.2
2.2 µF		2.0±0.2	2.0±0.2		
4.7 µF	2.5±0.2	2.5±0.2			

NOTE

1. Values in shaded cells indicate thickness class in mm
2. Capacitance value of non E3 series is on request

ELECTRICAL CHARACTERISTICS

X7R DIELECTRIC CAPACITORS; NI/SIN TERMINATIONS

Unless otherwise specified, all test and measurements shall be made under standard atmospheric conditions for testing as given in 5.3 of IEC 60068-1:

- Temperature: 15 °C to 35 °C
- Relative humidity: 25% to 75%
- Air pressure: 86 kPa to 106 kPa

Before the measurements are made, the capacitor shall be stored at the measuring temperature for a time sufficient to allow the entire capacitor to reach this temperature.

The period as prescribed for recovery at the end of a test is normally sufficient for this purpose.

RATED VOLTAGE AND CAPACITANCE

Table 5

SIZE CODE	RATED VOLTAGE (VDC)	CAPACITANCE (µF)	D.F.	RC @ 25 °C (Ω•F)	RC @ 125 °C (Ω•F)
0603	6.3	1.0	5.0%	500	50
	10	1.0	5.0%	500	50
	16	1.0	7.5%	100	5
	25	1.0	7.5%	100	5
0805	10	1.0	5.0%	500	50
	16	1.0	5.0%	500	50
	25	1.0	5.0%	500	50
	50	1.0	5.0%	500	10
	10	2.2	5.0%	100	10
	16	2.2	5.0%	100	10
	25	2.2	5.0%	100	10
	35	2.2	5.0%	100	10
	10	4.7	10.0%	100	10
	16	4.7	10.0%	100	10
	6.3	10.0	10.0%	100	10
	10	10.0	10.0%	100	10
1206	10	1.0	3.5%	500	10
	25	1.0	3.5%	500	10
	50	1.0	5.0%	500	10
	100	1.0	5.0%	500	10
	16	2.2	5.0%	500	50
	25	2.2	5.0%	500	50
	50	2.2	5.0%	500	10
	100	2.2	5.0%	500	10
	6.3	4.7	10.0%	50	5
	10	4.7	10.0%	50	5
	16	4.7	10.0%	50	5
1210	25	1.0	2.5%	500	50
	50	1.0	2.5%	500	50
	100	1.0	5.0%	500	50
	50	2.2	5.0%	500	50
	100	2.2	5.0%	500	50
	25	4.7	10.0%	500	10
	50	4.7	10.0%	500	10
1812	50	1.0	2.5%	500	50
	100	1.0	2.5%	500	50

SOLDERING RECOMMENDATION

Table 6

SOLDERING METHOD	SIZE 0201	0402	0603	0805	1206	≥ 1210
Reflow	Reflow only	≥ 0.1 µF	≥ 1.0 µF	≥ 2.2 µF	≥ 4.7 µF	Reflow only
Reflow/Wave		< 0.1 µF	< 1.0 µF	< 2.2 µF	< 4.7 µF	---

SOLDERING CONDITIONS

The lead free MLCCs are able to stand the reflow soldering conditions as below:

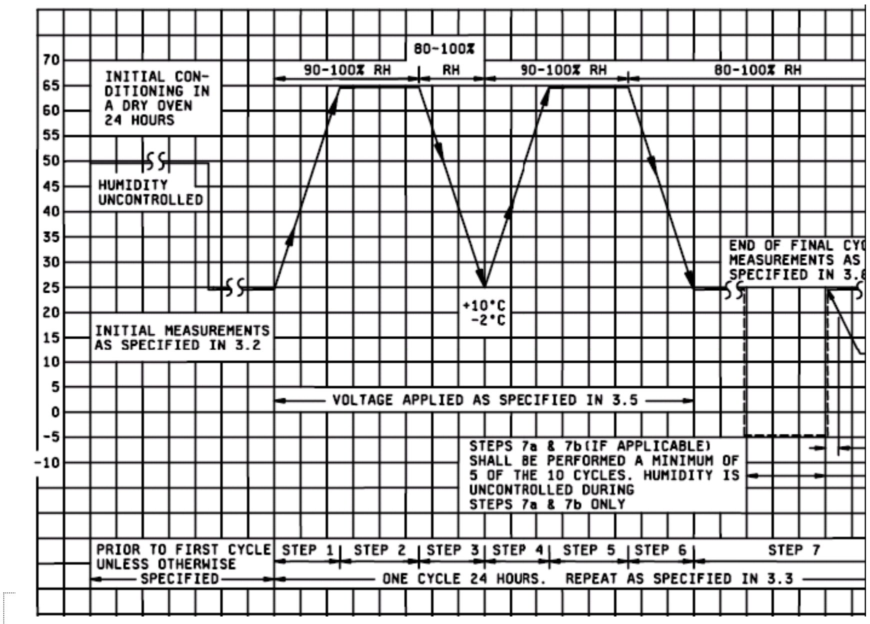
- Temperature: above 220 °C
- Endurance: 95 to 120 seconds
- Cycles: 3 times

The test of "soldering heat resistance" is carried out in accordance with the schedule of "MIL-STD-202G-method 210F", "The robust construction of chip capacitors allows them to be completely immersed in a solder bath of 260 °C for 10 seconds". Therefore, it is possible to mount MLCCs on one side of a PCB and other discrete components on the reverse (mixed PCBs). Surface Mount Capacitors are tested for solderability at 245 °C during 2 seconds. The test condition for no leaching is 260°C for 30 seconds.

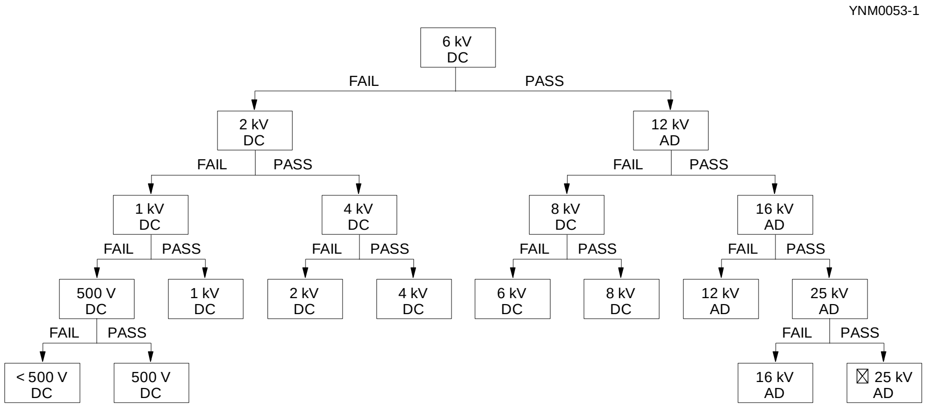
TESTS AND REQUIREMENTS

Table 7 Test procedures and requirements

NO	AEC-Q200 TEST	TEST METHOD	REQUIREMENTS
1	High Temperature Exposure	Unpowered ; 1000hours @ T=150 °C Measurement at 24±2 hours after test conclusion.	No visual damage
			ΔC/C X7R: Within ±10%
			D.F.: within initial specified value
			IR: within initial specified value
2	Temperature Cycling	Preconditioning; 150 +0/–10 °C for 1 hour, then keep for 24 ±1 hours at room temperature 1000 cycles with following detail: 30 minutes at lower category temperature 30 minutes at upper category temperature Recovery time 24 ±2 hours	No visual damage
			ΔC/C X7R: ±10%
			D.F. meet initial specified value
			IR meet initial specified value
3	Destructive Physical Analysis	Electrical test not required.	

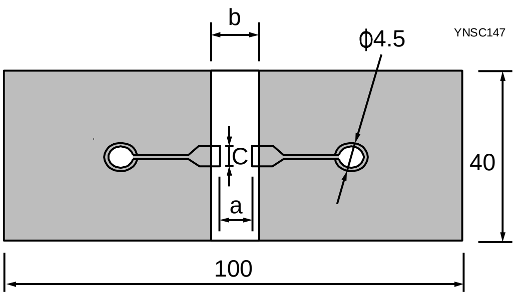
4	Moisture Resistance	T=24 hrs/per cycle; 10 continuous cycles unpowered. Measurement at 24 ±2 hours after test condition.	No visual damage ΔC/C X7R: ±15% D.F. Within initial specified value IR Meet initial specified value
		 **Fig. 3** Moisture resistant	
5	Biased Humidity	1. Preconditioning: 150 +0/-10 °C /1 hour, then keep for 24 ±1 hour at room temp 2. Initial measure: Spec. refer to initial spec. C. D. I.R. Note: Series with 100 KΩ 3. Test condition: 85 °C, 85% R.H. connected with 100 KΩ resistor, applied 1.5V/U_r (no more than 630V) for 1,000 hours. 4. Recovery: X7R/X7S: 24 ±2 hours 5. Final measure: C. D. I.R.	No visual damage after recovery ΔC/C X7R/X7S: ±15% D.F. X7R/X7S: Less than 200% of initial spec. I.R. The insulation resistance shall greater than 10% of initial spec.

6	High Temperature Operational Life	1. Preconditioning: 150 +0/-10 °C /1 hour, then keep for 24 ±1 hour at room temp 2. Initial measure: Spec: refer to initial spec C, D, IR 3. Endurance test: Temperature: 125 °C Specified stress voltage applied for 1,000 hours: Applied 150% x Ur. 4. Recovery time: 24 ±2 hours 5. Final measure: C, D, IR Note: If the capacitance value is less than the minimum value permitted, then after the other measurements have been made the capacitor shall be preconditioned according to "IEC 60384 4.1" and then the requirement shall be met.	No visual damage ΔC/C X7R/X7S: ±15% D.F. Less than 200% of initial spec. IR The insulation resistance shall be greater than 10% of initial spec.
7	External Visual	Any applicable method using × 10 magnification	In accordance with specification
8	Physical Dimension	Verify physical dimensions to the applicable device specification.	In accordance with specification
9	Mechanical Shock	Three shocks in each direction shall be applied along the three mutually perpendicular axes of the test specimen (18 shocks) Peak value: 1,500 g's Duration: 0.5 ms Velocity change: 15.4 ft/s Waveform: Half-sin	ΔC/C X7R/X7S: ±10% D.F. Within initial specified value IR Within initial specified value
10	Vibration	5 g's for 20 minutes, 12 cycles each of 3 orientations. Test from 10-2000 Hz.	ΔC/C X7R/X7S: ±10% D.F: meet initial specified value IR meet initial specified value
11	Resistance to Soldering Heat	Precondition: 150 +0/–10 °C for 1 hour, then keep for 24 ±1 hours at room temperature Preheating: for size ≤ 1206: 120 °C to 150 °C for 1 minute Preheating: for size >1206: 100 °C to 120 °C for 1 minute and 170 °C to 200 °C for 1 minute Solder bath temperature: 260±5 °C Dipping time: 10±0.5 seconds Recovery time: 24±2 hours	Dissolution of the end face plating shall not exceed 25% of the length of the edge concerned ΔC/C X7R/X7S: ±10% D.F. within initial specified value IR within initial specified value

12	Thermal Shock	1. Preconditioning: 150 +0/-10 °C /1 hour, then keep for 24±1 hour at room temp 2. Initial measure: Spec: refer to initial spec C, D, IR 3. Rapid change of temperature test: -55 °C to +125 °C; 300 cycles 15 minutes at -55°C ; 15 minutes at 125 °C 4. Recovery time: X7R/X7S 24±2 hours 5. Final measure: C, D, IR	No visual damage ΔC/C X7R/X7S: ±15% D.F: meet initial specified value IR meet initial specified value
13	ESD	Per AEC-Q200-002	A component passes a voltage level if all components stressed at that voltage level pass.
		 Note: Classify the components according to the highest ESD voltage level survived during ESD testing. **Fig. 4** Passive component HBM ESD test flow diagram (DC = Direct Contact Discharge, AD = Air Discharge)	
14	Solderability	1. Preheat at 155°C for 4 hours. After preheating, immerse the capacitor in a solution of ethanol and rosin (25% rosin in weight proportion). Immerse in eutectic solder solution for 5+0/-0.5 seconds at 235±5°C. 2. Should be placed into steam aging for 8 hours±15 minutes. After preheating, immerse the capacitor in a solution of ethanol and rosin (25% rosin in weight proportion). Immerse in eutectic solder solution for 5+0/-0.5 seconds at 235±5°C. 3. Should be placed into steam aging for 8 hours±15 minutes. After preheating, immerse the capacitor in a solution of Ethanol and rosin (25% rosin in weight proportion). Immerse in eutectic solder solution for 120±5 seconds at 260±5°C.	The solder should cover over 95% of the critical area of each termination.

<table>
<tr><td rowspan="5">15</td><td rowspan="5">Electrical Characterization</td><td>Capacitance</td><td>X7R/X7S:
At 25 °C, 24 hours after annealing
f = 1±0.1 KHz, measuring at voltage 1±0.2 V_{rms} at 25 °C</td><td>Within specified tolerance</td></tr>
<tr><td>Dissipation Factor (D.F.)</td><td>X7R/X7S:
At 25 °C, 24 hours after annealing
f = 1±0.1 KHz, measuring at voltage 1±0.2 V_{rms} at 25 °C</td><td>In accordance with specification on Table 5</td></tr>
<tr><td>Insulation Resistance (I.R.)</td><td>At U_r (DC) for 1 minute</td><td>In accordance with specification on Table 5</td></tr>
<tr><td>Temperature coefficient</td><td>Capacitance shall be measured by the steps shown in the following table.
The capacitance change should be measured after 5 min at each specified temperature stage.
<table>
<tr><th>Step</th><th>Temperature(°C)</th></tr>
<tr><td>a</td><td>25±2</td></tr>
<tr><td>b</td><td>Lower temperature±3°C</td></tr>
<tr><td>c</td><td>25±2</td></tr>
<tr><td>d</td><td>Upper Temperature±2°C</td></tr>
<tr><td>e</td><td>25±2</td></tr>
</table>
X7R
Capacitance Change shall be calculated from the formula as below
$$\Delta C = \frac{C2 - C1}{C1} \times 100\%$$
C1: Capacitance at step c
C2: Capacitance at step b or d</td><td>ΔC/C

X7R: ±15%
X7S: ± 22%</td></tr>
<tr><td>Voltage Proof</td><td>1. Specified stress voltage applied for 1~5 seconds
2. Ur ≤ 100 V: series applied 2.5 Ur
Charge/Discharge current is less than 50 mA</td><td>No breakdown or flashover</td></tr>
</table>

<table>
<tr>
<td>16</td>
<td>Board Flex</td>
<td>Part mounted on a 100mm × 40mm FR4 PCB board, which is 1.6±0.2 mm thick and has a layer-thickness 35μm±10 μm.
Part should be mounted using the following soldering reflow profile.
Conditions:
X7R/X7S:
Bending 2 mm at a rate of 1 mm/s, radius jig 340 mm
Test Substrate:


unit: mm</td>
<td>No visual damage
ΔC/C
X7R/X7S: ±10%
<table>
<tr><td></td><td colspan="3">Dimension(mm)</td></tr>
<tr><td>Type</td><td>a</td><td>b</td><td>c</td></tr>
<tr><td>0201</td><td>0.3</td><td>0.9</td><td>0.3</td></tr>
<tr><td>0402</td><td>0.4</td><td>1.5</td><td>0.5</td></tr>
<tr><td>0603</td><td>1.0</td><td>3.0</td><td>1.2</td></tr>
<tr><td>0805</td><td>1.2</td><td>4.0</td><td>1.65</td></tr>
<tr><td>1206</td><td>2.2</td><td>5.0</td><td>1.65</td></tr>
<tr><td>1210</td><td>2.2</td><td>5.0</td><td>2.0</td></tr>
<tr><td>1808</td><td>3.5</td><td>7.0</td><td>3.7</td></tr>
</table>
</td>
</tr>
<tr>
<td>17</td>
<td>Terminal Strength</td>
<td>With the component mounted on a PCB obtained with the device to be tested, apply a 17.7N (1.8Kg) force to the side of a device being tested.
This force shall be applied for 60+1 seconds.
Also the force shall be applied gradually as not to apply a shock to the component being tested.
* Apply 2N force for 0402 size.
* Apply 1N force for 0201 size.</td>
<td>Magnification of 20X or greater may be employed for inspection of the mechanical integrity of the device body, terminals and body/terminal junction.
Before, during and after the test, the device shall comply with all electrical requirements stated in this specification.</td>
</tr>
<tr>
<td>18</td>
<td>Beam Load Test</td>
<td>Place the part in the beam load fixture. Apply a force until the part breaks or the minimum acceptable force level required in the user specification(s) is attained.</td>
<td>≤ 0805
Thickness > 0.5mm: 20N
Thickness ≤ 0.5mm: 8N
≥ 1206
Thickness ≥1.25 mm: 54N
Thickness < 1.25 mm: 15N</td>
</tr>
</table>

THICKNESS CLASSES AND PACKING QUANTITY

Table 8

SIZE CODE	THICKNESS CLASSIFICATION	PACKING CODE		TAPE WIDTH	QUANTITY PER REEL			
					Ø180 MM / 7 INCH		Ø330 MM / 13 INCH	
		7 INCH	13 INCH		Paper	Blister	Paper	Blister
0201	0.3 ±0.03 mm	R	P	8 mm	15,000	---	50,000	---
0402	0.5 ±0.05 mm	R	P	8 mm	10,000	---	50,000	---
0603	0.8 ±0.1 mm	R	P	8 mm	4,000	---	15,000	---
0805	0.6 ±0.1 mm	R	P	8 mm	4,000	---	20,000	---
	0.85 ±0.1 mm	R	P	8 mm	4,000	---	15,000	---
	1.25 ±0.2 mm	K	F	8 mm	---	3,000	---	10,000
1206	0.6 ±0.1 mm	R	P	8 mm	4,000	---	20,000	---
	0.85 ±0.1 mm	R	P	8 mm	4,000	---	15,000	---
	1.0/1.15 ±0.1 mm	K	F	8 mm	---	3,000	---	10,000
	1.25 ±0.2 mm	K	F	8 mm	---	3,000	---	10,000
	1.60 ±0.2 mm	K	F	8 mm	---	2,000	---	8,000
1210	0.85 ±0.1 mm	K	F	8 mm	---	4,000	---	10,000
	1.15 ±0.1 mm	K	F	8 mm	---	3,000	---	10,000
	1.25 ±0.2 mm	K	F	8 mm	---	3,000	---	10,000
	2.0 ±0.2 mm	K		8 mm	---	2,000	---	---
	2.5 ±0.2 mm	K		8 mm	---	1,000	---	---
1812	0.6 / 0.85±0.1 mm	K		12 mm	---	2,000	---	---
	1.15±0.1 mm	K		12 mm	---	1,000	---	---
	1.25±0.2 mm	K		12 mm	---	1,000	---	---
	1.6 ±0.2 mm	K		12 mm	---	2,000	---	---

PAPER/PE TAPE SPECIFICATION

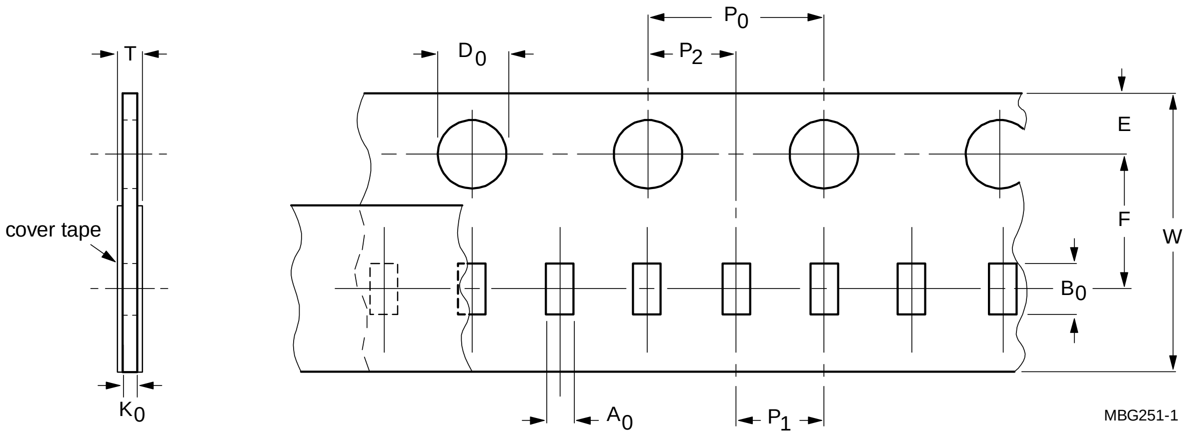


Fig. 5 Paper/PE tape

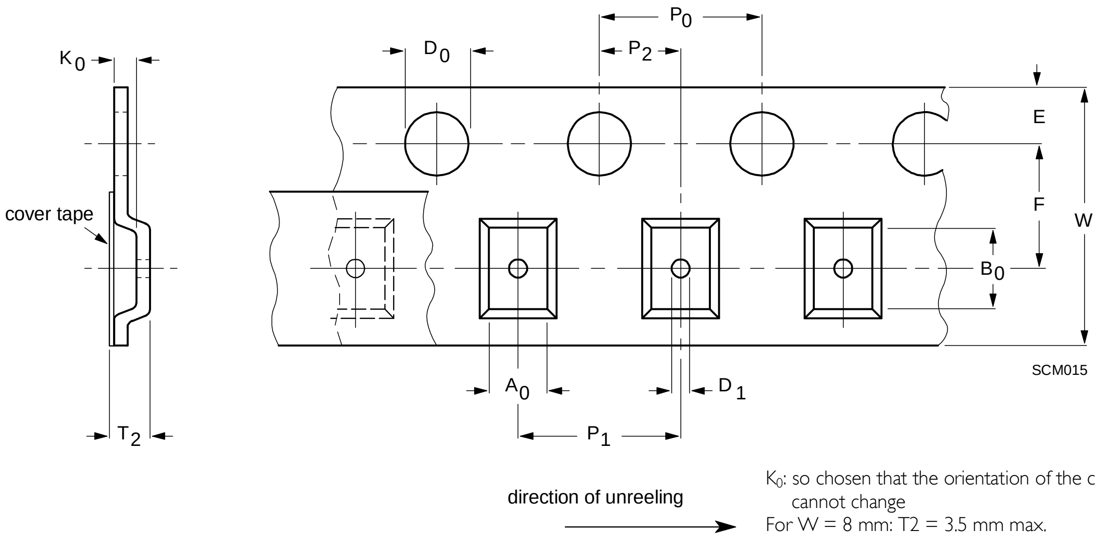
Table 9 Dimensions of paper/PE tape for relevant chip size; see Fig.5

SIZE	SYMBOL										Unit: mm
CODE	A0	B0	W	E	F	P0 (1)	P1	P2	ØD0	K0	T
0201	0.39 ± 0.06	0.70 ± 0.06	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.05	2.0 ± 0.05	2.0 ± 0.05	1.55 ± 0.03	0.38 ± 0.05	(0.47 / 0.55)±0.10
0402	0.70 ± 0.15	1.21 ± 0.12	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.05	2.0 ± 0.05	2.0 ± 0.05	1.50 +0.1 /-0	(0.75 / 0.60)±0.10	(0.85 / 0.70)±0.10
0603	1.05 ± 0.14	1.86 ± 0.13	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.10	4.0 ± 0.10	2.0 ± 0.05	1.50 +0.1 /-0	(1.05 / 0.95 / 0.75)±0.10	(1.15 / 1.05 / 0.85)±0.10
0805	1.50 ± 0.15	2.26 ± 0.20	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.10	4.0 ± 0.10	2.0 ± 0.05	1.50 +0.1 /-0	(1.05 / 0.95 / 0.75)±0.10	(1.15 / 1.05 / 0.85)±0.10
1206	1.90 ± 0.15	3.50 ± 0.20	8.0 ± 0.20	1.75 ± 0.1	3.50 ± 0.05	4.0 ± 0.10	4.0 ± 0.10	2.0 ± 0.05	1.50 +0.1 /-0	(0.95 / 0.75)±0.10	(1.05 / 0.85)± 0.10

NOTE

1. P_0 pitch tolerance over any 10 pitches is ±0.2 mm

BLISTER TAPE SPECIFICATION



K_0: so chosen that the orientation of the component cannot change
For W = 8 mm: T2 = 3.5 mm max.
For W = 12 mm: T2 = 6.5 mm max.

Fig. 6 Blister tape

Table 10 Dimensions of blister tape for relevant chip size; see Fig.6

SIZE CODE	SYMBOL															Unit: mm
	A_0		B_0		K_0		W	E	F	ØD_0	ØD_1	P_0 (2)	P_1	P_2	T2	
	Min.	Max.	Min.	Max.	Min.	Max.					Min.				Min.	Max.
0805	1.29	1.65	2.09	2.60	1.25	1.62	8.1 ±0.20	1.75 ±0.1	3.5 ±0.05	1.5 +0.1/-0.0	1 +0.1/-0.0	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.30	1.67
1206	1.65	2.12	3.30	3.75	1.22	2.15	8.1 ±0.20	1.75 ±0.1	3.5 ±0.05	1.5 +0.1/-0.0	1 +0.1/-0.0	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.27	2.20
1210	2.55	3.02	3.31	3.88	0.97	2.92	8.1 ±0.20	1.75 ±0.1	3.5 ±0.05	1.5 +0.1/-0.0	1 +0.1/-0.0	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.02	2.97
1808	2.05	2.55	4.80	5.45	1.30	2.45	12.1 ±0.20	1.75 ±0.1	5.5 ±0.05	1.5 +0.1/-0.0	1.5 +0.1/-0.0	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.35	2.50
1812	3.35	3.75	4.70	5.33	0.70	2.40	12.1 ±0.20	1.75 ±0.1	5.5 ±0.05	1.5 +0.1/-0.0	1.5 +0.1/-0.0	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	0.75	2.45

NOTE

1. Typical capacitor displacement in pocket
2. P_0 pitch tolerance over any 10 pitches is ±0.2 mm

REEL SPECIFICATION

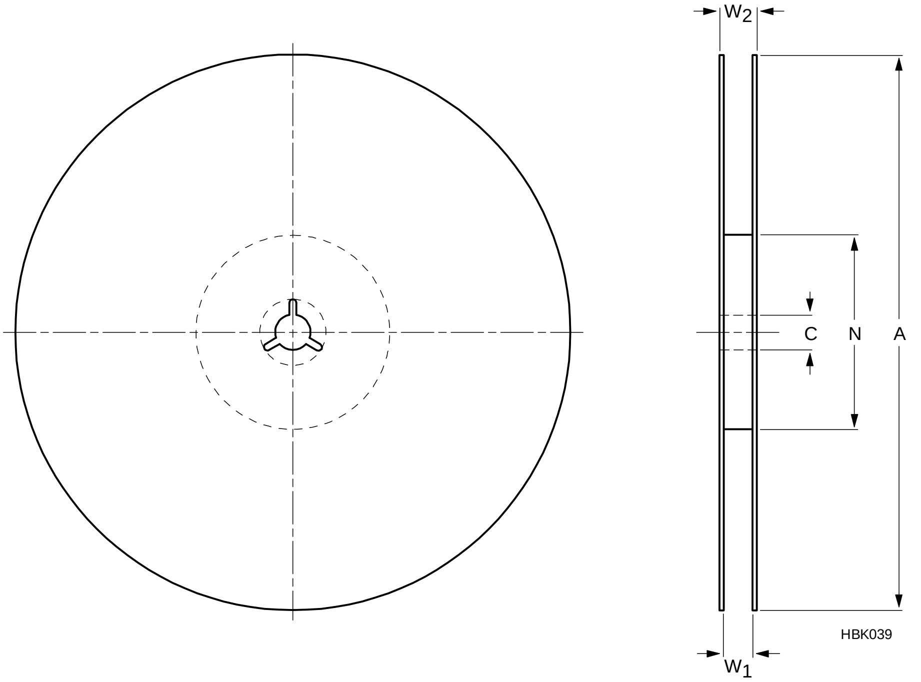


Fig. 7 Reel

Table11 Reel dimensions; see Fig.7

TAPE WIDTH	SYMBOL				Unit: mm
	A	N	C	W_1	$W_{2max.}$
8 (Ø178 mm/7")	178 ±1.0	60 ±1.0	13 +0.50/-0.20	9.4 ±1.5	14.4
8 (Ø330 mm/13")	330 ±1.0	100 ±1.0	13 +0.50/-0.20	9.0 ±0.2	14.4
12 (Ø178 mm/7")	178 ±1.0	60 ±1.0	13 +0.50/-0.20	13.4 ±1.5	18.4

PROPERTIES OF REEL

Material: polystyrene

Surface resistance: <10^{10} X/sq.

MOUNTING

SOLDER REPAIRS

Conventional solder repairs are carried out with a soldering iron as shown as Tab.13. The tip of the soldering iron should not directly touch the chip component to avoid thermal shock on the interface between termination and body during mounting, repairing or de-mounting processes. Ensure the termination solder has melted before removing the chip component.

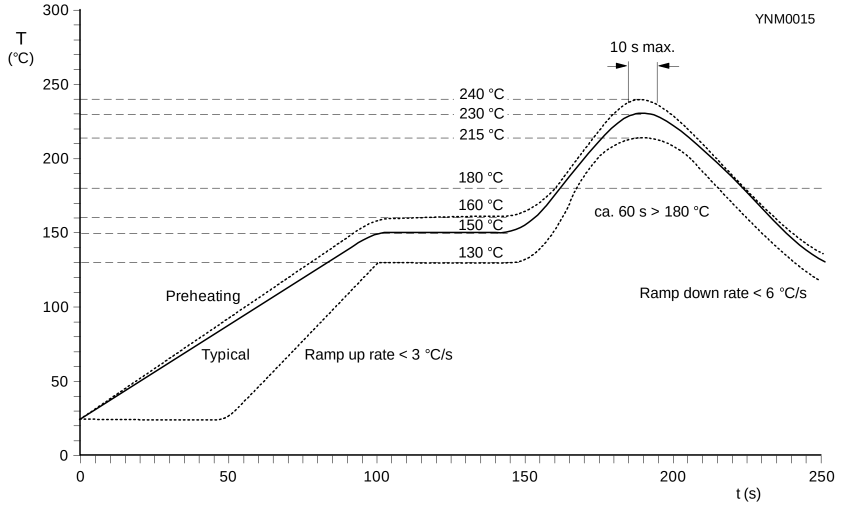
Table 12 Recommended soldering iron condition

SIZE	Temp(°C)	DURATION (SEC.)	PREHEATING TEMP(°C)	ATMOSPHERE
0201/0402/0603/0805/1206	350 max.	3 max.	150 min.	air
1210/1808/1812/2220	280 max.	3 max.	150 min.	air

SOLDERING CONDITIONS

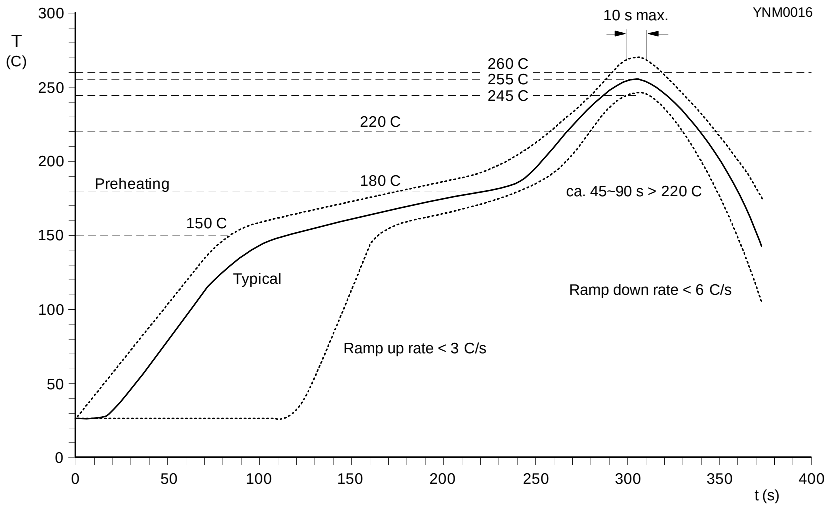
For normal use the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering or conductive adhesive in accordance with *IEC 61760-1* (Standard method for the specification of surface mounting components). For advised soldering profiles see Figs 8, 9, 10.

An improper combination of soldering, substrate and chip size can lead to a damaging of the component. The risk increases with the chip size and with temperature fluctuations (>100 °C).



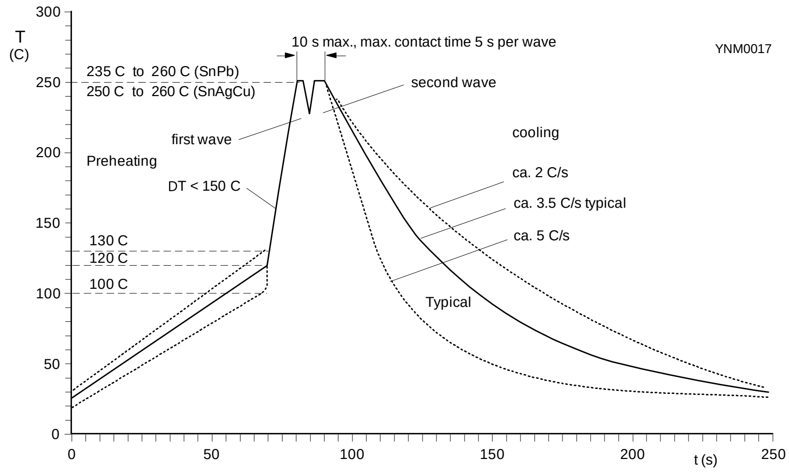
Solid line: Typical process (terminal temperature)
Dotted lines: Process limits - bottom process limit (terminal temperature) & upper process limit (top surface temperature).

Fig. 8 Infrared soldering, forced gas convection reflow soldering - Temperature/time profile for SnPb solders



Solid line: Typical process (terminal temperature)
Dotted lines: Process limits - bottom process limit (terminal temperature) & upper process limit (top surface temperature).

Fig. 9 Infrared soldering, forced gas convection reflow soldering - Temperature/time profile for lead-free SnAgCu solders



Solid line: Typical process
Dotted lines: Process limits

Fig. 10 Double wave soldering for SnPb and lead-free SnAgCu solder - Temperature/time profile (terminal temperature)

FOOTPRINT DIMENSIONS

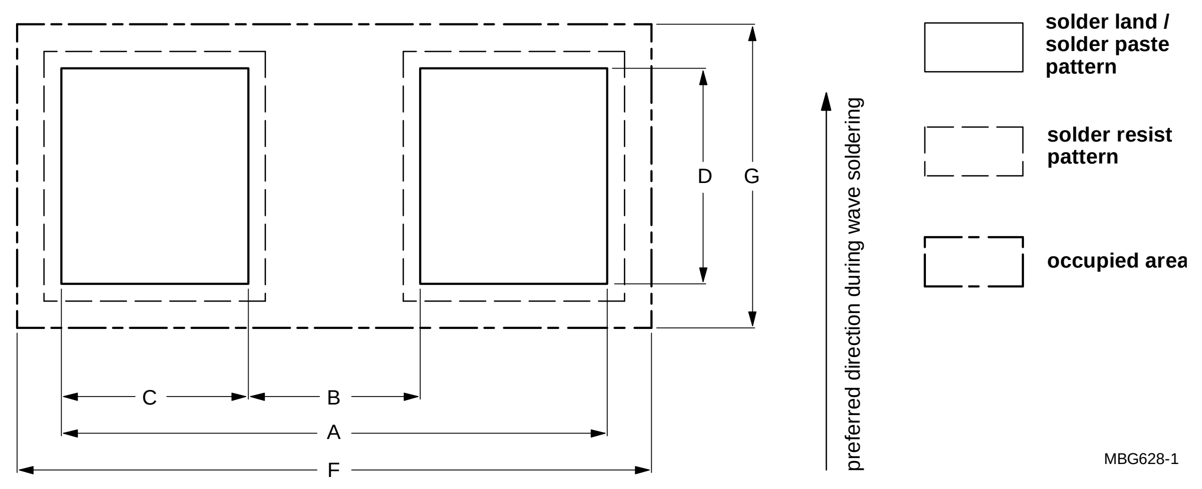


Fig. 11 **Discrete capacitors** recommended dimensions of footprint

Table 13 Reflow soldering; for footprint dimensions see Fig.11

SIZE	FOOTPRINT DIMENSIONS						Unit: mm
CODE	A	B	C	D	F	G	Processing remarks
0201	0.8 ±0.20	0.25 ±0.05	0.28 ±0.07	0.3 ±0.10	---	---	IR or hot plate soldering
0402	1.5 ±0.15	0.5 ±0.15	0.5 ±0.15	0.5 ±0.15	1.75 ±0.15	0.95 ±0.15	
0603	2.3 ±0.15	0.7 ±0.15	0.8 ±0.15	0.9 ±0.15	2.7 ±0.15	1.5 ±0.15	
0603	2.3 ±0.25	0.5 ±0.25	0.9 ±0.25	0.9 ±0.25	2.7 ±0.25	1.5 ±0.25	
0805	2.8 ±0.25	0.9 ±0.25	0.95 ±0.25	1.4 ±0.25	3.2 ±0.25	2.1 ±0.25	
1206	4.0 ±0.25	2.0 ±0.25	1.0 ±0.25	1.8 ±0.25	4.4 ±0.25	2.5 ±0.25	
1210	4.0 ±0.25	2.0 ±0.25	1.0 ±0.25	2.7 ±0.25	4.4 ±0.25	3.4 ±0.25	
1808	5.4 ±0.25	3.3 ±0.25	1.05 ±0.25	2.3 ±0.25	5.8 ±0.25	2.9 ±0.25	Ceramic substrate only
1812	5.4 ±0.25	3.3 ±0.25	1.05 ±0.25	3.5 ±0.25	5.8 ±0.25	4.1 ±0.25	
2220	6.6 ±0.25	4.5 ±0.25	1.05 ±0.25	5.3 ±0.25	7.0 ±0.25	5.9 ±0.25	

REVISION HISTORY

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version 0	Aug. 31, 2022	-	- New
Version 1	Sep. 15, 2022	-	- Add 0805/X7R/10V/10uF

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