Ampere® Altra® 64-Bit Multi-Core Processor Features

Processor Subsystem

- 80 Arm® v8.2+ 64-bit CPU cores up to 3.3 GHz maximum
- 64 KB L1 I-cache, 64 KB L1 D-cache per core
- 1 MB L2 cache per core
- 32 MB System Level Cache (SLC)
- 2x full-width (128b) SIMD
- Coherent Mesh Interconnect (CMI):
  - Distributed snoop filtering

Memory

- 8x 72-bit DDR4-3200 channels
- SECDED ECC, Symbol-based ECC, and DDR4 RAS features
- Up to 16 DIMMs and 4 TB/socket

System Resources

- Full interrupt virtualization (GICv3)
- Full I/O virtualization (SMMUv3)
- Enterprise server-class RAS

Connectivity

- 128 lanes of PCIe Gen4
  - 8 x8 PCIe + 4 x16 PCIe/CCIX with Extended Speed Mode (ESM) support for data transfers at 20/25 GT/s
  - 32 controllers to support up to 128 PCIe Gen4 x4 lanes in 1P configuration
- 48 controllers to support up to 192 PCIe Gen4 x4 lanes in 2P configuration
- Coherent multi-socket support
- 4 x16 CCIX lanes

Technology and Functionality

- Armv8.2+, SBSA Level 4
- Advanced Power Management
  - Dynamic estimation, Voltage droop mitigation

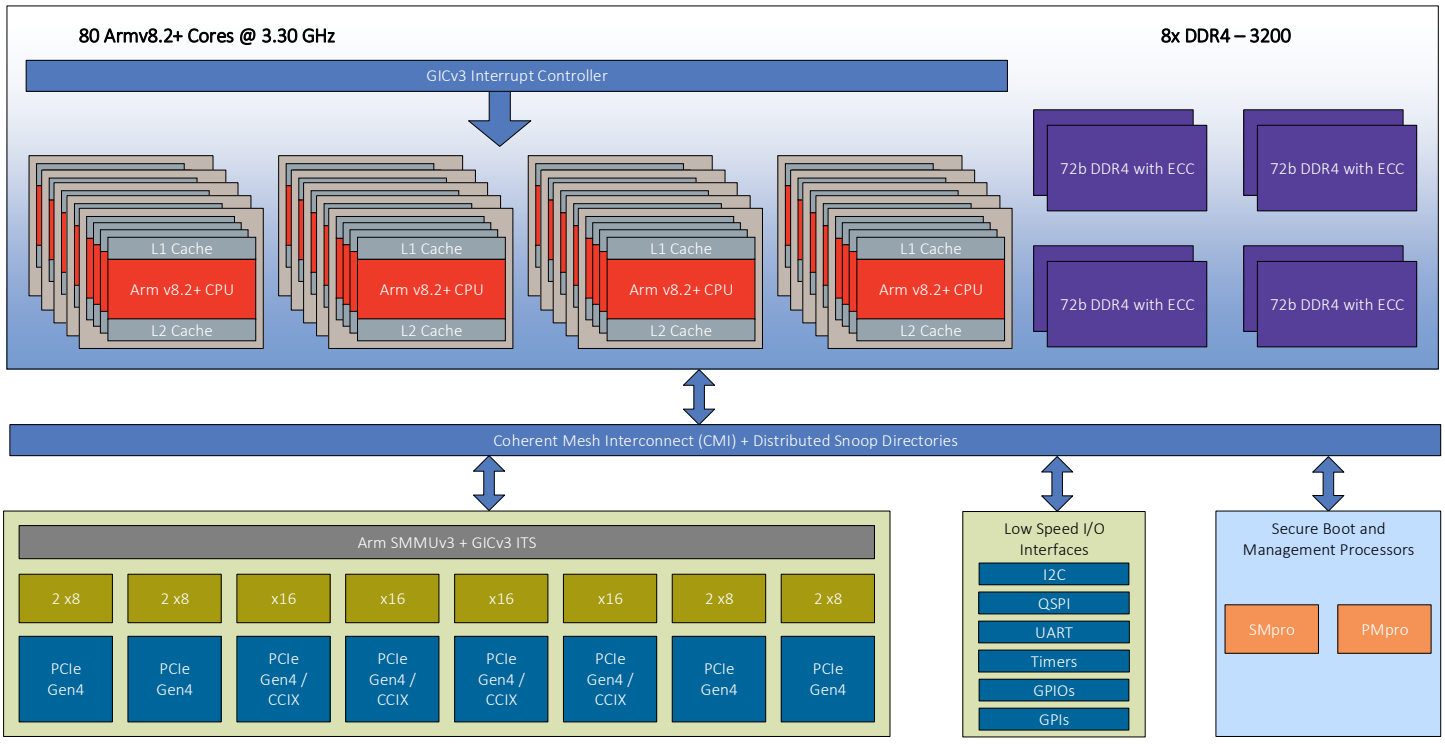
Performance and Power

- Est. SPECrate® 2017_int_base (SKU: AC-108025002): 301 at Usage Power: 187 W
- Max TDP: 250 W

Process Technology

- TSMC 7 nm FinFET

Ampere® Altra® Block Diagram



January 30, 2024

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This document is the Ampere® Altra® datasheet. Make sure you are using the correct edition for the level of the product.

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4655 Great America Parkway, Santa Clara, CA 95054
Phone: (669) 770-3700
https://www.amperecomputing.com

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1. Device Ordering Information

For device ordering information, visit https://amperecomputing.com/briefs/ampere-altra-family-product-brief.

2. Ampere® Altra® Multi-Core 64-Bit Processor

The Ampere Altra first-generation multi-core 64-bit Arm-based server-class processor is custom built for large-scale public and private cloud environments. It supports accelerated delivery and deployment of cloud workloads within an efficient power envelope of 45 W to 250 W. The device also features enterprise grade Reliability, Availability and Serviceability (RAS) capabilities and Arm server standard compliance, providing a substantial reduction in the Total Cost of Ownership (TCO).

Combining 80 Armv8.2+ cores to deliver an estimated SPECrate® 2017_int_base throughput of 300, Altra provides very high computing performance, large memory bandwidth and capacity, and a lot of flexible interconnect—via PCIe Gen4—to off-chip devices. The device is fully compliant with the Arm Server Base System Architecture (SBSA) Level 4 and Server Base Boot Requirements (SBBR) standards.

The following sections provide information on the features of Altra.

2.1. Processor Complex (PCP)

The Altra Processor Complex consists of 80 Processor Modules (PMDs). Each PMD contains a high-performance Altra core, each of which has its own 64 KB L1 I-cache, 64 KB L1 D-cache, and a 1 MB L2 cache. All 80 PMDs share a 32 MB System Level Cache (SLC).

The Altra Processor Complex features include:

- 80 Armv8.2+ 64-bit CPU cores at up to 3.3 GHz maximum
- 64 KB L1 I-cache, 64 KB L1 D-cache per core
- 1 MB L2 cache per core
- 32 MB System Level Cache (SLC)
- 2x full-width (128b) SIMD
- Coherent Mesh Interconnect (CMI):
  - Distributed snoop filtering

2.2. Core Features

The Altra core contains a superscalar, pipelined processing unit, along with other functional elements required by servers. These other functions include memory management, cache control, ANSI 128-bit double precision FPU, timers, and debug facilities. Separate Level 1 instruction and data caches are provided, with 1 MB Level 2 cache per core. The core connects to a 32 MB System Level Cache through a high-performance coherent interface.

Altra core features include:

- Armv8.1/v8.2+ architecture compliance, including Statistical Profiling and UDOT/SDOT instructions (as well as all other optional features other than SVE)
- Support for EL0 AArch32 (no support for EL1 AArch32)
- SBSA Level 4 compliance
- 48-bit logical and physical addressing supported throughout the system
- 80 Arm cores with dedicated low-latency per-core 1 MB L2 cache
  - Four-wide superscalar aggressive out-of-order execution CPU
  - Dual full-width (128-bit wide) SIMD execution pipes
  - 2:1 (aka MP2) DSU-based connect to Arm switch fabric nodes
  - DSU-level Snoop Filter
  - ETR-based per-core ETM trace-to-memory
- Unified “PCP/SoC” switch fabric based on Arm Coherent Mesh Interconnect (CMI)
  - CHI.B bus and coherency protocol enhancements
  - Efficient bandwidth and request ordering scalability with mesh-based topology
  - 32 distributed home nodes and directory-based snoop filters
  - Parity protection on transactions across fabric
  - Transport for ETM trace-to-memory traffic, and for PEM (Power Events Monitor) and TSM (Temp Sensors Monitor) data updates-to-PMpro traffic
    - From locally aggregated 8-core groups (not “clusters”) of associated trace streams, PEMs, and TSMs
- Full CPU, I/O, interrupt, and timer virtualization
- Compliant with GIC v3.0 and GIC v4.0
- Full set of static and dynamic power management features

2.3. L1 Cache Features

2.3.1. L1 Data Cache

- 64 KB, 4-way, set associative data cache with 64-byte cache lines and ECC protection per 32 bits
- Fully associative L1 data TLB with native support for 4 KB, 16 KB, 64 KB, 2 MB, and 512 MB page sizes

2.3.2. L1 Instruction Cache

- 64 KB, 4-way, set associative
- Fully associative L1 instruction TLB with native support for 4 KB, 16 KB, 64 KB, 2 MB, and 32 MB page sizes

2.4. L2 Cache Features

The L2 cache system services L1 instruction and data cache misses from the CPU core.

The L2 cache system includes:

- An 8-way set associative 1024 KB L2 cache with 64-byte lines and data ECC protection per 64 bits

- The DSU interfaces with the mesh over a 256 bit wide CHI-B compliant interface
- SECDED ECC protection for all RAM structures except victim array
- Strictly inclusive with L1D and L1I data caches (I and D hardware coherency)
- Dynamic biased replacement policy
- Modified Exclusive Shared Invalid (MESI) coherency

2.5. System Level Cache (SLC) Features

The 32 MB SLC consists of:

- A 32 MB distributed on-chip cache shared between all processors
- Memory-side cache for processor evictions providing caching of larger data and instruction structures for overall performance enhancements
- Mostly exclusive with L2 cache
- 256 bit data buses all around
- 16 ways, ECC protected

2.6. Generic Interrupt Controller (GIC) Features

The GIC provides registers for managing interrupt sources, interrupt behavior, and interrupt routing to one or more cores. It supports:

- Based on and complies with *ARM Generic Interrupt Controller Architecture Specification Version 3.0* and *4.0*.
- Multiprocessor environments to support 80 cores
- The following interrupt types:
  - Locality-specific Peripheral Interrupts (LPIs). These interrupts are generated by a peripheral writing to a memory-mapped register in the GIC-600
  - Shared Peripheral Interrupts (SPIs)
  - 16 Private Peripheral Interrupts (PPIs), that are independent for each core
  - 16 SGIs, that are generated through the GIC CPU interface of a core
- Interrupt Translation Service (ITS) which provides device isolation and ID translation for message-based interrupts, allowing virtual machines to program devices directly
- Distributed redistributor system that supports better layout
- Distributed ITS system which has 8 ITSs for 8 RCs
- Memory-mapped access to all registers
- Interrupt masking and prioritization which has 32 priority values with 5 bits for each interrupt
- Programmable interrupt routing based on affinity
- Three different interrupt groups, which allow interrupts to target different exception levels:
  - Group 0
  - Non-secure Group 1
  - Secure Group 1
- A global *Disable Security* (DS) bit which allows support for systems with and without security

2.7. System MMU (SMMU)

The Altra System-level Memory Management Unit (SMMU) design translates an input address to an output address. This translation is based on address mapping and memory attribute information that is available in the internal registers and translation tables.

The SMMU implements the Arm SMMU architecture version 3.1 (SMMUv3.1), as defined by the *Arm System Memory Management Unit Architecture Specification, SMMU architecture version 3.0* and *3.1*.

The SMMU provides the following features:

- Compliance with the SMMUv3.1 architecture
- Support for AMBA interfaces
- Support for flexible integration
- Support for high-performance translation

The SMMU contains the following key components:

- Translation Buffer Units (TBUs) that use TLB to cache translation tables
- A Translation Control Unit (TCU) that controls and manages address translations
- Distributed Translation Interface (DTI) interconnect components that connect multiple TBUs to the TCU

2.7.1. Translation Buffer Unit (TBU)

The TBU contains *Translation Lookaside Buffers* (TLBs) that cache translation tables. The MMU-600 implements at least one TBU for each connected master, and these TBUs are local to the corresponding master.

2.7.2. Translation Control Unit (TCU)

The TCU controls and manages the address translations. The MMU-600 implements a single TCU. In MMU-600-based systems, the AMBA DTI protocol defines the standard for communicating with the TCU.

2.7.3. DTI Interconnect

The DTI interconnect connects multiple TBUs to the TCU.

2.8. Generic Timer

Generic Timer (GT) comprises of two parts:

- Centralized Counter module that runs continuously at a constant frequency of 25 MHz
- Per-processor Timer modules

The 56-bit Count output of the Counter is distributed to the per-processor Timer modules to provide the time base/timer clock to all the Timers. The 25 MHz clock is sourced from the TMR_CLK pin.

2.9. Watchdog Timer

Altra contains two Watchdog timers (WDT). One WDT is used for non-secure mode and the other is dedicated for secure mode.

2.10. Eight DDR4-3200 SDRAM Memory Controllers

Eight 72-bit DDR4 channels featuring:

- Up to DDR4-3200
- Up to 2DPC
- Up to 4 TB of memory
- Support for x4 and x8, and for 8 Gb and 16 Gb, DRAM devices
- Support for RDIMMs, LRDIMMs, and Stacked (3DS) RDIMMs
- Support for 1/2/4/6/8 active channels (1 and 2 only for engineering debug/bring-up)
- Hashed memory interleave across active channels

- Full RAS features (including JEDEC DDR4 features and symbol-based ECC)

2.11. PCI Express (PCIe) Controller

The Altra processor provides I/O expansion via PCIe Gen4. The device features 128 PCIe Gen4 lanes via 32 controllers operating at x4 in a single-socket (1P) configuration. A dual-socket (2P) configuration uses two x16 CCIX links for inter-socket connectivity (refer to *Table 1* and *Table 2* for the supported PCIe bifurcation configurations). The 128 lanes can be configured as PCIe x16 or x8 or x4 or x2. This provides flexibility for PCIe add-on networking cards up to 100 GbE or more, and storage expanders or NVMe storage devices, making it well suited for big data applications.

- PCIe Gen1/2/3/4, Root Port
- Support for x16/x8/x4/x2 controllers
- x16 controller supports CCIX ESM20/25 and EP mode for chip-to-chip communication
- Hot-plug support across all controllers
- Supports SRIS, SRNS, common clock
- AER support
- ARI Forwarding support
- ACS support
- Vendor-specific extended capability as part of RAS debug and analysis feature
- ECAM support
- DTI interface to support ATS (Address Translation Service)
- Supports L0, L0s, L1, and L2 power management states
- SMMU v3.1
- ECRC support
- Arm SBSA version 4.0 compliant
- Compliant with PCI Express Base Specification 4.0 v1.0
- Integrated PCIe Gen4 PHY using PIPE v4.4.1
- Support for CXS interface for CCIX
- RAM ECC protection
- Extensive debug and analysis feature as part of RAS

Table 1 lists the supported bifurcations for root complex A[0:3] per the PCIe lane order (refer to *Table 7 on page 54* for details).

Table 1: Supported Bifurcation Options for PCIe Root Complex A

BIFURCATION OPTION	LANE ORDER				DESCRIPTION
	L0 L3	L4 L7	L8 L11	L12 L15	
0	x16				One x16 CCIX PCIe interface
1	x8		x8		Two x8 PCIe interfaces
2	x8		x4	x4	One x8 and two x4 PCIe interfaces
3	x4	x4	x4	x4	Four x4 PCIe interfaces

Thus, root complex A[0:3] provides a maximum of 16 controllers operating at x4.

Note: *Altra does not support the x4[L0:L3], x4[L4:L7], x8[L8:L15] bifurcation configuration.*

Table 2 lists the supported bifurcations for root complex B[0:3]A / B[0:3]B per the PCIe lane order (refer to Table 7 on page 54 for details).

Table 2: Supported Bifurcation Options for PCIe Root Complex B

BIFURCATION OPTION	LANE ORDER								DESCRIPTION
	L0	L1	L2	L3	L4	L5	L6	L7	
0	x8								One Root Port (RP) mode x8 PCIe interface
1	x4				x4				Two RP mode x4 PCIe interfaces
2	x4				x2		x2		One x4 and two x2 PCIe interfaces
3	x2		x2		x2		x2		Four RP mode x2 PCIe interfaces

On a 1P system, root complex A[0:3] provide a maximum of 16 controllers operating at x4. Root complex B[0:3]A and root complex B[0:3]B combined provide a maximum of 16 controllers operating at x4. This way, in a 1P configuration, the Altra processor provides a total of 32 PCIe Gen4 controllers providing 128 lanes operating at x4.

On a 2P system, two RCAs (RCA0 and RCA1) on each socket are used for inter-socket connectivity. The two remaining RCAs (RCA2 and RCA3) on each socket together provide a maximum of 16 controllers operating at x4. Root complex B[0:3]A and root complex B[0:3]B on each socket together provide a maximum of 32 controllers operating at x4. This way, in a 2P configuration, the two Altra processors together provide a total of 48 PCIe Gen4 controllers providing 192 lanes operating at x4.

2.11.1. Supported Maximum Payload Sizes (MPS)

Altra has different Maximum Payload Sizes (MPS) for different root ports. Root ports with a maximum width of x16 and x8 have an MPS of 512B. Root ports with a maximum width of x4 and x2 have an MPS of 256B. This is fixed in hardware and cannot be configured any larger. Root ports can always be configured with a smaller MPS.

Table 3 summarizes the MPS sizes for x2, x4, x8, and x16 root ports on Altra.

Table 3: Supported MPS Sizes for PCIe Root Ports

ROOT PORT	MAXIMUM PAYLOAD SIZE (MPS)
x16, x8	512B
x4, x2	256B

2.12. System Control Processors (SMpro and PMpro)

2.12.1. SMpro Features

The SMpro contains a bootstrap and I^2C controller that interfaces to an external I^2C device running at a default frequency of 400 kHz. This I^2C1 is private to SMpro and is thus neither visible to nor accessible by others. The SMpro features include:

- Arm Cortex-M3 processor
- Maximum core frequency of 400 MHz
- Local instruction/data RAM:
  - Total 256KB I-RAM pin-strap selectable 64/128/192 KB, remainder D-RAM.
  - I-RAM and D-RAM accesses are always zero wait-state.
- No cache
- AHB-Lite processor interfaces
- 1.25 DMIPs/MHz

- 3-stage pipeline
- Debug/Trace support
- 32 external interrupts
- 4 bits of priority
- Implements logic for asserting side band signal S/NS (Secure/Not secure) if the access is to a secure memory address range (specified in a set of four BARs)
- Implements 4 address mappers from the local 32b AHB bus to the 42b address width of the I/O fabric
- SMpro also handles:
  - BMC interface
  - Error handling
  - Interface with CPUs/PMpro (such as Doorbell interrupts and messaging)
  - System booting (with support for different boot modes)
  - Power fail detection

2.12.2. PMpro Features

The PMpro features include:

- Arm Cortex-M3 processor
- Provides SoC power management
- Interfaces to the IOF interconnect
- Contains 256 KB RAM configurable in 64 KB increments as I-RAM or D-RAM
- Contains one I^2C controller (master and slave capability) with SMBus 3.0 and PMBus 1.3 capability
- No cache
- Provides doorbells to communicate with SMpro and CPUs: 2 sets of 9 doorbells (secure and non-secure)
- Capability to generate secure and non-secure transactions towards the system memory via the mappers
- PMpro is always considered as a secure element
- PCP PLL control registers: there are two sets of control registers for the PLLs in the PCP. One set controls the PCP PLL (clock source for CMN mesh fabric) and the other set controls all of the QCPU PLLs (there is one PLL for 4 cores; all QCPU PLLs share the same set of control registers). These registers are located in PMpro (requiring PMpro to be brought out of a hardware reset before the CPUs can be brought up).
- LPI Request hardware logic to facilitate software requesting core or system power state
- PMpro also handles:
  - All sensor logic
  - Die temperature control
  - Dynamic voltage and frequency scaling (DVFS)
  - ACPI interface and logic

2.13. Low-Speed Interfaces

The AHBC block hosts the low speed peripherals and interfaces to the system I/O fabric via a 32-bit AHB bus.

2.13.1. I^2C Interface

- Contains nine I^2C controllers up to 1 MHz which can be a master or slave (statically).
  - All I^2C ports are SMBus 3.0 and PMBus 1.3 capable but without AVSBus support

– Note that only I^2C ports [I^2C2:I^2C10] that belong to the AHBC block support multi-master. I^2C0 and I^2C1 belong to PMpro and SMpro blocks and hence do not fully support multi-master.

The AHBC block integrates nine I^2C controllers that support SMBus. These controllers reside on the internal APB bus.

Each I^2C controller can be configured as either a Master or a Slave. In addition to the I^2C clock and data I/O pins, SCL and SDA, each I^2C bus also has an associated SMBus active low PMALERT_N I/O pin. When an I^2C controller is configured as a master, the associated PMALERT_N I/O pin must be tri-stated and enabled onto one of the internal SPI type interrupts. When configured as a slave, the PMALERT_N I/O pin can be asserted LOW by software to cause an interrupt to the external I^2C master.

The I^2C logic provides one configuration register and one status register plus interrupt mask register and one interrupt status register to support the SMBus ALERT I/O pins.

2.13.2. Quad Serial Peripheral Interface (QSPI)

- Contains two QSPI up to 33 MHz for SPI flash and TPM connectivity
- No-memory-mapped mode supported as there is no intention to execute code directly from NOR flash

2.13.3. UART

- Contains five PL011 UART configurations:
  - One 4-pin UART – for BMC interface (UART0)
  - Four 2-pin UARTs – for SMpro, PMpro, EL3 and operating system/hypervisor consoles
  - No functional I/O sharing among the 5 UARTs. All ports have dedicated I/Os.
  - UART4_S is a secure target

The AHBC block integrates five UARTs on the internal APB bus. Four of the UARTs, UART1 – UART4, implement a simple two wire transmit and receive interface. The UART0 instance supports a four wire interface with an option to select the control pair as RTS/CTS or DTR/DSR via the UART_MODE_SEL configuration register.

The UART ports on Altra are configured as per the mapping listed in *Table 4*.

Table 4: UART Assignment

UART PORT	SOCKET	DESCRIPTION	NOTES
UART_0	Master	UEFI main console with Serial over LAN (SoL)	Non-secure main console for UEFI (and the OS)
UART_1	Master	SCP console	Recommended for SoL
UART_2	Master	Debugger console	Debugger console (required for Windows server)
UART_4	Master	Secure world console (with SoL)	Secure world console
UART_1	Slave	SCP console	Recommended for SoL

2.13.4. Timers

- Contains timers per Arm specifications
- Altra supports four timer frames (CNTBaseN) and two control bases (CNTCTLBase)

2.13.5. General Purpose I/Os (GPIOs)

- Contains three sets of 8 GPIOs with interrupt capability. Each set (GPIO0-7, GPIO8-15 or GPIO16-23) can be configured as secure or non-secure. The GPIOs can be configured:
  - As inputs in which the pin value is read through registers, or
  - As outputs in which the output value and output enable of the pad are controlled through registers

Note: To mimic an open drain output, software can set the output value to '0' and drive the output enable when required to drive a '0' or tri-state the pad when required to drive a '1' (a pull-up on the board is needed in this case).

- When configured as an input, the GPIO can be configured to support external interrupt. The polarity is configurable. Interrupts are routed to GIC, SMpro and PMpro. The interrupt must be enabled at one of the three destinations.

2.13.6. General Purpose Inputs (GPIs)

- Contains 8 GPIs (General Purpose Inputs) with no interrupt capability in the non-secure world. The signal states must be readable by software via a read-only register. These 8 GPIs cannot route external interrupts to GIC/SMpro/PMpro and cannot be configured as outputs.

2.13.7. JTAG

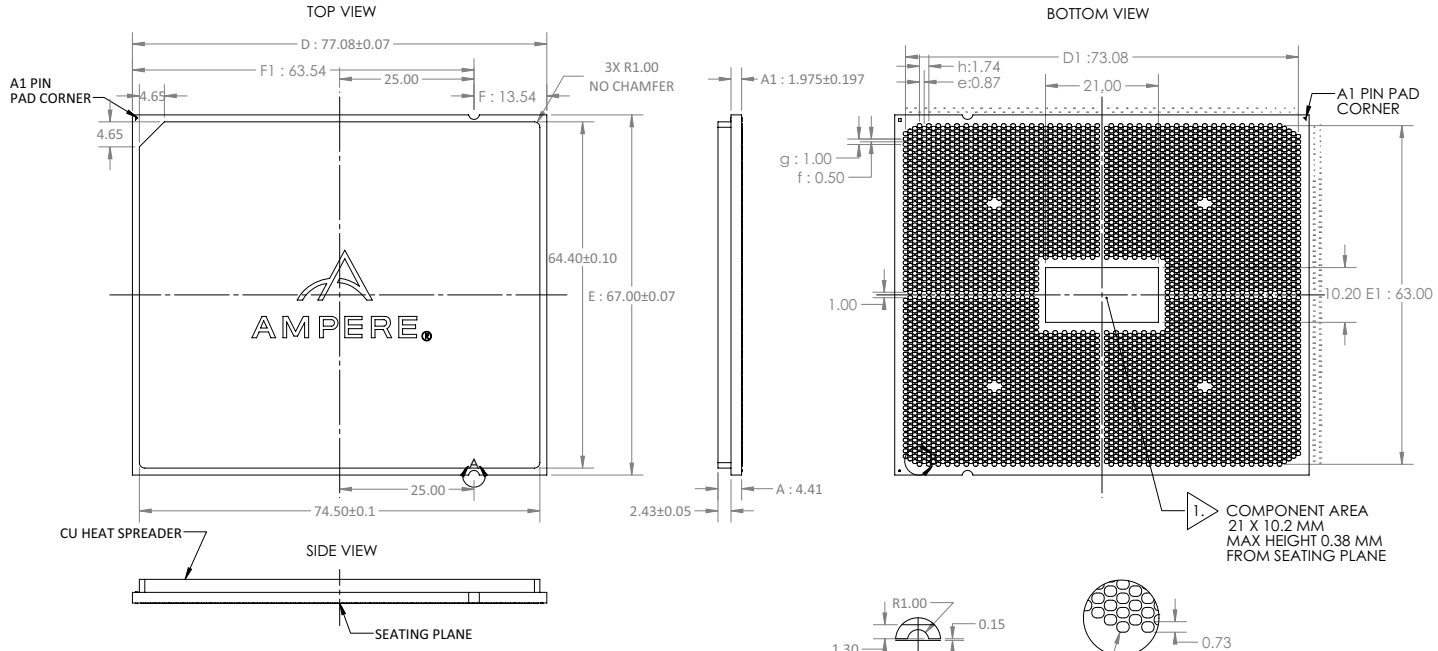
Altra provides four JTAG debug interfaces in two categories:

- SoC debug/test:
  - SoC Test Access Port (TAP): Used for manufacturing and RMA testing
- System debug:
  - System DAP: Used to debug Altra processors, caches, and CMI
  - SMpro DAP: Used to debug the SMpro ROM and firmware
  - PMpro DAP: Used to debug PMpro firmware

Refer to the DAP JTAG subsection in *Table 7 on page 54* for details on the implementation of the DAP interface.

3. Mechanical Data and Package Marking

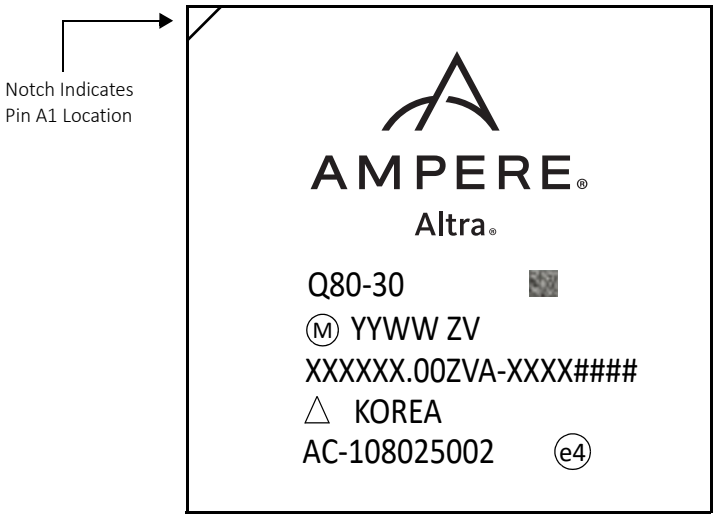
Figure 1: Altra 77.08 mm × 67.00 mm 4926-Pin Flip Chip Land Grid Array (FCLGA) Mechanical Data



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	-	4.41	4.67	
A1	1.778	1.975	2.172	
D	77.01	77.08	77.15	
E	66.93	67.000	67.07	
D1	-	73.080	-	
E1		63.000		
F		13.54		
F1		63.54		
e	0.87 BASIC			
f	0.50 BASIC			
g	1.00 BASIC			
h	1.74 BASIC			

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
LINEAR:
X.X ±0.1
X.XX ±0.05
X.XXX ±0.030
ANGULAR: ±1°

Figure 2: Altra Package Marking – Silicon Revision A1



First Line: Ampere Computing logo
Second Line: Ampere Computing Product Name
Third Line: Ampere SKU ID and 2D QR Code (26 Digits)
Fourth Line: M: Mask Protection Symbol (fixed) and Date Code:
YY: Year Date Code of Assembly
WW: Work Week Date Code of Assembly
ZV: Substrate Supplier and Substrate Version (Internal Use Only)
Fifth Line: 21 Digits from Assembly Lot + Substrate Version + Wafer ID + X/Y Coordinate
Sixth Line: △: ESD Symbol (fixed) and Country of Origin
Seventh Line: Ampere Ordering Part Number and RoHS Symbol
For more information, see *"Device Ordering Information" on page 7*

4. Processor Mass Specification

The typical weight of the processor is 112 grams, which includes the weight of all the components in the package.

5. Pin Assignment — Sorted by Pin Number

Table 5 lists the Altra pins sorted by pin number. Note that only the default signal name is shown for each pin (ball).

Note: *Pound sign (#) represents a depopulated ball location.*

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 1 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
A1	#	A65	VSS	B46	DDR4_ADDR_6	C25	DDR4_DATA_36
A3	#	A67	VSS	B48	DDR4_ADDR_9	C27	DDR4_ODT_1
A5	VSS	A69	VSS	B50	DDR4_BG_0	C29	DDR4_CS_N_3
A7	VSS	A71	VSS	B52	DDR4_CKE_3	C31	DDR4_ADDR_15_CAS_N
A9	VSS	A73	VSS	B54	DDR4_DATA_67	C33	DDR4_CS_N_0
A11	VSS	A75	VSS	B56	DDR4_DSTR_8_P	C35	DDR4_BA_1
A13	VSS	A77	VSS	B58	DDR4_DATA_65	C37	DDR4_CLK_0_N
A15	VSS	A79	VSS	B60	DDR4_DATA_27	C39	DDR4_CLK_1_N
A17	VSS	A81	VSS	B62	DDR4_DSTR_3_P	C41	DDR4_CLK_2_N
A19	VSS	A83	#	B64	DDR4_DATA_25	C43	DDR4_ADDR_2
A21	VSS	B2	#	B66	DDR4_DATA_19	C45	DDR4_ADDR_5
A23	VSS	B4	DDR4_DSTR_16_N	B68	DDR4_DSTR_2_P	C47	DDR4_ADDR_11
A25	VSS	B6	DDR4_DATA_61	B70	DDR4_DATA_17	C49	DDR4_BG_1
A27	VDDQ_DDR4567	B8	DDR4_DATA_55	B72	DDR4_DATA_11	C51	DDR4_CKE_2
A29	VSS	B10	DDR4_DSTR_15_N	B74	DDR4_DSTR_1_P	C53	VSS
A31	VDDQ_DDR4567	B12	DDR4_DATA_53	B76	DDR4_DATA_9	C55	DDR4_DATA_66
A33	VSS	B14	DDR4_DATA_47	B78	DDR4_DATA_3	C57	DDR4_DSTR_8_N
A35	VDDQ_DDR4567	B16	DDR4_DSTR_14_N	B80	DDR4_DSTR_0_P	C59	DDR4_DATA_64
A37	VSS	B18	DDR4_DATA_45	B82	DDR4_DATA_1	C61	DDR4_DATA_26
A39	VDDQ_DDR4567	B20	DDR4_DATA_39	B84	#	C63	DDR4_DSTR_3_N
A41	VSS	B22	DDR4_DSTR_13_N	C1	#	C65	DDR4_DATA_24
A43	VSS	B24	DDR4_DATA_37	C3	DDR4_DATA_62	C67	DDR4_DATA_18
A45	VSS	B26	DDR4_ATB0	C5	DDR4_DSTR_16_P	C69	DDR4_DSTR_2_N
A47	VDDQ_DDR4567	B28	DDR4_ODT_3	C7	DDR4_DATA_60	C71	DDR4_DATA_16
A49	VSS	B30	DDR4_CS_N_1	C9	DDR4_DATA_54	C73	DDR4_DATA_10
A51	VDDQ_DDR4567	B32	DDR4_ODT_0	C11	DDR4_DSTR_15_P	C75	DDR4_DSTR_1_N
A53	VSS	B34	DDR4_ADDR_16_RAS_N	C13	DDR4_DATA_52	C77	DDR4_DATA_8
A55	VSS	B36	DDR4_ADDR_0	C15	DDR4_DATA_46	C79	DDR4_DATA_2
A57	VSS	B38	DDR4_CLK_0_P	C17	DDR4_DSTR_14_P	C81	DDR4_DSTR_0_N
A59	VSS	B40	DDR4_CLK_1_P	C19	DDR4_DATA_44	C83	DDR4_DATA_0
A61	VSS	B42	DDR4_CLK_2_P	C21	DDR4_DATA_38	D2	VSS
A63	VSS	B44	DDR4_ADDR_1	C23	DDR4_DSTR_13_P	D4	VSS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 2 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
D6	VSS	D78	VSS	E65	DDR4_DATA_28	F54	DDR4_DATA_71
D8	VSS	D80	VSS	E67	DDR4_DATA_22	F56	DDR4_DSTR_17_N
D10	VSS	D82	VSS	E69	DDR4_DSTR_11_P	F58	DDR4_DATA_69
D12	VSS	D84	VSS	E71	DDR4_DATA_20	F60	DDR4_DATA_31
D14	VSS	E1	DDR4_DATA_63	E73	DDR4_DATA_14	F62	DDR4_DSTR_12_N
D16	VSS	E3	DDR4_DATA_58	E75	DDR4_DSTR_10_P	F64	DDR4_DATA_29
D18	VSS	E5	DDR4_DSTR_7_N	E77	DDR4_DATA_12	F66	DDR4_DATA_23
D20	VSS	E7	DDR4_DATA_56	E79	DDR4_DATA_6	F68	DDR4_DSTR_11_N
D22	VSS	E9	DDR4_DATA_50	E81	DDR4_DSTR_9_P	F70	DDR4_DATA_21
D24	VSS	E11	DDR4_DSTR_6_N	E83	DDR4_DATA_5	F72	DDR4_DATA_15
D26	VSS	E13	DDR4_DATA_48	F2	DDR4_DATA_59	F74	DDR4_DSTR_10_N
D28	VDDQ_DDR4567	E15	DDR4_DATA_42	F4	DDR4_DSTR_7_P	F76	DDR4_DATA_13
D30	VDDQ_DDR4567	E17	DDR4_DSTR_5_N	F6	DDR4_DATA_57	F78	DDR4_DATA_7
D32	VDDQ_DDR4567	E19	DDR4_DATA_40	F8	DDR4_DATA_51	F80	DDR4_DSTR_9_N
D34	VDDQ_DDR4567	E21	DDR4_DATA_34	F10	DDR4_DSTR_6_P	F82	DDR4_DATA_4
D36	VDDQ_DDR4567	E23	DDR4_DSTR_4_N	F12	DDR4_DATA_49	F84	VSS
D38	VDDQ_DDR4567	E25	DDR4_DATA_32	F14	DDR4_DATA_43	G1	VSS
D40	VDDQ_DDR4567	E27	DDR4_CID_0	F16	DDR4_DSTR_5_P	G3	VSS
D42	VDDQ_DDR4567	E29	DDR4_CID_2	F18	DDR4_DATA_41	G5	VSS
D44	VDDQ_DDR4567	E31	DDR4_ADDR_13	F20	DDR4_DATA_35	G7	VSS
D46	VDDQ_DDR4567	E33	DDR4_CS_N_2	F22	DDR4_DSTR_4_P	G9	VSS
D48	VDDQ_DDR4567	E35	DDR4_ADDR_10	F24	DDR4_DATA_33	G11	VSS
D50	VDDQ_DDR4567	E37	DDR4_PAR	F26	DDR4_ATB1	G13	VSS
D52	VDDQ_DDR4567	E39	VDDQ_DDR4567	F28	DDR4_CID_1	G15	VSS
D54	VSS	E41	DDR4_CLK_3_N	F30	DDR4_ADDR_17	G17	VSS
D56	VSS	E43	DDR4_ADDR_3	F32	DDR4_ODT_2	G19	VSS
D58	VSS	E45	DDR4_ADDR_8	F34	DDR4_ADDR_14_WE_N	G21	VSS
D60	VSS	E47	DDR4_ADDR_12	F36	DDR4_BA_0	G23	VSS
D62	VSS	E49	DDR4_ACT_N	F38	VSS	G25	VSS
D64	VSS	E51	DDR4_CKE_1	F40	VDDQ_DDR4567	G27	VDDQ_DDR4567
D66	VSS	E53	VSS	F42	DDR4_CLK_3_P	G29	VSS
D68	VSS	E55	DDR4_DATA_70	F44	DDR4_ADDR_4	G31	VDDQ_DDR4567
D70	VSS	E57	DDR4_DSTR_17_P	F46	DDR4_ADDR_7	G33	VSS
D72	VSS	E59	DDR4_DATA_68	F48	DDR4_ALERT_N	G35	VDDQ_DDR4567
D74	VSS	E61	DDR4_DATA_30	F50	DDR4_CKE_0	G37	VSS
D76	VSS	E63	DDR4_DSTR_12_P	F52	DDR4_RESETN	G39	VDDQ_DDR4567

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 3 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
G41	VSS	H30	VDDQ_DDR4567	J17	DDR5_DSTR_14_P	K6	DDR5_DATA_56
G43	VSS	H32	VDDQ_DDR4567	J19	DDR5_DATA_44	K8	DDR5_DATA_50
G45	VSS	H34	VDDQ_DDR4567	J21	DDR5_DATA_38	K10	DDR5_DSTR_15_N
G47	VDDQ_DDR4567	H36	VDDQ_DDR4567	J23	DDR5_DSTR_13_P	K12	DDR5_DATA_48
G49	VSS	H38	VDDQ_DDR4567	J25	DDR5_DATA_36	K14	DDR5_DATA_42
G51	VDDQ_DDR4567	H40	VDDQ_DDR4567	J27	DDR5_CID_1	K16	DDR5_DSTR_14_N
G53	VSS	H42	VSS	J29	DDR5_ADDR_17	K18	DDR5_DATA_40
G55	VSS	H44	VDDQ_DDR4567	J31	DDR5_ODT_2	K20	DDR5_DATA_34
G57	VSS	H46	VDDQ_DDR4567	J33	DDR5_ADDR_14_WE_N	K22	DDR5_DSTR_13_N
G59	VSS	H48	VDDQ_DDR4567	J35	DDR5_BA_0	K24	DDR5_DATA_32
G61	VSS	H50	VDDQ_DDR4567	J37	DDR5_CLK_0_N	K26	DDR5_ATB0
G63	VSS	H52	VDDQ_DDR4567	J39	DDR5_CLK_2_N	K28	DDR5_ODT_3
G65	VSS	H54	VSS	J41	VDDQ_DDR4567	K30	DDR5_CS_N_1
G67	VSS	H56	VSS	J43	DDR5_ADDR_2	K32	DDR5_ODT_0
G69	VSS	H58	VSS	J45	DDR5_ADDR_5	K34	DDR5_ADDR_16_RAS_N
G71	VSS	H60	VSS	J47	DDR5_ADDR_11	K36	DDR5_ADDR_0
G73	VSS	H62	VSS	J49	DDR5_BG_1	K38	DDR5_CLK_0_P
G75	VSS	H64	VSS	J51	DDR5_CKE_2	K40	DDR5_CLK_2_P
G77	VSS	H66	VSS	J53	VSS	K42	VDDQ_DDR4567
G79	VSS	H68	VSS	J55	DDR5_DATA_71	K44	DDR5_ADDR_3
G81	VSS	H70	VSS	J57	DDR5_DSTR_8_N	K46	DDR5_ADDR_8
G83	VSS	H72	VSS	J59	DDR5_DATA_69	K48	DDR5_ADDR_12
H2	VSS	H74	VSS	J61	DDR5_DATA_31	K50	DDR5_ACT_N
H4	VSS	H76	VSS	J63	DDR5_DSTR_3_N	K52	DDR5_CKE_1
H6	VSS	H78	VSS	J65	DDR5_DATA_29	K54	DDR5_DATA_67
H8	VSS	H80	VSS	J67	DDR5_DATA_23	K56	DDR5_DSTR_8_P
H10	VSS	H82	VSS	J69	DDR5_DSTR_2_N	K58	DDR5_DATA_65
H12	VSS	H84	VSS	J71	DDR5_DATA_21	K60	DDR5_DATA_27
H14	VSS	J1	VSS	J73	DDR5_DATA_15	K62	DDR5_DSTR_3_P
H16	VSS	J3	DDR5_DATA_62	J75	DDR5_DSTR_1_N	K64	DDR5_DATA_25
H18	VSS	J5	DDR5_DSTR_16_P	J77	DDR5_DATA_13	K66	DDR5_DATA_19
H20	VSS	J7	DDR5_DATA_60	J79	DDR5_DATA_7	K68	DDR5_DSTR_2_P
H22	VSS	J9	DDR5_DATA_54	J81	DDR5_DSTR_0_N	K70	DDR5_DATA_17
H24	VSS	J11	DDR5_DSTR_15_P	J83	DDR5_DATA_1	K72	DDR5_DATA_11
H26	VSS	J13	DDR5_DATA_52	K2	DDR5_DATA_63	K74	DDR5_DSTR_1_P
H28	VDDQ_DDR4567	J15	DDR5_DATA_46	K4	DDR5_DSTR_16_N	K76	DDR5_DATA_9

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 4 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
K78	DDR5_DATA_3	L65	VSS	M54	DDR5_DATA_66	N41	DDR5_CLK_3_P
K80	DDR5_DSTR_0_P	L67	VSS	M56	DDR5_DSTR_17_N	N43	DDR5_ADDR_1
K82	DDR5_DATA_0	L69	VSS	M58	DDR5_DATA_64	N45	DDR5_ADDR_6
K84	VSS	L71	VSS	M60	DDR5_DATA_26	N47	DDR5_ADDR_9
L1	VSS	L73	VSS	M62	DDR5_DSTR_12_N	N49	DDR5_BG_0
L3	VSS	L75	VSS	M64	DDR5_DATA_24	N51	DDR5_CKE_3
L5	VSS	L77	VSS	M66	DDR5_DATA_18	N53	VSS
L7	VSS	L79	VSS	M68	DDR5_DSTR_11_N	N55	DDR5_DATA_70
L9	VSS	L81	VSS	M70	DDR5_DATA_16	N57	DDR5_DSTR_17_P
L11	VSS	L83	VSS	M72	DDR5_DATA_10	N59	DDR5_DATA_68
L13	VSS	M2	DDR5_DATA_58	M74	DDR5_DSTR_10_N	N61	DDR5_DATA_30
L15	VSS	M4	DDR5_DSTR_7_P	M76	DDR5_DATA_8	N63	DDR5_DSTR_12_P
L17	VSS	M6	DDR5_DATA_57	M78	DDR5_DATA_2	N65	DDR5_DATA_28
L19	VSS	M8	DDR5_DATA_51	M80	DDR5_DSTR_9_N	N67	DDR5_DATA_22
L21	VSS	M10	DDR5_DSTR_6_P	M82	DDR5_DATA_5	N69	DDR5_DSTR_11_P
L23	VSS	M12	DDR5_DATA_49	M84	VSS	N71	DDR5_DATA_20
L25	VSS	M14	DDR5_DATA_43	N1	VSS	N73	DDR5_DATA_14
L27	VDDQ_DDR4567	M16	DDR5_DSTR_5_P	N3	DDR5_DATA_59	N75	DDR5_DSTR_10_P
L29	VDDQ_DDR4567	M18	DDR5_DATA_41	N5	DDR5_DSTR_7_N	N77	DDR5_DATA_12
L31	VDDQ_DDR4567	M20	DDR5_DATA_35	N7	DDR5_DATA_61	N79	DDR5_DATA_6
L33	VDDQ_DDR4567	M22	DDR5_DSTR_4_P	N9	DDR5_DATA_55	N81	DDR5_DSTR_9_P
L35	VDDQ_DDR4567	M24	DDR5_DATA_33	N11	DDR5_DSTR_6_N	N83	DDR5_DATA_4
L37	VDDQ_DDR4567	M26	DDR5_ATB1	N13	DDR5_DATA_53	P2	VSS
L39	VDDQ_DDR4567	M28	DDR5_ODT_1	N15	DDR5_DATA_47	P4	VSS
L41	VDDQ_DDR4567	M30	DDR5_CS_N_3	N17	DDR5_DSTR_5_N	P6	VSS
L43	VDDQ_DDR4567	M32	DDR5_ADDR_15_CAS_N	N19	DDR5_DATA_45	P8	VSS
L45	VDDQ_DDR4567	M34	DDR5_CS_N_0	N21	DDR5_DATA_39	P10	VSS
L47	VDDQ_DDR4567	M36	DDR5_BA_1	N23	DDR5_DSTR_4_N	P12	VSS
L49	VDDQ_DDR4567	M38	DDR5_CLK_1_N	N25	DDR5_DATA_37	P14	VSS
L51	VDDQ_DDR4567	M40	DDR5_CLK_3_N	N27	DDR5_CID_0	P16	VSS
L53	VSS	M42	VDDQ_DDR4567	N29	DDR5_CID_2	P18	VSS
L55	VSS	M44	DDR5_ADDR_4	N31	DDR5_ADDR_13	P20	VSS
L57	VSS	M46	DDR5_ADDR_7	N33	DDR5_CS_N_2	P22	VSS
L59	VSS	M48	DDR5_ALERT_N	N35	DDR5_ADDR_10	P24	VSS
L61	VSS	M50	DDR5_CKE_0	N37	DDR5_PAR	P26	VSS
L63	VSS	M52	DDR5_RESETN	N39	DDR5_CLK_1_P	P28	VDDQ_DDR4567

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 5 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
P30	VDDQ_DDR4567	R17	VSS	T6	DDR6_DATA_56	T78	DDR6_DATA_3
P32	VDDQ_DDR4567	R19	VSS	T8	DDR6_DATA_50	T80	DDR6_DSTR_0_P
P34	VDDQ_DDR4567	R21	VSS	T10	DDR6_DSTR_15_N	T82	DDR6_DATA_1
P36	VDDQ_DDR4567	R23	VSS	T12	DDR6_DATA_48	T84	VSS
P38	VDDQ_DDR4567	R25	VSS	T14	DDR6_DATA_42	U1	VSS
P40	VDDQ_DDR4567	R27	VDDQ_DDR4567	T16	DDR6_DSTR_14_N	U3	DDR6_DATA_63
P42	VSS	R29	VSS	T18	DDR6_DATA_40	U5	DDR6_DSTR_16_P
P44	VDDQ_DDR4567	R31	VDDQ_DDR4567	T20	DDR6_DATA_34	U7	DDR6_DATA_60
P46	VDDQ_DDR4567	R33	VSS	T22	DDR6_DSTR_13_N	U9	DDR6_DATA_54
P48	VDDQ_DDR4567	R35	VDDQ_DDR4567	T24	DDR6_DATA_32	U11	DDR6_DSTR_15_P
P50	VDDQ_DDR4567	R37	VSS	T26	DDR6_ATB0	U13	DDR6_DATA_52
P52	VDDQ_DDR4567	R39	VDDQ_DDR4567	T28	DDR6_ODT_3	U15	DDR6_DATA_46
P54	VSS	R41	VSS	T30	DDR6_CS_N_1	U17	DDR6_DSTR_14_P
P56	VSS	R43	VSS	T32	DDR6_ODT_0	U19	DDR6_DATA_44
P58	VSS	R45	VSS	T34	DDR6_ADDR_16_RAS_N	U21	DDR6_DATA_38
P60	VSS	R47	VDDQ_DDR4567	T36	DDR6_ADDR_0	U23	DDR6_DSTR_13_P
P62	VSS	R49	VSS	T38	DDR6_CLK_0_P	U25	DDR6_DATA_36
P64	VSS	R51	VDDQ_DDR4567	T40	DDR6_CLK_2_P	U27	DDR6_CID_1
P66	VSS	R53	VSS	T42	VSS	U29	DDR6_ADDR_17
P68	VSS	R55	VSS	T44	DDR6_ADDR_3	U31	DDR6_ODT_2
P70	VSS	R57	VSS	T46	DDR6_ADDR_8	U33	DDR6_ADDR_14_WE_N
P72	VSS	R59	VSS	T48	DDR6_ADDR_12	U35	DDR6_BA_0
P74	VSS	R61	VSS	T50	DDR6_ACT_N	U37	DDR6_CLK_0_N
P76	VSS	R63	VSS	T52	DDR6_CKE_1	U39	DDR6_CLK_2_N
P78	VSS	R65	VSS	T54	DDR6_DATA_67	U41	VDDQ_DDR4567
P80	VSS	R67	VSS	T56	DDR6_DSTR_8_P	U43	DDR6_ADDR_2
P82	VSS	R69	VSS	T58	DDR6_DATA_65	U45	DDR6_ADDR_5
P84	VSS	R71	VSS	T60	DDR6_DATA_27	U47	DDR6_ADDR_11
R1	VSS	R73	VSS	T62	DDR6_DSTR_3_P	U49	DDR6_BG_1
R3	VSS	R75	VSS	T64	DDR6_DATA_25	U51	DDR6_CKE_2
R5	VSS	R77	VSS	T66	DDR6_DATA_19	U53	VSS
R7	VSS	R79	VSS	T68	DDR6_DSTR_2_P	U55	DDR6_DATA_71
R9	VSS	R81	VSS	T70	DDR6_DATA_17	U57	DDR6_DSTR_8_N
R11	VSS	R83	VSS	T72	DDR6_DATA_11	U59	DDR6_DATA_69
R13	VSS	T2	DDR6_DATA_62	T74	DDR6_DSTR_1_P	U61	DDR6_DATA_31
R15	VSS	T4	DDR6_DSTR_16_N	T76	DDR6_DATA_9	U63	DDR6_DSTR_3_N

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 6 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
U65	DDR6_DATA_29	V54	VSS	W41	DDR6_CLK_3_P	Y30	DDR6_CS_N_3
U67	DDR6_DATA_23	V56	VSS	W43	DDR6_ADDR_1	Y32	DDR6_ADDR_15_CAS_N
U69	DDR6_DSTR_2_N	V58	VSS	W45	DDR6_ADDR_6	Y34	DDR6_CS_N_0
U71	DDR6_DATA_21	V60	VSS	W47	DDR6_ADDR_9	Y36	DDR6_BA_1
U73	DDR6_DATA_15	V62	VSS	W49	DDR6_BG_0	Y38	DDR6_CLK_1_N
U75	DDR6_DSTR_1_N	V64	VSS	W51	DDR6_CKE_3	Y40	DDR6_CLK_3_N
U77	DDR6_DATA_13	V66	VSS	W53	VSS	Y42	VSS
U79	DDR6_DATA_7	V68	VSS	W55	DDR6_DATA_70	Y44	DDR6_ADDR_4
U81	DDR6_DSTR_0_N	V70	VSS	W57	DDR6_DSTR_17_P	Y46	DDR6_ADDR_7
U83	DDR6_DATA_0	V72	VSS	W59	DDR6_DATA_68	Y48	DDR6_ALERT_N
V2	VSS	V74	VSS	W61	DDR6_DATA_30	Y50	DDR6_CKE_0
V4	VSS	V76	VSS	W63	DDR6_DSTR_12_P	Y52	DDR6_RESETN
V6	VSS	V78	VSS	W65	DDR6_DATA_28	Y54	DDR6_DATA_66
V8	VSS	V80	VSS	W67	DDR6_DATA_22	Y56	DDR6_DSTR_17_N
V10	VSS	V82	VSS	W69	DDR6_DSTR_11_P	Y58	DDR6_DATA_64
V12	VSS	V84	VSS	W71	DDR6_DATA_20	Y60	DDR6_DATA_26
V14	VSS	W1	VSS	W73	DDR6_DATA_14	Y62	DDR6_DSTR_12_N
V16	VSS	W3	DDR6_DATA_58	W75	DDR6_DSTR_10_P	Y64	DDR6_DATA_24
V18	VSS	W5	DDR6_DSTR_7_N	W77	DDR6_DATA_12	Y66	DDR6_DATA_18
V20	VSS	W7	DDR6_DATA_61	W79	DDR6_DATA_6	Y68	DDR6_DSTR_11_N
V22	VSS	W9	DDR6_DATA_55	W81	DDR6_DSTR_9_P	Y70	DDR6_DATA_16
V24	VSS	W11	DDR6_DSTR_6_N	W83	DDR6_DATA_5	Y72	DDR6_DATA_10
V26	VSS	W13	DDR6_DATA_53	Y2	DDR6_DATA_59	Y74	DDR6_DSTR_10_N
V28	VDDQ_DDR4567	W15	DDR6_DATA_47	Y4	DDR6_DSTR_7_P	Y76	DDR6_DATA_8
V30	VDDQ_DDR4567	W17	DDR6_DSTR_5_N	Y6	DDR6_DATA_57	Y78	DDR6_DATA_2
V32	VDDQ_DDR4567	W19	DDR6_DATA_45	Y8	DDR6_DATA_51	Y80	DDR6_DSTR_9_N
V34	VDDQ_DDR4567	W21	DDR6_DATA_39	Y10	DDR6_DSTR_6_P	Y82	DDR6_DATA_4
V36	VDDQ_DDR4567	W23	DDR6_DSTR_4_N	Y12	DDR6_DATA_49	Y84	VSS
V38	VDDQ_DDR4567	W25	DDR6_DATA_37	Y14	DDR6_DATA_43	AA1	VSS
V40	VDDQ_DDR4567	W27	DDR6_CID_0	Y16	DDR6_DSTR_5_P	AA3	VSS
V42	VDDQ_DDR4567	W29	DDR6_CID_2	Y18	DDR6_DATA_41	AA5	VSS
V44	VDDQ_DDR4567	W31	DDR6_ADDR_13	Y20	DDR6_DATA_35	AA7	VSS
V46	VDDQ_DDR4567	W33	DDR6_CS_N_2	Y22	DDR6_DSTR_4_P	AA9	VSS
V48	VDDQ_DDR4567	W35	DDR6_ADDR_10	Y24	DDR6_DATA_33	AA11	VSS
V50	VDDQ_DDR4567	W37	DDR6_PAR	Y26	DDR6_ATB1	AA13	VSS
V52	VDDQ_DDR4567	W39	DDR6_CLK_1_P	Y28	DDR6_ODT_1	AA15	VSS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 7 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
AA17	VSS	AB6	VSS	AB78	VSS	AC65	DDR7_DATA_29
AA19	VSS	AB8	VSS	AB80	VSS	AC67	DDR7_DATA_23
AA21	VSS	AB10	VSS	AB82	VSS	AC69	DDR7_DSTR_2_N
AA23	VSS	AB12	VSS	AB84	VSS	AC71	DDR7_DATA_21
AA25	VSS	AB14	VSS	AC1	VSS	AC73	DDR7_DATA_15
AA27	VDDQ_DDR4567	AB16	VSS	AC3	DDR7_DATA_62	AC75	DDR7_DSTR_1_N
AA29	VSS	AB18	VSS	AC5	DDR7_DSTR_16_P	AC77	DDR7_DATA_13
AA31	VDDQ_DDR4567	AB20	VSS	AC7	DDR7_DATA_60	AC79	DDR7_DATA_7
AA33	VSS	AB22	VSS	AC9	DDR7_DATA_54	AC81	DDR7_DSTR_0_N
AA35	VDDQ_DDR4567	AB24	VSS	AC11	DDR7_DSTR_15_P	AC83	DDR7_DATA_1
AA37	VSS	AB26	VSS	AC13	DDR7_DATA_52	AD2	DDR7_DATA_63
AA39	VDDQ_DDR4567	AB28	VDDQ_DDR4567	AC15	DDR7_DATA_46	AD4	DDR7_DSTR_16_N
AA41	VSS	AB30	VDDQ_DDR4567	AC17	DDR7_DSTR_14_P	AD6	DDR7_DATA_56
AA43	VSS	AB32	VDDQ_DDR4567	AC19	DDR7_DATA_44	AD8	DDR7_DATA_50
AA45	VSS	AB34	VDDQ_DDR4567	AC21	DDR7_DATA_38	AD10	DDR7_DSTR_15_N
AA47	VDDQ_DDR4567	AB36	VDDQ_DDR4567	AC23	DDR7_DSTR_13_P	AD12	DDR7_DATA_48
AA49	VSS	AB38	VDDQ_DDR4567	AC25	DDR7_DATA_36	AD14	DDR7_DATA_42
AA51	VDDQ_DDR4567	AB40	VDDQ_DDR4567	AC27	DDR7_CID_1	AD16	DDR7_DSTR_14_N
AA53	VSS	AB42	VSS	AC29	DDR7_ADDR_17	AD18	DDR7_DATA_40
AA55	VSS	AB44	VDDQ_DDR4567	AC31	DDR7_ODT_2	AD20	DDR7_DATA_34
AA57	VSS	AB46	VDDQ_DDR4567	AC33	DDR7_ADDR_14_WE_N	AD22	DDR7_DSTR_13_N
AA59	VSS	AB48	VDDQ_DDR4567	AC35	DDR7_BA_0	AD24	DDR7_DATA_32
AA61	VSS	AB50	VDDQ_DDR4567	AC37	DDR7_CLK_0_N	AD26	DDR7_ATB0
AA63	VSS	AB52	VDDQ_DDR4567	AC39	DDR7_CLK_2_N	AD28	DDR7_ODT_3
AA65	VSS	AB54	VSS	AC41	VDDQ_DDR4567	AD30	DDR7_CS_N_1
AA67	VSS	AB56	VSS	AC43	DDR7_ADDR_2	AD32	DDR7_ODT_0
AA69	VSS	AB58	VSS	AC45	DDR7_ADDR_5	AD34	DDR7_ADDR_16_RAS_N
AA71	VSS	AB60	VSS	AC47	DDR7_ADDR_11	AD36	DDR7_ADDR_0
AA73	VSS	AB62	VSS	AC49	DDR7_BG_1	AD38	DDR7_CLK_0_P
AA75	VSS	AB64	VSS	AC51	DDR7_CKE_2	AD40	DDR7_CLK_2_P
AA77	VSS	AB66	VSS	AC53	VSS	AD42	VDDQ_DDR4567
AA79	VSS	AB68	VSS	AC55	DDR7_DATA_71	AD44	DDR7_ADDR_3
AA81	VSS	AB70	VSS	AC57	DDR7_DSTR_8_N	AD46	DDR7_ADDR_8
AA83	VSS	AB72	VSS	AC59	DDR7_DATA_69	AD48	DDR7_ADDR_12
AB2	VSS	AB74	VSS	AC61	DDR7_DATA_31	AD50	DDR7_ACT_N
AB4	VSS	AB76	VSS	AC63	DDR7_DSTR_3_N	AD52	DDR7_CKE_1

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 8 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
AD54	DDR7_DATA_67	AE41	VDDQ_DDR4567	AF30	DDR7_CS_N_3	AG17	DDR7_DSTR_5_N
AD56	DDR7_DSTR_8_P	AE43	VDDQ_DDR4567	AF32	DDR7_ADDR_15_CAS_N	AG19	DDR7_DATA_45
AD58	DDR7_DATA_65	AE45	VDDQ_DDR4567	AF34	DDR7_CS_N_0	AG21	DDR7_DATA_39
AD60	DDR7_DATA_27	AE47	VDDQ_DDR4567	AF36	DDR7_BA_1	AG23	DDR7_DSTR_4_N
AD62	DDR7_DSTR_3_P	AE49	VDDQ_DDR4567	AF38	DDR7_CLK_1_N	AG25	DDR7_DATA_37
AD64	DDR7_DATA_25	AE51	VDDQ_DDR4567	AF40	DDR7_CLK_3_N	AG27	DDR7_CID_0
AD66	DDR7_DATA_19	AE53	VSS	AF42	VSS	AG29	DDR7_CID_2
AD68	DDR7_DSTR_2_P	AE55	VSS	AF44	DDR7_ADDR_4	AG31	DDR7_ADDR_13
AD70	DDR7_DATA_17	AE57	VSS	AF46	DDR7_ADDR_7	AG33	DDR7_CS_N_2
AD72	DDR7_DATA_11	AE59	VSS	AF48	DDR7_ALERT_N	AG35	DDR7_ADDR_10
AD74	DDR7_DSTR_1_P	AE61	VSS	AF50	DDR7_CKE_0	AG37	DDR7_PAR
AD76	DDR7_DATA_9	AE63	VSS	AF52	DDR7_RESETN	AG39	DDR7_CLK_1_P
AD78	DDR7_DATA_3	AE65	VSS	AF54	DDR7_DATA_66	AG41	DDR7_CLK_3_P
AD80	DDR7_DSTR_0_P	AE67	VSS	AF56	DDR7_DSTR_17_N	AG43	DDR7_ADDR_1
AD82	DDR7_DATA_0	AE69	VSS	AF58	DDR7_DATA_64	AG45	DDR7_ADDR_6
AD84	VSS	AE71	VSS	AF60	DDR7_DATA_26	AG47	DDR7_ADDR_9
AE1	VSS	AE73	VSS	AF62	DDR7_DSTR_12_N	AG49	DDR7_BG_0
AE3	VSS	AE75	VSS	AF64	DDR7_DATA_24	AG51	DDR7_CKE_3
AE5	VSS	AE77	VSS	AF66	DDR7_DATA_18	AG53	VSS
AE7	VSS	AE79	VSS	AF68	DDR7_DSTR_11_N	AG55	DDR7_DATA_70
AE9	VSS	AE81	VSS	AF70	DDR7_DATA_16	AG57	DDR7_DSTR_17_P
AE11	VSS	AE83	VSS	AF72	DDR7_DATA_10	AG59	DDR7_DATA_68
AE13	VSS	AF2	DDR7_DATA_58	AF74	DDR7_DSTR_10_N	AG61	DDR7_DATA_30
AE15	VSS	AF4	DDR7_DSTR_7_P	AF76	DDR7_DATA_8	AG63	DDR7_DSTR_12_P
AE17	VSS	AF6	DDR7_DATA_57	AF78	DDR7_DATA_2	AG65	DDR7_DATA_28
AE19	VSS	AF8	DDR7_DATA_51	AF80	DDR7_DSTR_9_N	AG67	DDR7_DATA_22
AE21	VSS	AF10	DDR7_DSTR_6_P	AF82	DDR7_DATA_5	AG69	DDR7_DSTR_11_P
AE23	VSS	AF12	DDR7_DATA_49	AF84	VSS	AG71	DDR7_DATA_20
AE25	VSS	AF14	DDR7_DATA_43	AG1	VSS	AG73	DDR7_DATA_14
AE27	VDDQ_DDR4567	AF16	DDR7_DSTR_5_P	AG3	DDR7_DATA_59	AG75	DDR7_DSTR_10_P
AE29	VDDQ_DDR4567	AF18	DDR7_DATA_41	AG5	DDR7_DSTR_7_N	AG77	DDR7_DATA_12
AE31	VDDQ_DDR4567	AF20	DDR7_DATA_35	AG7	DDR7_DATA_61	AG79	DDR7_DATA_6
AE33	VDDQ_DDR4567	AF22	DDR7_DSTR_4_P	AG9	DDR7_DATA_55	AG81	DDR7_DSTR_9_P
AE35	VDDQ_DDR4567	AF24	DDR7_DATA_33	AG11	DDR7_DSTR_6_N	AG83	DDR7_DATA_4
AE37	VDDQ_DDR4567	AF26	DDR7_ATB1	AG13	DDR7_DATA_53	AH2	VSS
AE39	VDDQ_DDR4567	AF28	DDR7_ODT_1	AG15	DDR7_DATA_47	AH4	VSS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 9 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
AH6	VSS	AH78	VSS	AJ65	#	AK54	SLAVE_PRESENT_N
AH8	VSS	AH80	VSS	AJ67	JTAG_SELECT0	AK56	MASTER_2P
AH10	VSS	AH82	VSS	AJ69	JTAG_SELECT2	AK58	JTAG_PM_TCK
AH12	VSS	AH84	VSS	AJ71	VDDQ_DDR45_SENSE_P	AK60	JTAG_PM_TRSTN
AH14	VSS	AJ1	VSS	AJ73	VDDQ_DDR67_SENSE_P	AK62	JTAG_CMPL1
AH16	VSS	AJ3	GPIO_1	AJ75	JTAG_DAP_TDI	AK64	#
AH18	VSS	AJ5	GPIO_3	AJ77	JTAG_DAP_TCK	AK66	#
AH20	VSS	AJ7	GPIO_4	AJ79	JTAG_DAP_TRSTN	AK68	JTAG_SELECT1
AH22	VSS	AJ9	GPIO_6	AJ81	JTAG_SOC_TDO	AK70	JTAG_SELECT3
AH24	VSS	AJ11	GPIO_8	AJ83	JTAG_SOC_TMS	AK72	VDDQ_DDR45_SENSE_N
AH26	VSS	AJ13	GPIO_9	AK2	GPIO_0	AK74	VDDQ_DDR67_SENSE_N
AH28	VDDQ_DDR4567	AJ15	GPIO_11	AK4	GPIO_2	AK76	JTAG_DAP_TDO
AH30	VSS	AJ17	GPIO_13	AK6	VSS	AK78	JTAG_DAP_TMS
AH32	VDDQ_DDR4567	AJ19	GPIO_14	AK8	GPIO_5	AK80	JTAG_SOC_TDI
AH34	VSS	AJ21	#	AK10	GPIO_7	AK82	JTAG_SOC_TCK
AH36	VDDQ_DDR4567	AJ23	VSS	AK12	VSS	AK84	JTAG_SOC_TRSTN
AH38	VSS	AJ25	VSS	AK14	GPIO_10	AL1	VSS
AH40	VDDQ_DDR4567	AJ27	VSS	AK16	GPIO_12	AL3	VSS
AH42	VSS	AJ29	VSS	AK18	VSS	AL5	VSS
AH44	VDDQ_DDR4567	AJ31	VSS	AK20	#	AL7	VSS
AH46	VSS	AJ33	VSS	AK22	#	AL9	VSS
AH48	VDDQ_DDR4567	AJ35	VSS	AK24	VSS	AL11	VSS
AH50	VDDQ_DDR4567	AJ37	VSS	AK26	RFU_29	AL13	VSS
AH52	VDDQ_DDR4567	AJ39	VSS	AK28	ISOLATE_DIS0	AL15	VSS
AH54	VSS	AJ41	VSS	AK30	VSS	AL17	VSS
AH56	VSS	AJ43	VSS	AK32	GPIO_15	AL19	VSS
AH58	VSS	AJ45	VSS	AK34	VSS	AL21	#
AH60	VSS	AJ47	VSS	AK36	VSS	AL23	VSS
AH62	VSS	AJ49	VSS	AK38	JTAG_IPP_TRSTN	AL25	VSS
AH64	VSS	AJ51	VSS	AK40	VSS	AL27	RFU_30
AH66	VSS	AJ53	VSS	AK42	DDR6_PLL_TESTOUT_P	AL29	ISOLATE_DIS1
AH68	VSS	AJ55	TMR_CLK	AK44	VSS	AL31	GPIO_17
AH70	VSS	AJ57	JTAG_PM_TDO	AK46	VSS	AL33	GPIO_16
AH72	VSS	AJ59	JTAG_PM_TMS	AK48	TMR_RSTN	AL35	RFU_1
AH74	VSS	AJ61	JTAG_CMPL0	AK50	SYS_RESETN	AL37	JTAG_IPP_TDI
AH76	VSS	AJ63	JTAG_CMPL2	AK52	CLK_MON_OUT	AL39	JTAG_IPP_TMS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 10 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
AL41	DDR6_PLL_TESTOUT_N	AM30	GPIO_18	AN17	VSS	AP6	VSS
AL43	DDR7_PLL_TESTOUT_P	AM32	VSS	AN19	PCIERCA1_RX6_M	AP8	VSS
AL45	GPI_2	AM34	RFU_2	AN21	PCIERCA1_TX7_P	AP10	PCIERCA1_TX14_M
AL47	GPI_5	AM36	RFU_3	AN23	VSS	AP12	VSS
AL49	GPI_6	AM38	VSS	AN25	PCIERCA1_TX6_M	AP14	VSS
AL51	REF_TESTCLK	AM40	VSS	AN27	TRIGOUT0	AP16	PCIERCA1_RX7_M
AL53	VSS	AM42	VSS	AN29	TRIGOUT2	AP18	VSS
AL55	VSS	AM44	GPI_0	AN31	GPIO_19	AP20	VSS
AL57	JTAG_PM_TDI	AM46	GPI_3	AN33	RFU_4	AP22	PCIERCA1_TX7_M
AL59	VSS	AM48	VSS	AN35	VSS	AP24	VSS
AL61	VSS	AM50	SOC_PWRGD	AN37	JTAG_IPP_TDO	AP26	VSS
AL63	VSS	AM52	PCP_PWRCTL	AN39	OVERTEMP_N	AP28	TRIGOUT1
AL65	#	AM54	TEST_TMM_ENABLE	AN41	DDR4_PLL_TESTOUT_P	AP30	TRIGOUT3
AL67	VSS	AM56	GPIO_FAULT	AN43	DDR7_PLL_TESTOUT_N	AP32	GPIO_20
AL69	VSS	AM58	VSS	AN45	GPI_1	AP34	RFU_6
AL71	VSS	AM60	VSS	AN47	GPI_4	AP36	RFU_5
AL73	VSS	AM62	VSS	AN49	GPI_7	AP38	JTAG_IPP_TCK
AL75	VSS	AM64	VSS	AN51	MPA_TEST_RSTN	AP40	HIGHTEMP_N
AL77	VSS	AM66	VSS	AN53	PCP_PWRGD	AP42	DDR4_PLL_TESTOUT_N
AL79	VSS	AM68	VSS	AN55	VSS	AP44	VSS
AL81	VSS	AM70	VSS	AN57	VSS	AP46	VSS
AL83	VSS	AM72	VSS	AN59	PCIERCA3_RX15_M	AP48	VSS
AM2	VSS	AM74	VSS	AN61	PCIERCA3_RX14_M	AP50	VSS
AM4	VSS	AM76	VSS	AN63	VSS	AP52	VSS
AM6	PCIERCA1_RX15_P	AM78	VSS	AN65	PCIERCA3_TX15_M	AP54	VSS
AM8	VSS	AM80	VSS	AN67	PCIERCA3_TX14_M	AP56	VSS
AM10	VSS	AM82	VSS	AN69	PCIERCB3A_RX7_M	AP58	VSS
AM12	PCIERCA1_TX15_P	AM84	VSS	AN71	PCIERCB3A_RX6_M	AP60	PCIERCA3_RX15_P
AM14	VSS	AN1	VSS	AN73	PCIERCB3A_TX7_M	AP62	PCIERCA3_RX14_P
AM16	VSS	AN3	PCIERCA1_RX14_P	AN75	PCIERCB3A_TX6_M	AP64	PCIERCA3_TX15_P
AM18	PCIERCA1_RX6_P	AN5	VSS	AN77	PCIERCB3B_RX7_M	AP66	PCIERCA3_TX14_P
AM20	VSS	AN7	PCIERCA1_RX15_M	AN79	PCIERCB3B_RX6_M	AP68	VSS
AM22	VSS	AN9	PCIERCA1_TX14_P	AN81	PCIERCB3B_TX7_M	AP70	PCIERCB3A_RX7_P
AM24	PCIERCA1_TX6_P	AN11	VSS	AN83	PCIERCB3B_TX6_M	AP72	PCIERCB3A_RX6_P
AM26	VSS	AN13	PCIERCA1_TX15_M	AP2	VSS	AP74	PCIERCB3A_TX7_P
AM28	VSS	AN15	PCIERCA1_RX7_P	AP4	PCIERCA1_RX14_M	AP76	PCIERCB3A_TX6_P

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 11 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
AP78	PCIERCB3B_RX7_P	AR65	VSS	AT54	RFU_D2D	AU41	DDR5_PLL_TESTOUT_N
AP80	PCIERCB3B_RX6_P	AR67	VSS	AT56	RFU_D2D	AU43	VSS
AP82	PCIERCB3B_TX7_P	AR69	VSS	AT58	VSS	AU45	VSS
AP84	PCIERCB3B_TX6_P	AR71	VSS	AT60	VSS	AU47	VSS
AR1	VSS	AR73	VSS	AT62	VSS	AU49	VSS
AR3	VSS	AR75	VSS	AT64	VSS	AU51	VSS
AR5	VSS	AR77	VSS	AT66	VSS	AU53	VSS
AR7	VSS	AR79	VSS	AT68	VSS	AU55	VSS
AR9	VSS	AR81	VSS	AT70	VSS	AU57	RFU_D2D
AR11	VSS	AR83	VSS	AT72	VSS	AU59	PCIERCA3_RX13_M
AR13	VSS	AT2	VSS	AT74	VSS	AU61	PCIERCA3_RX12_M
AR15	VSS	AT4	VSS	AT76	VSS	AU63	VSS
AR17	VSS	AT6	PCIERCA1_RX13_P	AT78	VSS	AU65	PCIERCA3_TX13_M
AR19	VSS	AT8	VSS	AT80	VSS	AU67	PCIERCA3_TX12_M
AR21	VSS	AT10	VSS	AT82	VSS	AU69	PCIERCB3A_RX5_M
AR23	VSS	AT12	PCIERCA1_TX13_P	AT84	VSS	AU71	PCIERCB3A_RX4_M
AR25	VSS	AT14	VSS	AU1	VSS	AU73	PCIERCB3A_TX5_M
AR27	VSS	AT16	VSS	AU3	PCIERCA1_RX12_P	AU75	PCIERCB3A_TX4_M
AR29	VSS	AT18	PCIERCA1_RX4_P	AU5	VSS	AU77	PCIERCB3B_RX5_M
AR31	GPIO_22	AT20	VSS	AU7	PCIERCA1_RX13_M	AU79	PCIERCB3B_RX4_M
AR33	VSS	AT22	VSS	AU9	PCIERCA1_TX12_P	AU81	PCIERCB3B_TX5_M
AR35	VSS	AT24	PCIERCA1_TX4_P	AU11	VSS	AU83	PCIERCB3B_TX4_M
AR37	VSS	AT26	VSS	AU13	PCIERCA1_TX13_M	AV2	VSS
AR39	VSS	AT28	TRIGIN0	AU15	PCIERCA1_RX5_P	AV4	PCIERCA1_RX12_M
AR41	VSS	AT30	TRIGIN2	AU17	VSS	AV6	VSS
AR43	VDDQ_DDR4567	AT32	GPIO_21	AU19	PCIERCA1_RX4_M	AV8	VSS
AR45	RFU_D2D	AT34	RFU_10	AU21	PCIERCA1_TX5_P	AV10	PCIERCA1_TX12_M
AR47	RFU_D2D	AT36	RFU_7	AU23	VSS	AV12	VSS
AR49	RFU_D2D	AT38	RFU_12	AU25	PCIERCA1_TX4_M	AV14	VSS
AR51	RFU_D2D	AT40	RFU_14	AU27	TRIGIN1	AV16	PCIERCA1_RX5_M
AR53	RFU_D2D	AT42	DDR5_PLL_TESTOUT_P	AU29	TRIGIN3	AV18	VSS
AR55	RFU_D2D	AT44	RFU_D2D	AU31	GPIO_23	AV20	VSS
AR57	RFU_D2D	AT46	RFU_D2D	AU33	RFU_8	AV22	PCIERCA1_TX5_M
AR59	VSS	AT48	RFU_D2D	AU35	RFU_9	AV24	VSS
AR61	VSS	AT50	RFU_D2D	AU37	RFU_11	AV26	VSS
AR63	VSS	AT52	RFU_D2D	AU39	RFU_13	AV28	VSS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 12 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
AV30	VSS	AW17	VSS	AY6	PCIERCA1_RX11_P	AY78	VSS
AV32	VSS	AW19	VSS	AY8	VSS	AY80	VSS
AV34	VSS	AW21	VSS	AY10	VSS	AY82	VSS
AV36	VSS	AW23	VSS	AY12	PCIERCA1_TX11_P	AY84	VSS
AV38	VSS	AW25	VSS	AY14	VSS	BA1	VSS
AV40	VSS	AW27	VDDH_RCA1	AY16	VSS	BA3	PCIERCA1_RX10_P
AV42	VSS	AW29	VDDH_RCA1	AY18	PCIERCA1_RX2_P	BA5	VSS
AV44	VSS	AW31	RFU_35	AY20	VSS	BA7	PCIERCA1_RX11_M
AV46	VSS	AW33	VDD18_PCP_AVDD	AY22	VSS	BA9	PCIERCA1_TX10_P
AV48	VSS	AW35	VDD18_PCP_AVDD	AY24	PCIERCA1_TX2_P	BA11	VSS
AV50	VSS	AW37	VDD18_PCP_AVDD	AY26	VSS	BA13	PCIERCA1_TX11_M
AV52	VSS	AW39	VDD33_SOC	AY28	VDDH_RCA1	BA15	PCIERCA1_RX3_P
AV54	VSS	AW41	VDD33_SOC	AY30	RFU_34	BA17	VSS
AV56	RFU_D2D	AW43	RFU_D2D	AY32	VDD18_PCP_AVDD	BA19	PCIERCA1_RX2_M
AV58	VSS	AW45	RFU_D2D	AY34	VDD18_PCP_AVDD	BA21	PCIERCA1_TX3_P
AV60	PCIERCA3_RX13_P	AW47	RFU_D2D	AY36	VDD18_PCP_AVDD	BA23	VSS
AV62	PCIERCA3_RX12_P	AW49	RFU_D2D	AY38	VDD33_SOC	BA25	PCIERCA1_TX2_M
AV64	PCIERCA3_TX13_P	AW51	RFU_D2D	AY40	VDD33_SOC	BA27	VSS
AV66	PCIERCA3_TX12_P	AW53	RFU_D2D	AY42	VDD33_SOC	BA29	VSS
AV68	VSS	AW55	RFU_D2D	AY44	RFU_D2D	BA31	VSS
AV70	PCIERCB3A_RX5_P	AW57	RFU_D2D	AY46	RFU_D2D	BA33	VSS
AV72	PCIERCB3A_RX4_P	AW59	VSS	AY48	RFU_D2D	BA35	VSS
AV74	PCIERCB3A_TX5_P	AW61	VSS	AY50	RFU_D2D	BA37	VSS
AV76	PCIERCB3A_TX4_P	AW63	VSS	AY52	RFU_D2D	BA39	VSS
AV78	PCIERCB3B_RX5_P	AW65	VSS	AY54	RFU_D2D	BA41	VSS
AV80	PCIERCB3B_RX4_P	AW67	VSS	AY56	RFU_D2D	BA43	VSS
AV82	PCIERCB3B_TX5_P	AW69	VSS	AY58	VSS	BA45	VSS
AV84	PCIERCB3B_TX4_P	AW71	VSS	AY60	VSS	BA47	VSS
AW1	VSS	AW73	VSS	AY62	VSS	BA49	VSS
AW3	VSS	AW75	VSS	AY64	VSS	BA51	VSS
AW5	VSS	AW77	VSS	AY66	VSS	BA53	VSS
AW7	VSS	AW79	VSS	AY68	VSS	BA55	VSS
AW9	VSS	AW81	VSS	AY70	VSS	BA57	RFU_D2D
AW11	VSS	AW83	VSS	AY72	VSS	BA59	PCIERCA3_RX11_M
AW13	VSS	AY2	VSS	AY74	VSS	BA61	PCIERCA3_RX10_M
AW15	VSS	AY4	VSS	AY76	VSS	BA63	VSS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 13 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
BA65	PCIERCA3_TX11_M	BB54	VSS	BC41	VDDC_PCP	BD30	VDDC_RCA1
BA67	PCIERCA3_TX10_M	BB56	VSS	BC43	VDDC_PCP	BD32	VDDC_PCP
BA69	PCIERCB3A_RX3_M	BB58	VSS	BC45	VDDC_PCP	BD34	VDDC_PCP
BA71	PCIERCB3A_RX2_M	BB60	PCIERCA3_RX11_P	BC47	VDDC_PCP	BD36	VDDC_PCP
BA73	PCIERCB3A_TX3_M	BB62	PCIERCA3_RX10_P	BC49	VDDC_PCP	BD38	VDDC_PCP
BA75	PCIERCB3A_TX2_M	BB64	PCIERCA3_TX11_P	BC51	VDDC_PCP	BD40	VDDC_PCP
BA77	PCIERCB3B_RX3_M	BB66	PCIERCA3_TX10_P	BC53	VDDC_PCP	BD42	VDDC_PCP
BA79	PCIERCB3B_RX2_M	BB68	VSS	BC55	VDDC_SOC	BD44	VDDC_PCP
BA81	PCIERCB3B_TX3_M	BB70	PCIERCB3A_RX3_P	BC57	VDDC_SOC	BD46	VDDC_PCP
BA83	PCIERCB3B_TX2_M	BB72	PCIERCB3A_RX2_P	BC59	VSS	BD48	VDDC_PCP
BB2	VSS	BB74	PCIERCB3A_TX3_P	BC61	VSS	BD50	VDDC_PCP
BB4	PCIERCA1_RX10_M	BB76	PCIERCB3A_TX2_P	BC63	VSS	BD52	VDDC_PCP
BB6	VSS	BB78	PCIERCB3B_RX3_P	BC65	VSS	BD54	VDDC_SOC
BB8	VSS	BB80	PCIERCB3B_RX2_P	BC67	VSS	BD56	VDDC_SOC
BB10	PCIERCA1_TX10_M	BB82	PCIERCB3B_TX3_P	BC69	VSS	BD58	VSS
BB12	VSS	BB84	PCIERCB3B_TX2_P	BC71	VSS	BD60	VSS
BB14	VSS	BC1	VSS	BC73	VSS	BD62	VSS
BB16	PCIERCA1_RX3_M	BC3	VSS	BC75	VSS	BD64	VSS
BB18	VSS	BC5	VSS	BC77	VSS	BD66	VSS
BB20	VSS	BC7	VSS	BC79	VSS	BD68	VSS
BB22	PCIERCA1_TX3_M	BC9	VSS	BC81	VSS	BD70	VSS
BB24	VSS	BC11	VSS	BC83	VSS	BD72	VSS
BB26	VSS	BC13	VSS	BD2	VSS	BD74	VSS
BB28	VSS	BC15	VSS	BD4	VSS	BD76	VSS
BB30	VSS	BC17	VSS	BD6	PCIERCA1_RX9_P	BD78	VSS
BB32	VSS	BC19	VSS	BD8	VSS	BD80	VSS
BB34	VSS	BC21	VSS	BD10	VSS	BD82	VSS
BB36	VSS	BC23	VSS	BD12	PCIERCA1_TX9_P	BD84	VSS
BB38	VSS	BC25	VSS	BD14	VSS	BE1	VSS
BB40	VSS	BC27	VDDC_RCA1	BD16	VSS	BE3	PCIERCA1_RX8_P
BB42	VSS	BC29	VDDC_RCA1	BD18	PCIERCA1_RX0_P	BE5	VSS
BB44	VSS	BC31	VDDC_RCA1	BD20	VSS	BE7	PCIERCA1_RX9_M
BB46	VSS	BC33	VDDC_PCP	BD22	VSS	BE9	PCIERCA1_TX8_P
BB48	VSS	BC35	VDDC_PCP	BD24	PCIERCA1_TX0_P	BE11	VSS
BB50	VSS	BC37	VDDC_PCP	BD26	VSS	BE13	PCIERCA1_TX9_M
BB52	VSS	BC39	VDDC_PCP	BD28	VDDC_RCA1	BE15	PCIERCA1_RX1_P

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 14 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
BE17	VSS	BF6	VSS	BF78	PCIERCB3B_RX1_P	BG65	VSS
BE19	PCIERCA1_RX0_M	BF8	VSS	BF80	PCIERCB3B_RX0_P	BG67	VSS
BE21	PCIERCA1_TX1_P	BF10	PCIERCA1_TX8_M	BF82	PCIERCB3B_TX1_P	BG69	VSS
BE23	VSS	BF12	VSS	BF84	PCIERCB3B_TX0_P	BG71	VSS
BE25	PCIERCA1_TX0_M	BF14	VSS	BG1	VDDC_PCP	BG73	VSS
BE27	VSS	BF16	PCIERCA1_RX1_M	BG3	VSS	BG75	VSS
BE29	VSS	BF18	VSS	BG5	VSS	BG77	VSS
BE31	VSS	BF20	VSS	BG7	VSS	BG79	VSS
BE33	VSS	BF22	PCIERCA1_TX1_M	BG9	VSS	BG81	VSS
BE35	VSS	BF24	VSS	BG11	VSS	BG83	VSS
BE37	VSS	BF26	VSS	BG13	VSS	BH2	VSS
BE39	VSS	BF28	VSS	BG15	VSS	BH4	VSS
BE41	VSS	BF30	VSS	BG17	VSS	BH6	VDDC_PCP
BE43	VSS	BF32	VSS	BG19	VSS	BH8	VSS
BE45	VSS	BF34	VSS	BG21	VSS	BH10	VSS
BE47	VSS	BF36	VSS	BG23	VSS	BH12	VDDC_PCP
BE49	VSS	BF38	VSS	BG25	VSS	BH14	VSS
BE51	VSS	BF40	VSS	BG27	VDDC_PCP	BH16	VSS
BE53	VSS	BF42	VSS	BG29	VDDC_PCP	BH18	VDDC_PCP
BE55	VSS	BF44	VSS	BG31	VDDC_PCP	BH20	VSS
BE57	VDDC_SOC	BF46	VSS	BG33	VDDC_PCP	BH22	VSS
BE59	PCIERCA3_RX9_M	BF48	VSS	BG35	VDDC_PCP	BH24	VDDC_PCP
BE61	PCIERCA3_RX8_M	BF50	VSS	BG37	VDDC_PCP	BH26	VSS
BE63	VSS	BF52	VSS	BG39	VDDC_PCP	BH28	VDDC_PCP
BE65	PCIERCA3_TX9_M	BF54	VSS	BG41	VDDC_PCP	BH30	VDDC_PCP
BE67	PCIERCA3_TX8_M	BF56	VDDC_SOC	BG43	VDDC_PCP_SENSE_P	BH32	VDDC_PCP
BE69	PCIERCB3A_RX1_M	BF58	VSS	BG45	VDDC_PCP	BH34	VDDC_PCP
BE71	PCIERCB3A_RX0_M	BF60	PCIERCA3_RX9_P	BG47	VDDC_PCP	BH36	VDDC_PCP
BE73	PCIERCB3A_TX1_M	BF62	PCIERCA3_RX8_P	BG49	VDDC_PCP	BH38	VDDC_PCP
BE75	PCIERCB3A_TX0_M	BF64	PCIERCA3_TX9_P	BG51	VDDC_RCA3	BH40	VDDC_PCP
BE77	PCIERCB3B_RX1_M	BF66	PCIERCA3_TX8_P	BG53	VDDH_RCA3	BH42	VDDC_PCP
BE79	PCIERCB3B_RX0_M	BF68	VSS	BG55	VSS	BH44	VDDC_PCP_SENSE_N
BE81	PCIERCB3B_TX1_M	BF70	PCIERCB3A_RX1_P	BG57	VDDC_SOC	BH46	VDDC_PCP
BE83	PCIERCB3B_TX0_M	BF72	PCIERCB3A_RX0_P	BG59	VSS	BH48	VDDC_PCP
BF2	VSS	BF74	PCIERCB3A_TX1_P	BG61	VSS	BH50	VDDC_RCA3
BF4	PCIERCA1_RX8_M	BF76	PCIERCB3A_TX0_P	BG63	VSS	BH52	VDDC_RCA3

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 15 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
BH54	VDDH_RCA3	BJ41	VSS	BK30	VDDC_PCP	BL17	VDDC_PCP
BH56	VDDC_SOC	BJ43	VSS	BK32	VDDC_PCP	BL19	VDDC_PCP
BH58	VSS	BJ45	VSS	BK34	VDDC_PCP	BL21	VDDC_PCP
BH60	VSS	BJ47	VSS	BK36	VDDC_PCP	BL23	VDDC_PCP
BH62	VSS	BJ49	VSS	BK38	VDDC_PCP	BL25	VDDC_PCP
BH64	VSS	BJ51	VSS	BK40	VDDC_PCP	BL27	VDDC_PCP
BH66	VSS	BJ53	VSS	BK42	VDDC_PCP	BL29	VDDC_PCP
BH68	VSS	BJ55	VSS	BK44	VDDC_PCP	BL57	VDDC_SOC
BH70	VSS	BJ57	VDDC_SOC	BK46	VDDC_PCP	BL59	VSS
BH72	VSS	BJ59	PCIERCA3_RX7_M	BK48	VDDC_PCP	BL61	VSS
BH74	VSS	BJ61	PCIERCA3_RX6_M	BK50	VDDC_RCA3	BL63	VSS
BH76	VSS	BJ63	VSS	BK52	VDDC_RCA3	BL65	VSS
BH78	VSS	BJ65	PCIERCA3_TX7_M	BK54	VDDH_RCA3	BL67	VSS
BH80	VSS	BJ67	PCIERCA3_TX6_M	BK56	VDDC_SOC	BL69	VSS
BH82	VSS	BJ69	PCIERCB2B_RX7_M	BK58	VSS	BL71	VSS
BH84	VSS	BJ71	PCIERCB2B_RX6_M	BK60	PCIERCA3_RX7_P	BL73	VSS
BJ1	VDDC_PCP	BJ73	PCIERCB2B_TX7_M	BK62	PCIERCA3_RX6_P	BL75	VSS
BJ3	VDDC_PCP	BJ75	PCIERCB2B_TX6_M	BK64	PCIERCA3_TX7_P	BL77	VSS
BJ5	VDDC_PCP	BJ77	PCIERCB2A_RX7_M	BK66	PCIERCA3_TX6_P	BL79	VSS
BJ7	VDDC_PCP	BJ79	PCIERCB2A_RX6_M	BK68	VSS	BL81	VSS
BJ9	VDDC_PCP	BJ81	PCIERCB2A_TX7_M	BK70	PCIERCB2B_RX7_P	BL83	VSS
BJ11	VDDC_PCP	BJ83	PCIERCB2A_TX6_M	BK72	PCIERCB2B_RX6_P	BM2	VSS
BJ13	VDDC_PCP	BK2	VDDC_PCP	BK74	PCIERCB2B_TX7_P	BM4	VSS
BJ15	VDDC_PCP	BK4	VDDC_PCP	BK76	PCIERCB2B_TX6_P	BM6	VSS
BJ17	VDDC_PCP	BK6	VDDC_PCP	BK78	PCIERCB2A_RX7_P	BM8	VSS
BJ19	VDDC_PCP	BK8	VDDC_PCP	BK80	PCIERCB2A_RX6_P	BM10	VSS
BJ21	VDDC_PCP	BK10	VDDC_PCP	BK82	PCIERCB2A_TX7_P	BM12	VSS
BJ23	VDDC_PCP	BK12	VDDC_PCP	BK84	PCIERCB2A_TX6_P	BM14	VSS
BJ25	VDDC_PCP	BK14	VDDC_PCP	BL1	VDDC_PCP	BM16	VSS
BJ27	VSS	BK16	VDDC_PCP	BL3	VDDC_PCP	BM18	VSS
BJ29	VSS	BK18	VDDC_PCP	BL5	VDDC_PCP	BM20	VSS
BJ31	VSS	BK20	VDDC_PCP	BL7	VDDC_PCP	BM22	VSS
BJ33	VSS	BK22	VDDC_PCP	BL9	VDDC_PCP	BM24	VSS
BJ35	VSS	BK24	VDDC_PCP	BL11	VDDC_PCP	BM26	VSS
BJ37	VSS	BK26	VDDC_PCP	BL13	VDDC_PCP	BM28	VSS
BJ39	VSS	BK28	VDDC_PCP	BL15	VDDC_PCP	BM56	VDDC_SOC

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 16 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
BM58	VSS	BN71	PCIERCB2B_RX4_M	BR1	VDDC_PCP	BT16	VSS
BM60	VSS	BN73	PCIERCB2B_TX5_M	BR3	VDDC_PCP	BT18	VSS
BM62	VSS	BN75	PCIERCB2B_TX4_M	BR5	VDDC_PCP	BT20	VSS
BM64	VSS	BN77	PCIERCB2A_RX5_M	BR7	VDDC_PCP	BT22	VSS
BM66	VSS	BN79	PCIERCB2A_RX4_M	BR9	VDDC_PCP	BT24	VSS
BM68	VSS	BN81	PCIERCB2A_TX5_M	BR11	VDDC_PCP	BT26	VSS
BM70	VSS	BN83	PCIERCB2A_TX4_M	BR13	VDDC_PCP	BT28	VSS
BM72	VSS	BP2	VDDC_PCP	BR15	VDDC_PCP	BT56	VDDH_RCB3
BM74	VSS	BP4	VDDC_PCP	BR17	VDDC_PCP	BT58	VSS
BM76	VSS	BP6	VDDC_PCP	BR19	VDDC_PCP	BT60	VSS
BM78	VSS	BP8	VDDC_PCP	BR21	VDDC_PCP	BT62	VSS
BM80	VSS	BP10	VDDC_PCP	BR23	VDDC_PCP	BT64	VSS
BM82	VSS	BP12	VDDC_PCP	BR25	VDDC_PCP	BT66	VSS
BM84	VSS	BP14	VDDC_PCP	BR27	VDDC_PCP	BT68	VSS
BN1	VSS	BP16	VDDC_PCP	BR29	VDDC_PCP	BT70	VSS
BN3	VSS	BP18	VDDC_PCP	BR57	VDDH_RCB3	BT72	VSS
BN5	VSS	BP20	VDDC_PCP	BR59	VSS	BT74	VSS
BN7	VSS	BP22	VDDC_PCP	BR61	VSS	BT76	VSS
BN9	VSS	BP24	VDDC_PCP	BR63	VSS	BT78	VSS
BN11	VSS	BP26	VDDC_PCP	BR65	VSS	BT80	VSS
BN13	VSS	BP28	VDDC_PCP	BR67	VSS	BT82	VSS
BN15	VSS	BP56	VDDC_SOC	BR69	VSS	BT84	VSS
BN17	VSS	BP58	VSS	BR71	VSS	BU1	VSS
BN19	VSS	BP60	PCIERCA3_RX5_P	BR73	VSS	BU3	VSS
BN21	VSS	BP62	PCIERCA3_RX4_P	BR75	VSS	BU5	VSS
BN23	VSS	BP64	PCIERCA3_TX5_P	BR77	VSS	BU7	VSS
BN25	VSS	BP66	PCIERCA3_TX4_P	BR79	VSS	BU9	VSS
BN27	VSS	BP68	VSS	BR81	VSS	BU11	VSS
BN29	VSS	BP70	PCIERCB2B_RX5_P	BR83	VSS	BU13	VSS
BN57	VDDC_SOC	BP72	PCIERCB2B_RX4_P	BT2	VSS	BU15	VSS
BN59	PCIERCA3_RX5_M	BP74	PCIERCB2B_TX5_P	BT4	VSS	BU17	VSS
BN61	PCIERCA3_RX4_M	BP76	PCIERCB2B_TX4_P	BT6	VSS	BU19	VSS
BN63	VSS	BP78	PCIERCB2A_RX5_P	BT8	VSS	BU21	VSS
BN65	PCIERCA3_TX5_M	BP80	PCIERCB2A_RX4_P	BT10	VSS	BU23	VSS
BN67	PCIERCA3_TX4_M	BP82	PCIERCB2A_TX5_P	BT12	VSS	BU25	VSS
BN69	PCIERCB2B_RX5_M	BP84	PCIERCB2A_TX4_P	BT14	VSS	BU27	VSS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 17 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
BU29	VSS	BV70	PCIERCB2B_RX3_P	BW83	VSS	CA13	VSS
BU57	VDDH_RCB2	BV72	PCIERCB2B_RX2_P	BY2	VSS	CA15	VSS
BU59	PCIERCA3_RX3_M	BV74	PCIERCB2B_TX3_P	BY4	VSS	CA17	VSS
BU61	PCIERCA3_RX2_M	BV76	PCIERCB2B_TX2_P	BY6	VSS	CA19	VSS
BU63	VSS	BV78	PCIERCB2A_RX3_P	BY8	VSS	CA21	VSS
BU65	PCIERCA3_TX3_M	BV80	PCIERCB2A_RX2_P	BY10	VSS	CA23	VSS
BU67	PCIERCA3_TX2_M	BV82	PCIERCB2A_TX3_P	BY12	VSS	CA25	VSS
BU69	PCIERCB2B_RX3_M	BV84	PCIERCB2A_TX2_P	BY14	VSS	CA27	VSS
BU71	PCIERCB2B_RX2_M	BW1	VDDC_PCP	BY16	VSS	CA29	VSS
BU73	PCIERCB2B_TX3_M	BW3	VDDC_PCP	BY18	VSS	CA57	VDDC_RCB2
BU75	PCIERCB2B_TX2_M	BW5	VDDC_PCP	BY20	VSS	CA59	PCIERCA3_RX1_M
BU77	PCIERCB2A_RX3_M	BW7	VDDC_PCP	BY22	VSS	CA61	PCIERCA3_RX0_M
BU79	PCIERCB2A_RX2_M	BW9	VDDC_PCP	BY24	VSS	CA63	VSS
BU81	PCIERCB2A_TX3_M	BW11	VDDC_PCP	BY26	VSS	CA65	PCIERCA3_TX1_M
BU83	PCIERCB2A_TX2_M	BW13	VDDC_PCP	BY28	VSS	CA67	PCIERCA3_TX0_M
BV2	VDDC_PCP	BW15	VDDC_PCP	BY56	VDDC_RCB3	CA69	PCIERCB2B_RX1_M
BV4	VDDC_PCP	BW17	VDDC_PCP	BY58	VSS	CA71	PCIERCB2B_RX0_M
BV6	VDDC_PCP	BW19	VDDC_PCP	BY60	VSS	CA73	PCIERCB2B_TX1_M
BV8	VDDC_PCP	BW21	VDDC_PCP	BY62	VSS	CA75	PCIERCB2B_TX0_M
BV10	VDDC_PCP	BW23	VDDC_PCP	BY64	VSS	CA77	PCIERCB2A_RX1_M
BV12	VDDC_PCP	BW25	VDDC_PCP	BY66	VSS	CA79	PCIERCB2A_RX0_M
BV14	VDDC_PCP	BW27	VDDC_PCP	BY68	VSS	CA81	PCIERCB2A_TX1_M
BV16	VDDC_PCP	BW29	VDDC_PCP	BY70	VSS	CA83	PCIERCB2A_TX0_M
BV18	VDDC_PCP	BW57	VDDC_RCB3	BY72	VSS	CB2	VDDC_PCP
BV20	VDDC_PCP	BW59	VSS	BY74	VSS	CB4	VDDC_PCP
BV22	VDDC_PCP	BW61	VSS	BY76	VSS	CB6	VDDC_PCP
BV24	VDDC_PCP	BW63	VSS	BY78	VSS	CB8	VDDC_PCP
BV26	VDDC_PCP	BW65	VSS	BY80	VSS	CB10	VDDC_PCP
BV28	VDDC_PCP	BW67	VSS	BY82	VSS	CB12	VDDC_PCP
BV56	VDDH_RCB2	BW69	VSS	BY84	VSS	CB14	VDDC_PCP
BV58	VSS	BW71	VSS	CA1	VSS	CB16	VDDC_PCP
BV60	PCIERCA3_RX3_P	BW73	VSS	CA3	VSS	CB18	VDDC_PCP
BV62	PCIERCA3_RX2_P	BW75	VSS	CA5	VSS	CB20	VDDC_PCP
BV64	PCIERCA3_TX3_P	BW77	VSS	CA7	VSS	CB22	VDDC_PCP
BV66	PCIERCA3_TX2_P	BW79	VSS	CA9	VSS	CB24	VDDC_PCP
BV68	VSS	BW81	VSS	CA11	VSS	CB26	VDDC_PCP

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 18 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
CB28	VDDC_PCP	CC67	VSS	CD81	VSS	CF11	VSS
CB56	VDDC_RCB2	CC69	VSS	CD83	VSS	CF13	VSS
CB58	VSS	CC71	VSS	CE2	VDDC_PCP	CF15	VSS
CB60	PCIERCA3_RX1_P	CC73	VSS	CE4	VDDC_PCP	CF17	VSS
CB62	PCIERCA3_RX0_P	CC75	VSS	CE6	VDDC_PCP	CF19	VSS
CB64	PCIERCA3_TX1_P	CC77	VSS	CE8	VDDC_PCP	CF21	VSS
CB66	PCIERCA3_TX0_P	CC79	VSS	CE10	VDDC_PCP	CF23	VSS
CB68	VSS	CC81	VSS	CE12	VDDC_PCP	CF25	VSS
CB70	PCIERCB2B_RX1_P	CC83	VSS	CE14	VDDC_PCP	CF27	VSS
CB72	PCIERCB2B_RX0_P	CD1	VDDC_PCP	CE16	VDDC_PCP	CF29	VSS
CB74	PCIERCB2B_TX1_P	CD3	VDDC_PCP	CE18	VDDC_PCP	CF57	VDDC_RCB1
CB76	PCIERCB2B_TX0_P	CD5	VDDC_PCP	CE20	VDDC_PCP	CF59	PCIERCA2_RX1_M
CB78	PCIERCB2A_RX1_P	CD7	VDDC_PCP	CE22	VDDC_PCP	CF61	PCIERCA2_RX0_M
CB80	PCIERCB2A_RX0_P	CD9	VDDC_PCP	CE24	VDDC_PCP	CF63	VSS
CB82	PCIERCB2A_TX1_P	CD11	VDDC_PCP	CE26	VDDC_PCP	CF65	PCIERCA2_TX1_M
CB84	PCIERCB2A_TX0_P	CD13	VDDC_PCP	CE28	VDDC_PCP	CF67	PCIERCA2_TX0_M
CC1	VDDC_PCP	CD15	VDDC_PCP	CE56	VDDC_RCB1	CF69	PCIERCB1B_RX1_M
CC3	VDDC_PCP	CD17	VDDC_PCP	CE58	VSS	CF71	PCIERCB1B_RX0_M
CC5	VDDC_PCP	CD19	VDDC_PCP	CE60	PCIERCA2_RX1_P	CF73	PCIERCB1B_TX1_M
CC7	VDDC_PCP	CD21	VDDC_PCP	CE62	PCIERCA2_RX0_P	CF75	PCIERCB1B_TX0_M
CC9	VDDC_PCP	CD23	VDDC_PCP	CE64	PCIERCA2_TX1_P	CF77	PCIERCB1A_RX1_M
CC11	VDDC_PCP	CD25	VDDC_PCP	CE66	PCIERCA2_TX0_P	CF79	PCIERCB1A_RX0_M
CC13	VDDC_PCP	CD27	VDDC_PCP	CE68	VSS	CF81	PCIERCB1A_TX1_M
CC15	VDDC_PCP	CD29	VDDC_PCP	CE70	PCIERCB1B_RX1_P	CF83	PCIERCB1A_TX0_M
CC17	VDDC_PCP	CD57	VDDC_SOC_SENSE_N	CE72	PCIERCB1B_RX0_P	CG2	VSS
CC19	VDDC_PCP	CD59	VSS	CE74	PCIERCB1B_TX1_P	CG4	VSS
CC21	VDDC_PCP	CD61	VSS	CE76	PCIERCB1B_TX0_P	CG6	VSS
CC23	VDDC_PCP	CD63	VSS	CE78	PCIERCB1A_RX1_P	CG8	VSS
CC25	VDDC_PCP	CD65	VSS	CE80	PCIERCB1A_RX0_P	CG10	VSS
CC27	VDDC_PCP	CD67	VSS	CE82	PCIERCB1A_TX1_P	CG12	VSS
CC29	VDDC_PCP	CD69	VSS	CE84	PCIERCB1A_TX0_P	CG14	VSS
CC57	VDDC_SOC_SENSE_P	CD71	VSS	CF1	VSS	CG16	VSS
CC59	VSS	CD73	VSS	CF3	VSS	CG18	VSS
CC61	VSS	CD75	VSS	CF5	VSS	CG20	VSS
CC63	VSS	CD77	VSS	CF7	VSS	CG22	VSS
CC65	VSS	CD79	VSS	CF9	VSS	CG24	VSS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 19 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
CG26	VSS	CH65	VSS	CJ80	PCIERCB1A_RX2_P	CL10	VSS
CG28	VSS	CH67	VSS	CJ82	PCIERCB1A_TX3_P	CL12	VSS
CG56	VDDC_RCB0	CH69	VSS	CJ84	PCIERCB1A_TX2_P	CL14	VSS
CG58	VSS	CH71	VSS	CK1	VSS	CL16	VSS
CG60	VSS	CH73	VSS	CK3	VSS	CL18	VSS
CG62	VSS	CH75	VSS	CK5	VSS	CL20	VSS
CG64	VSS	CH77	VSS	CK7	VSS	CL22	VSS
CG66	VSS	CH79	VSS	CK9	VSS	CL24	VSS
CG68	VSS	CH81	VSS	CK11	VSS	CL26	VSS
CG70	VSS	CH83	VSS	CK13	VSS	CL28	VSS
CG72	VSS	CJ2	VDDC_PCP	CK15	VSS	CL56	VDDH_RCB0
CG74	VSS	CJ4	VDDC_PCP	CK17	VSS	CL58	VSS
CG76	VSS	CJ6	VDDC_PCP	CK19	VSS	CL60	VSS
CG78	VSS	CJ8	VDDC_PCP	CK21	VSS	CL62	VSS
CG80	VSS	CJ10	VDDC_PCP	CK23	VSS	CL64	VSS
CG82	VSS	CJ12	VDDC_PCP	CK25	VSS	CL66	VSS
CG84	VSS	CJ14	VDDC_PCP	CK27	VSS	CL68	VSS
CH1	VDDC_PCP	CJ16	VDDC_PCP	CK29	VSS	CL70	VSS
CH3	VDDC_PCP	CJ18	VDDC_PCP	CK57	VDDH_RCB1	CL72	VSS
CH5	VDDC_PCP	CJ20	VDDC_PCP	CK59	PCIERCA2_RX3_M	CL74	VSS
CH7	VDDC_PCP	CJ22	VDDC_PCP	CK61	PCIERCA2_RX2_M	CL76	VSS
CH9	VDDC_PCP	CJ24	VDDC_PCP	CK63	VSS	CL78	VSS
CH11	VDDC_PCP	CJ26	VDDC_PCP	CK65	PCIERCA2_TX3_M	CL80	VSS
CH13	VDDC_PCP	CJ28	VDDC_PCP	CK67	PCIERCA2_TX2_M	CL82	VSS
CH15	VDDC_PCP	CJ56	VDDH_RCB1	CK69	PCIERCB1B_RX3_M	CL84	VSS
CH17	VDDC_PCP	CJ58	VSS	CK71	PCIERCB1B_RX2_M	CM1	VDDC_PCP
CH19	VDDC_PCP	CJ60	PCIERCA2_RX3_P	CK73	PCIERCB1B_TX3_M	CM3	VDDC_PCP
CH21	VDDC_PCP	CJ62	PCIERCA2_RX2_P	CK75	PCIERCB1B_TX2_M	CM5	VDDC_PCP
CH23	VDDC_PCP	CJ64	PCIERCA2_TX3_P	CK77	PCIERCB1A_RX3_M	CM7	VDDC_PCP
CH25	VDDC_PCP	CJ66	PCIERCA2_TX2_P	CK79	PCIERCB1A_RX2_M	CM9	VDDC_PCP
CH27	VDDC_PCP	CJ68	VSS	CK81	PCIERCB1A_TX3_M	CM11	VDDC_PCP
CH29	VDDC_PCP	CJ70	PCIERCB1B_RX3_P	CK83	PCIERCB1A_TX2_M	CM13	VDDC_PCP
CH57	VDDC_RCB0	CJ72	PCIERCB1B_RX2_P	CL2	VSS	CM15	VDDC_PCP
CH59	VSS	CJ74	PCIERCB1B_TX3_P	CL4	VSS	CM17	VDDC_PCP
CH61	VSS	CJ76	PCIERCB1B_TX2_P	CL6	VSS	CM19	VDDC_PCP
CH63	VSS	CJ78	PCIERCB1A_RX3_P	CL8	VSS	CM21	VDDC_PCP

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 20 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
CM23	VDDC_PCP	CN64	PCIERCA2_TX5_P	CP77	PCIERCB1A_RX5_M	CT7	VDDC_PCP
CM25	VDDC_PCP	CN66	PCIERCA2_TX4_P	CP79	PCIERCB1A_RX4_M	CT9	VDDC_PCP
CM27	VDDC_PCP	CN68	VSS	CP81	PCIERCB1A_TX5_M	CT11	VDDC_PCP
CM29	VDDC_PCP	CN70	PCIERCB1B_RX5_P	CP83	PCIERCB1A_TX4_M	CT13	VDDC_PCP
CM57	VDDH_RCB0	CN72	PCIERCB1B_RX4_P	CR2	VSS	CT15	VDDC_PCP
CM59	VSS	CN74	PCIERCB1B_TX5_P	CR4	VSS	CT17	VDDC_PCP
CM61	VSS	CN76	PCIERCB1B_TX4_P	CR6	VSS	CT19	VDDC_PCP
CM63	VSS	CN78	PCIERCB1A_RX5_P	CR8	VSS	CT21	VDDC_PCP
CM65	VSS	CN80	PCIERCB1A_RX4_P	CR10	VSS	CT23	VDDC_PCP
CM67	VSS	CN82	PCIERCB1A_TX5_P	CR12	VSS	CT25	VDDC_PCP
CM69	VSS	CN84	PCIERCB1A_TX4_P	CR14	VSS	CT27	VDDC_PCP
CM71	VSS	CP1	VSS	CR16	VSS	CT29	VDDC_PCP
CM73	VSS	CP3	VSS	CR18	VSS	CT57	VDDC_SOC
CM75	VSS	CP5	VSS	CR20	VSS	CT59	VSS
CM77	VSS	CP7	VSS	CR22	VSS	CT61	VSS
CM79	VSS	CP9	VSS	CR24	VSS	CT63	VSS
CM81	VSS	CP11	VSS	CR26	VSS	CT65	VSS
CM83	VSS	CP13	VSS	CR28	VSS	CT67	VSS
CN2	VDDC_PCP	CP15	VSS	CR56	VDDC_SOC	CT69	VSS
CN4	VDDC_PCP	CP17	VSS	CR58	VSS	CT71	VSS
CN6	VDDC_PCP	CP19	VSS	CR60	VSS	CT73	VSS
CN8	VDDC_PCP	CP21	VSS	CR62	VSS	CT75	VSS
CN10	VDDC_PCP	CP23	VSS	CR64	VSS	CT77	VSS
CN12	VDDC_PCP	CP25	VSS	CR66	VSS	CT79	VSS
CN14	VDDC_PCP	CP27	VSS	CR68	VSS	CT81	VSS
CN16	VDDC_PCP	CP29	VSS	CR70	VSS	CT83	VSS
CN18	VDDC_PCP	CP57	VDDC_SOC	CR72	VSS	CU2	VDDC_PCP
CN20	VDDC_PCP	CP59	PCIERCA2_RX5_M	CR74	VSS	CU4	VDDC_PCP
CN22	VDDC_PCP	CP61	PCIERCA2_RX4_M	CR76	VSS	CU6	VDDC_PCP
CN24	VDDC_PCP	CP63	VSS	CR78	VSS	CU8	VDDC_PCP
CN26	VDDC_PCP	CP65	PCIERCA2_TX5_M	CR80	VSS	CU10	VDDC_PCP
CN28	VDDC_PCP	CP67	PCIERCA2_TX4_M	CR82	VSS	CU12	VDDC_PCP
CN56	VDDC_SOC	CP69	PCIERCB1B_RX5_M	CR84	VSS	CU14	VDDC_PCP
CN58	VSS	CP71	PCIERCB1B_RX4_M	CT1	VDDC_PCP	CU16	VDDC_PCP
CN60	PCIERCA2_RX5_P	CP73	PCIERCB1B_TX5_M	CT3	VDDC_PCP	CU18	VDDC_PCP
CN62	PCIERCA2_RX4_P	CP75	PCIERCB1B_TX4_M	CT5	VDDC_PCP	CU20	VDDC_PCP

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 21 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
CU22	VDDC_PCP	CV9	VDDC_PCP	CV81	PCIERCB1A_TX7_M	CW70	VSS
CU24	VDDC_PCP	CV11	VDDC_PCP	CV83	PCIERCB1A_TX6_M	CW72	VSS
CU26	VDDC_PCP	CV13	VDDC_PCP	CW2	VSS	CW74	VSS
CU28	VDDC_PCP	CV15	VDDC_PCP	CW4	VSS	CW76	VSS
CU30	VDDC_PCP	CV17	VDDC_PCP	CW6	VDDC_PCP	CW78	VSS
CU32	VDDC_PCP	CV19	VDDC_PCP	CW8	VSS	CW80	VSS
CU34	VDDC_PCP	CV21	VDDC_PCP	CW10	VSS	CW82	VSS
CU36	VDDC_PCP	CV23	VDDC_PCP	CW12	VDDC_PCP	CW84	VSS
CU38	VDDC_PCP	CV25	VDDC_PCP	CW14	VSS	CY1	VDDC_PCP
CU40	VDDC_PCP	CV27	VSS	CW16	VSS	CY3	VSS
CU42	VDDC_PCP	CV29	VSS	CW18	VDDC_PCP	CY5	VSS
CU44	VDDC_PCP	CV31	VSS	CW20	VSS	CY7	VSS
CU46	VDDC_PCP	CV33	VSS	CW22	VSS	CY9	VSS
CU48	VDDC_PCP	CV35	VSS	CW24	VDDC_PCP	CY11	VSS
CU50	VDDC_RCA2	CV37	VSS	CW26	VSS	CY13	VSS
CU52	VDDC_RCA2	CV39	VSS	CW28	VDDC_PCP	CY15	VSS
CU54	VDDH_RCA2	CV41	VSS	CW30	VDDC_PCP	CY17	VSS
CU56	VDDC_SOC	CV43	VSS	CW32	VDDC_PCP	CY19	VSS
CU58	VSS	CV45	VSS	CW34	VDDC_PCP	CY21	VSS
CU60	PCIERCA2_RX7_P	CV47	VSS	CW36	VDDC_PCP	CY23	VSS
CU62	PCIERCA2_RX6_P	CV49	VSS	CW38	VDDC_PCP	CY25	VSS
CU64	PCIERCA2_TX7_P	CV51	VSS	CW40	VDDC_PCP	CY27	VDDC_PCP
CU66	PCIERCA2_TX6_P	CV53	VSS	CW42	VDDC_PCP	CY29	VDDC_PCP
CU68	VSS	CV55	VSS	CW44	VDDC_PCP	CY31	VDDC_PCP
CU70	PCIERCB1B_RX7_P	CV57	VDDC_SOC	CW46	VDDC_PCP	CY33	VDDC_PCP
CU72	PCIERCB1B_RX6_P	CV59	PCIERCA2_RX7_M	CW48	VDDC_PCP	CY35	VDDC_PCP
CU74	PCIERCB1B_TX7_P	CV61	PCIERCA2_RX6_M	CW50	VDDC_RCA2	CY37	VDDC_PCP
CU76	PCIERCB1B_TX6_P	CV63	VSS	CW52	VDDC_RCA2	CY39	VDDC_PCP
CU78	PCIERCB1A_RX7_P	CV65	PCIERCA2_TX7_M	CW54	VDDH_RCA2	CY41	VDDC_PCP
CU80	PCIERCB1A_RX6_P	CV67	PCIERCA2_TX6_M	CW56	VDDC_SOC	CY43	VDDC_PCP
CU82	PCIERCB1A_TX7_P	CV69	PCIERCB1B_RX7_M	CW58	VSS	CY45	VDDC_PCP
CU84	PCIERCB1A_TX6_P	CV71	PCIERCB1B_RX6_M	CW60	VSS	CY47	VDDC_PCP
CV1	VDDC_PCP	CV73	PCIERCB1B_TX7_M	CW62	VSS	CY49	VDDC_PCP
CV3	VDDC_PCP	CV75	PCIERCB1B_TX6_M	CW64	VSS	CY51	VDDC_RCA2
CV5	VDDC_PCP	CV77	PCIERCB1A_RX7_M	CW66	VSS	CY53	VDDH_RCA2
CV7	VDDC_PCP	CV79	PCIERCB1A_RX6_M	CW68	VSS	CY55	VDDC_SOC_CLKBUFF_AVDD

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 22 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
CY57	VDDC_SOC	DA46	VSS	DB33	VSS	DC22	VSS
CY59	VSS	DA48	VSS	DB35	VSS	DC24	PCIERCA0_TX0_P
CY61	VSS	DA50	VSS	DB37	VSS	DC26	VSS
CY63	VSS	DA52	VSS	DB39	VSS	DC28	VDDC_RCA0
CY65	VSS	DA54	VSS	DB41	VSS	DC30	VDDC_RCA0
CY67	VSS	DA56	VDDC_SOC	DB43	VSS	DC32	VDDC_PCP
CY69	VSS	DA58	VSS	DB45	VSS	DC34	VDDC_PCP
CY71	VSS	DA60	PCIERCA2_RX9_P	DB47	VSS	DC36	VDDC_PCP
CY73	VSS	DA62	PCIERCA2_RX8_P	DB49	VSS	DC38	VDDC_PCP
CY75	VSS	DA64	PCIERCA2_TX9_P	DB51	VSS	DC40	VDDC_PCP
CY77	VSS	DA66	PCIERCA2_TX8_P	DB53	VSS	DC42	VDDC_PCP
CY79	VSS	DA68	VSS	DB55	VSS	DC44	VDDC_PCP
CY81	VSS	DA70	PCIERCB0A_RX1_P	DB57	VDDC_SOC	DC46	VDDC_PCP
CY83	VSS	DA72	PCIERCB0A_RX0_P	DB59	PCIERCA2_RX9_M	DC48	VDDC_PCP
DA2	VSS	DA74	PCIERCB0A_TX1_P	DB61	PCIERCA2_RX8_M	DC50	VDDC_PCP
DA4	PCIERCA0_RX8_M	DA76	PCIERCB0A_TX0_P	DB63	VSS	DC52	VDDC_PCP
DA6	VSS	DA78	PCIERCB0B_RX1_P	DB65	PCIERCA2_TX9_M	DC54	VDDC_SOC
DA8	VSS	DA80	PCIERCB0B_RX0_P	DB67	PCIERCA2_TX8_M	DC56	VDDC_SOC
DA10	PCIERCA0_TX8_M	DA82	PCIERCB0B_TX1_P	DB69	PCIERCB0A_RX1_M	DC58	VSS
DA12	VSS	DA84	PCIERCB0B_TX0_P	DB71	PCIERCB0A_RX0_M	DC60	VSS
DA14	VSS	DB1	VSS	DB73	PCIERCB0A_TX1_M	DC62	VSS
DA16	PCIERCA0_RX1_M	DB3	PCIERCA0_RX8_P	DB75	PCIERCB0A_TX0_M	DC64	VSS
DA18	VSS	DB5	VSS	DB77	PCIERCB0B_RX1_M	DC66	VSS
DA20	VSS	DB7	PCIERCA0_RX9_M	DB79	PCIERCB0B_RX0_M	DC68	VSS
DA22	PCIERCA0_TX1_M	DB9	PCIERCA0_TX8_P	DB81	PCIERCB0B_TX1_M	DC70	VSS
DA24	VSS	DB11	VSS	DB83	PCIERCB0B_TX0_M	DC72	VSS
DA26	VSS	DB13	PCIERCA0_TX9_M	DC2	VSS	DC74	VSS
DA28	VSS	DB15	PCIERCA0_RX1_P	DC4	VSS	DC76	VSS
DA30	VSS	DB17	VSS	DC6	PCIERCA0_RX9_P	DC78	VSS
DA32	VSS	DB19	PCIERCA0_RX0_M	DC8	VSS	DC80	VSS
DA34	VSS	DB21	PCIERCA0_TX1_P	DC10	VSS	DC82	VSS
DA36	VSS	DB23	VSS	DC12	PCIERCA0_TX9_P	DC84	VSS
DA38	VSS	DB25	PCIERCA0_TX0_M	DC14	VSS	DD1	VSS
DA40	VSS	DB27	VSS	DC16	VSS	DD3	VSS
DA42	VSS	DB29	VSS	DC18	PCIERCA0_RX0_P	DD5	VSS
DA44	VSS	DB31	VSS	DC20	VSS	DD7	VSS

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 23 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
DD9	VSS	DD81	VSS	DE70	PCIERCB0A_RX3_P	DF57	RFU_D2D
DD11	VSS	DD83	VSS	DE72	PCIERCB0A_RX2_P	DF59	PCIERCA2_RX11_M
DD13	VSS	DE2	VSS	DE74	PCIERCB0A_TX3_P	DF61	PCIERCA2_RX10_M
DD15	VSS	DE4	PCIERCA0_RX10_M	DE76	PCIERCB0A_TX2_P	DF63	VSS
DD17	VSS	DE6	VSS	DE78	PCIERCB0B_RX3_P	DF65	PCIERCA2_TX11_M
DD19	VSS	DE8	VSS	DE80	PCIERCB0B_RX2_P	DF67	PCIERCA2_TX10_M
DD21	VSS	DE10	PCIERCA0_TX10_M	DE82	PCIERCB0B_TX3_P	DF69	PCIERCB0A_RX3_M
DD23	VSS	DE12	VSS	DE84	PCIERCB0B_TX2_P	DF71	PCIERCB0A_RX2_M
DD25	VSS	DE14	VSS	DF1	VSS	DF73	PCIERCB0A_TX3_M
DD27	VDDC_RCA0	DE16	PCIERCA0_RX3_M	DF3	PCIERCA0_RX10_P	DF75	PCIERCB0A_TX2_M
DD29	VDDC_RCA0	DE18	VSS	DF5	VSS	DF77	PCIERCB0B_RX3_M
DD31	VDDC_RCA0	DE20	VSS	DF7	PCIERCA0_RX11_M	DF79	PCIERCB0B_RX2_M
DD33	VDDC_PCP	DE22	PCIERCA0_TX3_M	DF9	PCIERCA0_TX10_P	DF81	PCIERCB0B_TX3_M
DD35	VDDC_PCP	DE24	VSS	DF11	VSS	DF83	PCIERCB0B_TX2_M
DD37	VDDC_PCP	DE26	VSS	DF13	PCIERCA0_TX11_M	DG2	VSS
DD39	VDDC_PCP	DE28	VSS	DF15	PCIERCA0_RX3_P	DG4	VSS
DD41	VDDC_PCP	DE30	VSS	DF17	VSS	DG6	PCIERCA0_RX11_P
DD43	VDDC_PCP	DE32	VSS	DF19	PCIERCA0_RX2_M	DG8	VSS
DD45	VDDC_PCP	DE34	VSS	DF21	PCIERCA0_TX3_P	DG10	VSS
DD47	VDDC_PCP	DE36	VSS	DF23	VSS	DG12	PCIERCA0_TX11_P
DD49	VDDC_PCP	DE38	VSS	DF25	PCIERCA0_TX2_M	DG14	VSS
DD51	VDDC_PCP	DE40	VSS	DF27	VSS	DG16	VSS
DD53	VDDC_PCP	DE42	VSS	DF29	VSS	DG18	PCIERCA0_RX2_P
DD55	VDDC_SOC	DE44	VSS	DF31	VSS	DG20	VSS
DD57	VDDC_SOC	DE46	VSS	DF33	VSS	DG22	VSS
DD59	VSS	DE48	VSS	DF35	VSS	DG24	PCIERCA0_TX2_P
DD61	VSS	DE50	VSS	DF37	VSS	DG26	VSS
DD63	VSS	DE52	VSS	DF39	VSS	DG28	VDDH_RCA0
DD65	VSS	DE54	VSS	DF41	VSS	DG30	RFU_37
DD67	VSS	DE56	VSS	DF43	VSS	DG32	VDD18_SERDES_AVDD
DD69	VSS	DE58	VSS	DF45	VSS	DG34	VDD18_SERDES_AVDD
DD71	VSS	DE60	PCIERCA2_RX11_P	DF47	VSS	DG36	VDD18_DDR_AVDD
DD73	VSS	DE62	PCIERCA2_RX10_P	DF49	VSS	DG38	VDD18_SOC
DD75	VSS	DE64	PCIERCA2_TX11_P	DF51	VSS	DG40	RFU_15
DD77	VSS	DE66	PCIERCA2_TX10_P	DF53	VSS	DG42	RFU_39
DD79	VSS	DE68	VSS	DF55	VSS	DG44	RFU_D2D

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 24 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
DG46	RFU_D2D	DH33	VDD18_SERDES_AVDD	DJ22	PCIERCA0_TX5_M	DK9	PCIERCA0_TX12_P
DG48	RFU_D2D	DH35	VDD18_DDR_AVDD	DJ24	VSS	DK11	VSS
DG50	RFU_D2D	DH37	VDD18_DDR_AVDD	DJ26	VSS	DK13	PCIERCA0_TX13_M
DG52	RFU_D2D	DH39	VDD18_SOC	DJ28	VSS	DK15	PCIERCA0_RX5_P
DG54	RFU_D2D	DH41	RFU_36	DJ30	VSS	DK17	VSS
DG56	RFU_D2D	DH43	RFU_D2D	DJ32	VSS	DK19	PCIERCA0_RX4_M
DG58	VSS	DH45	RFU_D2D	DJ34	VSS	DK21	PCIERCA0_TX5_P
DG60	VSS	DH47	RFU_D2D	DJ36	VSS	DK23	VSS
DG62	VSS	DH49	RFU_D2D	DJ38	VSS	DK25	PCIERCA0_TX4_M
DG64	VSS	DH51	RFU_D2D	DJ40	VSS	DK27	VSS
DG66	VSS	DH53	RFU_D2D	DJ42	VSS	DK29	EFUSE_MFG_VDDQ1P8
DG68	VSS	DH55	RFU_D2D	DJ44	VSS	DK31	EFUSE_PCP_VDDQ1P8
DG70	VSS	DH57	RFU_D2D	DJ46	VSS	DK33	IIC_SDA_1
DG72	VSS	DH59	VSS	DJ48	VSS	DK35	RFU_22
DG74	VSS	DH61	VSS	DJ50	VSS	DK37	RFU_32
DG76	VSS	DH63	VSS	DJ52	VSS	DK39	RFU_33
DG78	VSS	DH65	VSS	DJ54	VSS	DK41	DDR1_PLL_TESTOUT_P
DG80	VSS	DH67	VSS	DJ56	RFU_D2D	DK43	VSS
DG82	VSS	DH69	VSS	DJ58	VSS	DK45	VSS
DG84	VSS	DH71	VSS	DJ60	PCIERCA2_RX13_P	DK47	VSS
DH1	VSS	DH73	VSS	DJ62	PCIERCA2_RX12_P	DK49	VSS
DH3	VSS	DH75	VSS	DJ64	PCIERCA2_TX13_P	DK51	VSS
DH5	VSS	DH77	VSS	DJ66	PCIERCA2_TX12_P	DK53	VSS
DH7	VSS	DH79	VSS	DJ68	VSS	DK55	VSS
DH9	VSS	DH81	VSS	DJ70	PCIERCB0A_RX5_P	DK57	RFU_D2D
DH11	VSS	DH83	VSS	DJ72	PCIERCB0A_RX4_P	DK59	PCIERCA2_RX13_M
DH13	VSS	DJ2	VSS	DJ74	PCIERCB0A_TX5_P	DK61	PCIERCA2_RX12_M
DH15	VSS	DJ4	PCIERCA0_RX12_M	DJ76	PCIERCB0A_TX4_P	DK63	VSS
DH17	VSS	DJ6	VSS	DJ78	PCIERCB0B_RX5_P	DK65	PCIERCA2_TX13_M
DH19	VSS	DJ8	VSS	DJ80	PCIERCB0B_RX4_P	DK67	PCIERCA2_TX12_M
DH21	VSS	DJ10	PCIERCA0_TX12_M	DJ82	PCIERCB0B_TX5_P	DK69	PCIERCB0A_RX5_M
DH23	VSS	DJ12	VSS	DJ84	PCIERCB0B_TX4_P	DK71	PCIERCB0A_RX4_M
DH25	VSS	DJ14	VSS	DK1	VSS	DK73	PCIERCB0A_TX5_M
DH27	VDDH_RCA0	DJ16	PCIERCA0_RX5_M	DK3	PCIERCA0_RX12_P	DK75	PCIERCB0A_TX4_M
DH29	VDDH_RCA0	DJ18	VSS	DK5	VSS	DK77	PCIERCB0B_RX5_M
DH31	RFU_38	DJ20	VSS	DK7	PCIERCA0_RX13_M	DK79	PCIERCB0B_RX4_M

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 25 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
DK81	PCIERCB0B_TX5_M	DL70	VSS	DM57	RFU_D2D	DN46	VSS
DK83	PCIERCB0B_TX4_M	DL72	VSS	DM59	VSS	DN48	VSS
DL2	VSS	DL74	VSS	DM61	VSS	DN50	VSS
DL4	VSS	DL76	VSS	DM63	VSS	DN52	VSS
DL6	PCIERCA0_RX13_P	DL78	VSS	DM65	VSS	DN54	VSS
DL8	VSS	DL80	VSS	DM67	VSS	DN56	VSS
DL10	VSS	DL82	VSS	DM69	VSS	DN58	VSS
DL12	PCIERCA0_TX13_P	DL84	VSS	DM71	VSS	DN60	PCIERCA2_RX15_P
DL14	VSS	DM1	VSS	DM73	VSS	DN62	PCIERCA2_RX14_P
DL16	VSS	DM3	VSS	DM75	VSS	DN64	PCIERCA2_TX15_P
DL18	PCIERCA0_RX4_P	DM5	VSS	DM77	VSS	DN66	PCIERCA2_TX14_P
DL20	VSS	DM7	VSS	DM79	VSS	DN68	VSS
DL22	VSS	DM9	VSS	DM81	VSS	DN70	PCIERCB0A_RX7_P
DL24	PCIERCA0_TX4_P	DM11	VSS	DM83	VSS	DN72	PCIERCB0A_RX6_P
DL26	VSS	DM13	VSS	DN2	VSS	DN74	PCIERCB0A_TX7_P
DL28	EFUSE_SOC_VDDQ1P8	DM15	VSS	DN4	PCIERCA0_RX14_M	DN76	PCIERCB0A_TX6_P
DL30	EFUSE_TMM_VDDQ1P8	DM17	VSS	DN6	VSS	DN78	PCIERCB0B_RX7_P
DL32	IIC_SCL_1	DM19	VSS	DN8	VSS	DN80	PCIERCB0B_RX6_P
DL34	RFU_21	DM21	VSS	DN10	PCIERCA0_TX14_M	DN82	PCIERCB0B_TX7_P
DL36	RFU_23	DM23	VSS	DN12	VSS	DN84	PCIERCB0B_TX6_P
DL38	VSS	DM25	VSS	DN14	VSS	DP1	VSS
DL40	RFU_24	DM27	PQT_VDM_EXTVREF	DN16	PCIERCA0_RX7_M	DP3	PCIERCA0_RX14_P
DL42	DDR1_PLL_TESTOUT_N	DM29	SYS_TS_AN_IO_1	DN18	VSS	DP5	VSS
DL44	RFU_D2D	DM31	VSS	DN20	VSS	DP7	PCIERCA0_RX15_M
DL46	RFU_D2D	DM33	VSS	DN22	PCIERCA0_TX7_M	DP9	PCIERCA0_TX14_P
DL48	RFU_D2D	DM35	VSS	DN24	VSS	DP11	VSS
DL50	RFU_D2D	DM37	VSS	DN26	VSS	DP13	PCIERCA0_TX15_M
DL52	RFU_D2D	DM39	VSS	DN28	SYS_TS_AN_IO_0	DP15	PCIERCA0_RX7_P
DL54	RFU_D2D	DM41	VSS	DN30	VSS	DP17	VSS
DL56	RFU_D2D	DM43	VDDQ_DDR0123	DN32	VSS	DP19	PCIERCA0_RX6_M
DL58	VSS	DM45	RFU_D2D	DN34	VSS	DP21	PCIERCA0_TX7_P
DL60	VSS	DM47	RFU_D2D	DN36	VSS	DP23	VSS
DL62	VSS	DM49	RFU_D2D	DN38	VSS	DP25	PCIERCA0_TX6_M
DL64	VSS	DM51	RFU_D2D	DN40	RFU_25	DP27	VSS
DL66	VSS	DM53	RFU_D2D	DN42	DDR2_PLL_TESTOUT_N	DP29	VSS
DL68	VSS	DM55	RFU_D2D	DN44	VSS	DP31	IIC_SDA_4

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 26 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
DP33	ALERT4_N	DR22	VSS	DT9	VSS	DT81	VSS
DP35	ALERT3_N	DR24	PCIERCA0_TX6_P	DT11	VSS	DT83	VSS
DP37	ALERT2_N	DR26	VSS	DT13	VSS	DU2	IIC_SCL_10
DP39	RFU_26	DR28	IIC_SCL_5	DT15	VSS	DU4	ALERT10_N
DP41	DDR2_PLL_TESTOUT_P	DR30	ALERT5_N	DT17	VSS	DU6	VSS
DP43	DDR3_PLL_TESTOUT_N	DR32	VSS	DT19	VSS	DU8	ALERT9_N
DP45	VSS	DR34	VSS	DT21	#	DU10	IIC_SDA_8
DP47	VSS	DR36	VSS	DT23	VSS	DU12	VSS
DP49	VSS	DR38	IIC_SDA_0	DT25	VSS	DU14	IIC_SDA_7
DP51	SYS_REFCLK_SRIS_N	DR40	PMALERT_N	DT27	RFU_27	DU16	IIC_SCL_6
DP53	SYS_REFCLK_SRNS_N	DR42	VSS	DT29	IIC_SDA_5	DU18	VSS
DP55	VSS	DR44	RFU_16	DT31	IIC_SCL_4	DU20	#
DP57	VSS	DR46	RFU_18	DT33	IIC_SCL_3	DU22	#
DP59	PCIERCA2_RX15_M	DR48	RFU_20	DT35	IIC_SDA_3	DU24	VSS
DP61	PCIERCA2_RX14_M	DR50	VSS	DT37	IIC_SDA_2	DU26	RFU_28
DP63	VSS	DR52	SYS_REFCLK_SRIS_P	DT39	IIC_SCL_0	DU28	VSS
DP65	PCIERCA2_TX15_M	DR54	SYS_REFCLK_SRNS_P	DT41	DDR0_PLL_TESTOUT_N	DU30	VSS
DP67	PCIERCA2_TX14_M	DR56	SPI1_IO1	DT43	DDR3_PLL_TESTOUT_P	DU32	VSS
DP69	PCIERCB0A_RX7_M	DR58	VSS	DT45	RFU_17	DU34	VSS
DP71	PCIERCB0A_RX6_M	DR60	VSS	DT47	RFU_19	DU36	IIC_SCL_2
DP73	PCIERCB0A_TX7_M	DR62	VSS	DT49	SPI1_CS0	DU38	VSS
DP75	PCIERCB0A_TX6_M	DR64	VSS	DT51	VSS	DU40	VSS
DP77	PCIERCB0B_RX7_M	DR66	VSS	DT53	VSS	DU42	DDR0_PLL_TESTOUT_P
DP79	PCIERCB0B_RX6_M	DR68	VSS	DT55	VSS	DU44	VSS
DP81	PCIERCB0B_TX7_M	DR70	VSS	DT57	SPI1_CLK	DU46	VSS
DP83	PCIERCB0B_TX6_M	DR72	VSS	DT59	VSS	DU48	RFU_31
DR2	VSS	DR74	VSS	DT61	VSS	DU50	SPI1_CS1
DR4	VSS	DR76	VSS	DT63	VSS	DU52	SPI1_CS2
DR6	PCIERCA0_RX15_P	DR78	VSS	DT65	#	DU54	SPI1_IO0
DR8	VSS	DR80	VSS	DT67	VSS	DU56	SPI1_IO2
DR10	VSS	DR82	VSS	DT69	VSS	DU58	SPI0_IO1
DR12	PCIERCA0_TX15_P	DR84	VSS	DT71	VSS	DU60	SPI0_IO3
DR14	VSS	DT1	VSS	DT73	VSS	DU62	SPI0_CS1
DR16	VSS	DT3	VSS	DT75	VSS	DU64	#
DR18	PCIERCA0_RX6_P	DT5	VSS	DT77	VSS	DU66	#
DR20	VSS	DT7	VSS	DT79	VSS	DU68	UART_SCLK

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 27 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
DU70	UART_RTS0	DV57	SPI0_IO0	DW46	VSS	DY33	DDR3_CS_N_0
DU72	VDDQ_DDR01_SENSE_N	DV59	SPI0_IO2	DW48	VDDQ_DDR0123	DY35	DDR3_BA_0
DU74	VDDQ_DDR23_SENSE_N	DV61	SPI0_CS0	DW50	VDDQ_DDR0123	DY37	DDR3_PAR
DU76	UART_SIN1	DV63	SPI0_CS2	DW52	VDDQ_DDR0123	DY39	DDR3_CLK_0_P
DU78	UART_SIN3	DV65	#	DW54	VSS	DY41	DDR3_CLK_2_P
DU80	UART_SOUT0	DV67	SPI0_CLK	DW56	VSS	DY43	DDR3_ADDR_1
DU82	UART_SOUT2	DV69	UART_CTS0	DW58	VSS	DY45	DDR3_ADDR_6
DU84	UART_SOUT4	DV71	VDDQ_DDR01_SENSE_P	DW60	VSS	DY47	DDR3_ADDR_9
DV1	VSS	DV73	VDDQ_DDR23_SENSE_P	DW62	VSS	DY49	DDR3_BG_0
DV3	IIC_SDA_10	DV75	UART_SIN0	DW64	VSS	DY51	DDR3_CKE_1
DV5	IIC_SCL_9	DV77	UART_SIN2	DW66	VSS	DY53	VSS
DV7	IIC_SDA_9	DV79	UART_SIN4	DW68	VSS	DY55	DDR3_DATA_70
DV9	IIC_SCL_8	DV81	UART_SOUT1	DW70	VSS	DY57	DDR3_DSTR_17_P
DV11	ALERT8_N	DV83	UART_SOUT3	DW72	VSS	DY59	DDR3_DATA_68
DV13	IIC_SCL_7	DW2	VSS	DW74	VSS	DY61	DDR3_DATA_30
DV15	ALERT7_N	DW4	VSS	DW76	VSS	DY63	DDR3_DSTR_12_P
DV17	IIC_SDA_6	DW6	VSS	DW78	VSS	DY65	DDR3_DATA_28
DV19	ALERT6_N	DW8	VSS	DW80	VSS	DY67	DDR3_DATA_22
DV21	#	DW10	VSS	DW82	VSS	DY69	DDR3_DSTR_11_P
DV23	WSCAN_ENI	DW12	VSS	DW84	VSS	DY71	DDR3_DATA_20
DV25	WSCAN_ENO	DW14	VSS	DY1	VSS	DY73	DDR3_DATA_14
DV27	EDT_UPDATE	DW16	VSS	DY3	DDR3_DATA_59	DY75	DDR3_DSTR_10_P
DV29	VSS	DW18	VSS	DY5	DDR3_DSTR_7_N	DY77	DDR3_DATA_12
DV31	VSS	DW20	VSS	DY7	DDR3_DATA_61	DY79	DDR3_DATA_6
DV33	VSS	DW22	VSS	DY9	DDR3_DATA_55	DY81	DDR3_DSTR_9_P
DV35	VSS	DW24	VSS	DY11	DDR3_DSTR_6_N	DY83	DDR3_DATA_4
DV37	VSS	DW26	VSS	DY13	DDR3_DATA_53	EA2	DDR3_DATA_58
DV39	VSS	DW28	VDDQ_DDR0123	DY15	DDR3_DATA_47	EA4	DDR3_DSTR_7_P
DV41	VSS	DW30	VSS	DY17	DDR3_DSTR_5_N	EA6	DDR3_DATA_57
DV43	VSS	DW32	VDDQ_DDR0123	DY19	DDR3_DATA_45	EA8	DDR3_DATA_51
DV45	VSS	DW34	VSS	DY21	DDR3_DATA_39	EA10	DDR3_DSTR_6_P
DV47	VSS	DW36	VDDQ_DDR0123	DY23	DDR3_DSTR_4_N	EA12	DDR3_DATA_49
DV49	VSS	DW38	VSS	DY25	DDR3_DATA_37	EA14	DDR3_DATA_43
DV51	VSS	DW40	VDDQ_DDR0123	DY27	DDR3_CID_0	EA16	DDR3_DSTR_5_P
DV53	VSS	DW42	VSS	DY29	DDR3_CID_2	EA18	DDR3_DATA_41
DV55	SPI1_IO3	DW44	VDDQ_DDR0123	DY31	DDR3_ADDR_13	EA20	DDR3_DATA_35

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 28 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
EA22	DDR3_DSTR_4_P	EB9	VSS	EB81	VSS	EC70	DDR3_DATA_17
EA24	DDR3_DATA_33	EB11	VSS	EB83	VSS	EC72	DDR3_DATA_11
EA26	DDR3_ATB1	EB13	VSS	EC2	DDR3_DATA_63	EC74	DDR3_DSTR_1_P
EA28	DDR3_ODT_1	EB15	VSS	EC4	DDR3_DSTR_16_N	EC76	DDR3_DATA_9
EA30	DDR3_CS_N_3	EB17	VSS	EC6	DDR3_DATA_56	EC78	DDR3_DATA_3
EA32	DDR3_ODT_0	EB19	VSS	EC8	DDR3_DATA_50	EC80	DDR3_DSTR_0_P
EA34	DDR3_ADDR_14_WE_N	EB21	VSS	EC10	DDR3_DSTR_15_N	EC82	DDR3_DATA_0
EA36	DDR3_BA_1	EB23	VSS	EC12	DDR3_DATA_48	EC84	VSS
EA38	DDR3_CLK_0_N	EB25	VSS	EC14	DDR3_DATA_42	ED1	VSS
EA40	DDR3_CLK_2_N	EB27	VDDQ_DDR0123	EC16	DDR3_DSTR_14_N	ED3	DDR3_DATA_62
EA42	VSS	EB29	VDDQ_DDR0123	EC18	DDR3_DATA_40	ED5	DDR3_DSTR_16_P
EA44	DDR3_ADDR_4	EB31	VDDQ_DDR0123	EC20	DDR3_DATA_34	ED7	DDR3_DATA_60
EA46	DDR3_ADDR_7	EB33	VDDQ_DDR0123	EC22	DDR3_DSTR_13_N	ED9	DDR3_DATA_54
EA48	DDR3_ALERT_N	EB35	VDDQ_DDR0123	EC24	DDR3_DATA_32	ED11	DDR3_DSTR_15_P
EA50	DDR3_CKE_0	EB37	VDDQ_DDR0123	EC26	DDR3_ATB0	ED13	DDR3_DATA_52
EA52	DDR3_RESETN	EB39	VDDQ_DDR0123	EC28	DDR3_ODT_3	ED15	DDR3_DATA_46
EA54	DDR3_DATA_66	EB41	VDDQ_DDR0123	EC30	DDR3_CS_N_1	ED17	DDR3_DSTR_14_P
EA56	DDR3_DSTR_17_N	EB43	VDDQ_DDR0123	EC32	DDR3_ADDR_15_CAS_N	ED19	DDR3_DATA_44
EA58	DDR3_DATA_64	EB45	VDDQ_DDR0123	EC34	DDR3_ADDR_16_RAS_N	ED21	DDR3_DATA_38
EA60	DDR3_DATA_26	EB47	VDDQ_DDR0123	EC36	DDR3_ADDR_0	ED23	DDR3_DSTR_13_P
EA62	DDR3_DSTR_12_N	EB49	VDDQ_DDR0123	EC38	DDR3_CLK_1_P	ED25	DDR3_DATA_36
EA64	DDR3_DATA_24	EB51	VDDQ_DDR0123	EC40	DDR3_CLK_3_P	ED27	DDR3_CID_1
EA66	DDR3_DATA_18	EB53	VSS	EC42	VDDQ_DDR0123	ED29	DDR3_ADDR_17
EA68	DDR3_DSTR_11_N	EB55	VSS	EC44	DDR3_ADDR_3	ED31	DDR3_ODT_2
EA70	DDR3_DATA_16	EB57	VSS	EC46	DDR3_ADDR_8	ED33	DDR3_CS_N_2
EA72	DDR3_DATA_10	EB59	VSS	EC48	DDR3_ADDR_12	ED35	DDR3_ADDR_10
EA74	DDR3_DSTR_10_N	EB61	VSS	EC50	DDR3_ACT_N	ED37	DDR3_CLK_1_N
EA76	DDR3_DATA_8	EB63	VSS	EC52	DDR3_CKE_3	ED39	DDR3_CLK_3_N
EA78	DDR3_DATA_2	EB65	VSS	EC54	DDR3_DATA_67	ED41	VDDQ_DDR0123
EA80	DDR3_DSTR_9_N	EB67	VSS	EC56	DDR3_DSTR_8_P	ED43	DDR3_ADDR_2
EA82	DDR3_DATA_5	EB69	VSS	EC58	DDR3_DATA_65	ED45	DDR3_ADDR_5
EA84	VSS	EB71	VSS	EC60	DDR3_DATA_27	ED47	DDR3_ADDR_11
EB1	VSS	EB73	VSS	EC62	DDR3_DSTR_3_P	ED49	DDR3_BG_1
EB3	VSS	EB75	VSS	EC64	DDR3_DATA_25	ED51	DDR3_CKE_2
EB5	VSS	EB77	VSS	EC66	DDR3_DATA_19	ED53	VSS
EB7	VSS	EB79	VSS	EC68	DDR3_DSTR_2_P	ED55	DDR3_DATA_71

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 29 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
ED57	DDR3_DSTR_8_N	EE46	VDDQ_DDR0123	EF33	VSS	EG22	DDR2_DSTR_4_P
ED59	DDR3_DATA_69	EE48	VDDQ_DDR0123	EF35	VDDQ_DDR0123	EG24	DDR2_DATA_33
ED61	DDR3_DATA_31	EE50	VDDQ_DDR0123	EF37	VSS	EG26	DDR2_ATB1
ED63	DDR3_DSTR_3_N	EE52	VDDQ_DDR0123	EF39	VDDQ_DDR0123	EG28	DDR2_ODT_1
ED65	DDR3_DATA_29	EE54	VSS	EF41	VSS	EG30	DDR2_CS_N_3
ED67	DDR3_DATA_23	EE56	VSS	EF43	VSS	EG32	DDR2_ODT_0
ED69	DDR3_DSTR_2_N	EE58	VSS	EF45	VSS	EG34	DDR2_ADDR_14_WE_N
ED71	DDR3_DATA_21	EE60	VSS	EF47	VDDQ_DDR0123	EG36	DDR2_BA_1
ED73	DDR3_DATA_15	EE62	VSS	EF49	VSS	EG38	DDR2_CLK_0_N
ED75	DDR3_DSTR_1_N	EE64	VSS	EF51	VDDQ_DDR0123	EG40	DDR2_CLK_2_N
ED77	DDR3_DATA_13	EE66	VSS	EF53	VSS	EG42	VSS
ED79	DDR3_DATA_7	EE68	VSS	EF55	VSS	EG44	DDR2_ADDR_4
ED81	DDR3_DSTR_0_N	EE70	VSS	EF57	VSS	EG46	DDR2_ADDR_7
ED83	DDR3_DATA_1	EE72	VSS	EF59	VSS	EG48	DDR2_ALERT_N
EE2	VSS	EE74	VSS	EF61	VSS	EG50	DDR2_CKE_0
EE4	VSS	EE76	VSS	EF63	VSS	EG52	DDR2_RESETN
EE6	VSS	EE78	VSS	EF65	VSS	EG54	DDR2_DATA_66
EE8	VSS	EE80	VSS	EF67	VSS	EG56	DDR2_DSTR_17_N
EE10	VSS	EE82	VSS	EF69	VSS	EG58	DDR2_DATA_64
EE12	VSS	EE84	VSS	EF71	VSS	EG60	DDR2_DATA_26
EE14	VSS	EF1	VSS	EF73	VSS	EG62	DDR2_DSTR_12_N
EE16	VSS	EF3	VSS	EF75	VSS	EG64	DDR2_DATA_24
EE18	VSS	EF5	VSS	EF77	VSS	EG66	DDR2_DATA_18
EE20	VSS	EF7	VSS	EF79	VSS	EG68	DDR2_DSTR_11_N
EE22	VSS	EF9	VSS	EF81	VSS	EG70	DDR2_DATA_16
EE24	VSS	EF11	VSS	EF83	VSS	EG72	DDR2_DATA_10
EE26	SCAN_EN	EF13	VSS	EG2	DDR2_DATA_59	EG74	DDR2_DSTR_10_N
EE28	VDDQ_DDR0123	EF15	VSS	EG4	DDR2_DSTR_7_P	EG76	DDR2_DATA_8
EE30	VDDQ_DDR0123	EF17	VSS	EG6	DDR2_DATA_57	EG78	DDR2_DATA_2
EE32	VDDQ_DDR0123	EF19	VSS	EG8	DDR2_DATA_51	EG80	DDR2_DSTR_9_N
EE34	VDDQ_DDR0123	EF21	VSS	EG10	DDR2_DSTR_6_P	EG82	DDR2_DATA_4
EE36	VDDQ_DDR0123	EF23	VSS	EG12	DDR2_DATA_49	EG84	VSS
EE38	VDDQ_DDR0123	EF25	VSS	EG14	DDR2_DATA_43	EH1	VSS
EE40	VDDQ_DDR0123	EF27	VDDQ_DDR0123	EG16	DDR2_DSTR_5_P	EH3	DDR2_DATA_58
EE42	VSS	EF29	VSS	EG18	DDR2_DATA_41	EH5	DDR2_DSTR_7_N
EE44	VDDQ_DDR0123	EF31	VDDQ_DDR0123	EG20	DDR2_DATA_35	EH7	DDR2_DATA_61

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 30 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
EH9	DDR2_DATA_55	EH81	DDR2_DSTR_9_P	EJ70	VSS	EK57	DDR2_DSTR_8_N
EH11	DDR2_DSTR_6_N	EH83	DDR2_DATA_5	EJ72	VSS	EK59	DDR2_DATA_69
EH13	DDR2_DATA_53	EJ2	VSS	EJ74	VSS	EK61	DDR2_DATA_31
EH15	DDR2_DATA_47	EJ4	VSS	EJ76	VSS	EK63	DDR2_DSTR_3_N
EH17	DDR2_DSTR_5_N	EJ6	VSS	EJ78	VSS	EK65	DDR2_DATA_29
EH19	DDR2_DATA_45	EJ8	VSS	EJ80	VSS	EK67	DDR2_DATA_23
EH21	DDR2_DATA_39	EJ10	VSS	EJ82	VSS	EK69	DDR2_DSTR_2_N
EH23	DDR2_DSTR_4_N	EJ12	VSS	EJ84	VSS	EK71	DDR2_DATA_21
EH25	DDR2_DATA_37	EJ14	VSS	EK1	VSS	EK73	DDR2_DATA_15
EH27	DDR2_CID_0	EJ16	VSS	EK3	DDR2_DATA_63	EK75	DDR2_DSTR_1_N
EH29	DDR2_CID_2	EJ18	VSS	EK5	DDR2_DSTR_16_P	EK77	DDR2_DATA_13
EH31	DDR2_ADDR_13	EJ20	VSS	EK7	DDR2_DATA_60	EK79	DDR2_DATA_7
EH33	DDR2_CS_N_0	EJ22	VSS	EK9	DDR2_DATA_54	EK81	DDR2_DSTR_0_N
EH35	DDR2_BA_0	EJ24	VSS	EK11	DDR2_DSTR_15_P	EK83	DDR2_DATA_0
EH37	DDR2_PAR	EJ26	VSS	EK13	DDR2_DATA_52	EL2	DDR2_DATA_62
EH39	DDR2_CLK_0_P	EJ28	VDDQ_DDR0123	EK15	DDR2_DATA_46	EL4	DDR2_DSTR_16_N
EH41	DDR2_CLK_2_P	EJ30	VDDQ_DDR0123	EK17	DDR2_DSTR_14_P	EL6	DDR2_DATA_56
EH43	DDR2_ADDR_1	EJ32	VDDQ_DDR0123	EK19	DDR2_DATA_44	EL8	DDR2_DATA_50
EH45	DDR2_ADDR_6	EJ34	VDDQ_DDR0123	EK21	DDR2_DATA_38	EL10	DDR2_DSTR_15_N
EH47	DDR2_ADDR_9	EJ36	VDDQ_DDR0123	EK23	DDR2_DSTR_13_P	EL12	DDR2_DATA_48
EH49	DDR2_BG_0	EJ38	VDDQ_DDR0123	EK25	DDR2_DATA_36	EL14	DDR2_DATA_42
EH51	DDR2_CKE_1	EJ40	VDDQ_DDR0123	EK27	DDR2_CID_1	EL16	DDR2_DSTR_14_N
EH53	VSS	EJ42	VDDQ_DDR0123	EK29	DDR2_ADDR_17	EL18	DDR2_DATA_40
EH55	DDR2_DATA_70	EJ44	VDDQ_DDR0123	EK31	DDR2_ODT_2	EL20	DDR2_DATA_34
EH57	DDR2_DSTR_17_P	EJ46	VDDQ_DDR0123	EK33	DDR2_CS_N_2	EL22	DDR2_DSTR_13_N
EH59	DDR2_DATA_68	EJ48	VDDQ_DDR0123	EK35	DDR2_ADDR_10	EL24	DDR2_DATA_32
EH61	DDR2_DATA_30	EJ50	VDDQ_DDR0123	EK37	DDR2_CLK_1_N	EL26	DDR2_ATB0
EH63	DDR2_DSTR_12_P	EJ52	VDDQ_DDR0123	EK39	DDR2_CLK_3_N	EL28	DDR2_ODT_3
EH65	DDR2_DATA_28	EJ54	VSS	EK41	VDDQ_DDR0123	EL30	DDR2_CS_N_1
EH67	DDR2_DATA_22	EJ56	VSS	EK43	DDR2_ADDR_2	EL32	DDR2_ADDR_15_CAS_N
EH69	DDR2_DSTR_11_P	EJ58	VSS	EK45	DDR2_ADDR_5	EL34	DDR2_ADDR_16_RAS_N
EH71	DDR2_DATA_20	EJ60	VSS	EK47	DDR2_ADDR_11	EL36	DDR2_ADDR_0
EH73	DDR2_DATA_14	EJ62	VSS	EK49	DDR2_BG_1	EL38	DDR2_CLK_1_P
EH75	DDR2_DSTR_10_P	EJ64	VSS	EK51	DDR2_CKE_2	EL40	DDR2_CLK_3_P
EH77	DDR2_DATA_12	EJ66	VSS	EK53	VSS	EL42	VSS
EH79	DDR2_DATA_6	EJ68	VSS	EK55	DDR2_DATA_71	EL44	DDR2_ADDR_3

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 31 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
EL46	DDR2_ADDR_8	EM33	VSS	EN22	VSS	EP9	DDR1_DATA_55
EL48	DDR2_ADDR_12	EM35	VDDQ_DDR0123	EN24	VSS	EP11	DDR1_DSTR_6_N
EL50	DDR2_ACT_N	EM37	VSS	EN26	VSS	EP13	DDR1_DATA_53
EL52	DDR2_CKE_3	EM39	VDDQ_DDR0123	EN28	VDDQ_DDR0123	EP15	DDR1_DATA_47
EL54	DDR2_DATA_67	EM41	VSS	EN30	VDDQ_DDR0123	EP17	DDR1_DSTR_5_N
EL56	DDR2_DSTR_8_P	EM43	VSS	EN32	VDDQ_DDR0123	EP19	DDR1_DATA_45
EL58	DDR2_DATA_65	EM45	VSS	EN34	VDDQ_DDR0123	EP21	DDR1_DATA_39
EL60	DDR2_DATA_27	EM47	VDDQ_DDR0123	EN36	VDDQ_DDR0123	EP23	DDR1_DSTR_4_N
EL62	DDR2_DSTR_3_P	EM49	VSS	EN38	VDDQ_DDR0123	EP25	DDR1_DATA_37
EL64	DDR2_DATA_25	EM51	VDDQ_DDR0123	EN40	VDDQ_DDR0123	EP27	DDR1_CID_0
EL66	DDR2_DATA_19	EM53	VSS	EN42	VSS	EP29	DDR1_CID_2
EL68	DDR2_DSTR_2_P	EM55	VSS	EN44	VDDQ_DDR0123	EP31	DDR1_ADDR_13
EL70	DDR2_DATA_17	EM57	VSS	EN46	VDDQ_DDR0123	EP33	DDR1_CS_N_0
EL72	DDR2_DATA_11	EM59	VSS	EN48	VDDQ_DDR0123	EP35	DDR1_BA_0
EL74	DDR2_DSTR_1_P	EM61	VSS	EN50	VDDQ_DDR0123	EP37	DDR1_PAR
EL76	DDR2_DATA_9	EM63	VSS	EN52	VDDQ_DDR0123	EP39	DDR1_CLK_0_P
EL78	DDR2_DATA_3	EM65	VSS	EN54	VSS	EP41	DDR1_CLK_2_P
EL80	DDR2_DSTR_0_P	EM67	VSS	EN56	VSS	EP43	DDR1_ADDR_1
EL82	DDR2_DATA_1	EM69	VSS	EN58	VSS	EP45	DDR1_ADDR_6
EL84	VSS	EM71	VSS	EN60	VSS	EP47	DDR1_ADDR_9
EM1	VSS	EM73	VSS	EN62	VSS	EP49	DDR1_BG_0
EM3	VSS	EM75	VSS	EN64	VSS	EP51	DDR1_CKE_1
EM5	VSS	EM77	VSS	EN66	VSS	EP53	VSS
EM7	VSS	EM79	VSS	EN68	VSS	EP55	DDR1_DATA_70
EM9	VSS	EM81	VSS	EN70	VSS	EP57	DDR1_DSTR_17_P
EM11	VSS	EM83	VSS	EN72	VSS	EP59	DDR1_DATA_68
EM13	VSS	EN2	VSS	EN74	VSS	EP61	DDR1_DATA_30
EM15	VSS	EN4	VSS	EN76	VSS	EP63	DDR1_DSTR_12_P
EM17	VSS	EN6	VSS	EN78	VSS	EP65	DDR1_DATA_28
EM19	VSS	EN8	VSS	EN80	VSS	EP67	DDR1_DATA_22
EM21	VSS	EN10	VSS	EN82	VSS	EP69	DDR1_DSTR_11_P
EM23	VSS	EN12	VSS	EN84	VSS	EP71	DDR1_DATA_20
EM25	VSS	EN14	VSS	EP1	VSS	EP73	DDR1_DATA_14
EM27	VDDQ_DDR0123	EN16	VSS	EP3	DDR1_DATA_59	EP75	DDR1_DSTR_10_P
EM29	VSS	EN18	VSS	EP5	DDR1_DSTR_7_N	EP77	DDR1_DATA_12
EM31	VDDQ_DDR0123	EN20	VSS	EP7	DDR1_DATA_61	EP79	DDR1_DATA_6

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 32 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
EP81	DDR1_DSTR_9_P	ER70	DDR1_DATA_16	ET57	VSS	EU46	DDR1_ADDR_8
EP83	DDR1_DATA_4	ER72	DDR1_DATA_10	ET59	VSS	EU48	DDR1_ADDR_12
ER2	DDR1_DATA_58	ER74	DDR1_DSTR_10_N	ET61	VSS	EU50	DDR1_ACT_N
ER4	DDR1_DSTR_7_P	ER76	DDR1_DATA_8	ET63	VSS	EU52	DDR1_CKE_3
ER6	DDR1_DATA_57	ER78	DDR1_DATA_2	ET65	VSS	EU54	DDR1_DATA_67
ER8	DDR1_DATA_51	ER80	DDR1_DSTR_9_N	ET67	VSS	EU56	DDR1_DSTR_8_P
ER10	DDR1_DSTR_6_P	ER82	DDR1_DATA_5	ET69	VSS	EU58	DDR1_DATA_65
ER12	DDR1_DATA_49	ER84	VSS	ET71	VSS	EU60	DDR1_DATA_27
ER14	DDR1_DATA_43	ET1	VSS	ET73	VSS	EU62	DDR1_DSTR_3_P
ER16	DDR1_DSTR_5_P	ET3	VSS	ET75	VSS	EU64	DDR1_DATA_25
ER18	DDR1_DATA_41	ET5	VSS	ET77	VSS	EU66	DDR1_DATA_19
ER20	DDR1_DATA_35	ET7	VSS	ET79	VSS	EU68	DDR1_DSTR_2_P
ER22	DDR1_DSTR_4_P	ET9	VSS	ET81	VSS	EU70	DDR1_DATA_17
ER24	DDR1_DATA_33	ET11	VSS	ET83	VSS	EU72	DDR1_DATA_11
ER26	DDR1_ATB1	ET13	VSS	EU2	DDR1_DATA_63	EU74	DDR1_DSTR_1_P
ER28	DDR1_ODT_1	ET15	VSS	EU4	DDR1_DSTR_16_N	EU76	DDR1_DATA_9
ER30	DDR1_CS_N_3	ET17	VSS	EU6	DDR1_DATA_56	EU78	DDR1_DATA_3
ER32	DDR1_ODT_0	ET19	VSS	EU8	DDR1_DATA_50	EU80	DDR1_DSTR_0_P
ER34	DDR1_ADDR_14_WE_N	ET21	VSS	EU10	DDR1_DSTR_15_N	EU82	DDR1_DATA_0
ER36	DDR1_BA_1	ET23	VSS	EU12	DDR1_DATA_48	EU84	VSS
ER38	DDR1_CLK_0_N	ET25	VSS	EU14	DDR1_DATA_42	EV1	VSS
ER40	DDR1_CLK_2_N	ET27	VDDQ_DDR0123	EU16	DDR1_DSTR_14_N	EV3	DDR1_DATA_62
ER42	VDDQ_DDR0123	ET29	VDDQ_DDR0123	EU18	DDR1_DATA_40	EV5	DDR1_DSTR_16_P
ER44	DDR1_ADDR_4	ET31	VDDQ_DDR0123	EU20	DDR1_DATA_34	EV7	DDR1_DATA_60
ER46	DDR1_ADDR_7	ET33	VDDQ_DDR0123	EU22	DDR1_DSTR_13_N	EV9	DDR1_DATA_54
ER48	DDR1_ALERT_N	ET35	VDDQ_DDR0123	EU24	DDR1_DATA_32	EV11	DDR1_DSTR_15_P
ER50	DDR1_CKE_0	ET37	VDDQ_DDR0123	EU26	DDR1_ATB0	EV13	DDR1_DATA_52
ER52	DDR1_RESETN	ET39	VDDQ_DDR0123	EU28	DDR1_ODT_3	EV15	DDR1_DATA_46
ER54	DDR1_DATA_66	ET41	VDDQ_DDR0123	EU30	DDR1_CS_N_1	EV17	DDR1_DSTR_14_P
ER56	DDR1_DSTR_17_N	ET43	VDDQ_DDR0123	EU32	DDR1_ADDR_15_CAS_N	EV19	DDR1_DATA_44
ER58	DDR1_DATA_64	ET45	VDDQ_DDR0123	EU34	DDR1_ADDR_16_RAS_N	EV21	DDR1_DATA_38
ER60	DDR1_DATA_26	ET47	VDDQ_DDR0123	EU36	DDR1_ADDR_0	EV23	DDR1_DSTR_13_P
ER62	DDR1_DSTR_12_N	ET49	VDDQ_DDR0123	EU38	DDR1_CLK_1_P	EV25	DDR1_DATA_36
ER64	DDR1_DATA_24	ET51	VDDQ_DDR0123	EU40	DDR1_CLK_3_P	EV27	DDR1_CID_1
ER66	DDR1_DATA_18	ET53	VSS	EU42	VDDQ_DDR0123	EV29	DDR1_ADDR_17
ER68	DDR1_DSTR_11_N	ET55	VSS	EU44	DDR1_ADDR_3	EV31	DDR1_ODT_2

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 33 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
EV33	DDR1_CS_N_2	EW22	VSS	EY9	VSS	EY81	VSS
EV35	DDR1_ADDR_10	EW24	VSS	EY11	VSS	EY83	VSS
EV37	DDR1_CLK_1_N	EW26	VSS	EY13	VSS	FA2	DDR0_DATA_59
EV39	DDR1_CLK_3_N	EW28	VDDQ_DDR0123	EY15	VSS	FA4	DDR0_DSTR_7_P
EV41	VDDQ_DDR0123	EW30	VDDQ_DDR0123	EY17	VSS	FA6	DDR0_DATA_57
EV43	DDR1_ADDR_2	EW32	VDDQ_DDR0123	EY19	VSS	FA8	DDR0_DATA_51
EV45	DDR1_ADDR_5	EW34	VDDQ_DDR0123	EY21	VSS	FA10	DDR0_DSTR_6_P
EV47	DDR1_ADDR_11	EW36	VDDQ_DDR0123	EY23	VSS	FA12	DDR0_DATA_49
EV49	DDR1_BG_1	EW38	VDDQ_DDR0123	EY25	VSS	FA14	DDR0_DATA_43
EV51	DDR1_CKE_2	EW40	VDDQ_DDR0123	EY27	VDDQ_DDR0123	FA16	DDR0_DSTR_5_P
EV53	VSS	EW42	VSS	EY29	VSS	FA18	DDR0_DATA_41
EV55	DDR1_DATA_71	EW44	VDDQ_DDR0123	EY31	VDDQ_DDR0123	FA20	DDR0_DATA_35
EV57	DDR1_DSTR_8_N	EW46	VDDQ_DDR0123	EY33	VSS	FA22	DDR0_DSTR_4_P
EV59	DDR1_DATA_69	EW48	VDDQ_DDR0123	EY35	VDDQ_DDR0123	FA24	DDR0_DATA_33
EV61	DDR1_DATA_31	EW50	VDDQ_DDR0123	EY37	VSS	FA26	DDR0_ATB1
EV63	DDR1_DSTR_3_N	EW52	VDDQ_DDR0123	EY39	VDDQ_DDR0123	FA28	DDR0_CID_1
EV65	DDR1_DATA_29	EW54	VSS	EY41	VSS	FA30	DDR0_ADDR_17
EV67	DDR1_DATA_23	EW56	VSS	EY43	VSS	FA32	DDR0_ODT_2
EV69	DDR1_DSTR_2_N	EW58	VSS	EY45	VSS	FA34	DDR0_CS_N_2
EV71	DDR1_DATA_21	EW60	VSS	EY47	VDDQ_DDR0123	FA36	DDR0_ADDR_10
EV73	DDR1_DATA_15	EW62	VSS	EY49	VSS	FA38	VSS
EV75	DDR1_DSTR_1_N	EW64	VSS	EY51	VDDQ_DDR0123	FA40	VDDQ_DDR0123
EV77	DDR1_DATA_13	EW66	VSS	EY53	VSS	FA42	DDR0_CLK_2_P
EV79	DDR1_DATA_7	EW68	VSS	EY55	VSS	FA44	DDR0_ADDR_4
EV81	DDR1_DSTR_0_N	EW70	VSS	EY57	VSS	FA46	DDR0_ADDR_7
EV83	DDR1_DATA_1	EW72	VSS	EY59	VSS	FA48	DDR0_ALERT_N
EW2	VSS	EW74	VSS	EY61	VSS	FA50	DDR0_CKE_0
EW4	VSS	EW76	VSS	EY63	VSS	FA52	DDR0_RESETN
EW6	VSS	EW78	VSS	EY65	VSS	FA54	DDR0_DATA_71
EW8	VSS	EW80	VSS	EY67	VSS	FA56	DDR0_DSTR_17_N
EW10	VSS	EW82	VSS	EY69	VSS	FA58	DDR0_DATA_69
EW12	VSS	EW84	VSS	EY71	VSS	FA60	DDR0_DATA_31
EW14	VSS	EY1	VSS	EY73	VSS	FA62	DDR0_DSTR_12_N
EW16	VSS	EY3	VSS	EY75	VSS	FA64	DDR0_DATA_29
EW18	VSS	EY5	VSS	EY77	VSS	FA66	DDR0_DATA_23
EW20	VSS	EY7	VSS	EY79	VSS	FA68	DDR0_DSTR_11_N

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 34 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
FA70	DDR0_DATA_21	FB57	DDR0_DSTR_17_P	FC46	VDDQ_DDR0123	FD33	DDR0_ADDR_14_WE_N
FA72	DDR0_DATA_15	FB59	DDR0_DATA_68	FC48	VDDQ_DDR0123	FD35	DDR0_BA_1
FA74	DDR0_DSTR_10_N	FB61	DDR0_DATA_30	FC50	VDDQ_DDR0123	FD37	DDR0_CLK_1_N
FA76	DDR0_DATA_13	FB63	DDR0_DSTR_12_P	FC52	VDDQ_DDR0123	FD39	DDR0_CLK_0_N
FA78	DDR0_DATA_7	FB65	DDR0_DATA_28	FC54	VSS	FD41	DDR0_CLK_3_N
FA80	DDR0_DSTR_9_N	FB67	DDR0_DATA_22	FC56	VSS	FD43	DDR0_ADDR_2
FA82	DDR0_DATA_4	FB69	DDR0_DSTR_11_P	FC58	VSS	FD45	DDR0_ADDR_5
FA84	VSS	FB71	DDR0_DATA_20	FC60	VSS	FD47	DDR0_ADDR_11
FB1	DDR0_DATA_63	FB73	DDR0_DATA_14	FC62	VSS	FD49	DDR0_BG_1
FB3	DDR0_DATA_58	FB75	DDR0_DSTR_10_P	FC64	VSS	FD51	DDR0_CKE_2
FB5	DDR0_DSTR_7_N	FB77	DDR0_DATA_12	FC66	VSS	FD53	VSS
FB7	DDR0_DATA_56	FB79	DDR0_DATA_6	FC68	VSS	FD55	DDR0_DATA_66
FB9	DDR0_DATA_50	FB81	DDR0_DSTR_9_P	FC70	VSS	FD57	DDR0_DSTR_8_N
FB11	DDR0_DSTR_6_N	FB83	DDR0_DATA_5	FC72	VSS	FD59	DDR0_DATA_64
FB13	DDR0_DATA_48	FC2	VSS	FC74	VSS	FD61	DDR0_DATA_26
FB15	DDR0_DATA_42	FC4	VSS	FC76	VSS	FD63	DDR0_DSTR_3_N
FB17	DDR0_DSTR_5_N	FC6	VSS	FC78	VSS	FD65	DDR0_DATA_24
FB19	DDR0_DATA_40	FC8	VSS	FC80	VSS	FD67	DDR0_DATA_18
FB21	DDR0_DATA_34	FC10	VSS	FC82	VSS	FD69	DDR0_DSTR_2_N
FB23	DDR0_DSTR_4_N	FC12	VSS	FC84	VSS	FD71	DDR0_DATA_16
FB25	DDR0_DATA_32	FC14	VSS	FD1	#	FD73	DDR0_DATA_10
FB27	DDR0_CID_0	FC16	VSS	FD3	DDR0_DATA_62	FD75	DDR0_DSTR_1_N
FB29	DDR0_CID_2	FC18	VSS	FD5	DDR0_DSTR_16_P	FD77	DDR0_DATA_8
FB31	DDR0_ADDR_13	FC20	VSS	FD7	DDR0_DATA_60	FD79	DDR0_DATA_2
FB33	DDR0_CS_N_0	FC22	VSS	FD9	DDR0_DATA_54	FD81	DDR0_DSTR_0_N
FB35	DDR0_BA_0	FC24	VSS	FD11	DDR0_DSTR_15_P	FD83	DDR0_DATA_0
FB37	DDR0_PAR	FC26	VSS	FD13	DDR0_DATA_52	FE2	#
FB39	VDDQ_DDR0123	FC28	VDDQ_DDR0123	FD15	DDR0_DATA_46	FE4	DDR0_DSTR_16_N
FB41	DDR0_CLK_2_N	FC30	VDDQ_DDR0123	FD17	DDR0_DSTR_14_P	FE6	DDR0_DATA_61
FB43	DDR0_ADDR_3	FC32	VDDQ_DDR0123	FD19	DDR0_DATA_44	FE8	DDR0_DATA_55
FB45	DDR0_ADDR_8	FC34	VDDQ_DDR0123	FD21	DDR0_DATA_38	FE10	DDR0_DSTR_15_N
FB47	DDR0_ADDR_12	FC36	VDDQ_DDR0123	FD23	DDR0_DSTR_13_P	FE12	DDR0_DATA_53
FB49	DDR0_ACT_N	FC38	VDDQ_DDR0123	FD25	DDR0_DATA_36	FE14	DDR0_DATA_47
FB51	DDR0_CKE_3	FC40	VDDQ_DDR0123	FD27	DDR0_ODT_1	FE16	DDR0_DSTR_14_N
FB53	VSS	FC42	VDDQ_DDR0123	FD29	DDR0_CS_N_3	FE18	DDR0_DATA_45
FB55	DDR0_DATA_70	FC44	VDDQ_DDR0123	FD31	DDR0_ODT_0	FE20	DDR0_DATA_39

Table 5: Pin Assignment – Sorted by Pin Number (Sheet 35 of 35)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
FE22	DDR0_DSTR_13_N	FE60	DDR0_DATA_27	FF13	VSS	FF51	VDDQ_DDR0123
FE24	DDR0_DATA_37	FE62	DDR0_DSTR_3_P	FF15	VSS	FF53	VSS
FE26	DDR0_ATB0	FE64	DDR0_DATA_25	FF17	VSS	FF55	VSS
FE28	DDR0_ODT_3	FE66	DDR0_DATA_19	FF19	VSS	FF57	VSS
FE30	DDR0_CS_N_1	FE68	DDR0_DSTR_2_P	FF21	VSS	FF59	VSS
FE32	DDR0_ADDR_15_CAS_N	FE70	DDR0_DATA_17	FF23	VSS	FF61	VSS
FE34	DDR0_ADDR_16_RAS_N	FE72	DDR0_DATA_11	FF25	VSS	FF63	VSS
FE36	DDR0_ADDR_0	FE74	DDR0_DSTR_1_P	FF27	VDDQ_DDR0123	FF65	VSS
FE38	DDR0_CLK_1_P	FE76	DDR0_DATA_9	FF29	VSS	FF67	VSS
FE40	DDR0_CLK_0_P	FE78	DDR0_DATA_3	FF31	VDDQ_DDR0123	FF69	VSS
FE42	DDR0_CLK_3_P	FE80	DDR0_DSTR_0_P	FF33	VSS	FF71	VSS
FE44	DDR0_ADDR_1	FE82	DDR0_DATA_1	FF35	VDDQ_DDR0123	FF73	VSS
FE46	DDR0_ADDR_6	FE84	#	FF37	VSS	FF75	VSS
FE48	DDR0_ADDR_9	FF1	#	FF39	VDDQ_DDR0123	FF77	VSS
FE50	DDR0_BG_0	FF3	#	FF41	VSS	FF79	VSS
FE52	DDR0_CKE_1	FF5	VSS	FF43	VSS	FF81	VSS
FE54	DDR0_DATA_67	FF7	VSS	FF45	VSS	FF83	#
FE56	DDR0_DSTR_8_P	FF9	VSS	FF47	VDDQ_DDR0123	–	–
FE58	DDR0_DATA_65	FF11	VSS	FF49	VSS	–	–

6. Signal Descriptions

The Altra processor is packaged in a 4926-pin Flip-Chip Land Grid Array (FCLGA) package. The table in this section describes the package-level pinout.

Table 6: Pin Summary

GROUP	NUMBER OF PINS
Total Signal Pins (A)	1960
Total Power Pins (including Ground pins) (B)	2927
Reserved Pins (RFU) (C)	39
Total Pins on the Package (A+B+C)	**4926**

In *Table 7 on page 54*, each I/O signal is listed along with a short description of its function.

Note that:

1. Active low signals (for example, “DDR0_RESETN”) are labeled with the suffix “N”.
2. Differential signals, such as “DDR0_DSTR_0_P” and “DDR0_DSTR_0_N”, and “PCIERCA0_RX0_P” and “PCIERCA0_RX0_M” represent true and complement signals, respectively, of the differential pair.
3. Grouped signals, such as “DDR[0:7]_RESETN” represent the same signal on 8 different DDR4 channels ([0:7]). Thus, this convention represents eight different signals: DDR0_RESETN, DDR1_RESETN, DDR2_RESETN, DDR3_RESETN, ..., DDR7_RESETN.

6.1. Reserved Pins

The following pins are marked Reserved on this chip: AK26, AL27, AL35, AM34, AM36, AN33, AP34, AP36, AT34, AT36, AT38, AT40, AU33, AU35, AU37, AU39, AW31, AY30, DG30, DG40, DG42, DH31, DH41, DK35, DK37, DK39, DL34, DL36, DL40, DN40, DP39, DR44, DR46, DR48, DT27, DT45, DT47, DU26, DU48.

These pins are non-functional and must be left unconnected.

6.2. Signal Functional Descriptions

Table 7: Signal Descriptions (Sheet 1 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
DDR4 Interface Signals				
DDR[0:7]_ACT_N	8	O	1.5 V Stub Series Terminated Logic (SSTL)/1.2 V Pseudo Open Drain (POD)	Port Activate (open row) signal. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_ADDR_[0:13]	112	O	1.5 V SSTL/1.2 V POD	Port address signals [0:13]. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_ADDR_14_WE_N	8	O	1.5 V SSTL/1.2 V POD	Port address signal [14] shared with Write Enable. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_ADDR_15_CAS_N	8	O	1.5 V SSTL/1.2 V POD	Port address signal [15] shared with Column Address Strobe. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_ADDR_16_RAS_N	8	O	1.5 V SSTL/1.2 V POD	Port address signal [16] shared with Row Address Strobe. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_ADDR_17	8	O	1.5 V SSTL/1.2 V POD	Port address signal [17]. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_ALERT_N	8	I	1.5 V SSTL/1.2 V POD	Port parity error checking signals. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_ATB[0:1]	16	I/O	1.5 V SSTL/1.2 V POD	DDR PHY I/O Pad Analog Test Bus signals.
DDR[0:7]_BA_[0:1]	16	O	1.5 V SSTL/1.2 V POD	Bank Address select signals. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_BG_[0:1]	16	O	1.5 V SSTL/1.2 V POD	Bank Group Address select signals. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_CID_[0:2]	24	O	1.5 V SSTL/1.2 V POD	Chip ID (CID) signals (differential pair). Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_CKE_[0:3]	32	O	1.5 V SSTL/1.2 V POD	Clock enable signals. Maximum frequency 1600 MHz. Do not connect if unused.

Table 7: Signal Descriptions (Sheet 2 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
DDR[0:7]_CLK_[0:3]_P	32	O	1.5 V SSTL/1.2 V POD	DDR clock output – positive phase (differential pair). Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_CLK_[0:3]_N	32	O	1.5 V SSTL/1.2 V POD	DDR clock output – negative phase (differential pair). Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_CS_N_[0:3]	32	O	1.5 V SSTL/1.2 V POD	DDR Chip Select signals. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_DATA_[0:71]	576	I/O	1.5 V SSTL/1.2 V POD	DDR data signals. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_DSTR_[0:17]_P	144	I/O	1.5 V SSTL/1.2 V POD	DDR data strobe signals – positive phase (differential pair). Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_DSTR_[0:17]_N	144	I/O	1.5 V SSTL/1.2 V POD	DDR data strobe signals – negative phase (differential pair). Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_ODT_[0:3]	32	O	1.5 V SSTL/1.2 V POD	DDR On-Die Termination signals. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_PAR	8	O	1.5 V SSTL/1.2 V POD	DDR address parity check signals. Maximum frequency 1600 MHz. Do not connect if unused.
DDR[0:7]_PLL_TESTOUT_N	8	O	1.5 V SSTL/1.2 V POD	DDR PLL PHY Clock test points for de-skew – negative phase.
DDR[0:7]_PLL_TESTOUT_P	8	O	1.5 V SSTL/1.2 V POD	DDR PLL PHY Clock test points for de-skew – positive phase.
DDR[0:7]_RESETN	8	O	1.5 V SSTL/1.2 V POD	DDR port reset signals. Do not connect if unused.
EFUSEs				
EFUSE_MFG_VDDQ1P8	1	I	Supply	1.8 V supply for the MFG (Manufacturing) EFUSE array. Pull down to VSS if unused.
EFUSE_PCP_VDDQ1P8	1	I	Supply	1.8 V supply for the PCP EFUSE array. Pull down to VSS if unused.
EFUSE_SOC_VDDQ1P8	1	I	Supply	1.8 V supply for the SoC EFUSE array. Pull down to VSS if unused.
EFUSE_TMM_VDDQ1P8	1	I	Supply	1.8 V supply for the TMM EFUSE array. Pull down to VSS if unused.

Table 7: Signal Descriptions (Sheet 3 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
GPIO Interfaces				
GPI_[0:7]	8	I	3.3 V LVCMOS, No PU/PD CMOS Input Mode	General purpose inputs. Maximum load 50 pF. Maximum frequency 10 MHz. Pull down to VSS if unused.
GPIO_[0:23]	24	I/O	3.3 V LVCMOS, Slow/4 mA No PU/PD, CMOS Input Mode	General purpose inputs/outputs. Maximum load 50 pF. Maximum frequency 10 MHz. Pull down to VSS if unused.
GPIO_FAULT	1	O	3.3 V LVCMOS, Slow/4 mA	Used by the SMPro firmware to indicate a fault via an LED. An output only, but floated during scan mode. Maximum load 50 pF. Maximum frequency 10 MHz.
CPU Temperature Monitoring Signals				
HIGHTEMP_N	1	I/O	3.3 V LVCMOS, Slow/4 mA No PU/PD, CMOS Input Mode	Open drain Input/Output which indicates that the maximum operating temperature has been reached. Maximum load 50 pF. Maximum frequency 10 MHz.
OVERTEMP_N	1	O	3.3 V LVCMOS, Slow/4 mA	An output indicating that the critical temperature has been reached and the CPU must be powered off. Maximum load 50 pF. Maximum frequency 10 MHz.
Eleven I^2C Interfaces				
ALERT[2:10]_N	9	I/O	3.3 V LVCMOS, Slow/16 mA, No PU/PD, Schmitt Input Mode	Tri-state output. Maximum load 150 pF. Maximum frequency 1 MHz.
IIC_SCL_[0:10]	11	I/O	3.3 V LVCMOS, Slow/16 mA, No PU/PD, Schmitt Input Mode	I^2C Serial Clock. IIC_SCL_[1] (device address 0x52) is used for bootstrap in master mode only. Tri-state output. Maximum load 150 pF. Maximum frequency 1 MHz.
IIC_SDA_[0:10]	11	I/O	3.3 V LVCMOS, Slow/16 mA, No PU/PD, Schmitt Input Mode	I^2C Serial Data. IIC_SDA_[1] (device address 0x52) is used for bootstrap in master mode only. Tri-state output. Maximum load 150 pF. Maximum frequency 1 MHz.
PMALERT_N	1	I/O	3.3 V LVCMOS, Slow/16 mA, No PU/PD, Schmitt Input Mode	PMBus Alert (active low). Shared alert signal for PMBus. I^2C1 master port is used as the PMBus master. Tri-state output. Maximum load 150 pF. Maximum frequency 1 MHz.

Table 7: Signal Descriptions (Sheet 4 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
SoC DAP (Debug Access Port) JTAG Interface				
JTAG_DAP_TCK	1	I	1.8 V, No PU/PD	Test Clock. Pull down to VSS if unused. Maximum load 60 pF. Maximum frequency 25 MHz.
JTAG_DAP_TDI	1	I	1.8 V, No PU/PD	Test Data In. Do not connect if unused. Maximum load 60 pF. Maximum frequency 50 MHz.
JTAG_DAP_TDO	1	O	1.8 V 8 mA	Test Data Output. Do not connect if unused. Maximum frequency 50 MHz.
JTAG_DAP_TMS	1	I	1.8 V, No PU/PD	Test Mode Select. Do not connect if unused. Maximum load 60 pF. Maximum frequency 25 MHz.
JTAG_DAP_TRSTN	1	I	1.8 V	Test Reset. This signal is used to reset all internal JTAG test controller logic. Maximum load 60 pF.
TRIGIN[0:3]	4	I	3.3 V LVCMOS, No PU/PD Schmitt Input Mode	Trigger In. Maximum frequency 75 MHz.
TRIGOUT[0:3]	4	O	3.3 V LVCMOS, Fast/16 mA	Trigger Out. Maximum load 30 pF.
SMpro JTAG Interface				
JTAG_IPP_TCK	1	I	1.8 V, No PU/PD	Test Clock. Pull down to VSS if unused. Maximum load 60 pF. Maximum frequency 25 MHz.
JTAG_IPP_TDI	1	I	1.8 V, No PU/PD	Test Data In. Do not connect if unused. Maximum load 60 pF. Maximum frequency 50 MHz.
JTAG_IPP_TDO	1	O	1.8 V 8 mA	Test Data Out. Do not connect if unused. Maximum frequency 50 MHz.
JTAG_IPP_TMS	1	I	1.8 V, No PU/PD	Test Mode Select. Do not connect if unused. Maximum load 60 pF. Maximum frequency 25 MHz.
JTAG_IPP_TRSTN	1	I	1.8 V, No PU/PD	Test Reset. Maximum load 60 pF.
PMpro JTAG Interface				
JTAG_PM_TCK	1	I	1.8 V, No PU/PD	Test Clock. Pull down to VSS if unused. Maximum load 60 pF. Maximum frequency 25 MHz.
JTAG_PM_TDI	1	I	1.8 V, No PU/PD	Test Data Input. Do not connect if unused. Maximum load 60 pF. Maximum frequency 50 MHz.

Table 7: Signal Descriptions (Sheet 5 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
JTAG_PM_TDO	1	O	1.8 V 8 mA	Test Data Output. Do not connect if unused. Maximum frequency 50 MHz.
JTAG_PM_TMS	1	I	1.8 V, No PU/PD	Test Mode Select. Do not connect if unused. Maximum load 60 pF.
JTAG_PM_TRSTN	1	I	1.8 V, No PU/PD	Test Reset. This signal is used to reset all internal JTAG test controller logic. Maximum load 60 pF.
SoC DFT JTAG Interface				
JTAG_CMPL[0:2]	3	I	1.8 V, Internal PD	JTAG Boundary Scan Option Select. Do not connect if unused.
JTAG_SELECT[0:3]	4	I	1.8 V, No PU/PD	JTAG Select, internal pull-up. Maximum frequency 25 MHz. Maximum load 60 pF.
JTAG_SOC_TCK	1	I	1.8 V, No PU/PD	Test Clock. Pull down to VSS if unused. Maximum load 60 pF. Maximum frequency 25 MHz.
JTAG_SOC_TDI	1	I	1.8 V, No PU/PD	Test Data Input. Maximum frequency 50 MHz.
JTAG_SOC_TDO	1	O	1.8 V 8 mA, No PU/PD	Test Data Output. Do not connect if unused. Maximum load 60 pF. Maximum frequency 50 MHz.
JTAG_SOC_TMS	1	I	1.8 V, No PU/PD	Test Mode Select. Maximum load 60 pF. Maximum frequency 25 MHz.
JTAG_SOC_TRSTN	1	I	1.8 V, No PU/PD	Test Reset. This signal is used to reset all internal JTAG test controller logic and TSRSTN and SYS_RST_N on die. Maximum load 60 pF.
DFT Interface				
ISOLATE_DIS[0:1]	2	I	1.8 V, Internal PD	Power Domain Isolation Disable. Do not connect if unused.
SCAN_EN	1	I	1.8 V, Internal PD	Enable Scan Test. Pull down to VSS if unused. Maximum frequency 50 MHz.
WSCAN_ENI	1	I	1.8 V, No PU/PD	Wrapper Scan Chain Enable Input. Pull down to VSS if unused.
WSCAN_ENO	1	I	1.8 V, No PU/PD	Wrapper Scan Chain Enable Output. Pull down to VSS if unused.

Table 7: Signal Descriptions (Sheet 6 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
PCIe Gen4 Root Complex A[0:3] which may each be configured as: • One dual-mode x16 PCIe/ESM CCIX controller, or • Two x8 PCIe interfaces, or • One x8 and two x4 PCIe interfaces, or • Four x4 PCIe interfaces				
PCIERCA[0:3]_RX[0:15]_P	64	I	CML 4 mA	PCIe Root Complex A[0:3] receive data (differential signals). Do not connect if unused. Maximum frequency 8000 MHz.
PCIERCA[0:3]_RX[0:15]_M	64	I	CML 4 mA	
PCIERCA[0:3]_TX[0:15]_P	64	O	CML 4 mA	PCIe Root Complex A[0:3] transmit data (differential signals). Do not connect if unused. Maximum frequency 8000 MHz.
PCIERCA[0:3]_TX[0:15]_M	64	O	CML 4 mA	
PCIe Gen4 Root Complex consisting of B[0:3]A and B[0:3]B which may each be configured as: • One Root Port mode x8 PCIe interface, or • Two Root Port mode x4 PCIe interfaces, or • One x4 and two x2 PCIe interfaces, or • Four Root Port mode x2 PCIe interfaces				
PCIERCB[0:3]A_RX[0:7]_P	32	I	CML 4 mA	PCIe Root Complex B[0:3]A receive data (differential signals). Do not connect if unused. Maximum frequency 8000 MHz.
PCIERCB[0:3]A_RX[0:7]_M	32	I	CML 4 mA	
PCIERCB[0:3]A_TX[0:7]_P	32	O	CML 4 mA	PCIe Root Complex B[0:3]A transmit data (differential signals). Do not connect if unused. Maximum frequency 8000 MHz.
PCIERCB[0:3]A_TX[0:7]_M	32	O	CML 4 mA	
PCIERCB[0:3]B_RX[0:7]_P	32	I	CML 4 mA	PCIe Root Complex B[0:3]B receive data (differential signals). Do not connect if unused. Maximum frequency 8000 MHz.
PCIERCB[0:3]B_RX[0:7]_M	32	I	CML 4 mA	
PCIERCB[0:3]B_TX[0:7]_P	32	O	CML 4 mA	PCIe Root Complex B[0:3]B transmit data (differential signals). Do not connect if unused. Maximum frequency 8000 MHz.
PCIERCB[0:3]B_TX[0:7]_M	32	O	CML 4 mA	

Table 7: Signal Descriptions (Sheet 7 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
QSPI Interfaces				
SPI[0:1]_CLK	2	O	3.3 V LVCMOS, Fast/16 mA	Serial clock. Do not connect if unused. Maximum load 45 pF. Maximum frequency 33 MHz.
SPI[0:1]_CS[0:2]	6	O	3.3 V LVCMOS, Fast/16 mA	Slave/Chip Select. Do not connect if unused. Maximum load 45 pF. Maximum frequency 33 MHz.
SPI[0:1]_IO[0:3]	8	I/O	3.3 V LVCMOS, Fast/16 mA No PU/PD, CMOS Input Mode	Serial data input/output. Pull down to VSS if unused. Maximum load 45 pF. Maximum frequency 33 MHz.
UART0 / UART1 / UART2 / UART3 / UART4 Interfaces				
UART_CTS0	1	I	3.3 V LVCMOS, No PU/PD CMOS Input Mode	Clear to Send. Maximum load 32 pF.
UART_RTS0	1	O	3.3 V LVCMOS, Slow/4 mA	Request to Send. Do not connect if unused. Maximum load 32 pF. Maximum frequency 250 kHz.
UART_SCLK	1	I	3.3 V LVCMOS, No PU/PD CMOS Input Mode	Serial clock. Maximum load 32 pF.
UART_SIN[0:4]	5	I	3.3 V LVCMOS, No PU/PD CMOS Input Mode	Serial data in. Maximum load 32 pF.
UART_SOUT[0:4]	5	O	3.3 V LVCMOS, Slow/4 mA	Serial data out. Do not connect if unused. Maximum load 32 pF. Maximum frequency 250 kHz.
Reference Clocks, Resets, and Power Controls				
CLK_MON_OUT	1	O	3.3 V LVCMOS, Slow/4 mA	Clock monitor output. Maximum load 30 pF. Maximum frequency 1 MHz.
MPA_TEST_RSTN	1	I	1.8 V LVCMOS	SMpro Test Reset. Maximum frequency 1 MHz.
PCP_PWRCTL	1	O	3.3 V LVCMOS, Slow/4 mA	PCP power control: Drives low to power-down SoC power domain. Maximum load 30 pF. Maximum frequency 1 MHz.
PCP_PWRGD	1	I	3.3 V LVCMOS, No PU/PD Schmitt Input Mode	PCP domain PowerGood indicator. Maximum frequency 1 MHz.
REF_TESTCLK	1	I	1.8 V, Internal PD	Reference Test Clock. Pull down to VSS if unused.
SOC_PWRGD	1	I	3.3 V LVCMOS, No PU/PD Schmitt Input Mode	SoC domain PowerGood indicator. Maximum frequency 1 MHz.

Table 7: Signal Descriptions (Sheet 8 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
SYS_REFCLK_SRIS_P	1	I	0.75 V CML	100 MHz primary system reference clock with spread-spectrum clocking (SSC) (Differential signals). Maximum frequency 100 MHz.
SYS_REFCLK_SRIS_N	1	I	0.75 V CML	
SYS_REFCLK_SRNS_P	1	I	0.75 V CML	100 MHz primary system reference clock with non spread-spectrum clocking (SSC). (Differential signals). Maximum frequency 100 MHz.
SYS_REFCLK_SRNS_N	1	I	0.75 V CML	
SYS_RESETN	1	I	3.3 V LVCMOS, No PU/PD Schmitt Input Mode	System Reset. External logic must drive this pin low (for a minimum of 10 µs) to initiate a System Reset. A System Reset can also be initiated by software. Must be terminated if unused. Maximum frequency 1 MHz.
SYS_TS_AN_IO_[0:1]	2	I/O	1.8 V Analog	Debug pins for Ampere internal use only. Must be pulled down to VSS.
TMR_CLK	1	I	3.3 V LVCMOS, No PU/PD CMOS Input Mode	25 MHz Timer Clock.
TMR_RSTN	1	I/O	3.3 V LVCMOS, No PU/PD CMOS Input Mode	Timer Reset.
Power Supply Signals				
VDD18_DDR_AVDD	3	I	Supply	1.8 V analog supply rail for DDR.
VDD18_PCP_AVDD	6	I	Supply	1.8 V analog supply rail for PCP.
VDD18_SERDES_AVDD	3	I	Supply	1.8 V analog supply rail for SerDes.
VDD18_SOC	2	I	Supply	1.8 V supply rails for SoC domain.
VDD33_SOC	5	I	Supply	3.3 V supply rails for SoC domain.
VDDC_PCP	376	I	Supply	0.75 V – 1.232 V$^{\Psi}$ PCP domain core supply rail.
				0.75 V – 1.21 V$^{\Psi}$ PCP domain core supply rail.
$^{\Psi}$**Note**: For SKUs with a frequency of 3.3 GHz, the VDDC_PCP range is 0.75 V to 1.232 V. For SKUs with a frequency of 3.0 GHz or lower the VDDC_PCP range is 0.75 V to 1.21 V.				
VDDC_PCP_SENSE_P	1	O	Supply	Remote sense points for VDDC_PCP (differential signals).
VDDC_PCP_SENSE_N	1	O	Supply	

Table 7: Signal Descriptions (Sheet 9 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
VDDC_RCA[0:3]‡	20	I	Supply	0.90 V CCIX Root Complex A core supply rails. Do not connect if unused.
VDDC_RCB[0:3]‡	8	I	Supply	0.75 V PCIe Root Complex B core supply rails.
VDDC_SOC	28	I	Supply	0.75 V SoC domain core supply rail.
VDDC_SOC_CLKBUFF_AVDD‡	1	I	Supply	0.75 V SoC clock buffer supply rail.
‡**Note**: Voltages listed are for device package balls. VDDC_RCA[0:3], VDDC_RCB[0:3], and VDDC_SOC_CLKBUFF_AVDD supplies need a ferrite bead filter for isolation. Refer to the Ampere reference platform's design for details on how to connect the ferrite bead.				
VDDC_SOC_SENSE_P	1	O	Supply	Remote sense points for VDDC_SOC (differential signals).
VDDC_SOC_SENSE_N	1	O	Supply	
VDDH_RCA[0:3]	12	I	Supply	Supply rails for CCIX Root Complex A: • 1.5 V for data transfer rates ≤ 16 Gbps • 1.8 V for data transfer rates > 16 Gbps Do not connect if unused.
VDDH_RCB[0:3]	8	I	Supply	1.5 V PCIe Root Complex B supply rails.
VDDQ_DDR0123	129	I	Supply	1.2 V DDR[0:3] supply rails.
VDDQ_DDR4567	129	I	Supply	1.2 V DDR[4:7] supply rails.
VDDQ_DDR01_SENSE_P	1	O	Supply	Remote sense points for VDDQ for DDR01 (differential signals).
VDDQ_DDR01_SENSE_N	1	O	Supply	
VDDQ_DDR23_SENSE_P	1	O	Supply	Remote sense points for VDDQ for DDR23 (differential signals).
VDDQ_DDR23_SENSE_N	1	O	Supply	
VDDQ_DDR45_SENSE_P	1	O	Supply	Remote sense points for VDDQ for DDR45 (differential signals).
VDDQ_DDR45_SENSE_N	1	O	Supply	
VDDQ_DDR67_SENSE_P	1	O	Supply	Remote sense points for VDDQ for DDR67 (differential signals).
VDDQ_DDR67_SENSE_N	1	O	Supply	
PQT_VDM_EXTVREF	1	I	Supply	Core power (VDDC_PCP) voltage droop detection.
VSS	2121	I	Ground	Reference ground for the device.

Table 7: Signal Descriptions (Sheet 10 of 10)

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
Miscellaneous Signals				
EDT_UPDATE	1	I/O	1.8V LVCMOS, 8 mA	EDT Update. Pull down to VSS if unused.
MASTER_2P	1	I	3.3 V LVCMOS, No PU/PD CMOS Input Mode	Master Socket Select. Maximum frequency 10 MHz.
SLAVE_PRESENT_N	1	I/O	3.3 V LVCMOS, Slow/4 mA No PU/PD, CMOS Input Mode	Slave Socket Present. Maximum load 50 pF. Maximum frequency 10 MHz.
RFU_[1:39]	39	–	Reserved	Reserved for Future Use.
RFU_D2D#	64	–	Reserved	Reserved for Future Use.
#**Note**: Refer to the application note titled *Altra Platform Forward Compatibility with Altra Max* for the usage of these pins on the board/platform.				
TEST_TMM_ENABLE	1	I	1.8 V LVCMOS	Enable TMM Test. Pull down to VSS if unused.
Total Pins on the Package	**4926**			

7. Electrical Specifications

7.1. Absolute Maximum Ratings

Caution: *The absolute maximum ratings listed in Table 8 are stress ratings only. Operation beyond these maximum ratings can cause permanent damage to the device. None of the performance specifications contained in this document are guaranteed when operating at these maximum ratings.*

Table 8: Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	VALUE	UNIT	NOTES
Core logic supply voltages	VDDC_PCP	0 to +1.232	V	1, 3
		0 to +1.21		2, 3
	VDDC_SOC	0 to +1.1		3
PCIe Root Complex A[0:3] core voltages	VDDC_RCA0, VDDC_RCA1, VDDC_RCA2, VDDC_RCA3	0 to +1.1		
PCIe Root Complex A[0:3] supply voltages	VDDH_RCA0, VDDH_RCA1, VDDH_RCA2, VDDH_RCA3	0 to +1.98		
PCIe Root Complex B[0:3] core voltages	VDDC_RCB0, VDDC_RCB1, VDDC_RCB2, VDDC_RCB3	0 to +1.1		
PCIe Root Complex B[0:3] supply voltages	VDDH_RCB0, VDDH_RCB1, VDDH_RCB2, VDDH_RCB3	0 to +1.98		
3.3 V I/O supply voltage	VDD33_SOC	0 to +3.63		
1.8 V I/O supply voltages	VDD18_SOC	0 to +1.98		
SoC clock buffer voltage	VDDC_SOC_CLKBUFF_AVDD	0 to +1.1		
DDR4 supply voltage	VDD18_DDR_AVDD	0 to +1.98		
PCP domain supply voltage	VDD18_PCP_AVDD	0 to +1.98		
SerDes supply voltage	VDD18_SERDES_AVDD	0 to +1.98		
DDR4 I/O supply voltages	VDDQ_DDR0123, VDDQ_DDR4567	0 to +1.32		

Notes:
1. Applies to SKUs with a frequency of 3.3 GHz.
2. Applies to SKUs with a frequency of 3.0 GHz or lower.
3. All voltages are DC measurements at the ball of the device, except VDDC_PCP is measured as the voltage difference between VDDC_PCP_SENSE_P and VDDC_PCP_SENSE_N.

7.2. CPU Voltage Identification

The processor sets the voltage regulator to a nominal Voltage Identification set point (VID) at power on reset. Each processor may, at manufacturing time, be produced with unique VID values even within the same SKU (including speed grade). The range of possible VID values that must be supported by the VR, as well as corresponding DC and AC tolerances around the nominal set point, is specified in *Table 9*.

The VID value for a given processor is provided with a resolution of 1 mV. The system designer must account for quantization error in conversion from the provided VID value to the VID code table of the selected VR in order to ensure that the voltage is within the specified DC tolerance range. Note that:

- The VR must be connected to the I^2C0 port. Firmware provides conversion from the provided VID value to the VID code table of the selected VR. Refer to the document titled *Altra Platform Hardware Design Specification* for the list of supported VRs.
- The VR must support a default (boot) VID of 750 mV.

8. Recommended Operating Conditions

The CPU VRM (VDDC_PCP) must support setting VID within the range of 0.75 V to 1.12 V based on PMBus command from the CPU.

The minimum and maximum voltage values in *Table 9* represent the range of voltage transient undershoot and overshoot allowed at the device package power pins of the respective power domains. These voltage minimum and maximum values represent power delivery noise tolerances to account for both DC and AC load transients with VRM set at the associated nominal set point.

Caution: *Device operation beyond the conditions specified in Table 9 is not recommended. Voltage undershoots or overshoots outside these ranges can affect device performance and/or functionality.*

Table 9: Recommended Operating Conditions (Sheet 1 of 2)

PARAMETER	SYMBOL	MINIMUM	VRM SET POINT NOMINAL	MAXIMUM	UNIT	NOTES
Core logic supply voltages	VDDC_PCP	Nominal – 5%	0.75 – 1.12	Nominal + 7%	V	1, 3
		Nominal – 5%	0.75 – 1.1	Nominal + 7%	V	2, 3
	VDDC_SOC	0.713	0.75	0.788	V	3
Core power voltage droop detection.	PQT_VDM_EXTVREF	0.7522	0.756	0.7598	V	3
SoC clock buffer voltage	VDDC_SOC_CLKBUFF_AVDD	0.713	0.75	0.788	V	3, 10
3.3 V I/O supply voltages	VDD33_SOC	3.135	3.3	3.465	V	4
1.8 V I/O supply voltages	VDD18_SOC	1.71	1.8	1.89	V	4
DDR4 supply voltage	VDD18_DDR_AVDD	1.71	1.8	1.89	V	4
PCP domain supply voltage	VDD18_PCP_AVDD	1.71	1.8	1.89	V	4
SerDes supply voltage	VDD18_SERDES_AVDD	1.71	1.8	1.89	V	4
CCIX Root Complex A core voltages	VDDC_RCA0, VDDC_RCA1, VDDC_RCA2, VDDC_RCA3	0.855	0.90	0.945	V	9, 10
CCIX Root Complex A supply voltages	VDDH_RCA0, VDDH_RCA1, VDDH_RCA2, VDDH_RCA3	1.35	1.5	1.65	V	8
		1.62	1.8	1.98	V	9
PCIe Root Complex B core voltages	VDDC_RCB0, VDDC_RCB1, VDDC_RCB2, VDDC_RCB3	0.713	0.75	0.788	V	8, 10
PCIe Root Complex B supply voltages	VDDH_RCB0, VDDH_RCB1, VDDH_RCB2, VDDH_RCB3	1.35	1.5	1.65	V	–
DDR4 SDRAM I/O supply voltages	VDDQ_DDR0123, VDDQ_DDR4567	1.14	1.2	1.26	V	4
					V	4
Input logic high 3.3 V LVCMOS	V_{IH}	1.7	–	3.45	V	4
Input logic high 1.8 V LVTTL		0.65 × VDD18_SOC	–	1.98	V	4
Input logic low 3.3 V LVCMOS	V_{IL}	–0.3	–	0.8	V	–
Input logic low 1.8 V LVTTL		–0.3	–	0.35 × VDD18_SOC	V	–

Table 9: Recommended Operating Conditions (Sheet 2 of 2)

PARAMETER	SYMBOL	MINIMUM	VRM SET POINT NOMINAL	MAXIMUM	UNIT	NOTES
Output logic high 3.3 V LVCMOS	V_{OH}	2.4	–	–	V	5
Output logic high 1.8 V LVTTL		VDD18_SOC – 0.45	–	–	V	5
Output logic high (DDR4) (single-ended)		0.8 × VDDQ_DDR	–	–	V	5
Output logic low 3.3 V LVCMOS	V_{OL}	–	–	0.4	V	5
Output logic low 1.8 V LVTTL		–	–	0.45	V	5
Input leakage current 1.8 V LVTTL	I_{IL1max}	–10	–	10	mA	6, 7
Input leakage current 3.3 V LVCMOS	I_{IL2max}	–10	–	10	mA	6, 7

Notes:
All voltages measured at the ball unless otherwise specified.

1. Applies to SKUs with a frequency of 3.3 GHz.
2. Applies to SKUs with a frequency of 3.0 GHz or lower.
3. Must be measured differentially between the VDDC_SOC_SENSE_P and VDDC_SOC_SENSE_N pins (that is, VDDC_SOC_SENSE_N cannot be connected to PCB ground or oscilloscope ground).
4. All supply voltages must be measured using a standard 10 pF 1 MΩ 10:1 oscilloscope probe, at a point as close to the ball as possible (< 5 mm). The equipment and probe connection used must ensure a measurement bandwidth of at least 500 MHz. Length of the VSS lead must be minimized to avoid noise pickup.
5. Output voltage high/low measured at rated current.
6. Condition: Vi = 1.8 V or GND
7. Condition: Vi = 2.75 V or GND.
8. For data transfer rates ≤ 16 Gbps.
9. For data transfer rates > 16 Gbps.
10. These supplies include a ferrite bead for isolation. Refer to the Ampere reference platform's design for details on how to connect the ferrite bead.

9. Power Supply Sequencing

This section outlines the power sequencing requirements for the Altra device. Altra is connected to an external power control device that is used to drive the power supplies and inform Altra when the power supplies for the SoC and PCP power domains are stable.

List of power domains and the order in which they are powered up, starting with the first power domain:

1. SoC power domain (which includes MCUs, GIC, SoC peripherals, SMpro and PMpro).
2. PCP power domain (all 80 CPU cores, CPMs, and the mesh fabric)

Each power domain has several voltage rails as listed in *Table 10*.

Table 10: Voltage Rails and Power Supply Sequencing – SoC and PCP Domains

STEP	DOMAIN	POWER RAILS	VOLTAGE	SEQUENCE #
1	SOC	VDDC_SOC	0.75 V	1†
		VDDC_SOC_CLKBUFF_AVDD	0.75 V	
		VDDC_RCBx	0.75 V	
2	SOC	VDDC_RCAx	0.90 V	
3	SOC	VDD18_SOC, VDD18_DDR_AVDD, VDD18_SERDES_AVDD	1.8 V	2
4	SOC	VDDH_RCAx	1.5 V/1.8 V	3
5	SOC	VDDH_RCBx	1.5 V	
6	SOC	VDDQ_DDR0123, VDDQ_DDR4567	1.2 V	
7	SOC	VDD33_SOC	3.3 V	
SYS_RESETN can be released				
PMpro sets PCP_PWRCTL				
1	PCP	VDDC_PCP	0.75 V ~ 1.12 V‡	4
			0.75 V ~ 1.10 V‡	
2	PCP	VDD18_PCP_AVDD	1.8 V	5

†**Note**: Refer to the details on the margins for these rails in *Table 9 on page 65*.

‡**Note**: For SKUs with a frequency of 3.3 GHz, the VDDC_PCP range is 0.75 V to 1.12 V. For SKUs with a frequency of 3.0 GHz or lower, the VDDC_PCP range is 0.75 V to 1.1 V.

If a specific power domain requires multiple power supplies (for example, the SoC domain that requires different voltage levels for the I/Os), then the PowerGood output of the voltage regulators for these supplies must be connected in a daisy-chain fashion. The PowerGood output of one power supply must be used as the enable for the next power supply in the order that the supplies must be powered up. This way, the SMpro/PMpro can sample the PowerGood signal of the last power supply in order to determine whether all supplies for that domain powered up successfully or not. As such, power supply components (for example, LDOs, or DC-DC converters) must be selected with PowerGood output signaling.

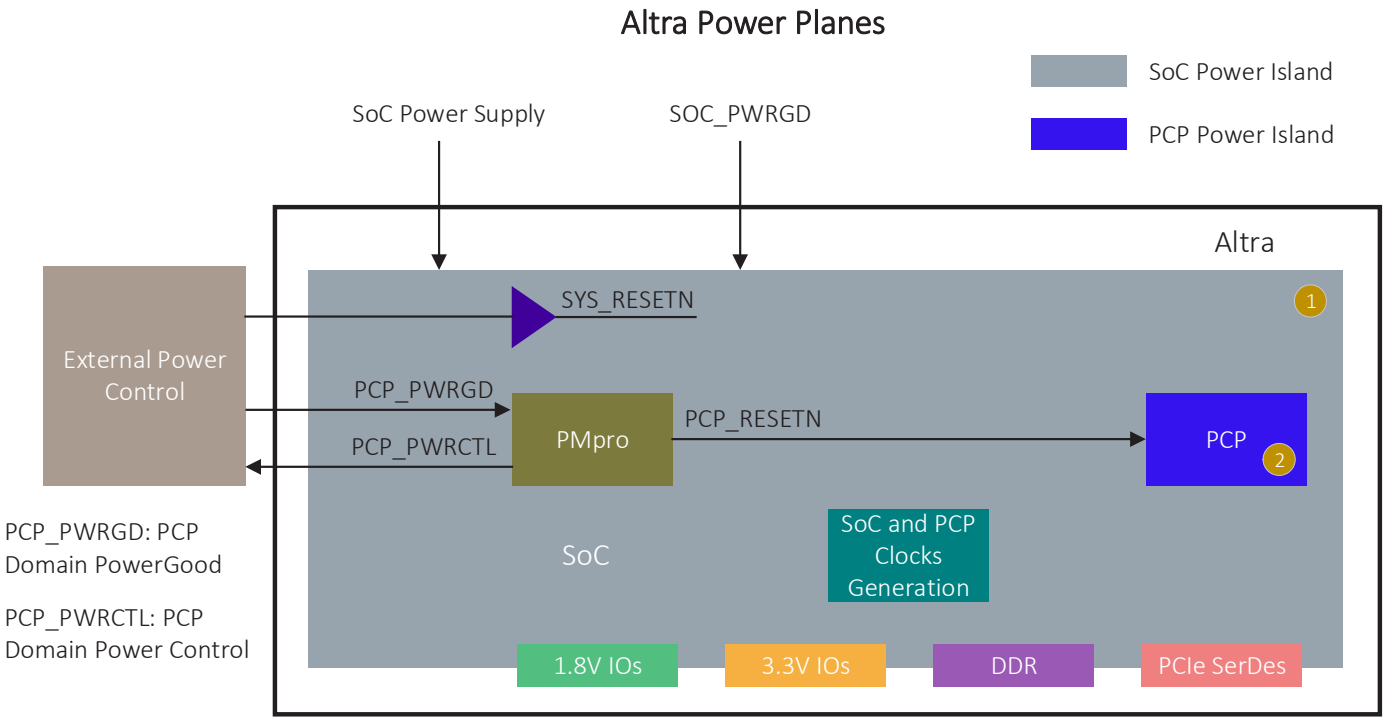
Within a power domain, the sequence must be followed as listed in *Table 10*. A sequence between the SoC and PCP power domains needs to be respected as well. The SoC domain must be brought up first, followed by the PCP domain when requested by PMpro.

Since there is no LPI state where the PCP domain is turned off, the power down sequence must be such that all power supplies must be

shut off at the same time.

Figure 3 shows the Altra processor's power planes.

Figure 3: Connecting Altra to an External Power Device



9.1. SoC Domain Power Sequencing

The SoC domain has the following power supplies:

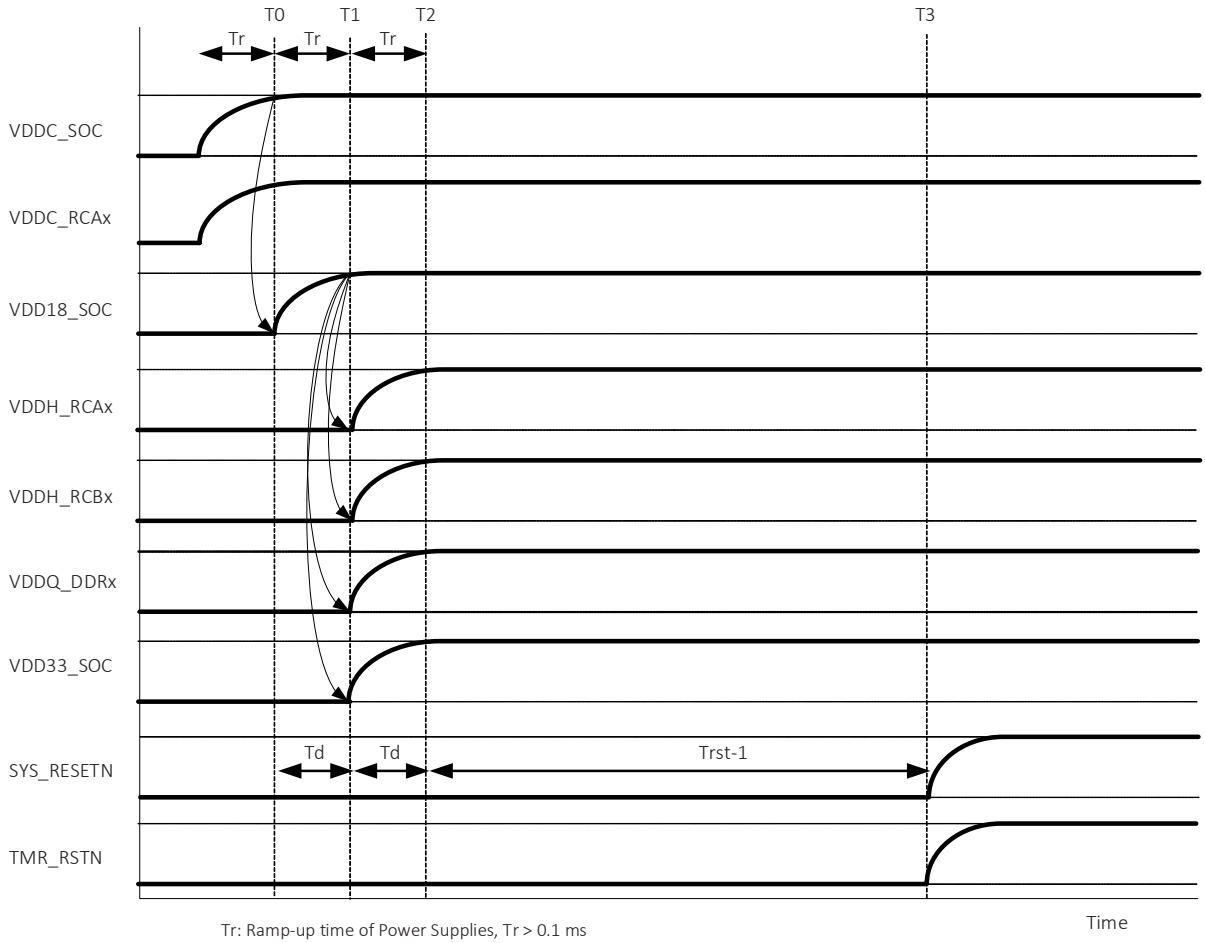
1. VDDC_SOC (consists of VDDC_SOC and VDDC_RCAx)
2. VDD18_SOC
3. VDDH_RCAx and VDDH_RCBx
4. VDDQ_DDRx (this voltage rail can be 1.1 V, 1.2 V, 1.35 V or 1.5 V depending on the DIMM technology)
5. VDD33_SOC

The power sequencing requirements are as follows:

1. Both VDDC_SOC and VDDC_RCAx must together ramp up first.
2. VDD18_SOC must ramp up next. Supplies specified in step 1 must reach 90% of their final value before supplies in this step reach 10% of their final value.
3. VDDH_RCAx, VDDH_RCBx, VDDQ_DDRx, and VDD33_SOC must ramp up next. Supplies specified in step 2 must reach 90% of their final value before supplies specified in this step reach 10% of their final value.

The timing diagrams for the SoC domain power-on voltage sequencing are shown in *Figure 4*.

Figure 4: Power-on Voltage Sequencing – SoC Domain



Tr: Ramp-up time of Power Supplies, Tr > 0.1 ms

Td: Delay between Power supplies, Td > 0.02 ms

Trst-1: $\overline{\text{SYS\_RESETN}}$ can be de-asserted after 3.3 V power rail is stable (Trst-1 > 10 µs)

Maximum allowable skew between assertion of TMR_RSTN to Socket0 and Socket1 is 1 ns.

The timing margins for the supplies to stabilize are provided in *Table 11*.

Table 11: Timing Margins for SoC Domain Power Sequencing

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
Ramp Time of Power Supplies	T_r	0.1	–	ms
Delay Between Power Supplies	T_d	0.02	50	ms
SYS_RESETN deasserted after 3.3 V supply is stable	$T_{rst} - 1$	10	–	µs

The power up sequence for the SoC domain is summarized as:

VDDC_SOC, VDDC_RCAx → VDD18_SOC → VDDH_RCAx, VDDH_RCBx, VDDQ_DDRx, VDD33_SOC

9.2. PCP Domain Power Sequencing

The PCP domain has only the following voltage rails:

1. VDDC_PCP

Note: *For SKUs with a frequency of 3.3 GHz, the VDDC_PCP range is 0.75 V to 1.12 V. For SKUs with a frequency of 3.0 GHz or lower, the VDDC_PCP range is 0.75 V to 1.1 V.*

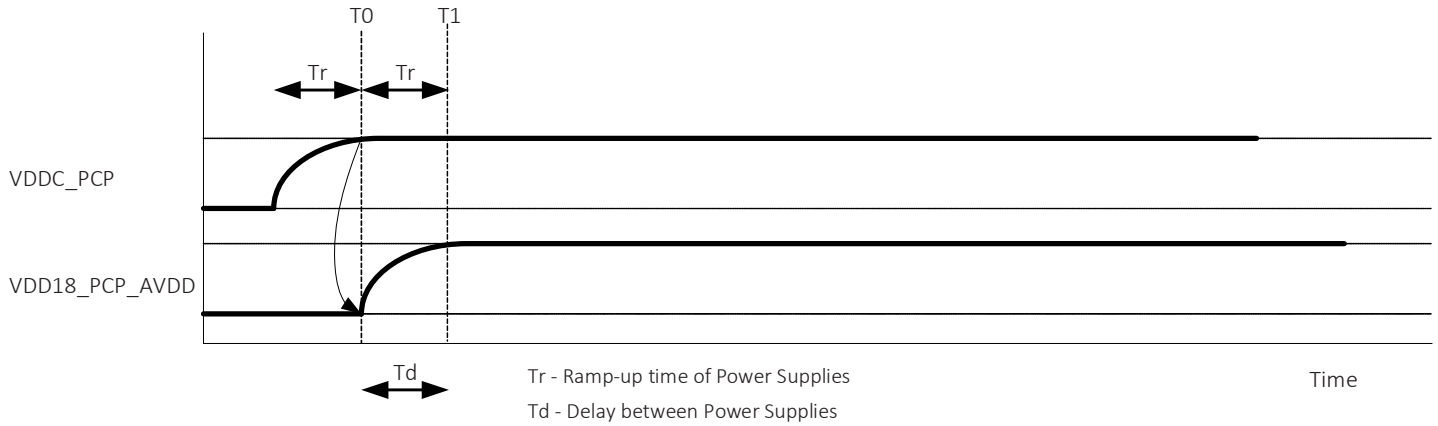
2. VDD18_PCP_AVDD (1.8 V for PLLs and temperature sensors)

The power sequencing requirements are as follows:

1. VDDC_PCP must ramp up first.
2. VDD18_PCP_AVDD must ramp up next. Supplies specified in step 1 must reach 90% of their final value before supplies in this step reach 10% of their final value.

Timing diagrams for the PCP domain power-on voltage sequencing are shown in *Figure 5*.

Figure 5: Power-on Voltage Sequencing – PCP Domain



The timing margins for the supplies to stabilize are provided in *Table 12*.

Table 12: Timing Margins for PCP Domain Power Sequencing

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
Ramp Time of Power Supplies	T_r	0.1	–	ms
Delay Between Power Supplies	T_d	0.02	20	ms

The power up sequence for the PCP domain is summarized as:

VDDC_PCP → VDD18_PCP_AVDD

Apart from the above power sequencing for the PCP domain, there is sequencing to be followed with respect to the SoC domain.

9.3. General Requirements

1. Power down sequence for Altra: Power supplies must be shut off at the same time.
2. External voltage must not be applied to chip I/O balls before the associated I/O power supply voltage is applied to the chip.
3. A chip power down cycle must complete (all I/O supply voltages and logic voltages are below 0.4 V) before next power-up cycle is started.
4. Failure to follow this reset sequence during power up cycle may result in unpredictable operation of the chip.

10. System Configuration from Power Domain Connectivity Perspective

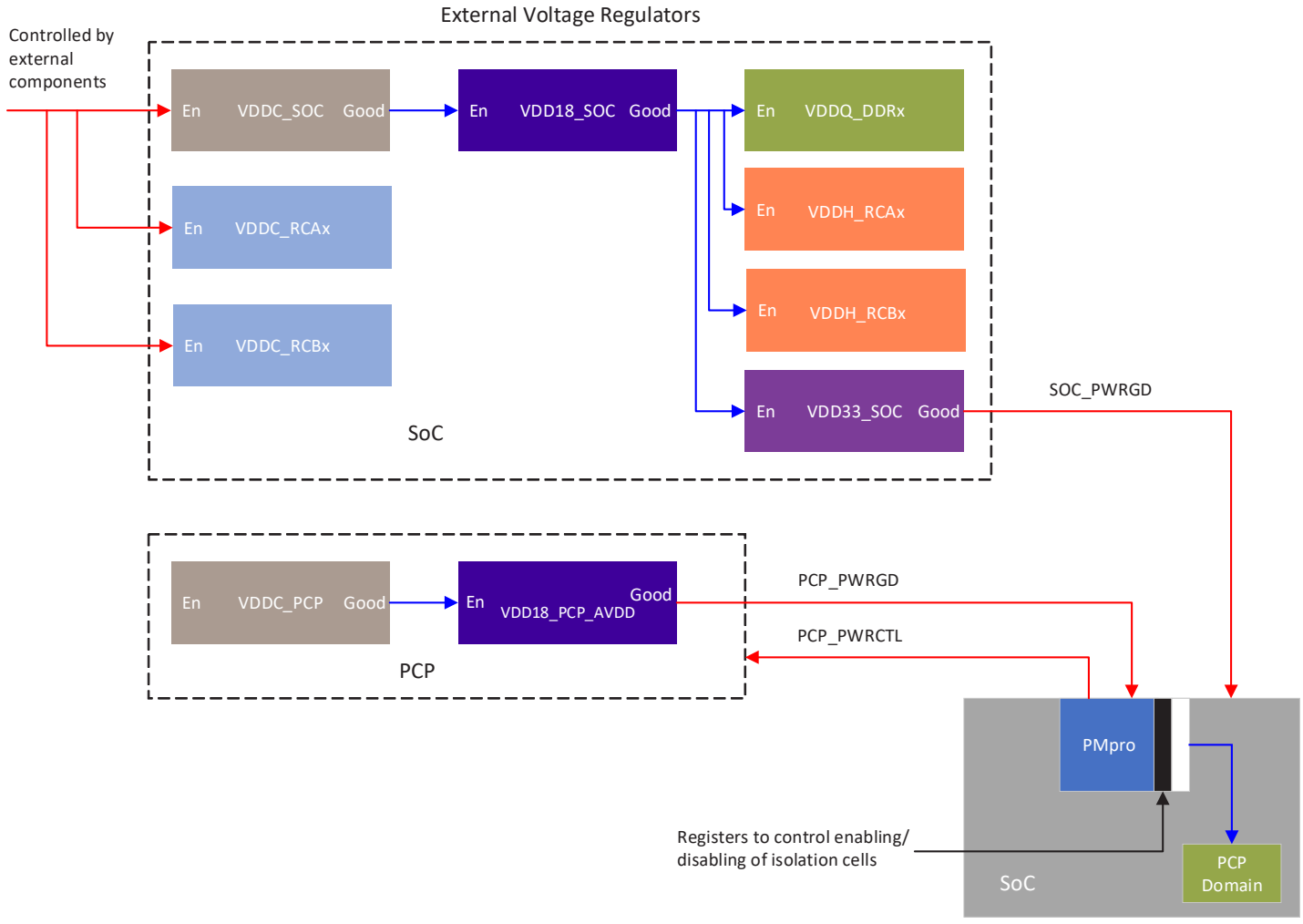
Altra only supports a system configuration on board where the SoC and PCP domains are independent and use distinct regulators.

SoC domain and PCP domain are independent power domains.

- External system component (for example, BMC) powers up the SoC domain and brings SMpro out of reset as outlined in the normal power sequencing flow.
- PCP_PWRCTL output must be connected to the voltage regulator that powers up the PCP. The voltage regulator power good signal must be connected to PCP_PWRGD input on the board.

Figure 6 shows the Altra system configuration using two voltage regulators.

Figure 6: System Configuration using Two Voltage Regulators



Isolation cells must be implemented at the PCP boundary as the PCP is powered down when the SoC domain is brought up. Isolation is only required from PCP to SoC. Controls to enable or disable the isolation are located in PMpro.

The power supply sequencing in this configuration is as shown below:

VDDC_SOC, VDDC_RCAx → VDD18_SOC, VDDH_RCAx, VDDH_RCBx, VDDQ_DDRx, VDD33_SOC

VDDC_PCP → VDD18_PCP_AVDD

Table 13 summarizes the steps to power up the Altra processor.

Table 13: Power-up Sequence for Altra

STEP	ACTION		
System Input Power is Applied			
SYS_RESETN is Active (*Pulled Low*)			
1	VDDC_SOC VDDC_RCAx	↓	
2		VDD18_SOC	↓
3			VDDH_RCAx VDDH_RCBx VDDQ_DDRx VDD33_SOC
SYS_RESETN is Released (*Goes High*)			
PMpro sets PCP_PWRCTL			
4	VDDC_PCP	↓	
5		VDD18_PCP_AVDD	
PCP_PWRGD can be Asserted			

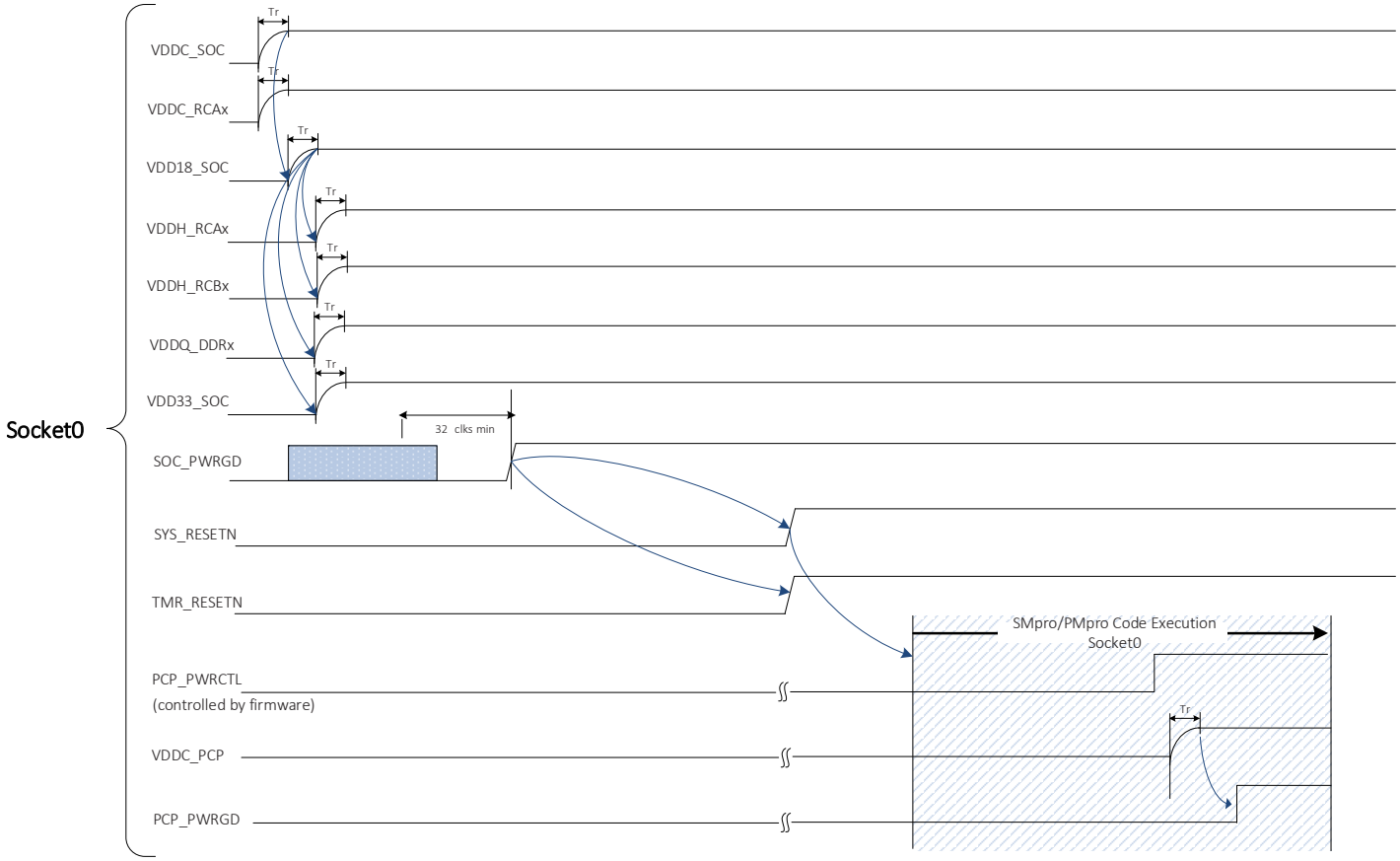
Note: *Ramp up time and Delay between power supplies must be met irrespective of whether the power planes are combined or not.*

11. Power-on Sequence

11.1. Power-on Sequence for a 1P Configuration

The power-on sequence for a 1P configuration is as shown in *Figure 7*.

Figure 7: Power-on Sequence for 1P Configuration



For a 1P configuration, the power-on sequence for Altra is as follows:

1. Socket0 SOC_PWRGD pin is asserted (pulled HIGH) *before* SYS_RESETN is asserted (pulled HIGH).
2. Once SYS_RESETN is released, SMpro code execution begins, triggering the boot process.

Note: *Clocks to PMpro must be stable before SYS_RESETN is released.*

11.2. Power-on Sequence for a 2P Configuration

When the SoC and PCP domains are independent, at power-on, once all voltage rails of the SoC domain and the system reference clock are stable, the BMC releases SYS_RESETN for Socket0 (*note that Socket1 is still under reset*). By default, the Master Socket (Socket0) accesses the EEPROM and boots-up first. When SMpro boot has completed for Socket0, ALERT9_N is driven HIGH and ALERT3_N is driven LOW.

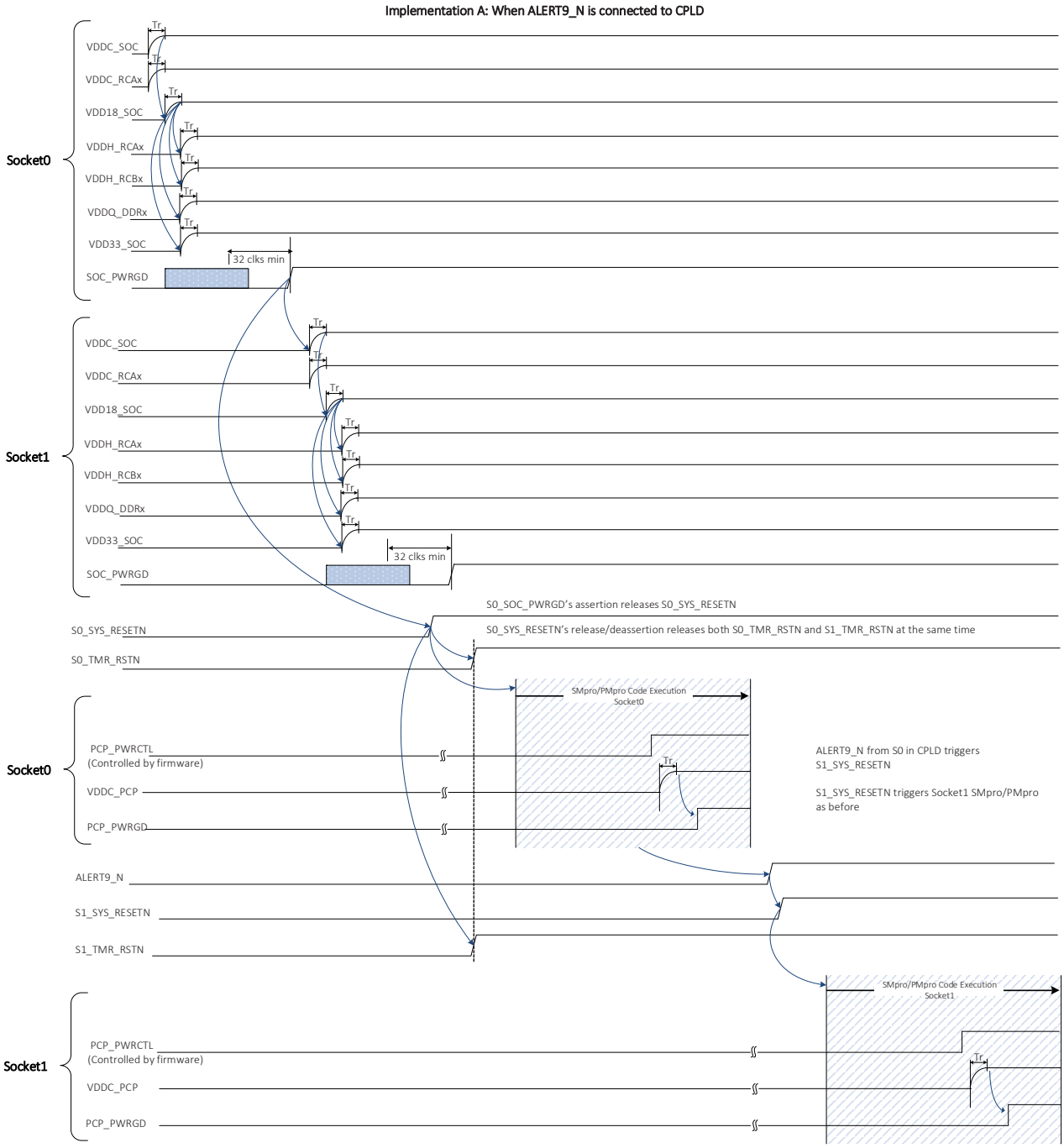
There are two separate implementations for the power-on and boot flow for a 2P configuration:

1. Implementation A: When ALERT9_N is connected to the external CPLD
2. Implementation B: When ALERT9_N is not connected to the CPLD

11.2.1. Power-on Sequence When ALERT9_N is Connected to CPLD

When ALERT9_N is connected to the CPLD, the power-on sequence shown in *Figure 8* applies for a 2P configuration.

Figure 8: Power-on Sequence for 2P Configuration when ALERT9_N is Connected to CPLD



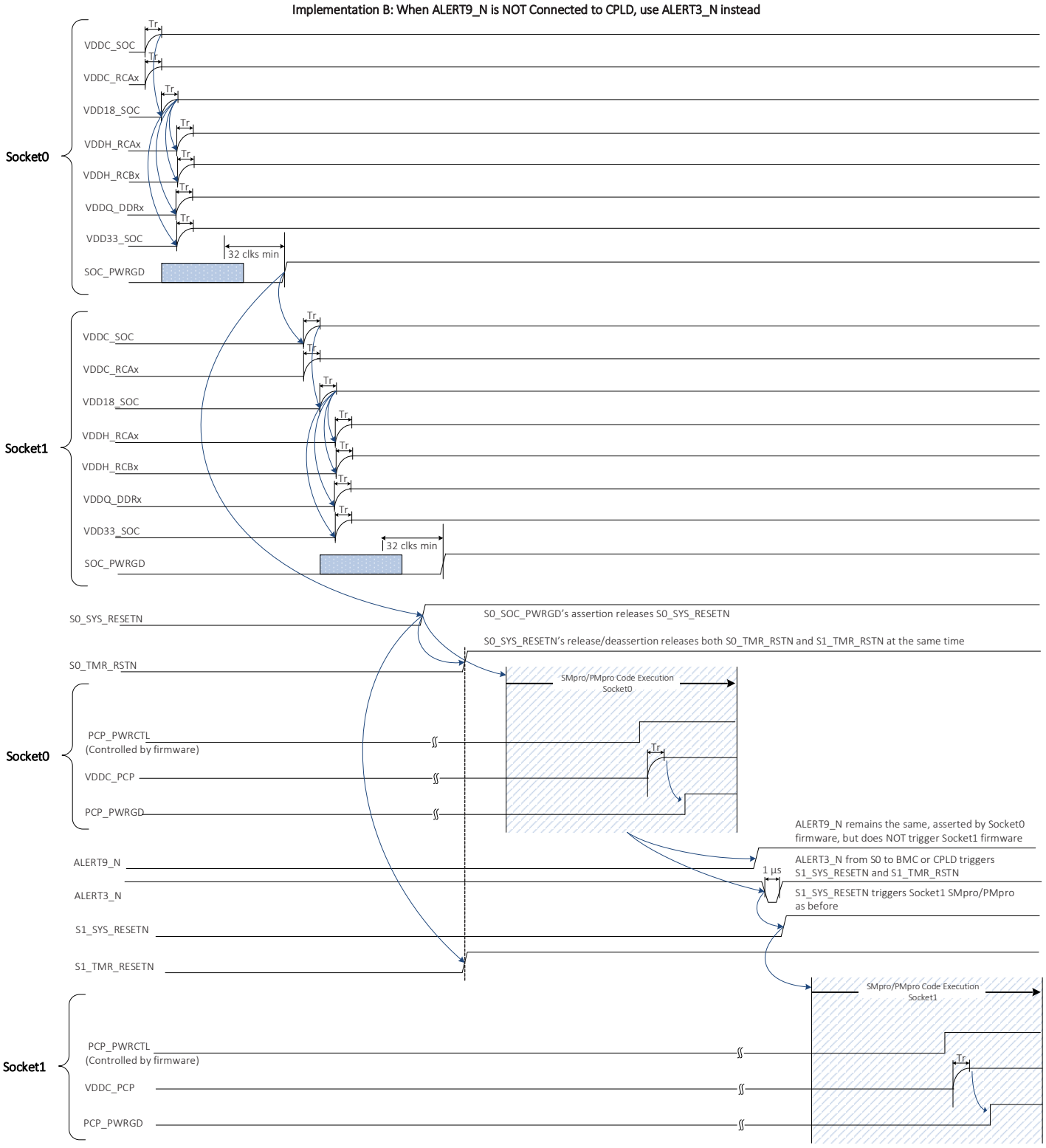
Notes:

- The T_{rst} delay must account for the SYS_REFCLK1 clock to be stable with a minimum of 32 clock cycles and for a minimum of 4 clock cycles where both SYS_RESETN and SOC_PWRGD are low.
- Maximum allowable skew between assertion of TMR_RSTN to Socket0 and Socket1 is 1 ns.

11.2.2. Power-on Sequence When ALERT9_N is Not Connected to CPLD

When ALERT9_N is not connected to the CPLD, the power-on sequence shown in *Figure 9* applies for a 2P configuration.

Figure 9: Power-on Sequence for 2P Configuration when ALERT9_N is Not Connected to CPLD



In general, for a 2P configuration, the Altra power-on sequence is as follows:

1. Socket0 SOC_PWRGD enables Socket1 voltages to ramp up.
2. On power up, once all voltage rails of the SoC domain and the system reference clock are stable, the CPLD or BMC releases S0_SYS_RESET_L. *Note that Socket1 is still under reset*.

   Note: If Socket1 power rail fails, the boot sequence continues with 1P boot flow on Socket0.

3. Socket0 SMpro is the master and boots first.
4. When Socket0 SMpro boot is complete, ALERT9_N is driven HIGH and ALERT3_N is driven LOW.
5. For the ALERT9_N signal:
   a) If ALERT9_N is connected to the CPLD (implementation A): A HIGH output on ALERT9_N indicates to the CPLD to release S1_SYS_RESET_L.
   b) If ALERT9_N is not connected to the CPLD (implementation B): If GPIO8=0 (SCP_FW_BOOT_OK), the falling edge of ALERT3_N indicates to the CPLD or BMC to release S1_SYS_RESET_L.

      Note: ALERT3_N is a dual-purpose pin and is used depending on the boot phase:

      1. If GPIO8=0 (SCP_FW_BOOT_OK), ALERT3_N is used as described above.
      2. If GPIO8=1 (SCP_FW_BOOT_OK), ALERT3_N is connected to the CPLD or BMC as an SMB ALERT signal from Altra.

6. Socket0 outputs a HIGH on S0_FW_BOOT_OK to indicate to the CPLD or BMC that Socket0 boot has completed.
7. After Socket1 boot is complete, Socket1 outputs a HIGH on S1_FW_BOOT_OK to indicate to the CPLD or BMC that Socket1 boot has completed.

For additional information on the power-on sequence and boot flows, refer to the document titled *Altra Platform Hardware Design Specification*.

12. Power Specifications

Table 14 provides the estimated power numbers under the conditions listed as **Notes** in the table.

Table 14: DC Power Supply Loads (Sheet 1 of 2)

PARAMETER	SYMBOL	SKU ID[1]										UNIT	NOTES
		Q80-33	Q80-30	Q80-28	Q80-26	Q72-30	Q64-33	Q64-30	Q64-26	Q64-22	Q32-17		
Maximum/Nominal frequency	–	3.30	3.00	2.80	2.60	3.00	3.30	3.00	2.60	2.20	1.70	GHz	–
Lowest frequency	–	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	GHz	2
Thermal Design Power	TDP	250	210	185	150	195	220	180	125	95	65	W	3
Lowest power limit	P_{LIMIT}	120	120	120	120	120	120	120	80	80	60	W	4
(*Variable V*) PCP (VDDC_PCP) active (continuous) operating current	I_{PCP}	240	200	170	135	180	205	165	110	85	55	A	5
(*Variable V*) PCP (VDDC_PCP) maximum operating current	$I_{PCP(MAX)}$	340	300	225	195	270	300	240	130	120	65	A	6
VDDC_SOC active operating current	I_{SOC}	22.17										A	–
VDDC_RCB[0:3] active operating current	I_{C_RCB}	4 (1 A per VDDC_RCB)										A	–
VDDC_SOC_CLKBUFF_AVDD (SoC clock buffer) active operating current	I_{C_CLKBUF}	0.5										A	–
VDDC_RCA[0:3] active operating current	I_{C_RCA}	16										A	–
VDDH_RCB[0:3] active operating current	I_{H_RCB}	4										A	–
VDDH_RCA[0:3] active operating current	I_{H_RCA}	5										A	–
VDDQ_DDR0123, VDDQ_DDR4567 (DDR4) active operating current	I_{DDQ}	10 (for each VDDQ)										A	7

Table 14: DC Power Supply Loads (Sheet 2 of 2)

PARAMETER	SYMBOL	SKU ID[1]										UNIT	NOTES
		Q80-33	Q80-30	Q80-28	Q80-26	Q72-30	Q64-33	Q64-30	Q64-26	Q64-22	Q32-17		
VDD18_DDR_AVDD DDR4 supply active operating current	I_{DDR}	0.5										A	–
VDD18_SERDES_AVDD SerDes active operating current	I_{SERDES}	0.5										A	–
VDD18_SOC active operating current	I_{O18}	0.5										A	–
VDD18_PCP_AVDD active operating current	I_{PCP18}	1										A	–
VDD33_SOC active operating current	I_{O33}	1										A	–

Notes:
1. Use the two digits following 'Q' as part of the SKU ID (such as 'Q80') to decode the CPU core count.
2. CPPC Lowest Performance Threshold register value. This is the minimum frequency at which a core can run.
3. Power measured at nominal voltage and max recommended operating temperature.
4. The lowest power capping value that BMC can program via the Power Limit register. Refer to the section titled *ACPI State Register Definitions* in the *Altra SoC BMC Interface Specification* for details about this register.
5. PCP active (continuous) operating current is estimated at the highest frequency with TDP and T_{CJ} per SKU as specified in *Table 15 on page 80* with best-case process part.
6. PCP maximum operating current is estimated at the maximum frequency per SKU, with T_{CJ} per SKU as specified in *Table 15 on page 80* with best-case process part (which drives worst-case power). For hot-swap controller OCP calculations, use VDDC_PCP = 1.1 V.
7. For DDR4: VDDQ_DDR0123, VDDQ_DDR4567 = 1.2 V.

Maximum current is estimated at the specified frequency with 0.90 V, 1.2 V, 1.5 V, 1.8 V, 3.3 V, and with the T_{CJ} per SKU as specified in *Table 15 on page 80* with best-case process part (which drives worst-case power). The maximum current values listed above are not guaranteed to be the highest obtainable. These values are dependent on many factors, including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, junction temperature, and the power supply voltages. Your specific application can produce significantly different results. Logic current and power are primarily dependent on the applications running and the use of internal chip functions (for example, PCIe). I/O current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.

13. Thermal Specifications

Table 15 lists the thermal resistance values for the package, the maximum continuous and operating junction temperatures, the thermal throttling and shut down temperatures, and the storage and operating temperature ranges for each SKU.

Table 15: Thermal Specifications

PARAMETER	SYMBOL	SKU ID[1]										UNIT	NOTES
		Q80-33	Q80-30	Q80-28	Q80-26	Q72-30	Q64-33	Q64-30	Q64-26	Q64-22	Q32-17		
Junction-to-case thermal resistance	θ_{JC}	0.11	0.12	0.10	0.10	0.11	0.13	0.11	0.10	0.085	0.085	°C/W	2, 3
Maximum continuous operating junction temperature	T_{CJ}	100	100	95	90	100	100	95	80	75	70	°C	4
SoC thermal throttling temperature	TM1	105	105	105	100	105	105	105	90	85	80	°C	4
SoC thermal shut down temperature	TM2	120										°C	4
Storage temperature range	T_{STG}	–55 to +150										°C	5
Operating junction temperature range	T_J	0 to +125										°C	5

Notes:

1. Use the two digits following 'Q' as part of the SKU ID (such as 'Q80') to decode the CPU core count.
2. Case temperature T_C is measured at top center of lid with device seated in ILM4926 socket.
3. θ_{JC} is measured based on boundary conditions of the reference thermal solution and all power is assumed to dissipate from package to thermal solution.
4. T_{CJ} as specified in this table is for use as a system thermal design guideline. The SoC can run continuously at this temperature.
   To achieve maximum performance, ensure that the thermal solution can maintain T_{CJ} at this value.
   In case of operational or cooling failures, the following built-in mechanism in firmware will protect the SoC from a thermal runaway or getting damaged:
   - HIGHTEMP_N (TM1): The SoC temperature at which thermal throttling will be triggered. The CPU frequency is throttled down in steps of 50 MHz.
   - OVERTEMP_N (TM2): The SoC temperature at which a shut down will be triggered. The entire SoC is powered off under this condition.
5. This value is not a specification of the operational temperature range; it is a stress rating only.

14. Clocking Specifications

Figure 10:Timing Diagram for DDR4, UART, DAP, SMpro, PMpro, and SoC JTAG Clocks

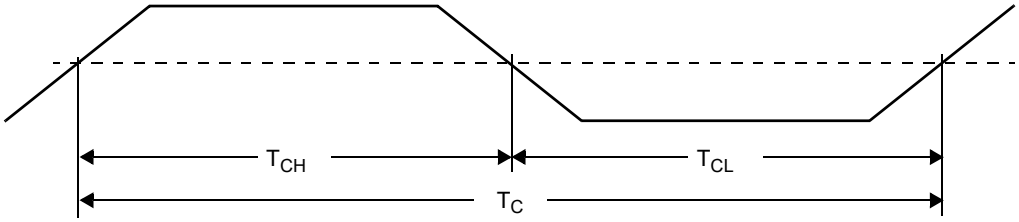


Table 16: Clocking Specifications

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
DDR4 Clock – DDRi_CLK_n (i = 0 to 7 and n = 0, 1, 2, or 3)					
Frequency	F_C	1600		MHz	–
Period	T_C	0.625		ns	
UART Clock – UART_SCLK					
Frequency	F_C	1.8432		MHz	1
Period	T_C	542.5		ns	
DAP, SMpro, PMpro, and SoC JTAG Clocks (JTAG_DAP_TCK, JTAG_IPP_TCK, JTAG_PM_TCK, JTAG_SOC_TCK)					
Frequency	F_C	25		MHz	–
Period	T_C	40		ns	
Timer Clock – TMR_CLK					
Frequency	F_C	25		MHz	2
Period	T_C	40		ns	

Notes:
1. Accuracy of ± 300 ppm. This is an optional clock required for applications where UART baud rate cannot be supported by internal PLL UART Reference Clock.
2. Accuracy of ± 25 ppm. TMR_CLK synchronizes time between sockets. TMR_CLK must be asserted synchronously with the same phase to both Socket0 and Socket1. Maximum allowable skew between two sockets is 1 ns.

14.1. System Reference Clock

Figure 11:SYS_REFCLK_SRNS_P/N and SYS_REFCLK_SRIS_P/N Reference Clocks

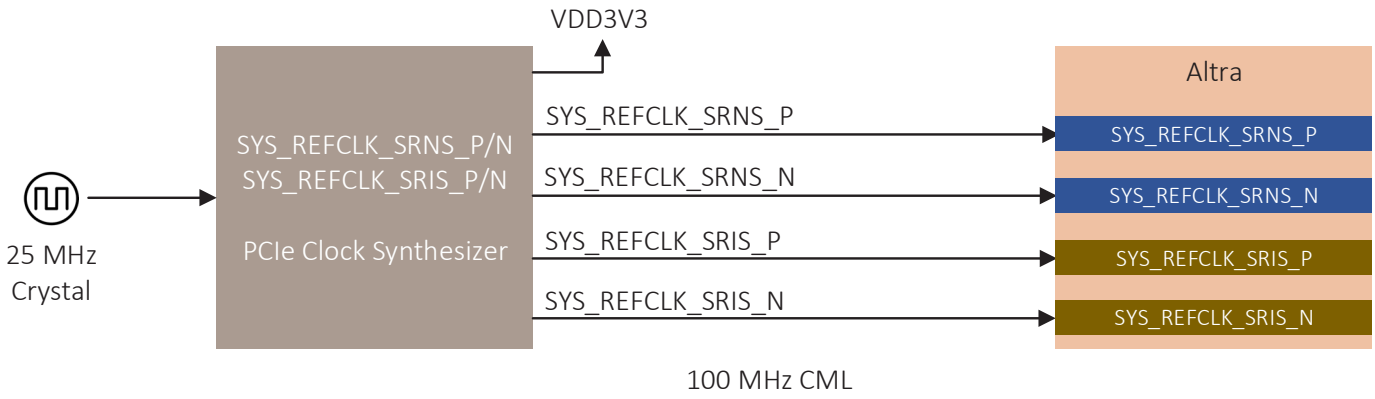


Table 17: System Reference Clock Specifications – SYS_REFCLK_SRNS_P/N, SYS_REFCLK_SRIS_P/N

DESCRIPTION	MIN	TYP	MAX	UNIT	CONDITION
Input Voltage Range	0	–	0.75	V	–
Input Differential Voltage	150	200	400	mVp	Peak voltage
Input Frequency	–	100	–	MHz	*Spread Spectrum Clocking (SSC). See **Notes** below.
Input Frequency Tolerance	–50	–	50	ppm	–
Input Duty Cycle Tolerance	45	–	55	%	–
Input Common Mode Voltage	0.222	0.234	0.246	V	–
Input Impedance, Differential	90	100	110	Ω	–
Rise time, Fall time	0.1	–	1	ns	–
Random Jitter	–	–	0.5	ps, RMS	Jitter Integrated from 50 kHz to 10 MHz
Maximum Peak-to-Peak Phase Jitter	–	–	25000	ps	Reference Clock with SSC active at 30 kHz
	–	–	1000	ps	Reference Clock with SSC active at 100 kHz
	–	–	25	ps	Reference Clock with SSC active at 500 kHz

Notes:
1. If Spread-Spectrum is needed, it is applied only to SYS_REFCLK_SRIS_P/N. If Spread-Spectrum is not needed, it must be 100 MHz. For PCI Express, The maximum spread spectrum is –0.5%, modulated between 30 kHz and 33 kHz.
   The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times.

15. PCIe Interface Specifications

Table 18: SerDes Transmitter AC Specifications (PCIe Gen4, 16 GT/s)

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNIT	COMMENTS	NOTES
Unit Interval	UI	62.48125	62.5	62.51875	ps	± 300 ppm	–
Differential Peak to Peak TX Voltage Amplitude	V_{pp}	800	–	1300	mV_{pp}	–	–
Rising Edge Rate	Rising Edge Rate	0.6	–	4.0	V/ns	–	–
Falling Edge Rate	Falling Edge Rate	0.6	–	4.0	V/ns	–	–
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	–	–	20	%	–	2
TX Uncorrelated Total Jitter	T_j	–	–	12.5	ps	–	–
DC Differential TX Impedance	R_{tx}	–	–	120	Ω	–	–
TX Lane to Lane Output Skew	–	–	–	1.25	ns	–	–
AC Coupling Capacitor	CTX	176	–	265	nF	–	–

Notes:
1. As measured with PCIe compliance test setup
2. Measurement taken from single ended waveform. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ must be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference must not exceed 20% of the slowest edge rate.

Table 19: SerDes Receiver AC Specifications (PCIe Gen4, 16 GT/s)

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNIT	COMMENTS	NOTES
Unit Interval	UI	62.48125	62.5	62.51875	ps	± 300 ppm	–
Differential Peak to Peak RX Voltage (Eye Height)	V_{pp}	15	–	–	mV_{pp}	–	1, 2
Differential RX Voltage (Eye Width)	–	0.3	–	–	UI	–	2, 3
Bit Error Rate	–	–	–	$10e^{-12}$	BER	–	–
Differential Termination	T_j	90	100	110	Ω	–	–
RX Lane to Lane Skew	R_{tx}	–	–	5	ns	–	–

Notes:
1. As measured with PCIe compliance test setup.
2. Receiver eye height/width at TP2P of compliance test point, target at BER $10e^{-12}$; (eye width and eye height are defined after applying post processing and are defined at TP2P).
3. At –3 dB channel Loss.

16. I/O Specifications

Figure 12:Input Setup and Hold Timing Diagrams

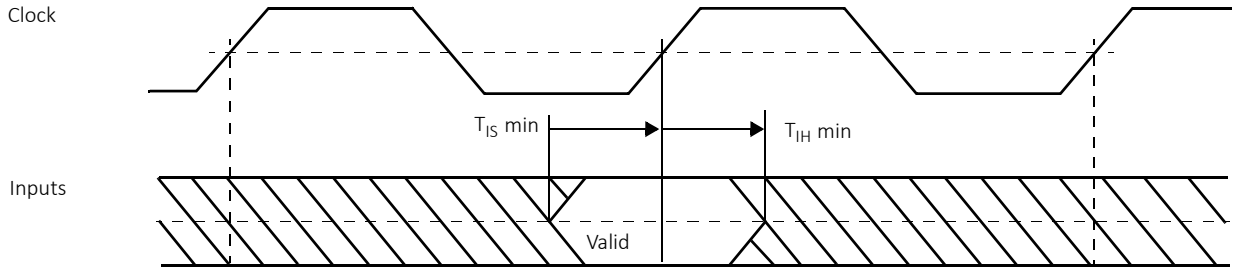


Figure 13:Output Delay and Float Timing Diagrams

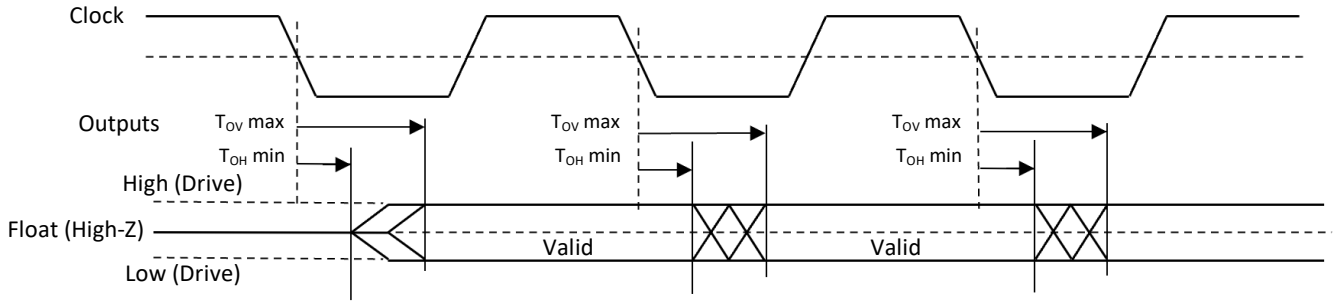


Table 20: I/O Specifications (Sheet 1 of 3)

SIGNAL	INPUT (ns)		OUTPUT (ns)		OUTPUT CURRENT (mA)		CLOCK	NOTES
	SETUP TIME (T_{IS} MIN)	HOLD TIME (T_{IH} MIN)	VALID DELAY (T_{OV} MAX)	HOLD TIME (T_{OH} MIN)	I_{OH} (MIN)	I_{OL} (MIN)		
GPIO Interface								
GPIO_[0:23]	N/A	N/A	N/A	N/A	4	4	async	–
GPI_[0:7]	N/A	N/A	N/A	N/A	N/A	N/A	async	–
I^2C Interface								
IIC_SCL_[0:10] IIC_SDA_[0:10] PMALERT_N ALERT[2:10]_N	N/A	N/A	N/A	N/A	N/A	16	async	1

Table 20: I/O Specifications (Sheet 2 of 3)

SIGNAL	INPUT (ns)		OUTPUT (ns)		OUTPUT CURRENT (mA)		CLOCK	NOTES
	SETUP TIME (T_{IS} MIN)	HOLD TIME (T_{IH} MIN)	VALID DELAY (T_{OV} MAX)	HOLD TIME (T_{OH} MIN)	I_{OH} (MIN)	I_{OL} (MIN)		
DAP JTAG Interface								
JTAG_DAP_TDI	3	–15	N/A	N/A	N/A	N/A	JTAG_DAP_TCK	2
JTAG_DAP_TDO	N/A	N/A	13	–15	8	8	Driven on falling edge of JTAG_DAP_TCK	3
JTAG_DAP_TMS	5	–15	N/A	N/A	N/A	N/A	JTAG_DAP_TCK	2
$\overline{\text{JTAG\_DAP\_TRSTN}}$	N/A	N/A	N/A	N/A	N/A	N/A	async	2
SMPro/PMpro JTAG Interface								
JTAG_IPP_TDI/ JTAG_PM_TDI	3	–15	N/A	N/A	N/A	N/A	JTAG_IPP_TCK/ JTAG_PM_TCK	2
JTAG_IPP_TDO/ JTAG_PM_TDO	N/A	N/A	7	–15	8	8	Driven on falling edge of JTAG_IPP_TCK/ JTAG_PM_TCK	3
JTAG_IPP_TMS/ JTAG_PM_TMS	4	–15	N/A	N/A	N/A	N/A	JTAG_IPP_TCK/ JTAG_PM_TCK	2
$\overline{\text{JTAG\_IPP\_TRSTN}}$/ $\overline{\text{JTAG\_PM\_TRSTN}}$	N/A	N/A	N/A	N/A	N/A	N/A	async	2
SoC JTAG Interface								
JTAG_SELECT[0:3]	N/A	N/A	N/A	N/A	N/A	N/A	async	2
JTAG_SOC_TDI	11	–15	N/A	N/A	N/A	N/A	JTAG_SOC_TCK	2
JTAG_SOC_TDO	N/A	N/A	14	–15	8	8	Driven on falling edge of JTAG_SOC_TCK	3
JTAG_SOC_TMS	7	–15	N/A	N/A	N/A	N/A	JTAG_SOC_TCK	2
$\overline{\text{JTAG\_SOC\_TRSTN}}$	N/A	N/A	N/A	N/A	N/A	N/A	async	2
Serial Peripheral Interface								
SPI[0:1]_CLK	N/A	N/A	N/A	N/A	16	16	33 MHz	–
SPI0_CS[0:2]	N/A	N/A	N/A	N/A	16	16	SPI0_CLK	4, 5, 6
SPI0_IO[0:3]	5.28	–1.32	9.6	–2.76	16	16	SPI0_CLK	4, 5, 6
SPI1_CS[0:2]	N/A	N/A	N/A	N/A	16	16	SPI1_CLK	4, 5, 6
SPI1_IO[0:3]	5.28	–1.32	9.6	–2.76	16	16	SPI1_CLK	4, 5, 6

Table 20: I/O Specifications (Sheet 3 of 3)

SIGNAL	INPUT (ns)		OUTPUT (ns)		OUTPUT CURRENT (mA)		CLOCK	NOTES
	SETUP TIME (T_{IS} MIN)	HOLD TIME (T_{IH} MIN)	VALID DELAY (T_{OV} MAX)	HOLD TIME (T_{OH} MIN)	I_{OH} (MIN)	I_{OL} (MIN)		
UART								
UART_SIN[0:4]	N/A	N/A	N/A	N/A	N/A	N/A	async	–
UART_SOUT[0:4]	N/A	N/A	N/A	N/A	4	4	async	–

Notes:
1. I^2C maximum load = 150 pF and maximum frequency = 1 MHz.
2. Captured at rising edge of JTAG_TCK clock.
3. Launched at falling edge of JTAG_TCK clock.
4. SPI ports are configured as Masters-only, with Frame Format (SPInCTRLR0 bits 5:4) = 00, Serial Clock Phase (SPInCTRLR0 bit 6) = 1, and Serial Clock Polarity (SPInCTRLR0 bit 7) = 1.
5. Data is launched on the falling edge of SPIn_CLK (n = 0 or 1) and captured on rising edge.
6. Data is held N cycles of APB clock from the rising edge of SPIn_CLK, and depends on the interface configuration. The T_{OH} values shown in the table are calculated as: TOH_ACTUAL + (N × TCLK_APB), where N = 2, TCLK_APB = 10.0 ns and TOH_ACTUAL is the 0-cycle hold measurement.
7. The data input path has path delay compensation capability, using which, it can shift the data input latch point by units of [1:15] AHBC clock cycles. The data input setup/hold time must add the compensation delay based on the setting of Receive Data Sample Delay in CTRLR register.

16.1. I²C I/O Specifications

Figure 14:I²C Bus Timing Diagram

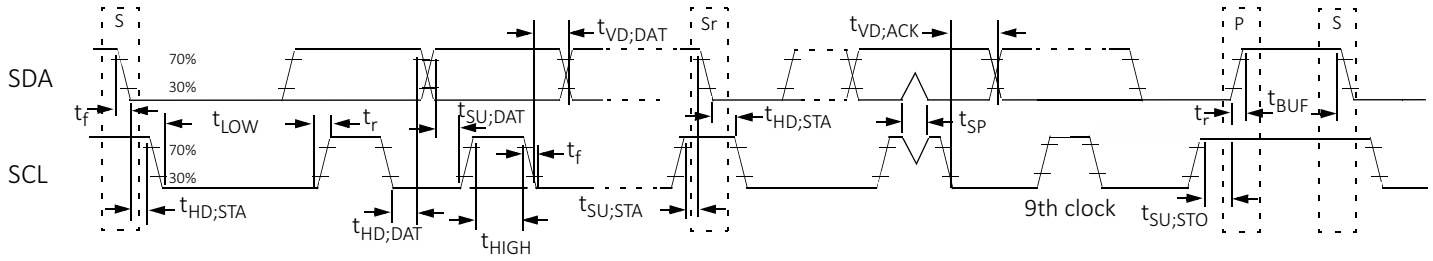


Table 21: I²C Timing Characteristics (Sheet 1 of 2)

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		FAST-MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	–	0.6	–	0.26	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	0.5	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	0.26	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	0.26	–	µs
Data hold time	$t_{HD;DAT}$	5.0	–	–	–	–	–	µs[3]
		0	–	0	–	0	–	µs[4]
Rise time of both SDA and SCL signals	t_r	–	1000	20	300	–	120	ns
Fall time of both SDA and SCL signals	t_f	–	300	–	300	–	120	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	0.26	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	0.5	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	–	550	pF
Data valid time	$t_{VD;DAT}$	–	3.45	–	0.9	–	0.45	µs
Data valid acknowledgment time	$t_{VD;ACK}$	–	3.45	–	0.9	–	0.45	µs

Table 21: I^2C Timing Characteristics (Sheet 2 of 2)

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		FAST-MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Noise margin at the LOW level (for each connected device, including hysteresis)	V_{nL}	0.1 × VDD	–	0.1 × VDD	–	0.1 × VDD	–	V
Noise margin at the HIGH level (for each connected device, including hysteresis)	V_{nH}	0.2 × VDD	–	0.2 × VDD	–	0.2 × VDD	–	V

Notes:
1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH_{min} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. For CBUS compatible masters: CBUS receivers can be connected to the Standard-mode I^2C-bus. However, a third bus line called DLEN must then be connected and the acknowledge bit omitted. Refer to the *I^2C-Bus Specification and User Manual* for more information.
4. For I^2C-bus devices.

17. Boot Configuration

Platform architects and system designers can leverage the following benefits that Altra offers:

- 256 KB EEPROM for booting SMpro and PMpro firmware
  - This will be validated and authenticated by an immutable ROM code that runs on the SMpro
- SPI-NOR flash is required to boot ARM Trusted Firmware (ATF) and UEFI
  - This will be validated and authenticated by SMpro.

17.1. Trusted Management Module (TMM)

The Trusted Management Module (TMM) runs on the system controller processor (SCP) of the SMpro and enables secure configuration and operation. The TMM provides a non-tamperable hardware platform that uses asymmetric public key operations to validate the actions being performed are authorized and legitimate. This is achieved by creating a partition of secure boundary within the Altra device that contains all the functions necessary to provide root of trust. Since the TMM functionality runs on the SMpro and is integrated into the Altra device, it has visibility and controllability of all internal buses and processing subsystems that is not possible when external trust devices are used. Additionally, because the TMM functionality runs on the SMpro core, it removes all dependency on the application software operating on the Altra cores. The TMM provides the following key capabilities:

- Separate non-tamperable hardware section integrated within the SoC
- Hardware partition prevents any access from rest of SoC
- No pre- or post-processing artifacts to compromise platform trustability
- Full visibility of SoC and system
- No dependency on application software
- No performance impact on application

18. Revision History

Table 22: Document Revision History (Sheet 1 of 2)

ISSUE	DATE	DESCRIPTION
1.50	January 30, 2024	• Deleted unbuffered DIMM (UDIMM) from *"Eight DDR4-3200 SDRAM Memory Controllers" on page 10* • Updated: – *Figure 14 (p. 87)* – Entries for *Rise time of both SDA and SCL signals* and *Fall time of both SDA and SCL signals* in *Table 21 on page 87*
1.45	December 15, 2023	• Updated: – Details for the package marking information in *Figure 2 on page 17* – Values for VDDC_RCA[0:3], VDDC_RCB[0:3], VDDC_SOC, and VDDC_SOC_CLKBUFF_AVDD in: ◦ *Table 7 on page 54* ◦ *Table 9 on page 65* ◦ *Table 10 on page 67* – Note 2 in *Table 20 on page 84*
1.40	August 9, 2023	• Updated: – *"Device Ordering Information" on page 7* (deleted the SKU stack and added a pointer to the list of SKUs on amperecomputing.com) – Values of VDDC_RCA[0:3], VDDC_RCB[0:3], VDDC_SOC, and VDDC_SOC_CLKBUFF_AVDD in *Table 7 on page 54*, *Table 8 on page 64*, *Table 9 on page 65*, and *Table 10 on page 67* • Removed support for DRAM throttling in *"Eight DDR4-3200 SDRAM Memory Controllers" on page 10* • Minor fixes and corrections
1.35	January 12, 2023	• Updated: – Package marking information in *Figure 2 on page 17* – Values of VDDC_PCP and VDDC_RCA[0:3] in *Table 7 on page 54* – *Table 8 on page 64* – Values of VDDC_PCP and VDDC_RCA[0:3] in *Table 9 on page 65*
1.30	July 28, 2022	• Added PQT_VDM_EXTVREF in *Table 9 on page 65* • Removed support for CCIX accelerator connectivity
1.27	March 31, 2022	• Updated the product branding
1.26	March 24, 2022	• Added *Usage Power* and *Est. SPECrate® 2017_int_base (SIR)* values in *"Device Ordering Information" on page 7*
1.25	December 30, 2021	• Updated the voltage range for VDDC_PCP for the QS80-33 SKU resulting in updates to: – *Table 8 on page 64* – *Table 9 on page 65* – *Table 10 on page 67* • Updated the values of 'Input Common Mode Voltage' in *Table 17 on page 82*

Table 22: Document Revision History (Sheet 2 of 2)

ISSUE	DATE	DESCRIPTION
1.20	September 23, 2021	• Updated: – *"Device Ordering Information" on page 7* – *"PCI Express (PCIe) Controller" on page 11* – *"Power Specifications" on page 78*
1.10	June 12, 2021	• Updated: – Estimated SPECrate® 2017_int_base value from '290' to '300' – *"Device Ordering Information" on page 7* with the Order Part Numbers for the Q64-22 and Q32-17 SKUs – *Table 5 on page 18* with the RFU_D2D pins on the package – *Table 7 on page 54* – *Table 14 on page 78* with the power specifications for the Q64-22 and Q32-17 SKUs – *Table 15 on page 80* with the thermal specifications for the Q64-22 and Q32-17 SKUs • Minor fixes and corrections
1.00	April 08, 2021	• Updated: – *"Device Ordering Information" on page 7* with the Mesh frequencies for all available SKUs – *"Generic Timer" on page 10* – *Table 8 on page 64* – *Table 14 on page 78* – *Table 15 on page 80*
0.95	December 23, 2020	• Updated: – *"Device Ordering Information" on page 7* to include data for additional SKUs – Package marking information in *Figure 2 (p. 17)* – Direction of the PQT_VDM_EXTVREF signal from Output to Input in *Table 7 on page 54* – *"Power-on Sequence for a 2P Configuration" on page 74* – Deleted the 'VDDC_D2D' signal from *Table 14 on page 78* – *Table 15 on page 80* to include data for additional SKUs – *Figure 13 (p. 84)* – Timing values for the SPI subsection in *Table 20 on page 84* – QSPI frequency to 33 MHz throughout the document
0.92	October 29, 2020	• Updated: – Estimated SPECrate® 2017_int_base value from '259+' to '290' – VDDC_PCP voltage range in *Table 9 on page 65 and Table 10 on page 67* – *"Power-on Sequence" on page 74* • Minor fixes and corrections
0.91	September 28, 2020	• Updated: – *"Device Ordering Information" on page 7* – *Table 14 on page 78*
0.90	September 18, 2020	Initial release.