MP5026

16V, 20A, 2.8mΩ $R_{DS(ON)}$, Hot-Swap Intelli-Fuse Solution

DESCRIPTION

The MP5026 is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients from its output. The device can achieve up to 20A of continuous output current (I_{OUT}) per device at room temperature.

The MP5026 limits the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the power supply voltage drop. The MP5026 also limits the internal MOSFET current (I_{FET}) by controlling the gate voltage (V_{GATE}) via a low-power resistor connected between the ISET pin and ground as well as soft-start ramp.

The MP5026 offers many features to simplify system design, such as an integrated current mirror that monitors I_{OUT} and the integrated on-die temperature sense. This eliminates the need for an external current-sense power resistor, power MOSFET, and temperature-sense device.

The maximum load at the output is current-limited via sense MOSFET topology. The current limit is controlled by a low-power resistor connected between ISET and ground.

The MP5026 provides a variety of fault protections, including over-current protection (OCP), short-circuit protection (SCP), over-temperature protection (OTP), damaged MOSFET detection, over-voltage protection (OVP), and under-voltage protection (UVP).

The MP5026 is available in an LGA-26 (4mmx4mm) package.

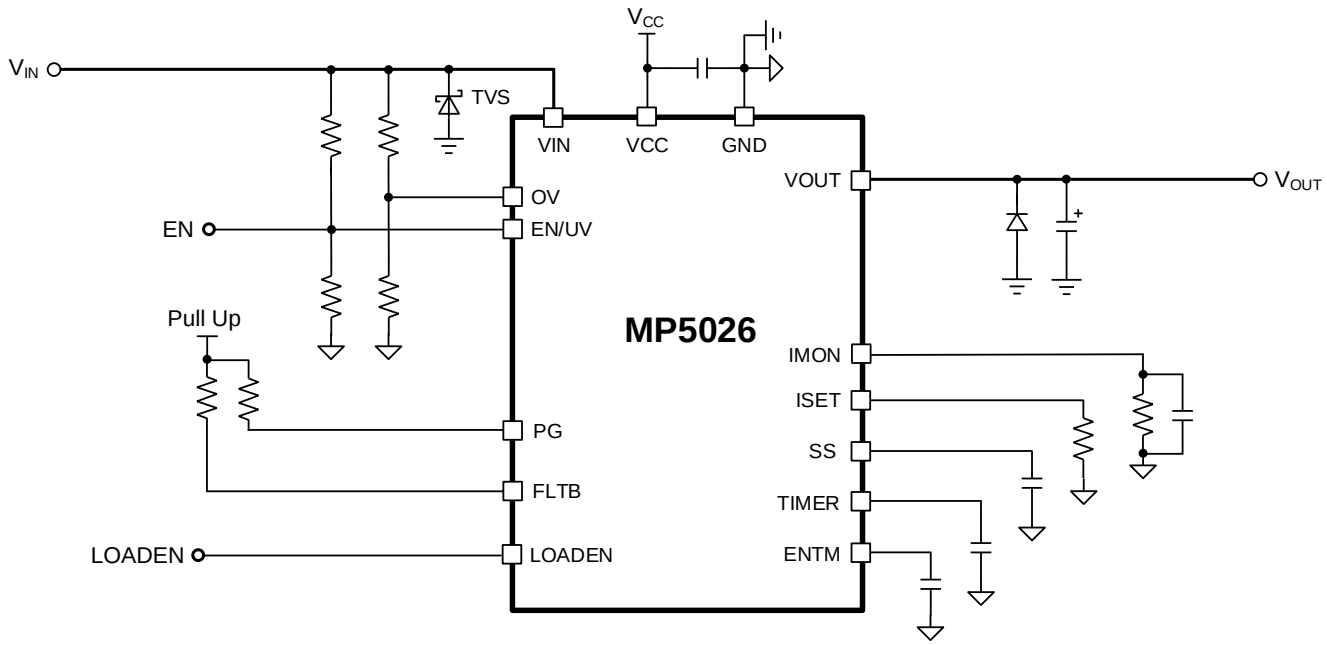
FEATURES

- 2.7V to 16V Operating Input Voltage (V_{IN}) Range
- Up to 20A Output Current (I_{OUT})
- 2.8mΩ Integrated Power MOSFET
- ±1% IMON Reporting Accuracy
- Built-In MOSFET Driver
- 3.3V Low-Dropout (LDO) Output
- Built-In Insertion Delay
- Configurable Soft Start (SS)
- Power Good (PG) Indication
- Fault Signal Output (FLTB)
- Integrated Current Sense with Sense Output (IMON)
- Configurable Over-Voltage Protection (OVP) Threshold
- Configurable Over-Current (OC) Limit
- Configurable Over-Current Protection (OCP) Fault Regulation Time
- Output Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP)
- Latch-Off Protection Mode
- Built-In Fuse Health Detection
- Available in an LGA-26 (4mmx4mm) Package

APPLICATIONS

- Hot Swap
- PC Cards
- Disk Drives
- Servers
- Networking
- Laptops

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5026GLRT	LGA-26 (4mmx4mm)	*See Below*	3

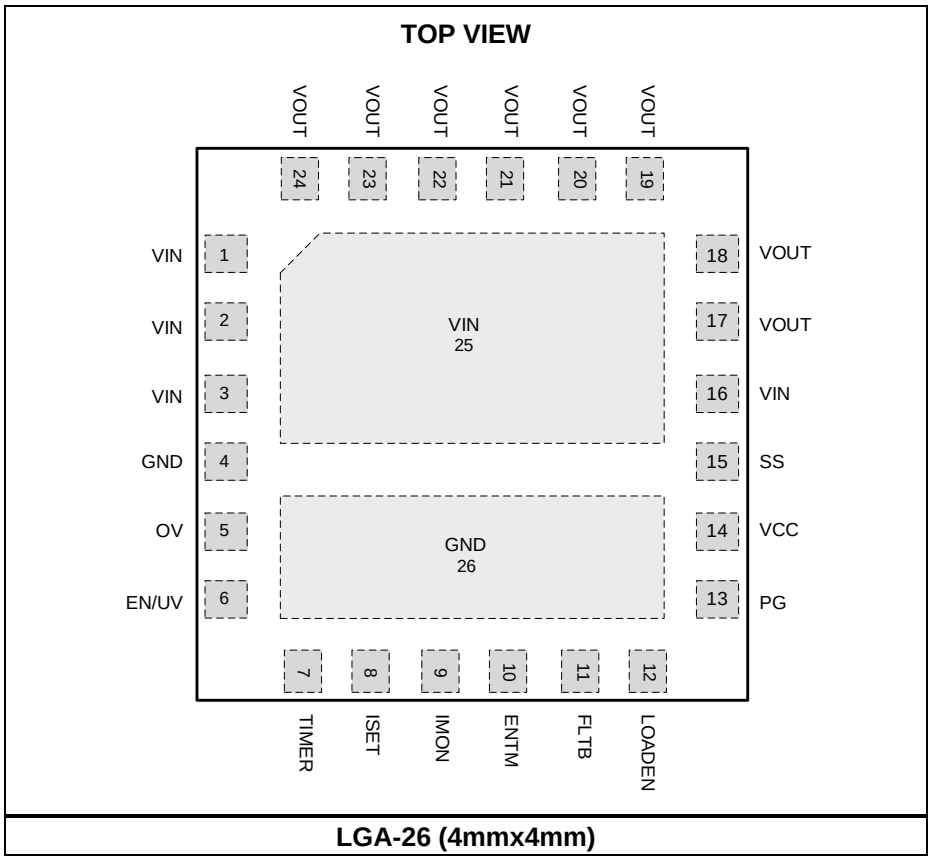
* For Tape & Reel, add suffix -Z (e.g. MP5026GLRT-Z).

TOP MARKING

MPSYWW
MP5026
LLLLLL
T

MPS: MPS prefix
Y: Year code
WW: Week code
MP5026: Part number
LLLLLL: Lot number
T: Thin package

PACKAGE REFERENCE



LGA-26 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3, 16, 25	VIN	**System input power supply.** The VIN pin is connected to the drain of the integrated power MOSFET.
4, 26	GND	**Ground.**
5	OV	**Over-voltage (OV) enable input.** Pull the OV pin high to turn off the internal MOSFET. Connect OV to an external resistor divider to set the over-voltage protection (OVP) threshold.
6	EN/UV	**Enable (EN) control and input voltage (V_{IN}) under-voltage lockout (UVLO) configuration.** The EN/UV pin is the control input that turns the device on and off, including the logic and power MOSFET. Pull EN/UV high to turn the device on; pull EN/UV low to turn it off. Connect EN/UV to a resistor divider between the VIN and GND pins to set the V_{IN} UVLO threshold. The internal VCC is not controlled by EN/UV. Do not float EN/UV.
7	TIMER	**Timer configuration.** Connect the TIMER pin to an external capacitor to set the hot-plug insertion delay time (t_{IDT}) and over-current (OC) fault time-out period.
8	ISET	**Current limit configuration.** Place a resistor between the ISET pin and ground to set the OC limit.
9	IMON	**Output current monitor.** The IMON pin provides a voltage (V_{IMON}) proportional to the current flowing through the power device. Connect a resistor (R_{IMON}) to ground to set the IMON output voltage gain. Place a capacitor greater than 10nF in parallel with R_{IMON} during application. Do not float IMON.
10	ENTM	**LOADEN blanking time configuration.** Connect the ENTM pin to an external capacitor to set the LOADEN blanking time. Once the EN/UV pin is active, the timer starts and LOADEN de-assertion is blanked. If a fault occurs or EN/UV is pulled low during the blanking time, then the device shuts down. If LOADEN is pulled low, the device does not turn off until the blanking time ends.
11	FLTB	**Fault bar.** The FLTB pin is an open-drain output that is pulled to ground once a fault occurs. The following faults can trigger FLTB: OC fault, short-circuit fault, over-temperature (OT) fault, over-voltage (OV) fault, and drain-to-source (DS) or gate-to-source (GS) short. Pull up FLTB to an external power supply via a 10kΩ to 100kΩ resistor.
12	LOADEN	**Load enable input.** The LOADEN pin is used in conjunction with EN/UV to turn the MP5026's main power device on or off. LOADEN also shuts down the power MOSFET after the LOADEN blanking time finishes. The power MOSFET cannot be turned back on by only cycling the power on LOADEN.
13	PG	**Power good.** The PG pin is an open-drain output. Pull PG up to an external power supply via a 10kΩ to 100kΩ resistor. PG high indicates power good.
14	VCC	**Internal 3.3V low-dropout (LDO) output.** Place a 1µF decoupling capacitor close to the VCC and GND pins.
15	SS	**Soft start.** Connect the SS pin to an external capacitor to set the soft-start time (t_{SS}) of the output voltage (V_{OUT}). The internal circuit controls the V_{OUT} slew rate at start-up. Float SS to set t_{SS} to the minimum time (1ms).
17, 18, 19, 20, 21, 22, 23, 24	VOUT	**Output voltage.** Connect the VOUT pin to the source of the integrated power MOSFET. Place a Schottky diode between the VOUT and GND pins to absorb the negative voltage spike.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} (DC).....-0.3V to +20V
V_{IN} (1µs)..... 24V
V_{IN} (25ns)..... 29V
V_{OUT}.....-0.3V to +20V
V_{OUT} (200ns) .....-1.5V
All other pins .....-0.3V to +4.2V
Continuous power dissipation (T_A = 25°C) (2)
..... 4.09W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +155°C

ESD Ratings (3)

Human body model (HBM).....Class 1C
Charged-device model (CDM).....Class C2B

Recommended Operating Conditions (4)

Input voltage (V_{IN}) .....2.7V to 16V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TLGA-26 (4mmx4mm).....30.5 ....26.3 . °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_{Q_IN}	Intelli-Fuse is on, no load		2.1	2.7	mA
		Fault protection, latch-off mode		1.9	2.4	mA
		Intelli-Fuse is off, EN/UV = 0, V_{IN} = 12V		1.6	2.5	mA
		Intelli-Fuse is off, EN/UV = 0, V_{IN} = 16V		1.65	2.5	mA
VCC Regulator and Under-Voltage Lockout (UVLO)						
VCC regulator output voltage	V_{CC}	I_{VCC} = 0mA	3.1	3.37	3.5	V
		I_{VCC} = 10mA		3.36		V
		I_{VCC} = 20mA		3.35		V
V_{CC} under-voltage lockout (UVLO) rising threshold	$V_{CC\_VTH\_R}$		2.36	2.46	2.56	V
V_{CC} UVLO falling threshold	$V_{CC\_VTH\_F}$		2.2	2.3	2.4	V
V_{CC} UVLO hysteresis	V_{CC_HYS}			160		mV
VIN Regulator and UVLO						
V_{IN} UVLO rising threshold	$V_{IN\_VTH\_R}$		2.46	2.56	2.66	V
V_{IN} UVLO falling threshold	$V_{IN\_VTH\_F}$		2.3	2.4	2.5	V
V_{IN} UVLO hysteresis	V_{IN_HYS}			160		mV
Enable and V_{IN} UVLO (EN/UV)						
EN/UV input rising threshold	V_{EN_R}		1.15	1.21	1.27	V
EN/UV input falling threshold	V_{EN_F}		1.05	1.1	1.17	V
EN/UV hysteresis	V_{EN_HYS}			110		mV
EN/UV blanking time	t_{EN/UV_BLANK}	Cycle the power on EN/UV		1.3		ms
Over-Voltage (OV)						
OV input rising threshold	V_{OV_R}		1.15	1.21	1.27	V
OV input falling threshold	V_{OV_F}		1.075	1.135	1.195	V
OV hysteresis	V_{OV_HYS}			75		mV
Power MOSFET						
On resistance	$R_{DS(ON)}$	T_J = 25°C, I_{OUT} = 2A, V_{IN} = 12V		2.8		mΩ
		T_J = 25°C, I_{OUT} = 2A, V_{IN} = 2.7V		2.8		
		T_J = 125°C, I_{OUT} = 2A, V_{IN} = 12V (6)		3.8		
		T_J = 125°C, I_{OUT} = 2A, V_{IN} = 2.7V (6)		3.8		
Off-state leakage current	I_{OFF}	V_{IN} = 16V, power MOSFET off			1	μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Current Monitor Output (IMON)						
IMON sense gain	I_{IMON} / I_{FET}	I_{OUT} > 3A	19.8	20	20.2	μA/A
IMON sense offset		I_{OUT} > 3A	-0.5		+0.5	μA
Current Limit						
ISET voltage	V_{ISET}		-3%	0.6	+3%	V
Over-current (OC) internal current-sense gain		1/10 of IMON gain		2		μA/A
Current limit during normal operation	I_{OC_NOR}	R_{ISET} = 12kΩ	-6%	25	+6%	A
Current limit at soft start	I_{OC_SS}	I_{OC_NOR} < 20A, V_{OUT} < 90% of V_{IN}		I_{OC_NOR}		A
		I_{OC_NOR} > 20A, V_{OUT} < 90% of V_{IN}		20		A
OC regulation time at soft start	t_{OC_REG}			1.5		ms
Short-circuit current limit	I_{SC}			50		A
Short-circuit protection (SCP) response time (6)	t_{SCP}			200		ns
TIMER						
Upper threshold	V_{TIMER_H}		1.11	1.21	1.31	V
Insertion delay charge current	I_{INSRT}		3.35	4	4.65	μA
Over-current protection (OCP) fault timeout charge current	I_{FLT_TIMER}		33.5	40	46.5	μA
Discharge on resistance	R_{TIMER}			10		Ω
Soft Start (SS)						
SS pull-up current	I_{SS}	V_{IN} = 12V	11.5	13.5	15.5	μA
Fault Bar (FLTB)						
Output low voltage	V_{OL}	10mA sink current			0.3	V
Off-state leakage current	I_{LK}	V_{FLT} = 3.3V			1	μA
Power Good Output (PG)						
PG rising threshold	PG_{VTH_R}	V_{IN} = 12V	85%	90%	95%	% of V_{IN}
		V_{IN} = 2.7V		V_{IN} - 0.5		V
PG falling threshold	PG_{VTH_F}	V_{IN} = 12V	70%	75%	80%	% of V_{IN}
		V_{IN} = 2.7V		V_{IN} - 0.7		V
Output low voltage	V_{OL}	10mA sink current			0.3	V
Off-state leakage current	I_{LK}	V_{FLT} = 3.3V			1	μA
MOSFET Short Detection						
MOSFET drain-to-source (DS) short entry threshold	V_{DSTH_ENT}	V_{IN} = 12V	85%	90%	95%	% of V_{IN}
		V_{IN} = 2.7V		V_{IN} - 0.5		V
MOSFET DS short recovery threshold	V_{DSTH_EXT}	V_{IN} = 12V	70%	75%	80%	% of V_{IN}
		V_{IN} = 2.7V		V_{IN} - 0.7		V
Gate-to-source (GS) short protection delay time (6)	t_{GS_ST}	V_{SS} > V_{CC} - 0.7	150	200	250	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
ENTM						
ENTM rising threshold	V_{ENTM_R}		1.15	1.2	1.25	V
Charge current	I_{ENTM}		0.8	1.1	1.4	µA
LOADEN						
LOADEN low voltage	V_{LOADEN_L}				0.8	V
LOADEN high voltage	V_{LOADEN_H}		2			V
Thermal Shutdown						
Over-temperature (OT) threshold (6)	T_{J_OTP}			148		°C

Note:

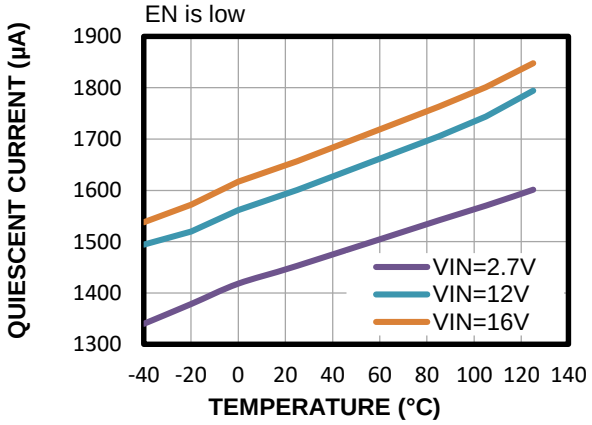
6) Guaranteed by design.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, R_{ISET} = 12kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

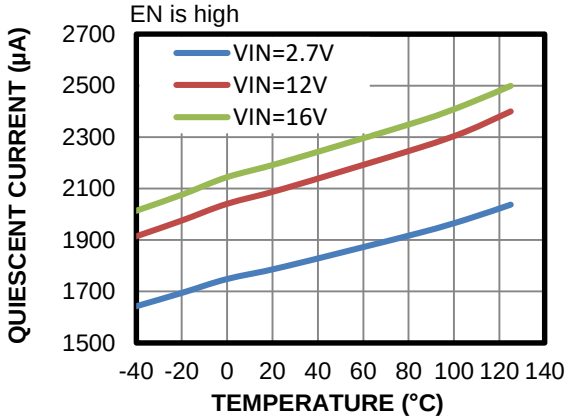
Quiescent Current vs. Temperature

EN is low

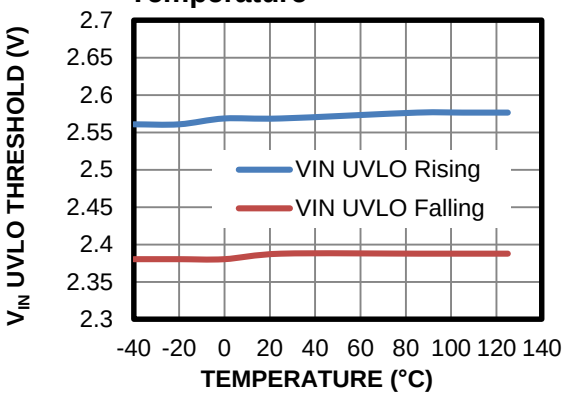


Quiescent Current vs. Temperature

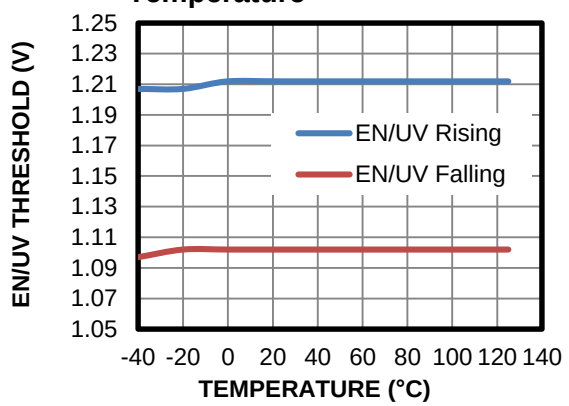
EN is high



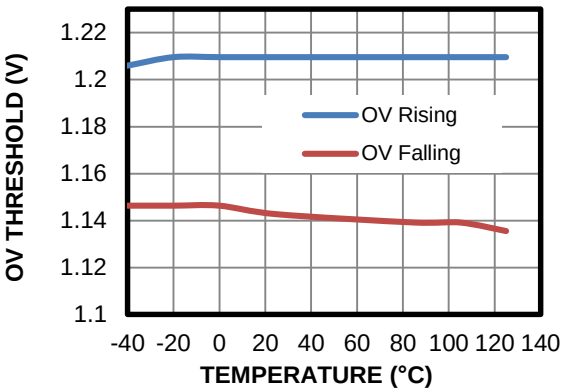
V_{IN} UVLO Threshold vs. Temperature



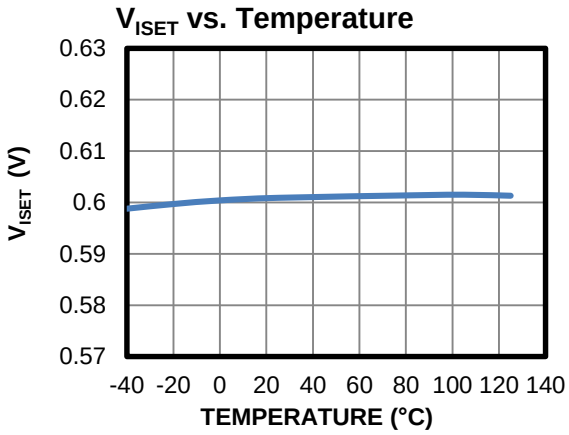
EN/UV Threshold vs. Temperature



OV Threshold vs. Temperature



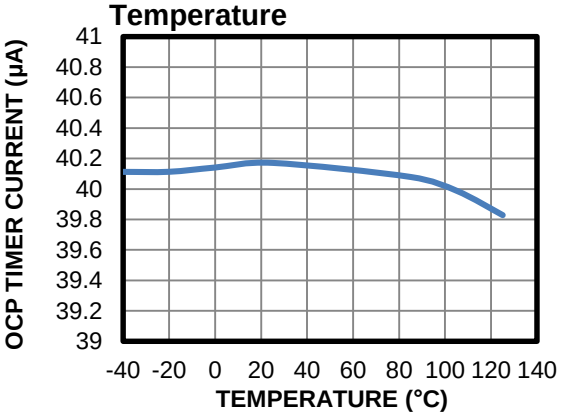
V_{ISET} vs. Temperature



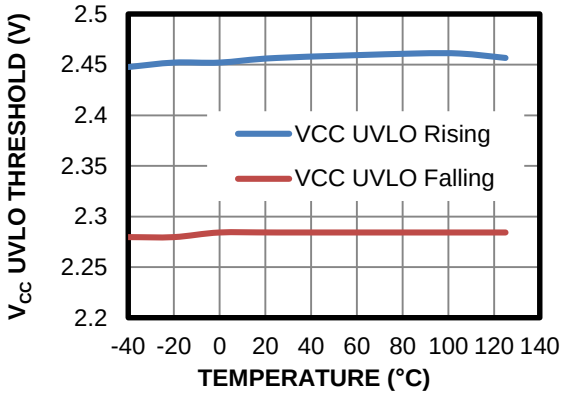
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{ISET} = 12kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

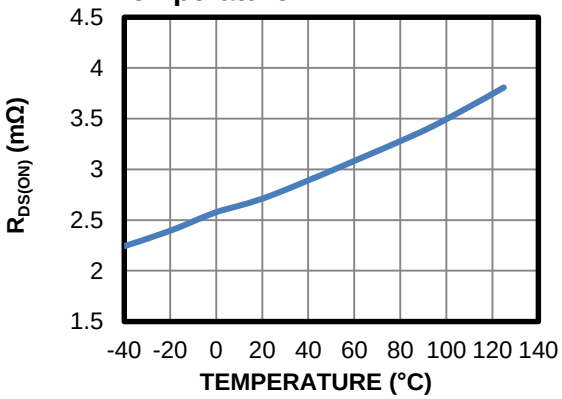
OCP Timer Current vs. Temperature



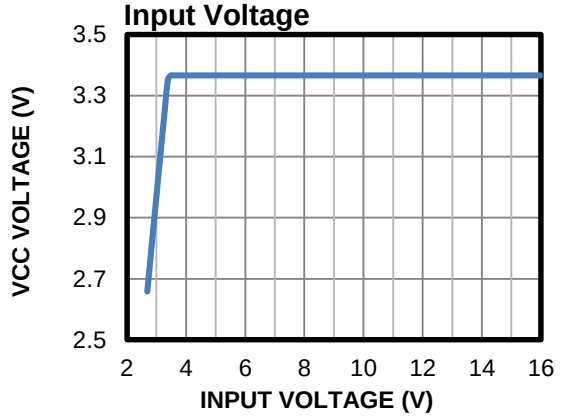
V_{CC} UVLO Threshold vs. Temperature



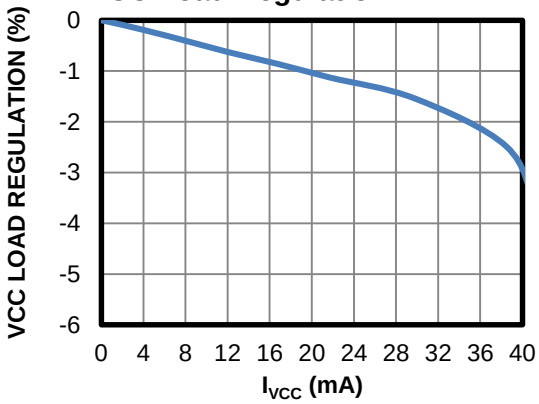
On Resistance vs. Temperature



VCC Voltage vs. Input Voltage

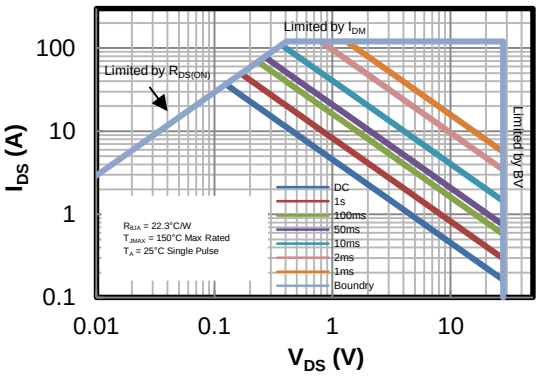


VCC Load Regulation



Safe Operating Area (SOA)

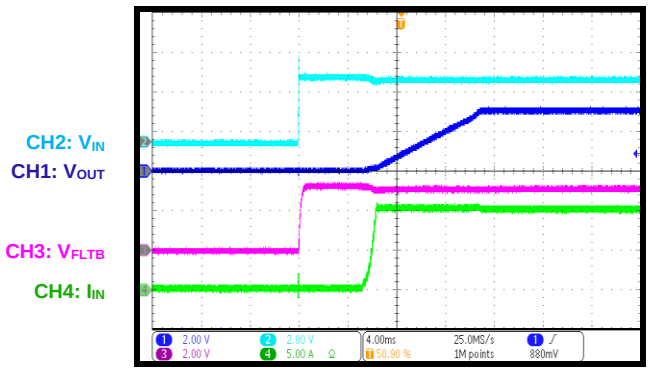
Tested on the EV5026-V-00A (6.35cmx 7.15cm), 4-layer PCB, 2oz per layer



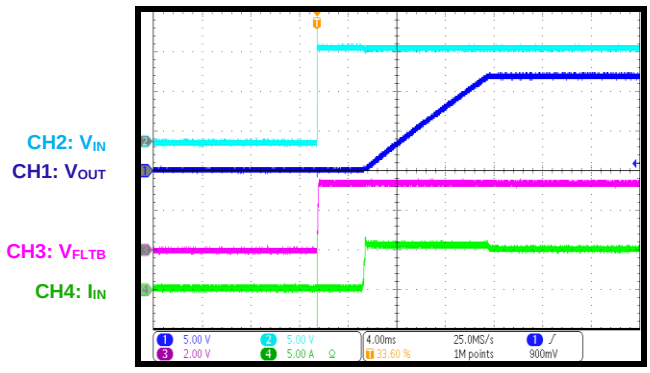
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, R_{ISET} = 12kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

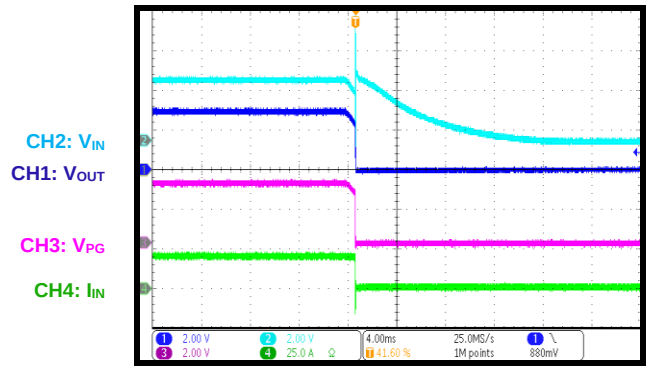
VIN Hot Plug
V_{IN} = 3.3V, I_{OUT} = 10A



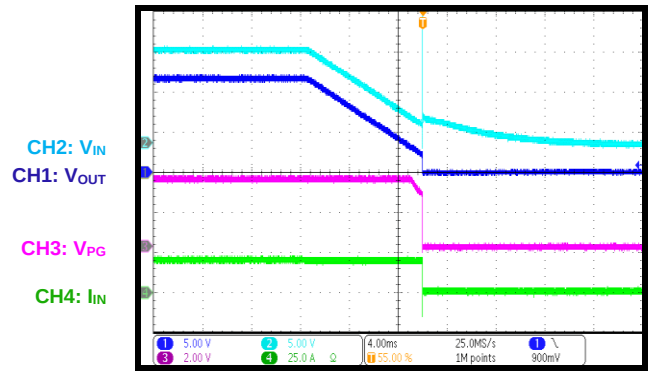
VIN Hot Plug
V_{IN} = 12V, I_{OUT} = 5A



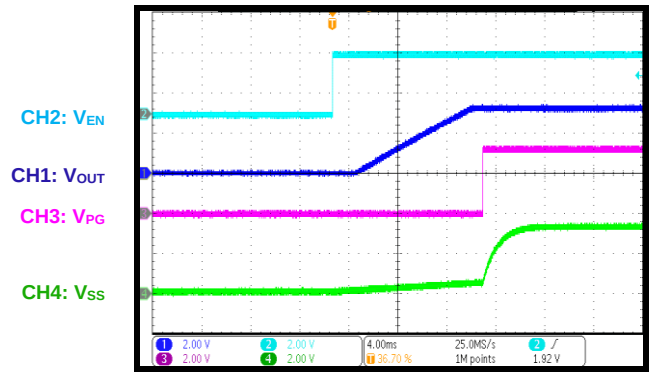
Shutdown through VIN
V_{IN} = 3.3V, I_{OUT} = 20A



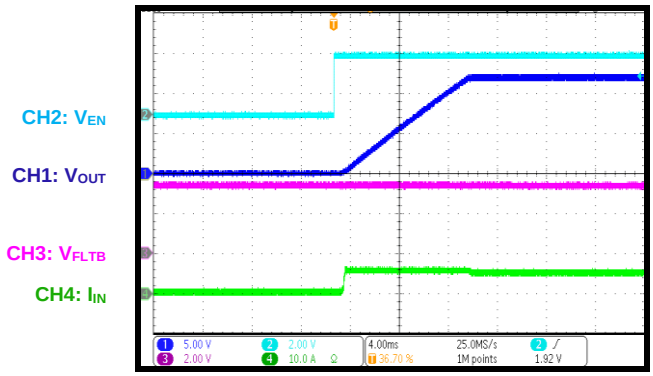
Shutdown through VIN
V_{IN} = 12V, I_{OUT} = 20A



Start-Up through EN/UV
V_{IN} = 3.3V, I_{OUT} = 0A



Start-Up through EN/UV
V_{IN} = 12V, I_{OUT} = 5A

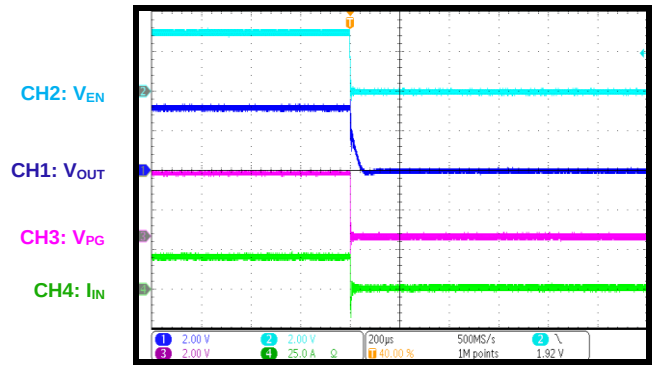


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{ISET} = 12kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

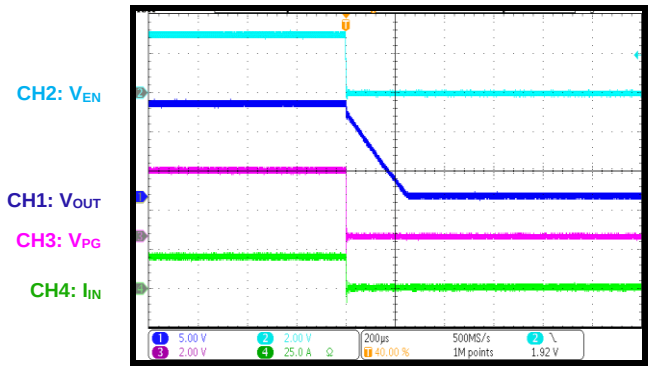
Shutdown through EN/UV

V_{IN} = 3.3V, I_{OUT} = 20A



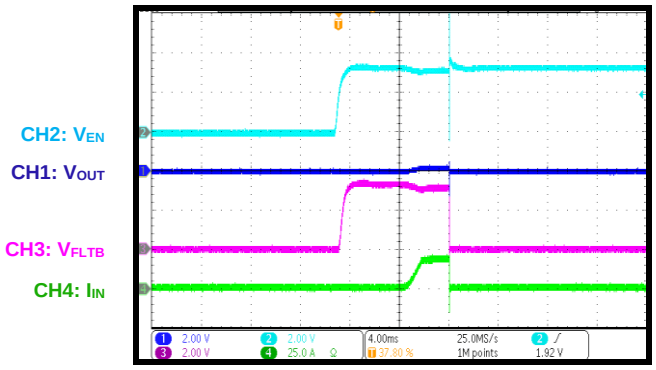
Shutdown through EN/UV

V_{IN} = 12V, I_{OUT} = 20A



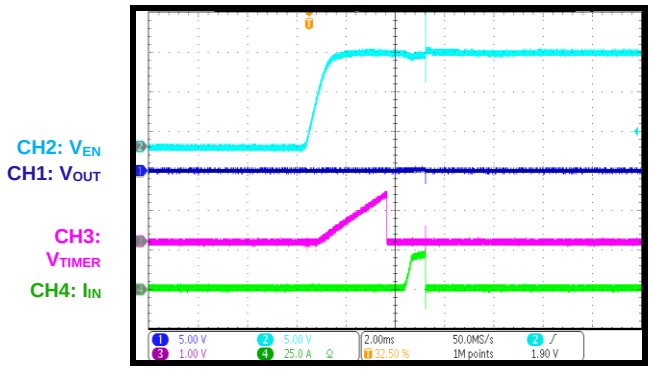
Short-Circuit Start-Up

V_{IN} = 3.3V



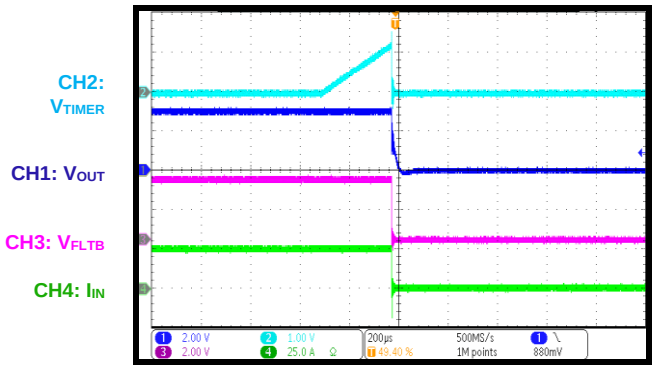
Short-Circuit Start-Up

V_{IN} = 12V



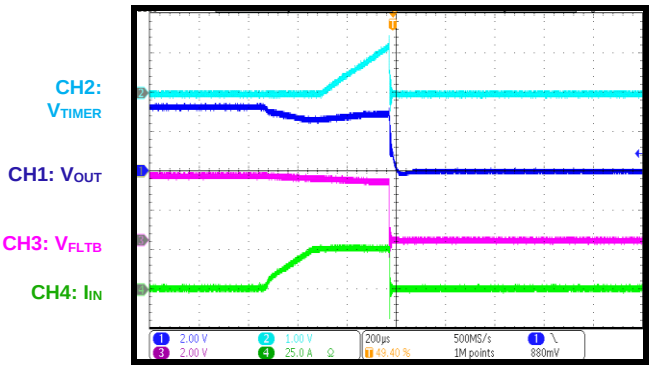
Over-Current Protection

V_{IN} = 3.3V, add load to 25A slowly



Over-Current Protection

V_{IN} = 3.3V, add load to 25A quickly

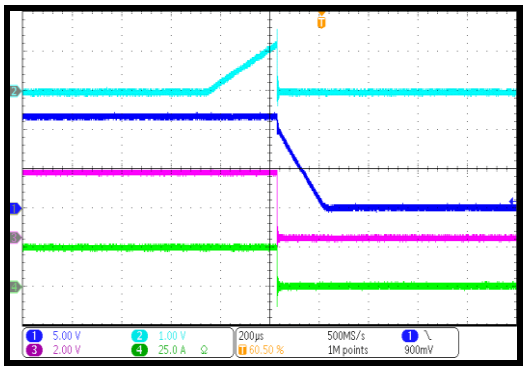


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{ISET} = 12kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

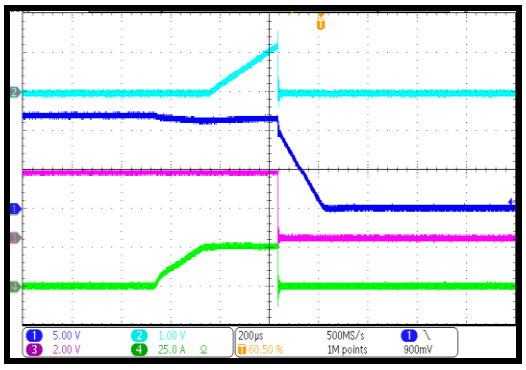
Over-Current Protection

V_{IN} = 12V, add load to 25A slowly



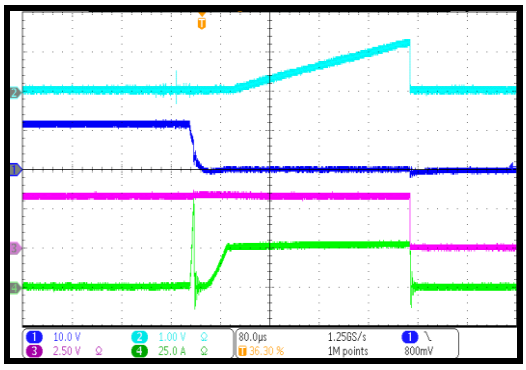
Over-Current Protection

V_{IN} = 12V, add load to 25A quickly

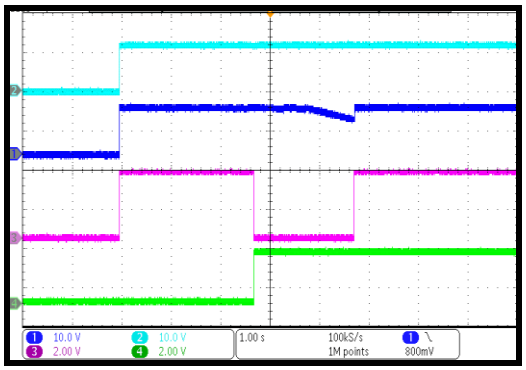


Short-Circuit Protection

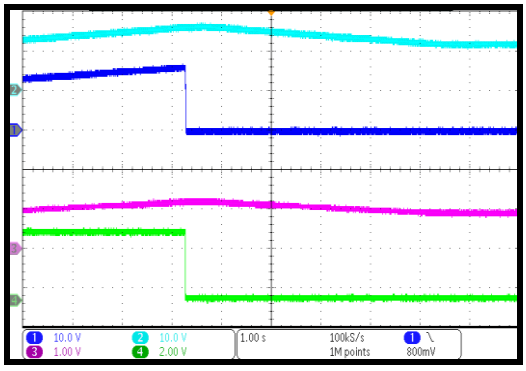
V_{IN} = 12V



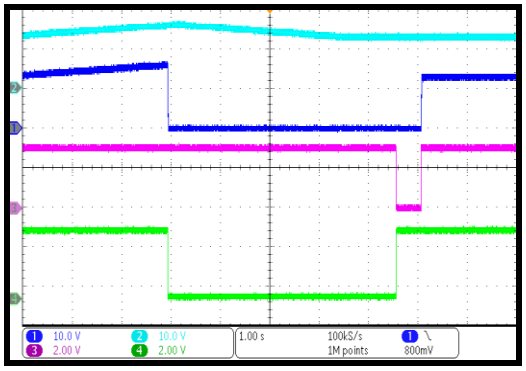
Drain-to-Source Short



V_{IN} OVP Shutdown



V_{IN} OVP Recovery



FUNCTIONAL BLOCK DIAGRAM

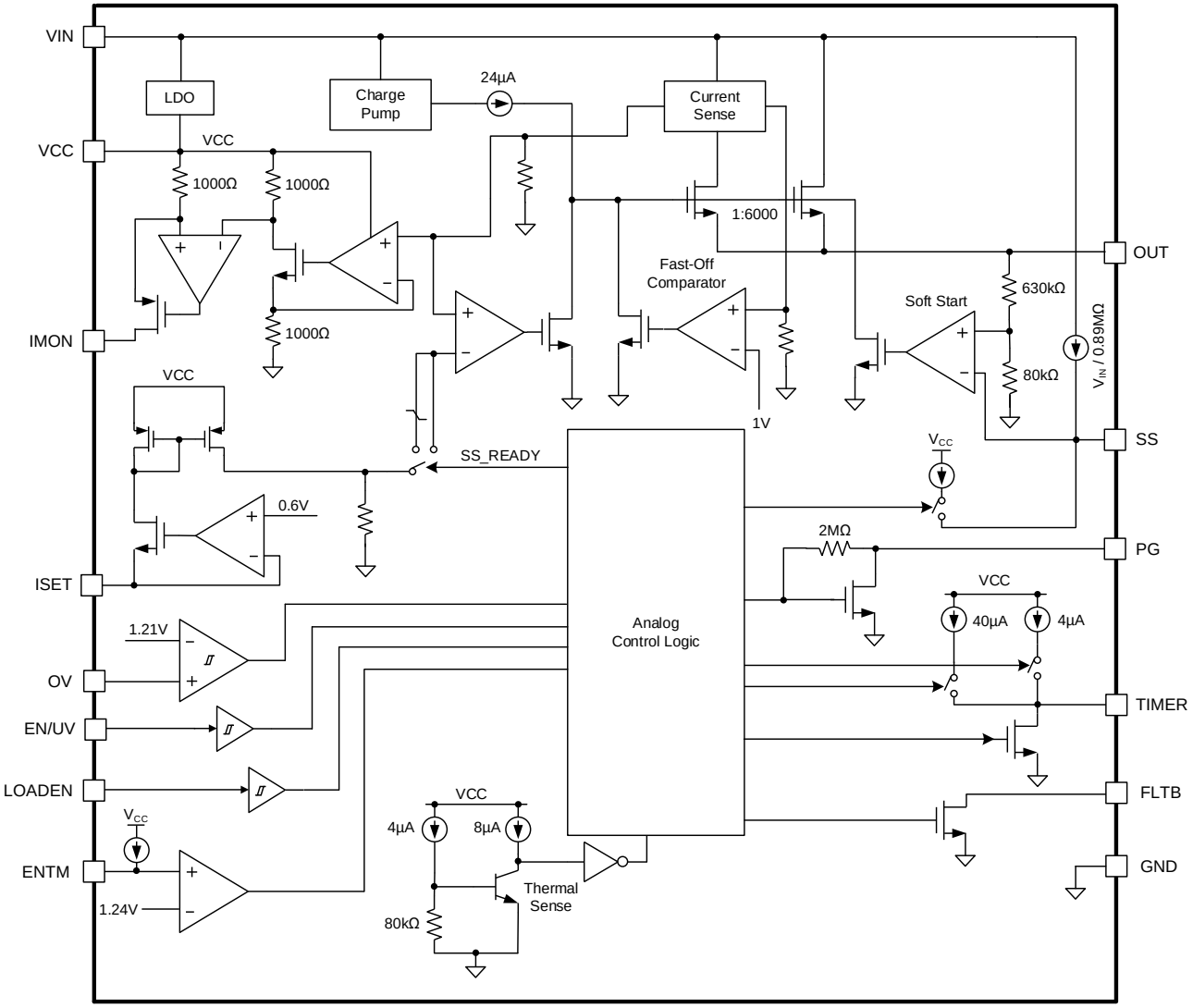


Figure 1: Functional Block Diagram

OPERATION

The MP5026 is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the backplane voltage drop and the dV/dt of the voltage to the load. The device provides an integrated solution for monitoring the input voltage (V_{IN}), output voltage (V_{OUT}), output current (I_{OUT}), and die temperature to eliminate the need for an external current-sense power resistor, power MOSFET, and temperature-sense device.

The maximum load at the output is current-limited via sense MOSFET topology. The current limit is controlled by a low-power resistor connected between the ISET pin and ground.

The MP5026 provides a variety of fault protections, including over-current protection (OCP), short-circuit protection (SCP), over-temperature protection (OTP), damaged MOSFET detection, over-voltage protection (OVP), and under-voltage protection (UVP).

Start-Up Sequence

For hot-swap applications, the MP5026's input can experience a voltage spike or transient during the hot-plug process. This is caused by the parasitic inductance of the input trace and the input capacitor. To help stabilize V_{IN}, an insertion delay is implemented before the main MOSFET turns on (see Figure 2).

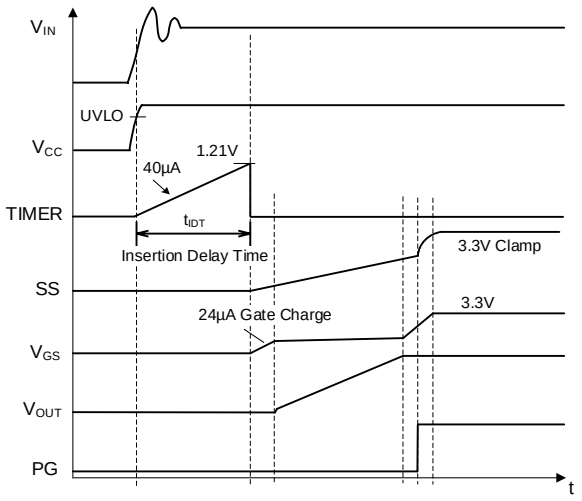


Figure 2: Start-Up Sequence

After V_{IN} and the VCC voltage (V_{CC}) exceed their respective under-voltage lockout (UVLO) thresholds, the TIMER pin charges the external timer capacitor (C_{TMR}) (nF) via a 4µA constant-current source.

The insertion delay time (t_{IDT}) is the time period during which C_{TMR} is charged from 0V to 1.21V via the internal 4µA current source. To set t_{IDT}, select a sufficient capacitance from TIMER to ground. t_{IDT} can be determined with Equation (1):

$$t_{IDT}(ms) = \frac{1.21}{4} \times C_{TMR}(nF) \quad (1)$$

For example, a 10nF capacitor requires a 3ms t_{IDT}.

Once t_{IDT} finishes and the EN/UV pin exceeds 1.4V, the MOSFET is charged via the internal 24µA charge pump. If the gate-to-source (GS) voltage (V_{GS}) exceeds its threshold (V_{GS_TH}), the MOSFET turns on and V_{OUT} rises.

Soft Start (SS)

A soft-start capacitor (C_{SS}) determines the soft-start time (t_{SS}). If EN/UV is pulled high and t_{IDT} finishes, a constant-current source proportional to V_{IN} charges the soft-start voltage (V_{SS}). This enables a constant t_{SS} independent of V_{IN}. V_{OUT} rises at a similar slew rate to V_{SS}.

C_{SS} can be calculated with Equation (2):

$$C_{SS}(nF) = 9 \times \frac{t_{SS}(ms)}{R_{SS}(M\Omega)} \quad (2)$$

Where the soft-start resistance (R_{SS}) is 0.89MΩ.

For example, a 100nF capacitor sets t_{SS} to 9.9ms. If the load capacitance is extremely large, then the current required to maintain the preset t_{SS} should exceed the start-up current limit. Then the rise time is controlled by the load capacitor (C_{LOAD}) and the start-up current limit.

Float the SS pin to generate a fast ramp-up voltage. A 24µA current source pulls up the power MOSFET gate. The gate charge current controls the V_{OUT} rise time, and t_{SS} is about 1ms, which is the minimum V_{OUT} t_{SS}.

EN/UV and LOADEN

The EN/UV and LOADEN pins control the MP5026's on and off status (see Table 1).

During the LOADEN blanking time, EN/UV high is sufficient to turn the MOSFET on. After the LOADEN blanking time expires, EN/UV and LOADEN must be pulled high to turn the device on. Pull EN/UV low to turn the MOSFET off. Cycle the power on EN/UV or VIN to restart the chip once it is latched off.

Table 1: EN/UV and LOADEN Blanking Time

Is the LOADEN Blanking Time Complete?	EN/UV	LOADEN	Status
No	0	0	Off
No	0	1	Off
No	1	0	On
No	1	1	On
Yes	0	0	Off
Yes	0	1	Off
Yes	1	0	Off
Yes	1	1	On

Note that LOADEN shuts down the power MOSFET after the LOADEN blanking time finishes. However, LOADEN cannot turn the power MOSFET on by cycling the power on LOADEN only (see Figure 3).

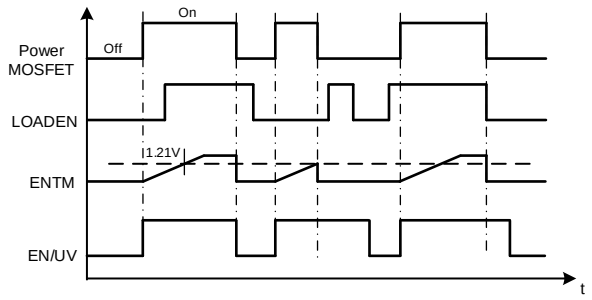


Figure 3: EN/UV and LOADEN Timing Diagram

If V_{IN} and V_{CC} are ready when the part is enabled, the internal 24μA current source charges the power MOSFET's gate. It takes about 1ms to charge V_{GS} to its threshold. Then V_{OUT} rises based on the SS-controlled slew rate.

LOADEN Blanking Time

LOADEN has a configurable blanking time that prevents the pin from de-asserting during the blanking time (see Figure 4).

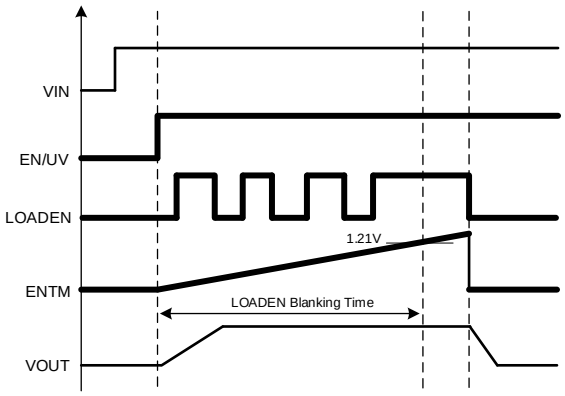


Figure 4: LOADEN Blanking Time

Since all fault functionalities are operative during start-up, the power MOSFET shuts down if a fault is detected. However, LOADEN going low during this blanking time does not turn the MOSFET off. At the end of the blanking time, LOADEN operates normally.

The LOADEN blanking time (t_{LDNB}) can be set by a capacitor placed at the ENTM pin. The LOADEN blanking time capacitor (C_{ENTM}) can be calculated with Equation (3):

$$C_{ENTM}(\mu F) = \frac{1.1}{1.24} \times t_{LDNB}(s) \quad (3)$$

For example, a 1μF capacitor requires a 1.13s t_{LDNB}. If LOADEN is not used, connect ENTM to GND.

Over-Current Protection (OCP)

The MP5026 provides a constant current limit that can be configured via an external resistor. The Intelli-Fuse over-current limit (I_{LIMIT}) is a function of the ISET resistor (R_{ISET}). I_{LIMIT} can be calculated with Equation (4):

$$I_{LIMIT}(A) = \frac{0.3V}{R_{ISET}(k\Omega)} \times 10^3 \quad (4)$$

If V_{OUT} is below the larger value between V_{IN} - 0.5V and 80% of V_{IN}, then the MP5026 enters start-up. To protect the device from overheating during start-up, I_{LIMIT} has a 20A internal current limit clamp. The actual start-up current limit (I_{LIMIT_SS}) is the smaller value between I_{LIMIT} and 20A (see Figure 5 on page 17).

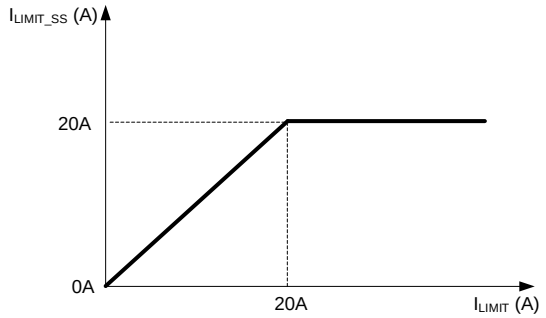


Figure 5: Start-Up and Normal Current Limit

The MP5026 exits start-up when V_{OUT} exceeds the larger value between V_{IN} - 0.5V and 80% of V_{IN}, and the power MOSFET gate voltage is close to the internal charge pump voltage.

Once the MP5026 detects that start-up has finished, the internal 20A current limit clamp is disabled. The current limit during normal operation (I_{OC_NOR}) is determined by I_{LIMIT} only.

When the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold constant current in the power MOSFET. The typical response time is about 20µs.

Intelli-Fuse Over-Current Protection (OCP) during Start-Up

During start-up, if the current through the MP5026 is regulated by the SS current limit (I_{LIMIT_SS}) for the soft-start over-current (OC) regulation time (t_{OC_REG}), the gate stops regulating and pulls low. Then the soft-start OC fault is triggered, the power MOSFET shuts down, and the FLTB and SS pins are pulled low (see Figure 6).

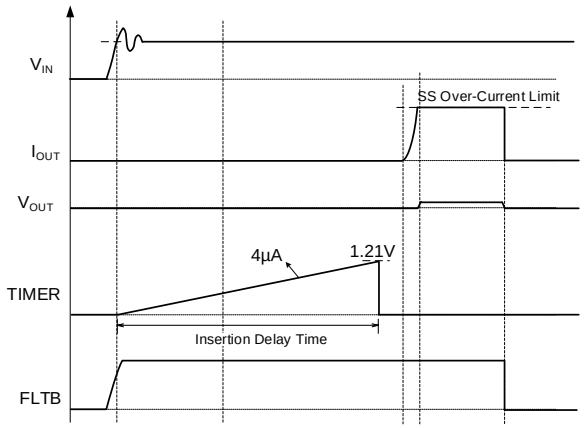


Figure 6: Soft-Start OCP Behavior

The typical t_{OC_REG} is 1.5ms, where the actual regulation time depends on the device's safe operating area (SOA). If OTP is triggered during t_{OC_REG}, the power MOSFET shuts down immediately.

Over-Current Protection (OCP) during Normal Operation

Once soft start completes, the MP5026 enters normal operation. If I_{LIMIT} is triggered, the fault timer starts. If I_{OUT} drops below I_{LIMIT} before the fault timeout period completes, then the MP5026 resumes normal operation. Otherwise, if the OC fault remains longer than the fault timeout period, the power MOSFET latches off. The OCP fault time (t_{OC}) can be determined with Equation (5):

$$t_{OC}(ms) = \frac{1.21}{40} \times C_{TMR}(nF) \quad (5)$$

For example, a 10nF capacitor requires a 0.3ms t_{OC}.

If the MP5026 reaches I_{LIMIT}, FLTB is pulled low with an 8µs propagation delay to indicate a fault (see Figure 7).

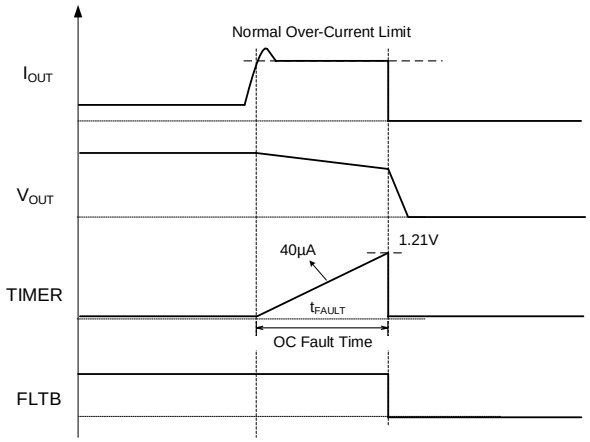


Figure 7: Normal OCP Behavior

Short-Circuit Protection (SCP)

If the load current (I_{LOAD}) increases rapidly due to a short circuit, then the current may exceed I_{LIMIT} significantly before the hot-swap control loop can respond. If the Intelli-Fuse current reaches the short-circuit current limit (I_{LIMIT_SC}) (typically 50A), then a fast turn-off circuit in the Intelli-Fuse is activated to turn the power MOSFET off. This limits the peak current through the MOSFET to limit the V_{IN} drop. The total short-circuit response time is about 200ns.

Once V_{GS} drops low, the MP5026 attempts to start up again faster to avoid V_{IN} line transients. The MOSFET gate is charged by an internal charge pump. If V_{GS} exceeds V_{GS_TH}, the device turns on. If the short condition remains, I_{LOAD} is limited by I_{LIMIT}. The fault timer ramps to 1.21V if the fault is not removed, and then the MP5026's power MOSFET turns off and FLTB is pulled low (see Figure 8).

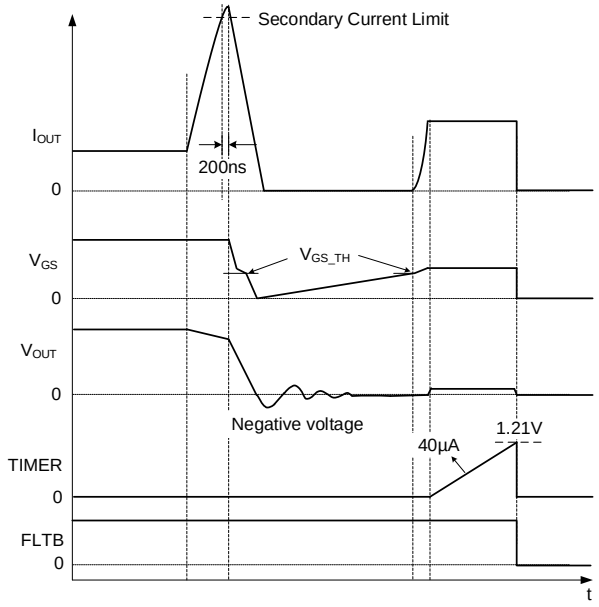


Figure 8: SCP Behavior

When a hard short occurs and V_{IN} is pulled below V_{CC} quickly, the power MOSFET gate voltage is pulled low immediately, regardless of whether the secondary current limit has been reached or not. The power MOSFET then retries once more with the same short-circuit condition present.

If the short persists after the timer expires, FLTB switches low.

Over-Voltage Protection (OVP)

The MP5026 provides internal voltage sensing to monitor V_{IN}. Connect a resistor divider between the VIN and AGND pins to set the input over-voltage (OV) threshold (V_{OV}) (see Figure 9).

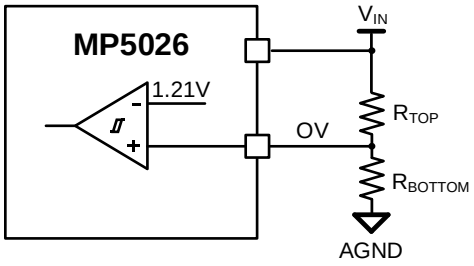


Figure 9: OV Connection

V_{OV} can be calculated with Equation (6):

$$V_{OV}(V) = 1.21 \times \left(1 + \frac{R_{TOP}}{R_{BOTTOM}}\right) \quad (6)$$

Regardless of whether EN/UV is high or low, OV detection and functionality remain active. If V_{OV} exceeds its rising threshold (V_{OV_R}) (typically 1.21V), then the power MOSFET turns off, and the FLTB and SS pins are pulled low. If V_{OV} drops below its falling threshold (V_{OV_F}), then the device can restart by cycling the power on VIN or EN/UV (see Figure 10). To disable OVP, connect the OV pin to GND.

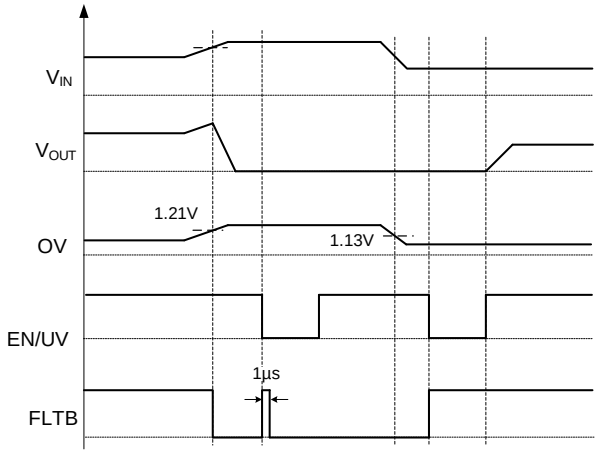


Figure 10: OV Protection Behavior

Power Good (PG)

Power good (PG) is an open-drain output that indicates whether V_{OUT} is within the normal range relative to V_{IN}. Pull PG up to the external power supply or VCC via a 10kΩ to 100kΩ resistor. During start-up, the PG output is pulled low, which commands the system to remain off and minimize the load on VOUT. As a result, inrush current and power dissipation is reduced during start-up.

The device must meet the following conditions to pull the PG signal high and for the system to draw full power:

- V_{OUT} > 90% of V_{IN}
- V_{GS} > 2V
- V_{OUT} > V_{IN} - 0.5V

PG indicates low if the device meets any of the following conditions:

- V_{OUT} < 75% of V_{IN}
- EN/UV is low
- Faults occur

If a pull-up supply is present without an input, PG remains logic low.

Fault Bar (FLTB)

Fault bar (FLTB) is an open-drain output that indicate whether a fault has occurred. Pull FLTB up to an external power supply or VCC via a 10kΩ to 100kΩ resistor.

FLTB is pulled low with an 8μs propagation delay if any of the following protections are triggered: OCP, SCP, OTP, OVP, or drain-to-source (DS) or gate-to-source (GS) short protection.

If any of these fault protections are triggered, FLTB indicates low and latches. After the fault condition is removed, the MP5026 can resume normal operation by cycling the power on VIN, VCC, or EN/UV.

If a DS short is detected, FLTB asserts low and holds until V_{OUT} drops below the DS short detection falling threshold.

Additional Protections

The MP5026 provides additional protections, including OTP, DS short detection, and GS short detection.

Over-Temperature Protection (OTP)

The MP5026 senses the junction temperature (T_J) internally. Once T_J exceeds 148°C, the power MOSFET shuts down and FLTB indicates low.

Drain-to-Source (DS) Short Detection

The internal DS short detection circuit starts to work when V_{IN} and V_{CC} exceed their respective UVLO thresholds. Once the device enters t_{SS}, it no longer detects the DS short condition. If V_{OUT} exceeds the smaller value between V_{IN} - 0.5V and 90% of V_{IN} during the detection period, the internal DS short flag is set.

If the following conditions are met, a DS short occurs:

- Internal DS short flag is set
- EN/UV is high
- t_{IDT} ends

Afterward, FLTB is pulled low, and the GATE voltage remains low to disable the power MOSFET.

DS short is a live protection. Once V_{OUT} drops below the smaller value between V_{IN} - 0.7V and 75% of V_{IN}, the device resumes normal operation and FLTB releases high.

Gate-to-Source (GS) Short Detection

If the following conditions are met, the device determines whether a GS short has occurred and shuts down the power MOSFET:

- V_{GATE} < V_{CP} - 0.9V
- V_{SS} > V_{CC} - 0.7V
- No OC fault has occurred
- 200ms delay

Where V_{CP} is the charge pump voltage.

APPLICATION INFORMATION

Selecting the Soft-Start Capacitor (C_{SS})

A capacitor connected to SS (C_{SS}) determines t_{SS}. V_{OUT} rises at a similar slew rate to the SS voltage (V_{SS}).

C_{SS} can be calculated with Equation (7):

$$C_{SS}(nF) = 9 \times \frac{t_{SS}(ms)}{R_{SS}(M\Omega)} \quad (7)$$

Where R_{SS} is 0.89MΩ.

Place a 100nF capacitor between SS and GND to achieve a 9.9ms t_{SS}.

Selecting the IMON Resistor (R_{IMON})

The MP5026 can monitor the power MOSFET current. Connect a resistor (R_{MON}) to ground to set the output gain.

The IMON current (I_{MON}) can be calculated with Equation (8):

$$I_{IMON} = I_{FET} \times 20\mu A/A \quad (8)$$

Where I_{FET} is the current flowing from the power MOSFET.

The IMON reference voltage (V_{IMON}) can be determined with Equation (9):

$$V_{IMON} = I_{IMON} \times R_{IMON} \quad (9)$$

Connect a 2kΩ resistor between IMON and GND to achieve a 40mV/A V_{IMON}. Place a capacitor greater than 10nF between IMON and GND to smooth the indicator voltage.

Do not float IMON. If not being used, connect IMON to GND.

To ensure that the internal current-sense circuit has sufficient headroom, the maximum VIMON voltage should be below V_{CC} - 1.5V (see Figure 11).

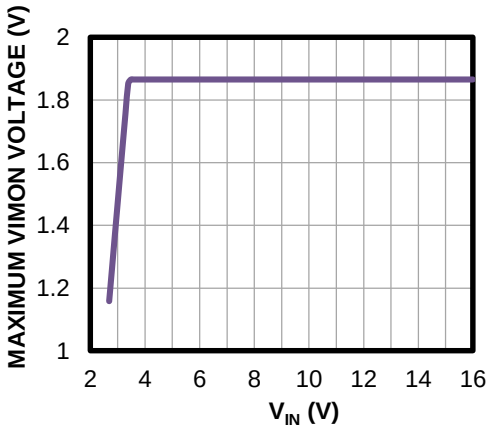


Figure 11: Maximum VIMON Range

Selecting the ISET Resistor (R_{ISET})

The MP5026's I_{LIMIT} should exceed the normal maximum I_{LOAD}, allowing for current-sense tolerances. I_{LIMIT} can be calculated with Equation (10):

$$I_{LIMIT}(A) = \frac{0.3V}{R_{ISET}(k\Omega)} \times 10^3 \quad (10)$$

Insertion Delay Time and OC Fault Timer Capacitor (C_{TMR})

The MP5026's TIMER pin provides two functions: t_{IDT} and t_{OC}.

t_{IDT} can be determined with Equation (11):

$$t_{IDT}(ms) = \frac{1.21}{4} \times C_{TMR}(nF) \quad (11)$$

t_{OC} can be determined with Equation (12):

$$t_{OC}(ms) = \frac{1.21}{40} \times C_{TMR}(nF) \quad (12)$$

Place a 10nF capacitor between TIMER and GND to achieve a 3ms t_{IDT} and 300µs t_{OC}.

PCB Layout Guidelines

Efficient PCB layout is critical for stable performance. A 4-layer layout is strongly recommended for improved thermal performance. For the best results, refer to Figure 12 and follow the guidelines below:

1. Place the MP5026 close to the board's input connector to minimize trace inductance.
2. Place a small input capacitor (e.g. 100nF) close to the VIN and GND pins to minimize transients on the input supply line. (Transients of several volts can occur easily if I_{LOAD} is shut off.)
3. Place a 1µF capacitor as close to VDD33 as possible.
4. Keep the high-current path between the board's input and load close to and in parallel with the return path to minimize loop inductance.
5. Connect the analog signal ground (AGND) plane to the PCB's power ground (PGND) planes at a single point.
6. Place multiple vias on the board for improved thermal performance:
   a. Place ≥6 vias on the bottom of the VIN pad.
   b. Place ≥3 vias on the bottom of the GND pad.
   c. Place ≥6 vias close to the MP5026's VIN and VOUT pads.
   d. Place ≥3 vias close to the pads of the input TVS.
   e. Place ≥3 vias close to the pads of the output Schottky diodes.

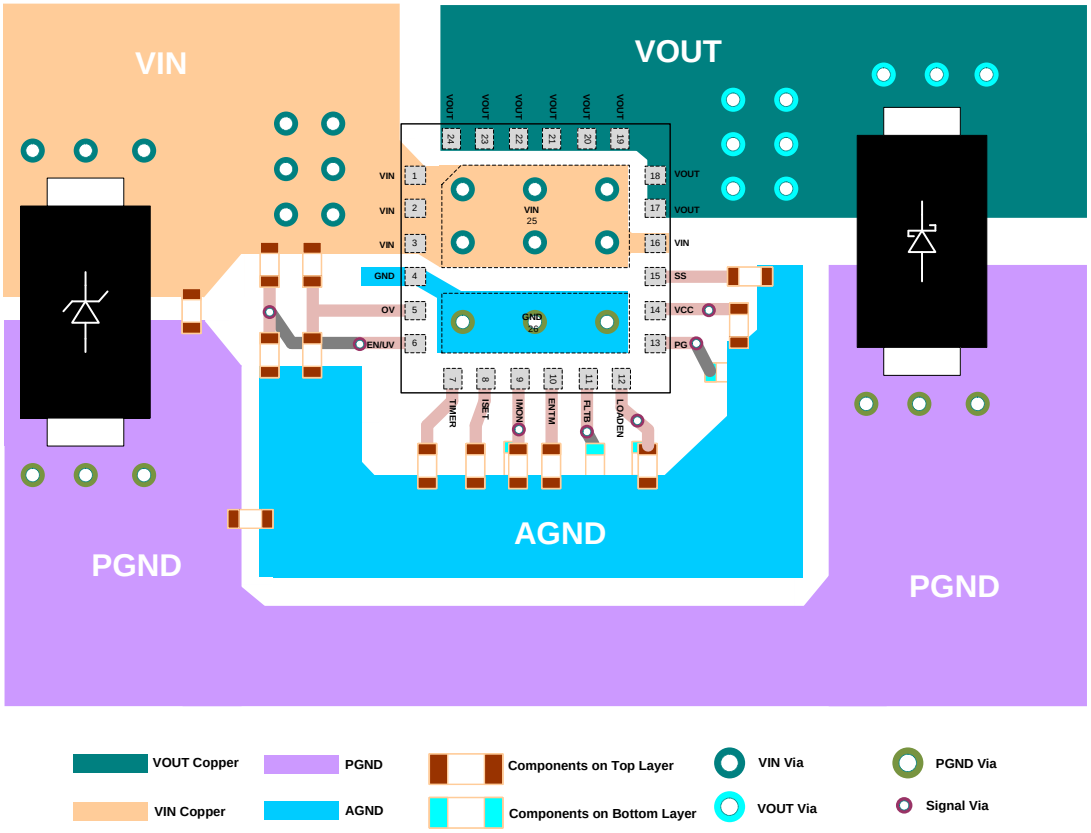


Figure 12: Recommended PCB Layout

VIN TVS Diode PN: SMDJ12A

VOUT Diode PN: B330A

TYPICAL APPLICATION CIRCUITS

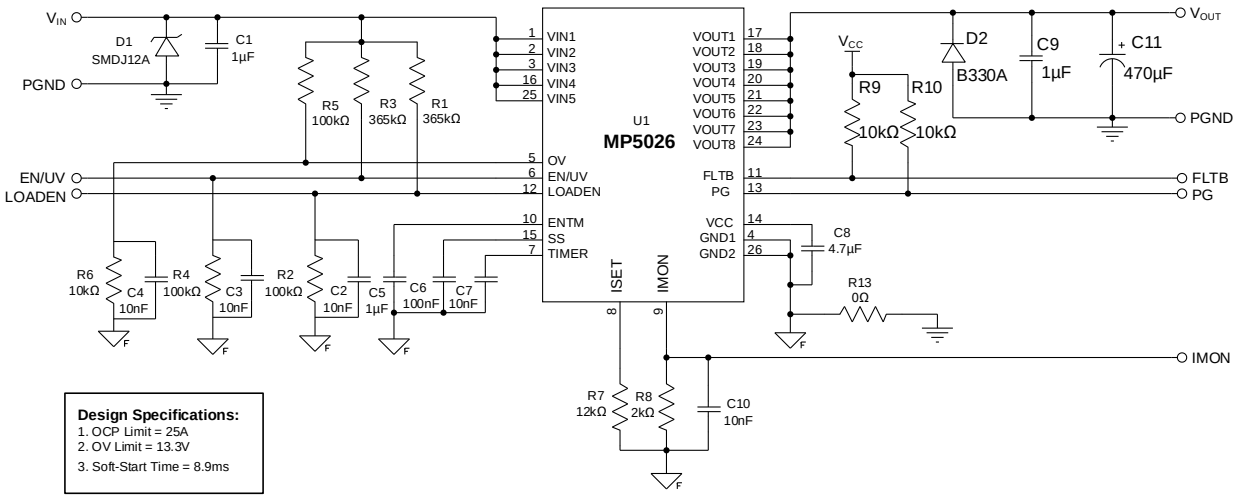


Figure 13: Typical Application Circuit (V_{IN} = 12V, OC Limit = 25A)

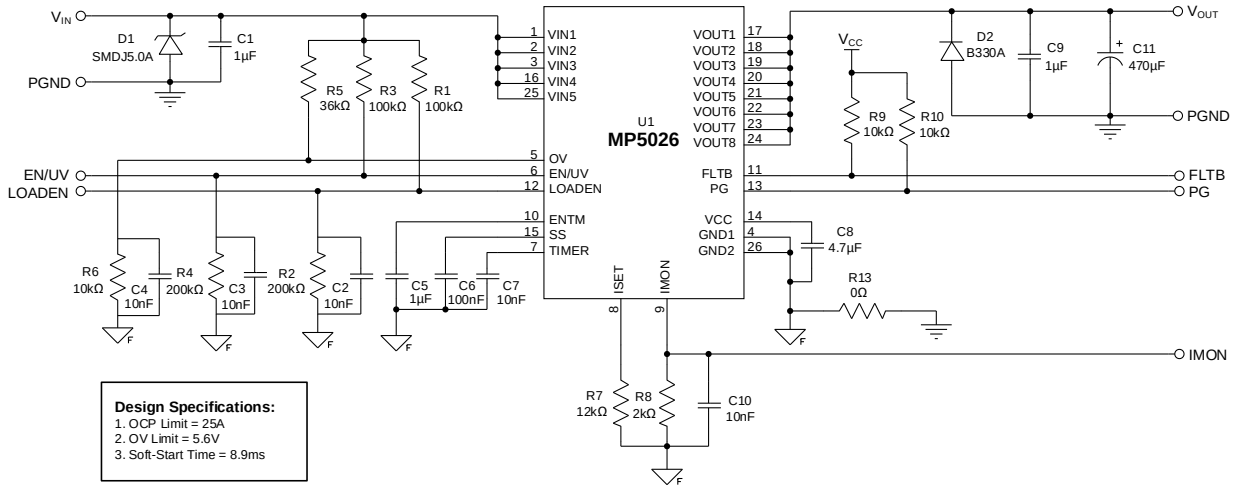
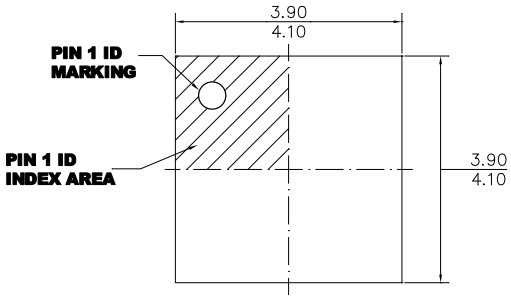


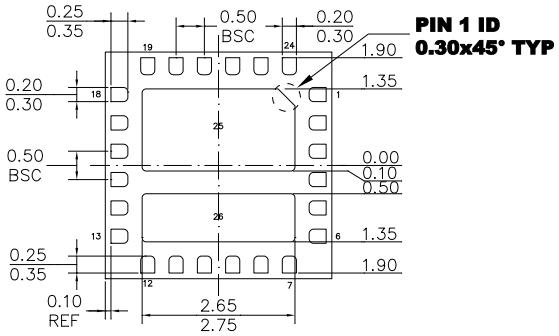
Figure 14: Typical Application Circuit (V_{IN} = 3.3V, OC Limit = 25A)

PACKAGE INFORMATION

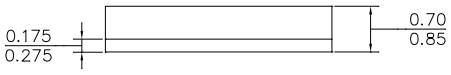
LGA-26 (4mmx4mm)



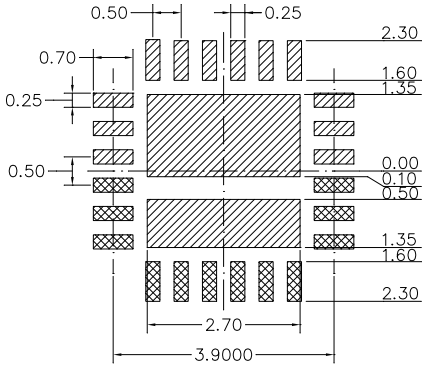
TOP VIEW



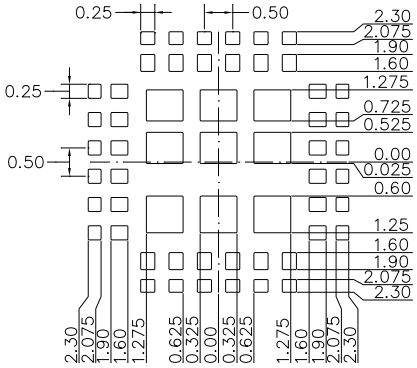
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

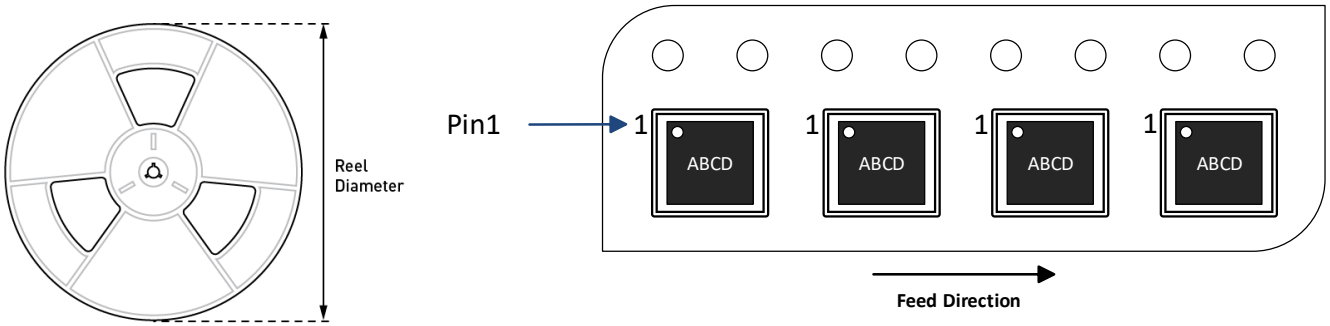


RECOMMENDED STENCIL OPENING

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.
5) THE ACCURACY FOR COMPONENT PLACEMENT SHOULD BE ADJUSTED TO ±30 MICROMETRES.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5026GLRT-Z	LGA-26 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm