MPQ79500FS

MPSafe™ ASIL-D 6-Channel Voltage Monitor, AEC-Q100 Qualified

DESCRIPTION

The MPQ79500FS is a 6-channel voltage monitor. It is engineered for automotive applications that require voltage rails to be monitored for safety, such as advanced driver assistance systems (ADAS) and autonomous driving platforms.

Each voltage monitor input has configurable over-voltage (OV) and under-voltage (UV) thresholds. Highly accurate high-frequency (HF) and low-frequency (LF) voltage monitoring can detect when the voltage thresholds are reached. Two of the inputs are differential, remote voltage sensing input pairs that are well-suited to monitor voltage rails with high current levels. Low-power mode (LPM) can be enabled to achieve extremely low quiescent currents.

The MPQ79500FS can record the order in which voltage rails are sequenced, as well as their associated timestamps. The device also provides a sync I/O function, which allows multiple devices to be connected together to increase the number of voltage rails that can perform these functions. The device is accessible through an I^2C interface.

With the integration of sophisticated functional safety features including built-in self-testing (BIST), diagnostics, and write protection, this device is targeted to support applications with a high automotive safety integrity level up to ASIL-D.

The MPQ79500FS is available in a QFN-16 (3mmx3mm) package with wettable flanks.

FEATURES

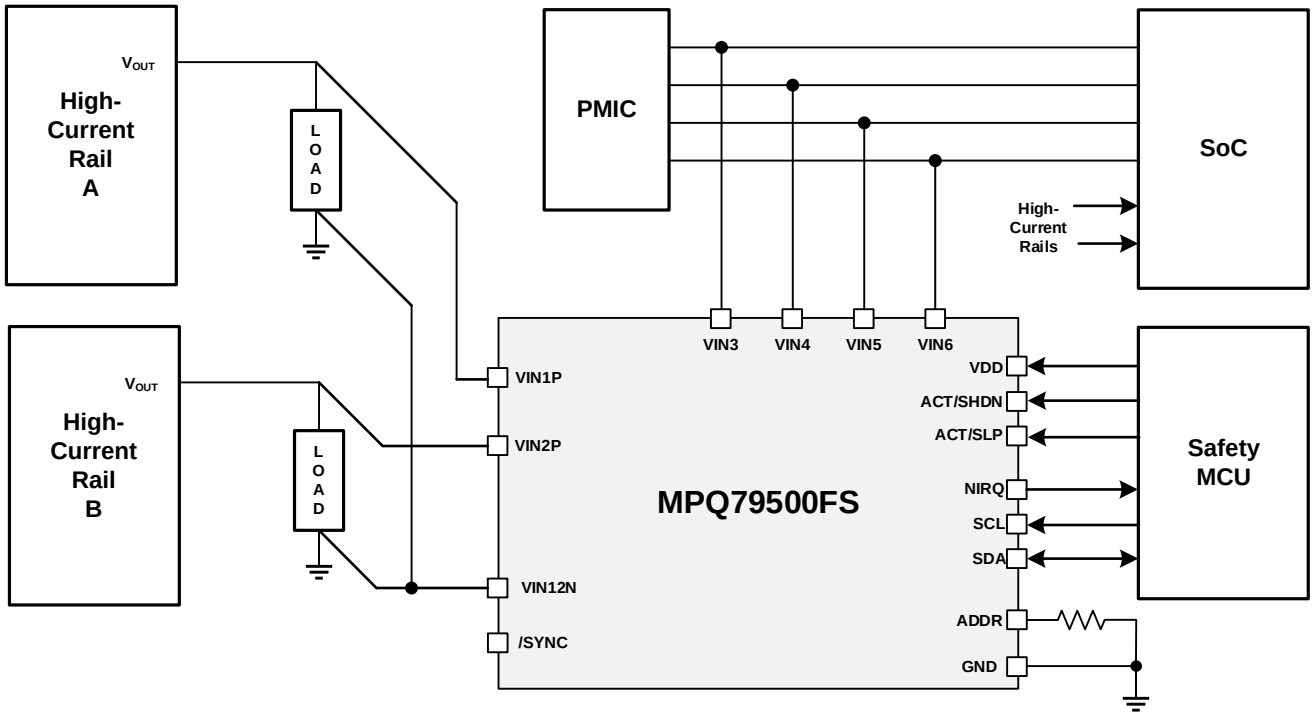
- Designed for Automotive ADAS and Autonomous Driving Platforms:
  - 2.7V to 5.5V Input Voltage (V_{IN}) Range
  - 6 Voltage Monitor Inputs: 4 Single-Ended, 2 Differential
  - Absolute OV/UV Thresholds for High-Frequency and Low-Frequency Components:
    - 0.2V to 1.475V, 5mV/Step
    - 0.8V to 5.5V, 20mV/Step
  - High DC Accuracy:
    - >1V, ±0.5%
    - <1V, ±5mV
  - ADC for Voltage-Level Readback
  - Selectable High-Power Mode (HPM) and Low-Power Mode (LPM)
  - Power Sequence Recording for Power On, Power Off, and Sleep Entry/Exit
  - SYNC I/O for Multi-Device Sequence Synchronization
  - Write Protection for Critical Registers
- Functional Safety:
  - Built-In Self-Testing (BIST)
  - Interrupt Output Pin (Fault Reporting)
  - Cyclic Redundancy Check (CRC) Protection on Registers
  - Support System up to ASIL D
  - ISO26262 Functional Safety Certified
- Flexible Application with I^2C Interface:
  - I^2C Interface with PEC
  - One-Time Programmable (OTP) Memory
- Additional Features:
  - Available in a QFN-16 (3mmx3mm) Package with 0.5mm Pitch and Wettable Flanks
  - Available in AEC-Q100 Grade 1

MPSafe™ Developed for Functional Safety Applications: ISO26262 Compliant

APPLICATIONS

- Advanced Driver Assistance Systems (ADAS)
- Autonomous Driving Platforms
- Functional Safety Systems with Multiple Power Rails
- Industrial Robotics

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ79500FSGQE-xxxx-AEC1**	QFN-16 (3mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ79500FSGQE-xxxx-AEC1-Z).

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. Each "x" can be a hexadecimal value between 0 and F. The default device uses the"-0000" code. Contact an MPS FAE to create this unique number.

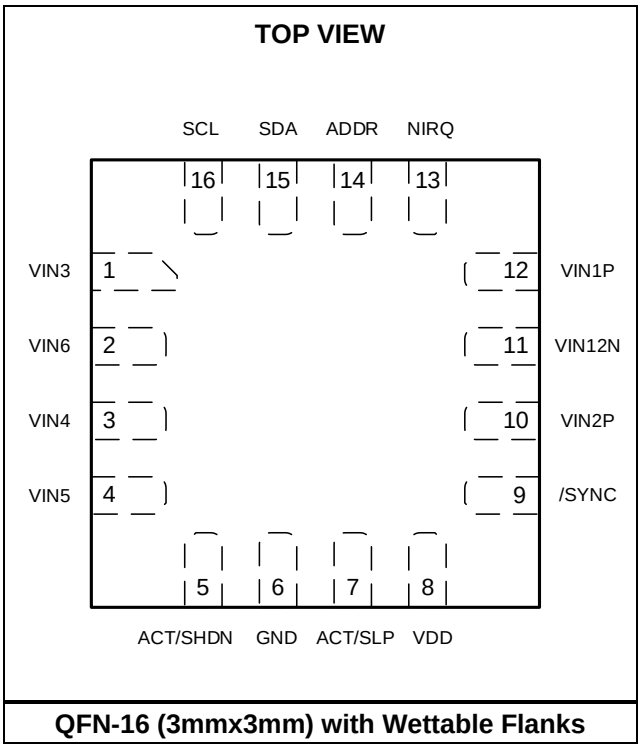
*** Moisture Sensitivity Level Rating.

TOP MARKING

$\overline{\text{BUTY}}$
LLLL

BUT: Production code
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm) with Wettable Flanks

PIN FUNCTIONS

Pin #	Name	Type	Description
1	VIN3	Analog In	**Voltage monitor input 3.** Connect the VIN3 pin to GND if it is not used.
2	VIN6	Analog In	**Voltage monitor input 6.** Connect the VIN6 pin to GND if it is not used.
3	VIN4	Analog In	**Voltage monitor input 4.** Connect the VIN4 pin to GND if it is not used.
4	VIN5	Analog In	**Voltage monitor input 5.** Connect the VIN5 pin to GND if it is not used.
5	ACT/SHDN	In	**Active/shutdown.** The ACT/SHDN pin is the power sequencer control input. Connect ACT/SHDN directly to a voltage or use a resistor (e.g. 10kΩ). If ACT/SHDN is floating, an internal 100kΩ resistor pulls this pin low. When this pin goes from low (SHDN) to high (ACT), the system starts up. When this pin goes from high (ACT) to low (SHDN), the system shuts down.
6	GND	Supply	**Power ground.** Electrically connect the GND pin to the system ground plane with the shortest, lowest-impedance connection possible.
7	ACT/SLP	In	**Active/sleep.** The ACT/SLP pin is used in conjunction with the sleep entry/exit sequence control registers. Connect ACT/SLP directly to a voltage or use a resistor (e.g. 10kΩ). If ACT/SLP is floating, an internal 100kΩ resistor pulls this pin low. When this pin goes from low (SLP) to high (ACT), the system exits sleep mode. When this pin goes from high (ACT) to low (SLP), the system enters sleep mode.
8	VDD	Supply	**Input supply voltage.** To minimize spikes, it is recommended to place a decoupling capacitor from the VDD pin to ground.
9	/SYNC	In/Out, OD	**Sequence monitor synchronization.** Float the /SYNC pin or connect it to VDD with a pull-up resistor. For the multiple IC sequence function, connect all of the /SYNC pins together.
10	VIN2P	Analog In	**Voltage monitor input 2 (differential).** Connect the VIN2P pin to GND if it is not used. The VIN2P voltage must always exceed the VIN12N voltage.
11	VIN12N	Analog In	**Voltage monitor shared negative input.** Do not float the VIN12N pin.
12	VIN1P	Analog In	**Voltage monitor input 1 (differential).** Connect the VIN1P pin to GND if it is not used. The VIN1P voltage must always exceed the VIN12N voltage.
13	NIRQ	Out, OD	**Interrupt.** The NIRQ pin is an active-low signal. If an event occurs that requires the device status to be read, this pin sends an interrupt output signal to the I^2C. This pin is an open-drain status pin. Connect NIRQ to an external power supply or VDD with a pull-up resistor.
14	ADDR	In	**I^2C address selection strap.**
15	SDA	In/Out, OD	**I^2C bus serial data input/output.** The SDA pin is an open-drain port. An external pull-up resistor is required to connect this pin to the I^2C bus supply rail. SDA supports up to 1Mbs of data transfer in fast-mode plus. If this pin is not used, connect it to the VDD pin through a resistor (e.g. 100kΩ).
16	SCL	In, OD	**I^2C bus serial clock input.** The SCL pin is an open-drain port. An external pull-up resistor is required to connect this pin to the I^2C bus supply rail. SCL supports up to 1Mbs of data transfer in fast-mode plus. If this pin is not used, connect it to the VDD pin through a resistor (e.g. 100kΩ).

ABSOLUTE MAXIMUM RATINGS (1)

All pins .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-16 (3mmx3mm) 2.4W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM)……Class 2 (3)
Charged device model (CDM)..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{DD}) .....2.7V to 5.5V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance (5) θ_{JA} θ_{JC} θ_{JB}

QFN-16(3mmx3mm).....52....6.5....7...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on JESD51-7, 4-layer PCB. The value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

Typical values are at V_{DD} = 3.3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{DD} = 3.3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VDD Supply						
Supply voltage	V_{DD}		2.7	3.3	5.5	V
VDD under-voltage lockout (UVLO) rising threshold	V_{UVLO_TH-R}		2.6	2.8	3.0	V
VDD UVLO falling threshold	$V_{UVLO\_TH\ -F}$		2.4	2.5	2.7	V
V_{IN} UVLO threshold hysteresis	V_{UVLO_HYS}			300		mV
VDD supply current (quiescent)	I_Q	HPM		6	8	mA
		LPM		560	690	µA
ACT/SHDN, ACT/SLP						
Input logic high	V_{IH}	V_{IH} of 3.3V and 1.8V/1.2V	0.84			V
Input logic low	V_{IL}	V_{IL} of 3.3V and 1.8V/1.2V			0.36	V
Enable input pull-down resistor	R_{PD}	Enable input pull-down to ensure a safe state in case of an open circuit on the enable pin		100		kΩ
VINx Monitoring						
VINx input load current	I_{VIN}			12	20	µA
Monitoring voltage minimum threshold (low-frequency channel)	V_{LP_MIN}	No scaling		0.2		V
	$V_{LP\_MIN\_X4}$	With x4 scaling		0.8		V
Monitoring voltage maximum threshold (low-frequency channel)	V_{LP_MAX}	No scaling		1.475		V
	$V_{LP\_MAX\_X4}$	With x4 scaling		5.5		V
Monitoring voltage minimum threshold (6) (high-frequency channel)	V_{HP_MIN}	No scaling		0.2		V
	$V_{HP\_MIN\_X4}$	With x4 scaling		0.8		V
Monitoring voltage maximum threshold (6) (high-frequency channel)	V_{HP_MAX}	No scaling		1.475		V
	$V_{HP\_MAX\_X4}$	With x4 scaling		5.5		V
Threshold granularity setting	LSB_T	No scaling		5		mV
	LSB_{T_X4}	With x4 scaling		20		mV
Low-pass filter (LPF) cutoff for low-frequency channel thresholds (6)	f_{LF}	Range of configurable values through the FC_LF[N] register	250	1000	4000	Hz
LPF cutoff for high-frequency channel thresholds (6)	f_{HF}				4	MHz
DC (<f_{LF}) voltage measurement accuracy (low-frequency channel) with no scaling	$V_{LP\_\Delta ERR}$	No scaling, T_J = 25°C	-1	0	1	LSB
		No scaling, T_J = -40°C to +150°C	-2	0	+2	LSB
DC (<f_{LF}) voltage measurement accuracy (low frequency channel) with x4 scaling	$V_{LP\_\Delta ERR\_X4}$	With x4 scaling	-1	0	+2	LSB

ELECTRICAL CHARACTERISTIC *(continued)*

Typical values are at V_{DD} = 3.3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{DD} = 3.3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
DC (>f_{HF}) voltage measurement accuracy (high-frequency channel) with no scaling (7)	$V_{HP\_\Delta ERR}$	>1V, T_J = 25°C	-0.5	0	+0.5	%
		>1V, T_J = -40°C to +150°C	-1	0	+1	%
		<1V, T_J = 25°C	-5	0	+5	mV
		<1V, T_J = -40°C to +150°C	-10	0	+10	mV
DC (>f_{HF}) voltage measurement accuracy (high-frequency channel) with x4 scaling (7)	$V_{HP\_\Delta ERR\_X4}$	>1V, T_J = 25°C	-2	0	+2	%
		>1V, T_J = -40°C to +150°C	-4	0	+4	%
		<1V, T_J = 25°C	-20	0	+20	mV
		<1V, T_J = -40°C to +150°C	-40	0	+40	mV
OFF voltage threshold (8)	V_{OFF}		140		+200	mV
Sequence timestamp range	t_{SEQ}	Time from the ACT/SHDN or ACT/SLP edge to the max timestamp counter	100			ms
Sequence timestamp resolution	t_{SEQ_LSB}			50		µs
Full monitoring active from the ACT/SHDN rising edge	t_{MON_ACT}				10	µs
Sequence tagging active from the ACT/SHDN or ACT/SLP edge	t_{SEQ_ACT}				10	µs
/SYNC (9) (Supports 1.2 V/1.8V, and 3.3V Signaling via DEV_CFG Option)						
Input high voltage	V_{IH_SYNC}	Rising (V_{IH} of 3.3V and 1.8V/1.2V)	0.84			V
Input low voltage	V_{IL_SYNC}	Falling (V_{IL} of 3.3V and 1.8V/1.2V)			0.36	V
Internal pull-up resistor	R_{PU_SYNC}		25		100	kΩ
Output low	V_{OL}	With an external 10kΩ pull-up resistor			0.01	V
NIRQ (Open Drain)						
Output low	V_{OL}	With an external 10kΩ pull-up resistor			0.01	V
Fault detection to NIRQ assertion latency	t_{NIRQ}				25	µs
Built-In Self-Testing (BIST)						
POR to ready with BIST	t_{CFG_WB}	Include BIST, OTP load with error-correction code (ECC)			20	ms
POR to ready without BIST	t_{CFG_NB}	Include OTP load with ECC, T_J = 25°C			5	ms
BIST time (6)	t_{BIST}	AT_POR = 1 or AT_SHDN			15	ms
Clocking						
Internal clock accuracy	Acc_{ICLK}	Clock used for timestamp and SYNC pulse	-5		+5	%
Thermal Shutdown						
Thermal shutdown	T_{SD}	Junction temperature rising		170		°C
Thermal shutdown hysteresis	T_{SD-HYS}			20		°C

Notes:

6) Guaranteed by design and bench characterization. Not tested in production.
7) MPS guarantees the accuracy at a factory-trimmed voltage level according to customer demand.
8) x4 scaling does not apply to the OFF voltage threshold.
9) If power domains other than V_{DD} are applied, consider the level-shifting. Otherwise, there may be additional leakage or current injection.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

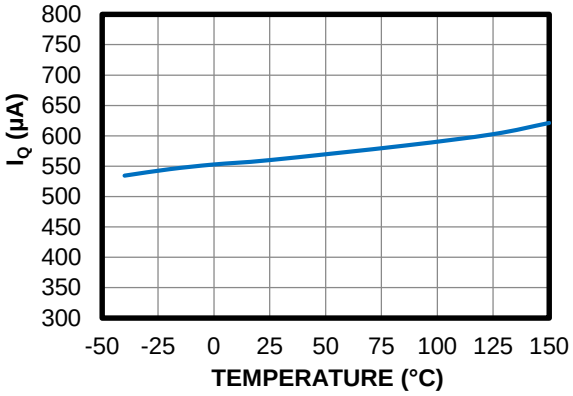
Typical values are at V_{DD} = 3.3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{DD} = 3.3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications (Supports 1.2V/1.8V, and 3.3V Signaling via DEV_CFG Option)						
Input logic high (SDA/SCL)	V_{IH_I2C}	Rising (VOD = 3.3V)	2.0			V
		Rising (VOD = 1.2V/1.8V)	0.84			V
Input logic low (SDA/SCL)	V_{IL_I2C}	Falling (VOD = 3.3V)			0.8	V
		Falling (VOD = 1.2V/1.8 V)			0.36	V
Output low	V_{OL}	SDA with a 10kΩ pull-up resistor			0.1	V
Input capacitance	C_{SDA}, C_{SDL}			5		pF
SCL clock frequency	f_{SCL}				1	MHz
SCL high time	t_{HIGH}		0.26			µs
SCL low time	t_{LOW}		0.5			µs
Data set-up time	t_{SU_DAT}		50			ns
Data hold time	t_{HD_DAT}		0			µs
Set-up time for a repeated start condition	t_{SU_STA}		0.26			µs
Hold time for start condition	t_{HD_STA}		0.26			µs
Bus free time between a start and stop condition	t_{BUF}		0.5			µs
Set-up time for stop condition	$t_{SU,STO}$		0.26			µs
SCL and SDA rising time	t_R		20 x (V_{DD} / 5.5V)		120	ns
SCL and SDA falling time	t_F		20 x (V_{DD} / 5.5V)		120	ns
Suppressed spike pulse width	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				550	pF

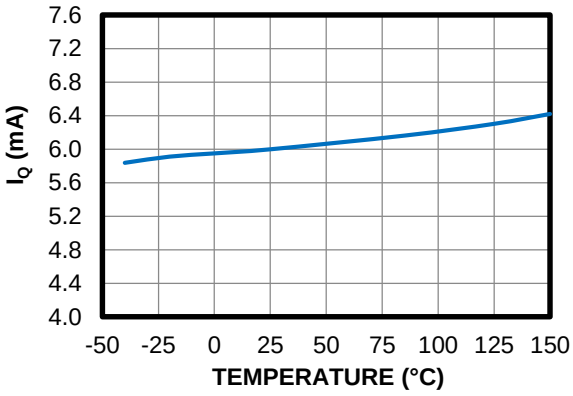
TYPICAL CHARACTERISTICS

V_{DD} = 3.3V, T_J = -40°C to +150°C, unless otherwise noted.

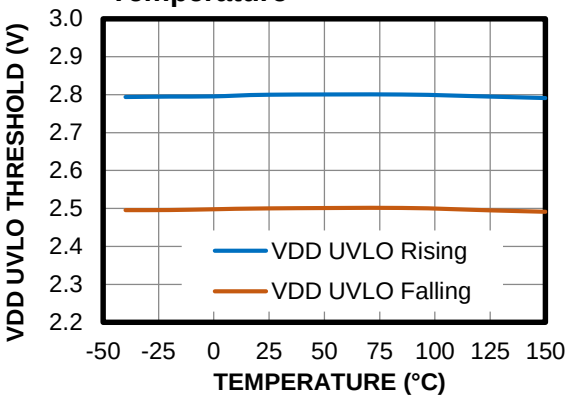
I_Q vs. Temperature
LPM



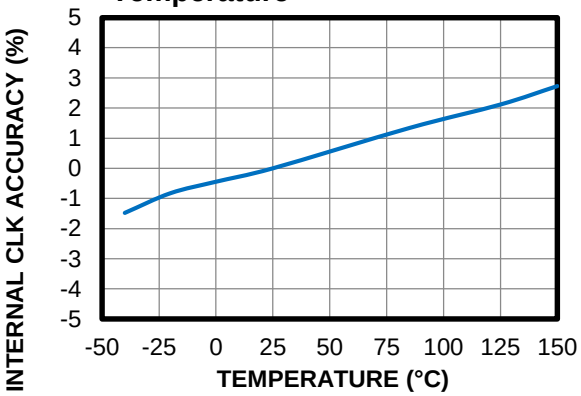
I_Q vs. Temperature
HPM



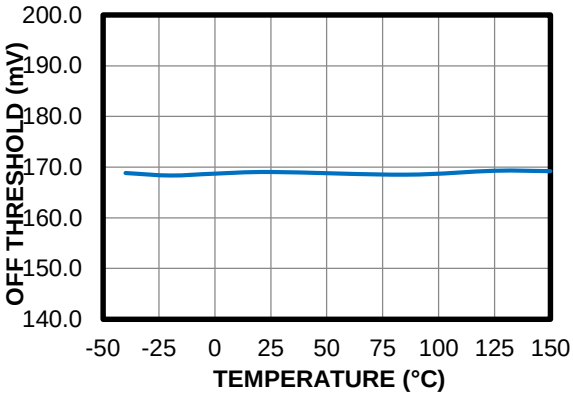
VDD UVLO Threshold vs. Temperature



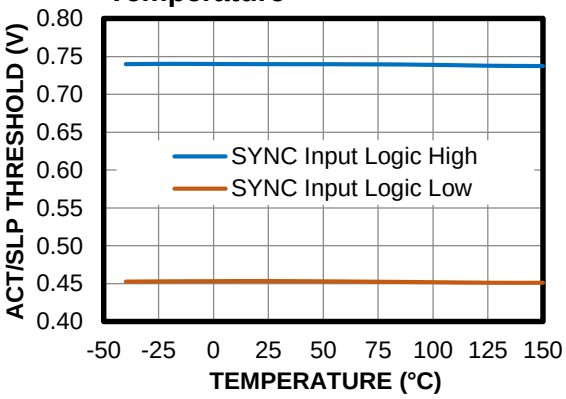
Internal CLK Accuracy vs. Temperature



OFF Threshold vs. Temperature



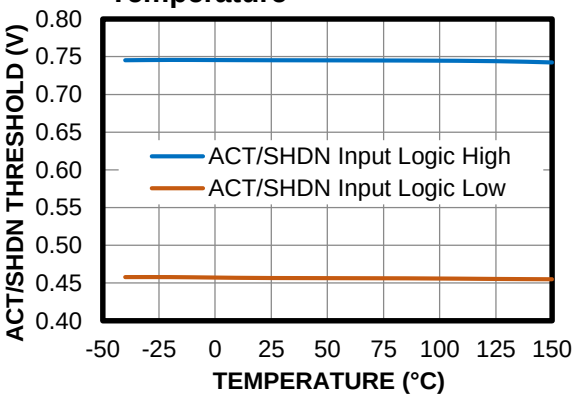
ACT/SLP Threshold vs. Temperature



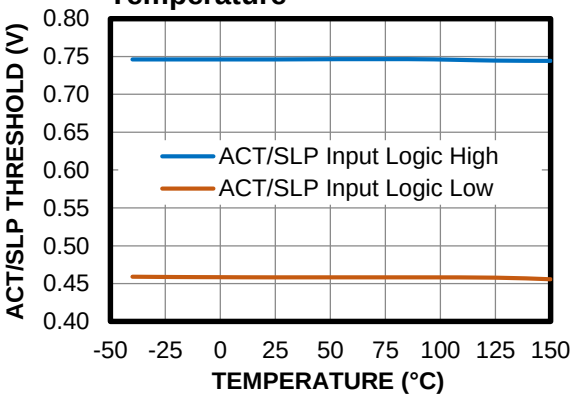
TYPICAL CHARACTERISTICS *(continued)*

VDD = 3.3V, T_J = -40°C to +150°C, unless otherwise noted.

ACT/SHDN Threshold vs. Temperature

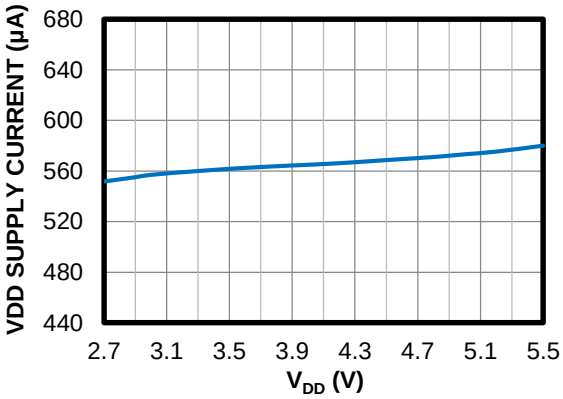


ACT/SLP Threshold vs. Temperature



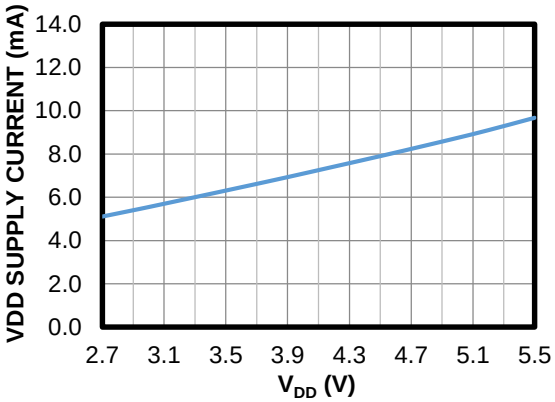
VDD Supply Current vs. V_{DD}

LPM, T_A = 25°C



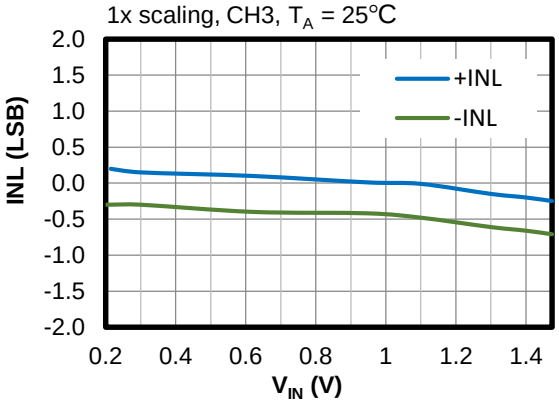
VDD Supply Current vs. V_{DD}

HPM, T_A = 25°C



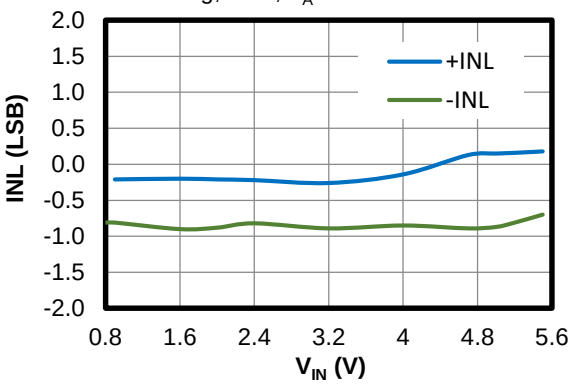
INL vs. V_{IN}

1x scaling, CH3, T_A = 25°C



INL vs. V_{IN}

4x scaling, CH3, T_A = 25°C



TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, VPU = 3.3V, T_A = 25°C, unless otherwise noted.

SEQ Monitoring On

Single MPQ79500FS device, ACT/SHDN = low to high, ACT/SLP = high

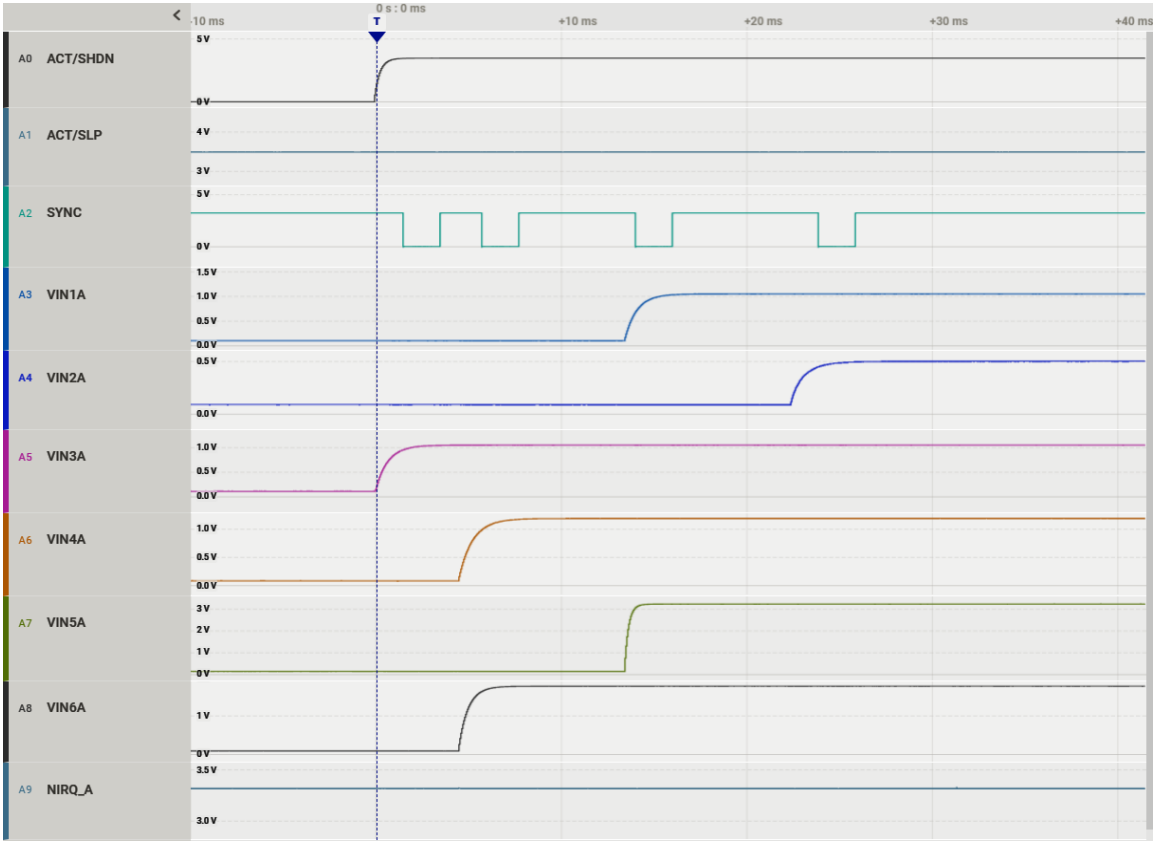


Table 1: Read Register after Timeout

Bank 0 of Part A				Bank 1 of Part A			
Add.	**Register Name**	**Read Result**	**Description**	**Add.**	**Register Name**	**Read Result**	**Description**
0x10	INT_SRC	00	No interrupt after SEQ is on.	0x13	IEN_UVHF	3F	UVHF monitoring for channels 1–6 is enabled.
0x11	INT_MONITOR	00	No interrupt after SEQ is on.	0x14	IEN_UVLF	3F	UVLF monitoring for channels 1–6 is enabled.
0x12	INT_UVHF	00	No UVHF fault has occurred.	0x15	IEN_OVHF	3F	OVHF monitoring for channels 1–6 is enabled.
0x14	INT_UVLF	00	No UVLF fault has occurred.	0x16	IEN_OVLF	3F	OVLF monitoring for channels 1–6 is enabled.
0x16	INT_OVHF	00	No OVHF fault has occurred.	0x17	IEN_SEQ_ON	3F	SEQ_ON monitoring for channels 1–6 is enabled.
0x18	INT_OVLF	00	No OVLF fault has occurred.	0x18	IEN_SEQ_OFF	3F	EQ_OFF for channels 1–6 is enabled.
0x1A	INT_SEQ_ON	00	No power up sequence fault has occurred.	0x19	IEN_SEQ_EXS	3F	SEQ_EXS for channels 1–6 is enabled.

0x1C	INT_SEQ_OFF	00	No power off sequence fault has occurred.	0x20	UV_HF[1]	80	The channel 1 UVHF threshold is 0.84V.
0x1E	INT_SEQ_EXS	00	No sleep exit sequence fault has occurred.	0x21	OV_HF[1]	D4	The channel 1 OVHF threshold is 1.26V.
0x20	INT_SEQ_ENS	00	No sleep entry sequence fault has occurred.	0x22	UV_LF[1]	94	The channel 1 UVLF threshold is 0.94V.
0x22	NT_CONTROL	00	No interrupt after SEQ is on.	0x23	OV_LF[1]	C0	The channel 1 OVLF threshold is 1.16V.
0x23	INT_TEST	00	No interrupt after SEQ is on.	0x24	FLT_HF[1]	22	The OV/UV debouncing time for the high-frequency threshold comparator for channel 1 is 0.4µs.
0x24	INT_VENDOR	00	No interrupt after SEQ is on.	0x25	FC_LF[1]	04	The low-frequency path cutoff frequency for channel 1 is 1kHz.
0x30	VMON_STAT	4E	The monitoring status is as expected.	0x32	UV_LF[2]	30	The channel 2 UVLF threshold is 0.44V.
0x31	TEST_INFO	00	No error for the internal self-testing and ECC.	0x35	FC_LF[2]	04	The low-frequency path cutoff frequency for channel 2 is 1kHz.
0x32	OFF_STAT	00	Channels 1–6 are in the on state.	0x42	UV_LF[3]	94	The channel 3 UVLF threshold is 0.94V.
0x36	SEQ_ORD_STAT	04	4 sync pulse count.	0x45	FC_LF[3]	04	The low-frequency path cutoff frequency for channel 3 is 1kHz.
0x40	VIN_LVL[1]	AC	VIN1A is 1.06V in the active state after SEQ on.	0x52	UV_LF[4]	B0	The channel 4 UVLF threshold is 1.08V.
0x41	VIN_LVL[2]	3D	VIN2A is 0.505V in the active state after SEQ on.	0x55	FC_LF[4]	04	The low-frequency path cutoff frequency for channel 4 is 1kHz.
0x42	VIN_LVL[3]	AA	VIN3A is 1.05V in the active state after SEQ on.	0x62	UV_LF[5]	6C	The channel 5 UVLF threshold is 2.96V.
0x43	VIN_LVL[4]	C8	VIN4A is 1.2V in the active state after SEQ on.	0x65	FC_LF[5]	04	The low-frequency path cutoff frequency for channel 5 is 1kHz.
0x44	VIN_LVL[5]	7B	VIN5A is 3.26V in the active state after SEQ on.	0x72	UV_LF[6]	29	The channel 6 UVLF threshold is 1.62V.
0x45	VIN_LVL[6]	32	VIN6A is 1.8V in the active state after SEQ is on.	0x75	FC_LF[6]	04	The low-frequency path cutoff frequency for channel 6 is 1kHz.
0x50	SEQ_ON_LOG[1]	03	The rail on VIN1A is up in the first SYNC pulse recording as first sequence log.	0x1A	IEN_SEQ_ENS	3F	SEQ_ENS monitoring for channels 1–6 is enabled.
0x51	SEQ_ON_LOG[2]	04	The rail on VIN2A is up in the fourth SYNC pulse record as fourth sequence log.	0x1E	VIN_CH_EN	3F	Channels 1–6 are enabled.
0x52	SEQ_ON_LOG[3]	01	The rail on VIN3A is up in the first SYNC pulse record as first sequence log.	0x1F	VRANGE_MULT	30	VIN1–VIN4 are 1x scaling, VIN5and VIN6 are 4x scaling.

0x53	SEQ_ON_LOG[4]	02	The rail on VIN4A is up in the second SYNC pulse record as second sequence log.	0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.
0x54	SEQ_ON_LOG[5]	03	The rail on VIN5A is up in the third SYNC pulse record as third sequence log.	0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 is enabled.
0x55	SEQ_ON_LOG[6]	02	The rail on VIN6A is up in the second SYNC pulse record as the second sequence log.	0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.
0x90	SEQ_TIME_MSB[1]	01	The up time of VIN1A is 14.75ms.	0xA4	AMSK_ENS	06	AMSK_ENS for VIN1, VIN4, VIN5, and VIN6 is enabled.
0x91	SEQ_TIME_LSB[1]	27		0xA5	SEQ_TOUT_MSB	00	The timeout set is to 38ms.
0x92	SEQ_TIME_MSB[2]	01	The up time of VIN2A is 23.8ms.	0xA6	SEQ_TOUT_LSB	25	
0x93	SEQ_TIME_LSB[2]	DC		0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.
0x94	SEQ_TIME_MSB[3]	00	The up time of VIN3A is 1.45ms.	0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.
0x95	SEQ_TIME_LSB[3]	1D		0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.
0x96	SEQ_TIME_MSB[4]	00	The up time of VIN4A is 6.15ms.	0xB0	SEQ_ON_EXP[1]	03	The expected sequence log for VIN1A is 3.
0x97	SEQ_TIME_LSB[4]	7B		0xB1	SEQ_ON_EXP[2]	04	The expected sequence log for VIN2A is 4.
0x98	SEQ_TIME_MSB[5]	01	The up time of VIN5A is 13.95ms.	0xB2	SEQ_ON_EXP[3]	01	The expected sequence log for VIN3A is 1.
0x99	SEQ_TIME_LSB[5]	17		0xB3	SEQ_ON_EXP[4]	02	The expected sequence log for VIN4A is 2.
0x9A	SEQ_TIME_MSB[6]	00	The up time of VIN6A is 5.7ms.	0xB4	SEQ_ON_EXP[5]	03	The expected sequence log for VIN5A is 3.
0x9B	SEQ_TIME_MSB[6]	72		0xB5	SEQ_ON_EXP[6]	02	The expected sequence log for VIN6A is 2.

SEQ Monitoring On with Multiple MPQ79500FS Devices

Three MPQ79500FS devices, ACT/SHDN = low to high, ACT/SLP = high

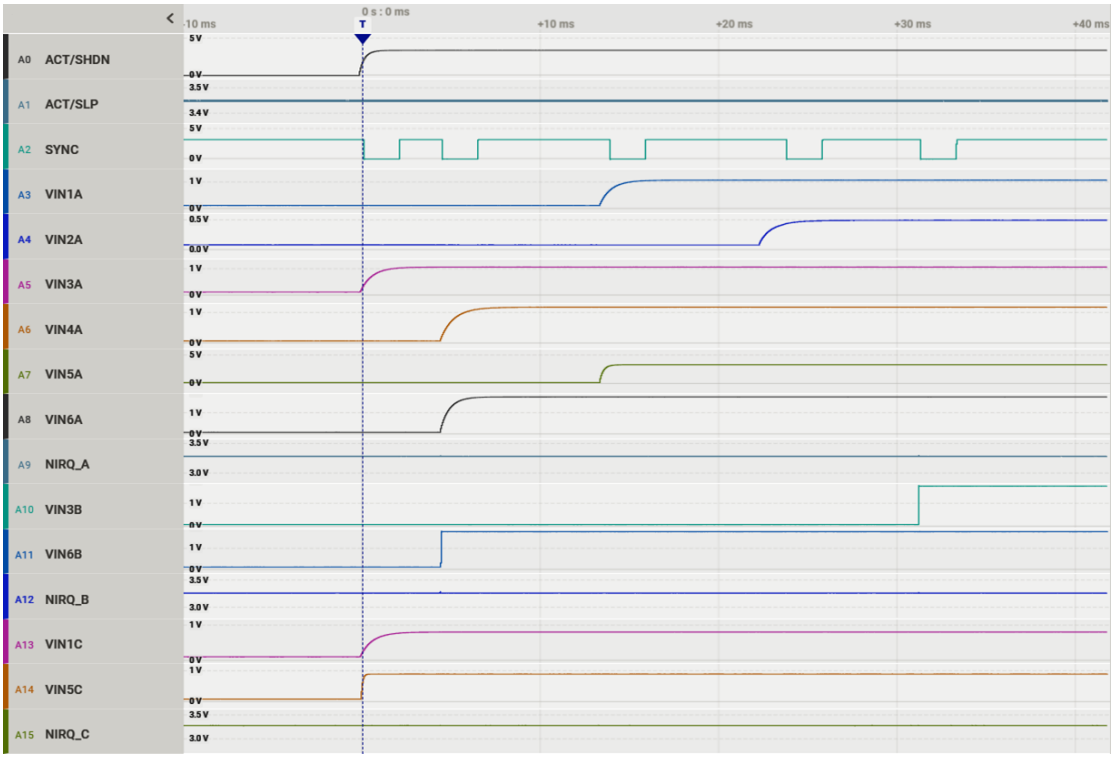


Table 2: Read Register after Timeout

		Part A		Part B		Part C	
Add.	**Register Name**	**Read Result**	**Description**	**Read Result**	**Description**	**Read Result**	**Description**
Bank 0							
0x10 ~10x 24	Interrupt Information Registers	00	No interrupt after SEQ_ON.	00	No interrupt after SEQ is on.	00	No interrupt after SEQ_ON.
0x32	OFF_ STAT	00	Channels 1–6 are in the on state.	1B	Channel 3 and channel 6 are in the on state.	2E	Channel 1 and channel 5 are in the on state.
0x36	SEQ_ ORD_ STAT	05	5 sync pulse count.	05	5 sync pulse count.	05	5 sync pulse count.
0x40	VIN_ LVL[1]	AC	VIN1A is 1.06V in the active state after SEQ_ON.	00	VIN1B is not on.	78	VIN1A is 0.8V at active state after SEQ_ON.
0x41	VIN_ LVL[2]	3D	VIN2A is 0.505V in active state after SEQ_ON.	00	VIN2B is not on.	00	VIN2C is not on.
0x42	VIN_LVL[3]	AA	VIN3A is 1.05V in the active state after SEQ_ON.	32	VIN3B is 1.8V at active state after SEQ is on.	00	VIN3C is not on.
0x43	VIN_LVL[4]	C8	VIN4A is 1.2V in the active state after SEQ_ON.	00	VIN4B is not on.	00	VIN4C is not on.
0x44	VIN_LVL[5]	7B	VIN5A is 3.26V in the active state after SEQ_ON.	00	VIN5B is not on.	8C	VIN5C is 0.9V at active state after SEQ_ON.
0x45	VIN_LVL[6]	32	VIN6A is 1.8V in the active state after SEQ_ON.	32	VIN6B is 1.8V at active state after SEQ_ON.	00	VIN6C is not on.
0x50	SEQ_ON_L OG[1]	03	The rail on VIN1A is up in the first SYNC pulse record as the first sequence log.	00	VIN1B does not have a sequence when SEQ is on.	01	The rail on VIN1C is up in the first SYNC pulse record as the first sequence log.

0x51	SEQ_ON_LOG[2]	04	The rail on VIN2A is up in the fourth SYNC pulse record as the fourth sequence log.	00	VIN2B does not have a sequence when SEQ is on.	00	VIN2C does not have a sequence when SEQ is on.
0x52	SEQ_ON_LOG[3]	01	The rail on VIN3A is up in the first SYNC pulse record as the first sequence log.	05	The rail on VIN3B is up in the fifth SYNC pulse record as the fifth sequence log.	00	VIN3C does not have a sequence when SEQ is on.
0x53	SEQ_ON_LOG[4]	02	The rail on VIN4A is up in the second SYNC pulse record as the second sequence log.	00	VIN4B does not have a sequence when SEQ is on.	00	VIN4C does not have a sequence when SEQ is on.
0x54	SEQ_ON_LOG[5]	03	The rail on VIN5A is up in the third SYNC pulse record as the third sequence log.	00	VIN5B does not have a sequence when SEQ is on.	01	The rail on VIN5C is up in the first SYNC pulse record as the first sequence log.
0x55	SEQ_ON_LOG[6]	02	The rail on VIN6A is up in the second SYNC pulse record as the second sequence log.	02	The rail on VIN6B is up in the second SYNC pulse record as the second sequence log.	00	VIN6C does not have a sequence when SEQ is on.
0x90	SEQ_TIME_MSB[1]	01	The up time for VIN1A is 14.8ms.	00	VIN1B does not have a sequence when SEQ is on.	00	The up time of VIN1C is 1.55ms.
0x91	SEQ_TIME_LSB[1]	28		00		1F	
0x92	SEQ_TIME_MSB[2]	01	The up time for VIN2A is 23.85ms.	00	VIN2B does not have a sequence when SEQ is on.	00	VIN2C does not have a sequence when SEQ is on.
0x93	SEQ_TIME_LSB[2]	DD		00		00	
0x94	SEQ_TIME_MSB[3]	00	The up time for VIN3A is 1.45ms.	02	The up time of VIN3B is 31.25ms.	00	VIN3C does not have a sequence when SEQ is on.
0x95	SEQ_TIME_LSB[3]	1D		71		00	
0x96	SEQ_TIME_MSB[4]	00	The up time for VIN4A is 6.15ms.	00	VIN4B does not have a sequence when SEQ is on.	00	VIN4C does not have a sequence when SEQ is on.
0x97	SEQ_TIME_LSB[4]	7B		00		00	
0x98	SEQ_TIME_MSB[5]	01	The up time for VIN5A is 13.95ms.	00	VIN5B does not have a sequence when SEQ is on.	00	The up time of VIN5C is 0.15ms.
0x99	SEQ_TIME_LSB[5]	17		00		03	
0x9A	SEQ_TIME_MSB[6]	00	The up time for VIN6A is 5.7ms.	00	The up time of VIN6B is 4.55ms.	00	VIN6C does not have a sequence when SEQ is on.
0x9B	SEQ_TIME_MSB[6]	72		5B		00	
Bank 1							
0x1E	VIN_CH_EN	3F	Channels 1–6 are enabled.	24	Channel 3 and channel 6 are enabled.	11	Channel 1 and channel 5 are all enabled.
0x1F	VRANGE_MULT	30	VIN1–VIN4 are 1x scaling, VIN5 and VIN6 are 4x scaling.	37	VIN3 and VIN6 are 4x scaling.	37	VIN1 and VIN5 are 1x scaling.
0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.	3C	AMSK_ON for VIN3 and VIN6 is enabled.	3C	AMSK_ON for VIN1 and VIN5 is enabled.
0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 are all enabled.	3C	AMSK_OFF for VIN3 and VIN6 is enabled.	3C	AMSK_OFF for VIN1 and VIN5 is enabled.
0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_EXS for VIN6 is enabled, AMSK_EXS of VIN3 is disabled.	20	AMSK_EXS for VIN1 and VIN5 is enabled.
0xA4	AMSK_ENS	06	AMSK_ENS for VIN1, VIN4, VIN5, and VIN6 are enabled.	20	AMSK_ENS for VIN6 is enabled, AMSK_ENS of VIN3 is disabled.	20	AMSK_ENS for VIN1 and VIN5 is enabled.

0xA5	SEQ_TOUT_MSB	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.
0xA6	SEQ_TOUT_LSB	25		25		25	
0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.
0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.
0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.
0xB0	SEQ_ON_EXP[1]	03	The expected sequence log of VIN1A is 3.	00	The expected sequence log of VIN1B is 0.	01	Expected sequence log of VIN1C is 1.
0xB1	SEQ_ON_EXP[2]	04	The expected sequence log of VIN2A is 4.	00	The expected sequence log of VIN2B is 0.	00	The expected sequence log of VIN2C is 0.
0xB2	SEQ_ON_EXP[3]	01	The expected sequence log of VIN3A is 1.	05	The expected sequence log of VIN3B is 5.	00	The expected sequence log of VIN3C is 0.
0xB3	SEQ_ON_EXP[4]	02	The expected sequence log of VIN4A is 2.	00	The expected sequence log of VIN4B is 0.	00	The expected sequence log of VIN4C is 0.
0xB4	SEQ_ON_EXP[5]	03	The expected sequence log of VIN5A is 3.	00	The expected sequence log of VIN5B is 0.	01	The expected sequence log of VIN5C is 1.
0xB5	SEQ_ON_EXP[6]	02	The expected sequence log of VIN6A is 2.	02	The expected sequence log of VIN6B is 2.	00	The expected sequence log of VIN6C is 0.

SEQ Monitoring Off with Multiple MPQ79500FS Devices

Three MPQ79500FS devices, ACT/SHDN = high to low, ACT/SLP = high

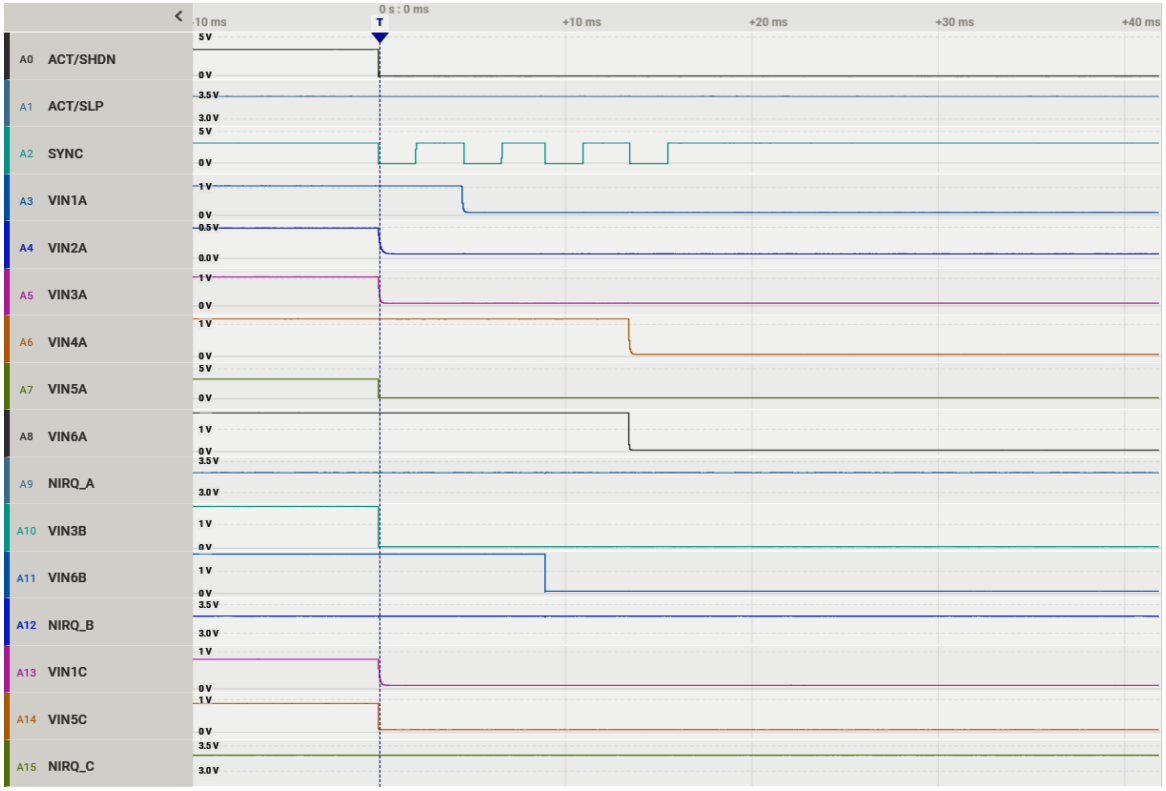


Table 3: Read Register after Timeout

		Part A		Part B		Part C	
Add.	**Register Name**	**Read Result**	**Description**	**Read Result**	**Description**	**Read Result**	**Description**
Bank 0							
0x10~ 0x24	Interrupt Information Registers	00	No interrupt after SEQ_OFF.	00	No interrupt after SEQ_OFF.	00	No interrupt after SEQ_OFF.
0x32	OFF_STAT	3F	Channels 1–6 are in an off state.	3F	Channel 3 and channel 6 are in an off state.	2E	Channel 1 and channel 5 are in an on state.
0x36	SEQ_ORD _STAT	04	4 sync pulse count.	04	4 sync pulse count.	04	4 sync pulse count.
0x40	VIN_LVL[1]	00	VIN1A < 0.2V after SEQ_OFF.	00	VIN1B < 0.8V after SEQ_OFF.	00	VIN1C < 0.2V after SEQ_OFF.
0x41	VIN_LVL[2]	00	VIN2A < 0.2V after SEQ_OFF.	00	VIN2B < 0.8V after SEQ_OFF.	00	VIN2C < 0.8V after SEQ_OFF.
0x42	VIN_LVL[3]	00	VIN3A < 0.2V after SEQ_OFF.	00	VIN3B < 0.8V after SEQ_OFF.	00	VIN3C < 0.8V after SEQ_OFF.
0x43	VIN_LVL[4]	00	VIN4A < 0.2V after SEQ_OFF.	00	VIN4B < 0.2V after SEQ_OFF.	00	VIN4C < 0.8V after SEQ_OFF.
0x44	VIN_LVL[5]	00	VIN5A < 0.8V after SEQ_OFF.	00	VIN5B < 0.8V after SEQ_OFF.	00	VIN5C < 0.2V after SEQ_OFF.
0x45	VIN_LVL[6]	00	VIN6A < 0.8V after SEQ_OFF.	00	VIN6B < 0.8V after SEQ_OFF.	00	VIN6C < 0.2V after SEQ_OFF.
0x60	SEQ_OFF_ LOG[1]	02	The rail on VIN1A Is down in the second SYNC pulse record as the first sequence log.	00	VIN1B does not have a sequence when SEQ is off.	01	The rail on VIN1C is down in the first SYNC pulse record as the first sequence log.
0x61	SEQ_OFF_ LOG[2]	01	The rail on VIN2A is down in the first SYNC pulse record as the first sequence log.	00	VIN2B does not have a sequence when SEQ is off.	00	VIN2C does not have a sequence when SEQ is off.
0x62	SEQ_OFF_ LOG[3]	01	The rail on VIN3A is down in the first SYNC pulse record as the first sequence log.	01	The rail on VIN3B is down in the first SYNC pulse record as the first sequence log.	00	VIN3C does not have a sequence when SEQ is off.
0x63	SEQ_OFF_ LOG[4]	04	The rail on VIN4A is down in the fourth SYNC pulse record as the fourth sequence log.	00	VIN4B does not have a sequence when SEQ is off.	00	VIN4C does not have a sequence when SEQ is off.
0x64	SEQ_OFF_ LOG[5]	01	The rail on VIN5A is down in the first SYNC pulse record as the first sequence log.	00	VIN5B does not have a sequence when SEQ is off.	01	The rail on VIN5C is down in the first SYNC pulse record as the first sequence log.
0x65	SEQ_OFF_ LOG[6]	04	The rail on VIN6A Is Down in the fourth SYNC pulse record as the fourth sequence log.	03	The rail on VIN6B is down in the third SYNC pulse record as the third sequence log.	00	VIN6C does not have a sequence when SEQ is off.

0x90	SEQ_TIME_MSB[1]	00	The off time of VIN1A is 4.6ms.	00	VIN1B does not have a sequence when SEQ is off.	00	The off time of VIN1C Is 0.15ms.
0x91	SEQ_TIME_LSB[1]	5C		00		03	
0x92	SEQ_TIME_MSB[2]	00	The off time of VIN2A is 0.15ms.	00	VIN2B does not have a sequence when SEQ is off.	00	VIN2C does not have a sequence when SEQ is off.
0x93	SEQ_TIME_LSB[2]	03		00		00	
0x94	SEQ_TIME_MSB[3]	00	The off time of VIN3A is 0.1ms.	00	The off time of VIN3B Is 0ms.	00	VIN3C does not have a sequence when SEQ is off.
0x95	SEQ_TIME_LSB[3]	02		00		00	
0x96	SEQ_TIME_MSB[4]	01	The off time of VIN4A is 13.5ms.	00	VIN4B does not have a sequence when SEQ is off.	00	VIN4C does not have a sequence when SEQ is off.
0x97	SEQ_TIME_LSB[4]	0E		00		00	
0x98	SEQ_TIME_MSB[5]	00	The off time of VIN5A is 0ms.	00	VIN5B does not have a sequence when SEQ is off.	00	The off time of VIN5C is 0ms.
0x99	SEQ_TIME_LSB[5]	00		00		00	
0x9A	SEQ_TIME_MSB[6]	01	The off time of VIN6A is 13.45ms.	00	The off time of VIN6B is 8.9ms.	00	VIN6C does not have a sequence when SEQ is off.
0x9B	SEQ_TIME_MSB[6]	0D		B2		00	
Bank 1							
0x1E	VIN_CH_EN	3F	Channels 1-6 are all enabled.	24	Channel 3 and channel 6 are all enabled.	11	Channel 1 and channel 5 are all enabled.
0x1F	VRANGE_MULT	30	VIN1–VIN4 are 1x scaling, VIN5 and VIN6 are 4x scaling.	37	VIN3 and VIN6 are 4x scaling.	37	VIN1 and VIN5 are 1x scaling.
0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.	3C	AMSK_ON for VIN3 and VIN6 is enabled.	3C	AMSK_ON for VIN1 and VIN5 is enabled.
0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 is enabled.	3C	AMSK_OFF for VIN3 and VIN6 is enabled.	3C	AMSK_OFF for VIN1 and VIN5 is enabled.
0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_EXS for VIN6 is enabled, AMSK_EXS for VIN3 is disabled.	20	AMSK_EXS for VIN1 and VIN5 is enabled.
0xA4	AMSK_ENS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_ENS for VIN6 is enabled, AMSK_ENS for VIN3 is disabled.	20	AMSK_ENS for VIN1 and VIN5 is enabled.
0xA5	SEQ_TOUT_MSB	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.
0xA6	SEQ_TOUT_LSB	25		25		25	
0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.
0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.
0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.

0xC0	SEQ_OFF_EXP[1]	02	The expected sequence log of VIN1A is 2.	00	The expected sequence log of VIN1B is 0.	01	The expected sequence log of VIN1C is 1.
0xC1	SEQ_OFF_EXP[2]	01	The expected sequence log of VIN2A is 1.	00	The expected sequence log of VIN2B is 0.	00	The expected sequence log of VIN2C is 0.
0xC2	SEQ_OFF_EXP[3]	01	The expected sequence log of VIN3A is 1.	01	The expected sequence log of VIN3B is 1.	00	The expected sequence log of VIN3C is 0.
0xC3	SEQ_OFF_EXP[4]	04	The expected sequence log of VIN4A is 4.	00	The expected sequence log of VIN4B is 0.	00	The expected sequence log of VIN4C is 0.
0xC4	SEQ_OFF_EXP[5]	01	The expected sequence log of VIN5A is 1.	00	The expected log of VIN5B is 0.	01	The expected sequence log of VIN5C is 1.
0xC5	SEQ_OFF_EXP[6]	04	The expected sequence log of VIN6A is 4.	03	The expected sequence log of VIN6B is 3.	00	The expected sequence log of VIN6C is 0.

SEQ Sleep Entry Monitoring with Multiple MPQ79500FS Devices

Three MPQ79500FS devices, ACT/SHDN = high, ACT/SLP = high to low

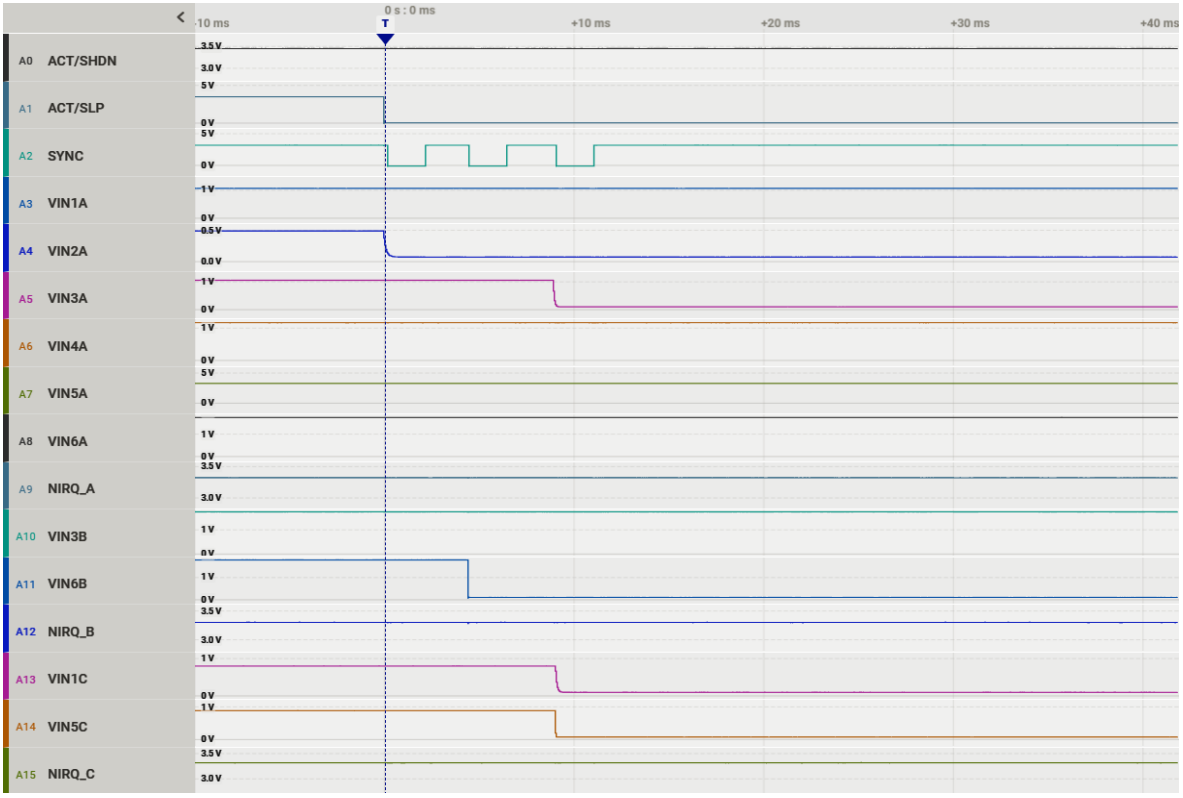


Table 4: Read Register after Timeout

		Part A		Part B		Part C	
Add.	**Register Name**	**Read Result**	**Description**	**Read Result**	**Description**	**Read Result**	**Description**
Bank 0							
0x10~ 0x24	Interrupt Information Registers	00	No interrupt after SEQ_ENS.	00	No interrupt after SEQ_ENS.	00	No interrupt after SEQ_ENS.
0x32	OFF_STAT	00	Channels 1–6 are in the on state.	3B	Channel 3 is in the on state; the other channels are off.	3F	Channels 1–6 are in the off state.
0x36	SEQ_ORD _STAT	03	3 sync pulse count.	03	3 sync pulse count.	03	3 sync pulse count.
0x40	VIN_LVL[1]	AA	1.05V.	00	VIN1B < 0.8V after SEQ_ENS.	00	VIN1C < 0.2V after SEQ_ENS.
0x41	VIN_LVL[2]	3D	VIN2A < 0.2V after SEQ_ENS.	00	VIN2B < 0.8V after SEQ_ENS.	00	VIN2C < 0.8V after SEQ_ENS.
0x42	VIN_LVL[3]	00	VIN3A < 0.2V after SEQ_ENS.	32	1.8V.	00	VIN3C < 0.8V after SEQ_ENS.
0x43	VIN_LVL[4]	C8	1.2V.	00	VIN4B < 0.2V after SEQ_ENS.	00	VIN4C < 0.8V after SEQ_ENS.
0x44	VIN_LVL[5]	7B	3.26V.	00	VIN5B < 0.8V after SEQ_ENS.	00	VIN5C < 0.2V after SEQ_ENS.
0x45	VIN_LVL[6]	32	1.8V.	00	VIN6B < 0.8V after SEQ_ENS.	00	VIN6C < 0.2V after SEQ_ENS.
0x80	SEQ_ENS _LOG[1]	00	VIN1A does not have a sequence during SEQ_ENS.	00	VIN1B does not have a sequence during SEQ_ENS.	03	The rail on VIN1C is down in the third SYNC pulse record as the third sequence log.
0x81	SEQ_ENS _LOG[2]	01	The rail on VIN2A is down in the first SYNC pulse record as the first sequence log.	00	VIN2B does not have a sequence during SEQ_ENS.	00	VIN2C does not have a sequence during SEQ_ENS.
0x82	SEQ_ENS _LOG[3]	03	The rail on VIN3A is down in the third SYNC pulse record as the third sequence log.	00	VIN3B does not have a sequence during SEQ_ENS.	00	VIN3C does not have a sequence during SEQ_ENS.
0x83	SEQ_ENS _LOG[4]	00	VIN4A does not have a sequence during SEQ_ENS.	00	VIN4B does not have a sequence during SEQ_ENS.	00	VIN4C does not have a sequence during SEQ_ENS.
0x84	SEQ_ENS _LOG[5]	00	VIN5A does not have a sequence during SEQ_ENS.	00	VIN5B does not have a sequence during SEQ_ENS.	03	The rail on VIN5C is down in the third SYNC pulse record as the third sequence log.
0x85	SEQ_ENS _LOG[6]	00	VIN6A does not have a sequence during SEQ_ENS.	02	The rail on VIN6B is down in the second SYNC pulse record as the second sequence log.	00	VIN6C does not have a sequence during SEQ_ENS.
0x90	SEQ_TIME _MSB[1]	00	VIN1A does not have a sequence during SEQ_ENS.	00	VIN1B does not have a sequence during SEQ_ENS.	00	The off time of VIN1C is 9.15ms.
0x91	SEQ_TIME _LSB[1]	00		00		B7	
0x92	SEQ_TIME _MSB[2]	00	The OFF time of VIN2A is 0.15ms.	00	VIN2B does not have a sequence during SEQ_ENS.	00	VIN2C does not have a sequence during SEQ_ENS.
0x93	SEQ_TIME _LSB[2]	03		00		00	

0x94	SEQ_TIME_MSB[3]	00	The OFF time of VIN3A is 9.05ms.	00	VIN3B does not have a sequence during SEQ_ENS.	00	VIN3C does not have a sequence during SEQ_ENS.
0x95	SEQ_TIME_LSB[3]	B5		00		00	
0x96	SEQ_TIME_MSB[4]	00	VIN4A does not have a sequence during SEQ_ENS, but VIN5 does.	00	VIN4B does not have a sequence during SEQ_ENS.	00	VIN4C does not have a sequence during SEQ_ENS.
0x97	SEQ_TIME_LSB[4]	00		00		00	
0x98	SEQ_TIME_MSB[5]	00	VIN6A and VIN4A do not have a sequence during SEQ_ENS.	00	VIN5B does not have a sequence during SEQ_ENS.	00	The off time of VIN5C is 9.05ms.
0x99	SEQ_TIME_LSB[5]	00		00		B5	
0x9A	SEQ_TIME_MSB[6]	00	VIN5A does not have a sequence during SEQ_ENS.	00	The off time of VIN6B is 4.45ms.	00	VIN6C does not have a sequence during SEQ_ENS.
0x9B	SEQ_TIME_MSB[6]	00		59		00	
Bank 1							
0x1E	VIN_CH_EN	3F	Channels 1–6 are all enabled.	24	Channel 3 and channel 6 are enabled.	11	Channel 1 and channel 5 are enabled.
0x1F	VRANGE_MULT	30	VIN1–VIN4 are 1x scaling, VIN and VIN6 are 4x scaling.	37	VIN3 and VIN6 are 4x scaling.	37	VIN1 and VIN5 are 1x scaling.
0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.	3C	AMSK_ON for VIN3 and VIN6 is enabled.	3C	AMSK_ON for VIN1 and VIN5 is enabled.
0xA2	AMSK_OFF	3F	AMSK_OFF v VIN1–VIN6 is enabled.	3C	AMSK_OFF for VIN3 and VIN6 is enabled.	3C	AMSK_OFF for VIN1 and VIN5 is enabled.
0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_EXS for VIN6 is enabled, AMSK_EXS for VIN3 is disabled.	20	AMSK_EXS for VIN1 and VIN5 is enabled.
0xA4	AMSK_ENS	06	AMSK ENS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_ENS for VIN6 is enabled, AMSK_ENS for VIN3 is disabled.	20	AMSK_ENS for VIN1 and VIN5 is enabled.
0xA5	SEQ_TOUT_MSB	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.
0xA6	SEQ_TOUT_LSB	25		25		25	
0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.
0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.
0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.
0xE0	SEQ_ENS_EXP[1]	00	The expected sequence log of VIN1A is 0.	00	The expected sequence log of VIN1B is 0.	03	The expected sequence log of VIN1C is 3.
0xE1	SEQ_ENS_EXP[2]	01	The expected sequence log of VIN2A is 1.	00	The expected sequence log of VIN2B is 0.	00	The expected sequence log of VIN2C is 0.
0xE2	SEQ_ENS_EXP[3]	03	The expected sequence log of VIN3A is 3.	00	The expected sequence log of VIN3B is 0.	00	The expected sequence log of VIN3C is 0.
0xE3	SEQ_ENS_EXP[4]	00	The expected sequence log of VIN4A is 0.	00	The expected sequence log of VIN4B is 0.	00	The expected sequence log of VIN4C is 0.
0xE4	SEQ_ENS_EXP[5]	00	The expected sequence log of VIN5A is 0.	00	The expected sequence log of VIN5B is 0.	03	The expected sequence log of VIN5C is 3.
0xE5	SEQ_ENS_EXP[6]	00	The expected sequence log of VIN6A is 0.	02	The expected sequence log of VIN6B is 2.	00	The expected sequence log of VIN6C is 0.

SEQ Sleep Exit Monitoring with Multiple MPQ79500FS Devices

Three MPQ79500FS devices, ACT/SHDN = high, ACT/SLP = low to high

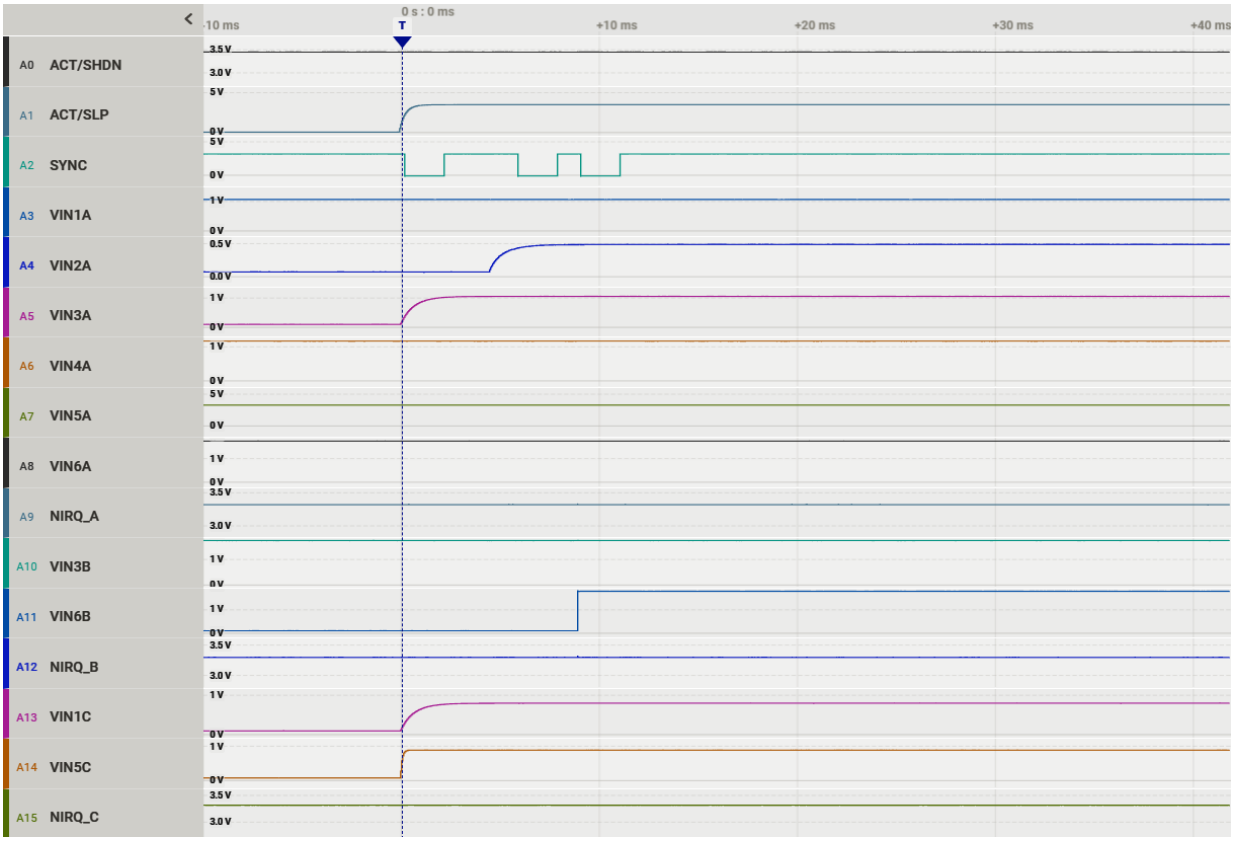


Table 5: Read Register after Timeout

		Part A		Part B		Part C	
Add.	**Register Name**	**Read Result**	**Description**	**Read Result**	**Description**	**Read Result**	**Description**
Bank 0							
0x10 - 0x24	Interrupts information registers	00	No interrupt after SEQ_EXS.	00	No interrupt after SEQ_EXS.	00	No interrupt after SEQ_EXS.
0x32	OFF_STAT	06	Channel 1, channel 4, channel 5, and channel 6 are in the on state; channel 2 and channel 3 are in the off state.	1B	Channel 3 and channel 6 are in the on state; channel 1, channel 2, channel 4, and channel 5 are in the off state.	2E	Channel 1 and channel 5 are in the on state; channel 2, channel 3, channel 4, channel 6 are in the off state.
0x36	SEQ_ORD_STAT	03	3 sync pulse count.	03	3 sync pulse count.	03	3 sync pulse count.
0x40	VIN_LVL[1]	AC	VIN1A is 1.06V in the active state after SEQ_EXS.	00	VIN1B < 0.8V.	78	0.8V.
0x41	VIN_LVL[2]	3D	VIN2A is 0.505V in the active state after SEQ_EXS.	00	VIN2B < 0.8V.	00	VIN2C < 0.8V.
0x42	VIN_LVL[3]	AA	VIN3A is 1.05V in the active state after SEQ_EXS.	32	1.8V.	00	VIN3C < 0.8V.

0x43	VIN_LVL[4]	C8	VIN4A is 1.2V in the active state after SEQ_EXS.	00	VIN4B < 0.2V.	00	VIN4C < 0.8V.
0x44	VIN_LVL[5]	7B	VIN5A is 3.26V in the active state after SEQ_EXS.	00	VIN5B < 0.8V.	8C	0.9V.
0x45	VIN_LVL[6]	32	VIN6A is 1.8V in the active state after SEQ_EXS.	32	1.8V.	00	VIN6C < 0.2V.
0x70	SEQ_EXS_LOG[1]	00	VIN1A does not have a sequence during SEQ_EXS.	00	VIN1B does not have a sequence during SEQ_EXS.	01	The rail on VIN1C is up in the first SYNC pulse record as the first sequence log.
0x71	SEQ_EXS_LOG[2]	02	The rail on VIN2A is up in the second SYNC pulse record as the second sequence log.	00	VIN2B does not have a sequence during SEQ_EXS.	00	VIN2C does not have a sequence during SEQ_EXS.
0x72	SEQ_EXS_LOG[3]	01	The rail on VIN3A is up in the first SYNC pulse record as the first sequence log.	00	VIN3B does not have a sequence during SEQ_EXS.	00	VIN3C does not have a sequence during SEQ_EXS.
0x73	SEQ_EXS_LOG[4]	00	VIN4A does not have a sequence during SEQ_EXS.	00	VIN4B does not have a sequence during SEQ_EXS.	00	VIN4C does not have a sequence during SEQ_EXS.
0x74	SEQ_EXS_LOG[5]	00	VIN5A does not have a sequence during SEQ_EXS.	00	VIN5B does not have a sequence during SEQ_EXS.	01	The rail on VIN5C is up in the first SYNC pulse record as the first sequence log.
0x75	SEQ_EXS_LOG[6]	00	VIN6A does not have a sequence during SEQ_EXS.	03	The rail on VIN6B is up in the third SYNC pulse record as the third sequence log.	00	VIN6C does not have a sequence during SEQ_EXS.
0x90	SEQ_TIME_MSB[1]	00	VIN1A does not have a sequence during SEQ_EXS.	00	VIN1B does not have a sequence during SEQ_EXS.	00	The up time of VIN1C is 1.5ms.
0x91	SEQ_TIME_LSB[1]	00		00		1E	
0x92	SEQ_TIME_MSB[2]	00	The up time of VIN2A is 0.15ms.	00	VIN2B does not have a sequence during SEQ_EXS.	00	VIN2C does not have a sequence during SEQ_EXS.
0x93	SEQ_TIME_LSB[2]	75		00		00	
0x94	SEQ_TIME_MSB[3]	00	The up time of VIN3A is 9.05ms.	00	VIN3B does not have a sequence during SEQ_EXS.	00	VIN3C does not have a sequence during SEQ_EXS.
0x95	SEQ_TIME_LSB[3]	1D		00		00	
0x96	SEQ_TIME_MSB[4]	00	VIN4A does not have a sequence during SEQ_EXS.	00	VIN4B does not have a sequence during SEQ_EXS.	00	VIN4C does not have a sequence during SEQ_EXS.
0x97	SEQ_TIME_LSB[4]	00		00		00	
0x98	SEQ_TIME_MSB[5]	00	VIN5A does not have a sequence during SEQ_EXS.	00	VIN5B does not have a sequence during SEQ_EXS.	00	The up time of VIN5C is 0.15ms.
0x9A	SEQ_TIME_MSB[6]	00	VIN6A do not have sequence when SEQ_EXS.	00	The up time of VIN6B is 9.05ms.	00	VIN6C do not have sequence when SEQ_EXS.
0x9B	SEQ_TIME_MSB[6]	00		B5		00	
Bank 1							
0x1E	VIN_CH_EN	3F	Channels 1–6 are all enabled.	24	Channel 3 and channel 6 are enabled.	11	Channel 1 and channel 5 are enabled.

0x1F	VRANGE_MULT	30	VIN1–4 are 1x scaling, VIN5 and VIN6 are 4x scaling.	37	VIN3 and VIN6 are 4x scaling.	37	VIN1 and VIN5 are 1x scaling.
0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.	3C	AMSK_ON for VIN3 and VIN6 is enabled.	3C	AMSK_ON for VIN1 and VIN5 is enabled.
0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 is enabled.	3C	AMSK_OFF for VIN3 and VIN6 is enabled.	3C	AMSK_OFF for VIN1 and VIN5 is enabled.
0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_EXS for VIN6 is enabled, AMSK_EXS for VIN3 is disabled.	20	AMSK EXS for VIN1 and VIN5 is enabled.
0xA4	AMSK_ENS	06	AMSK_ENS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_ENS for VIN6 is enabled, AMSK_ENS for VIN3 is disabled.	20	AMSK ENS for VIN1 and VIN5 is enabled.
0xA5	SEQ_TOUT_MSB	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.
0xA6	SEQ_TOUT_LSB	25		25		25	
0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.
0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.
0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.
0xD0	SEQ_EXS_EXP[1]	00	The expected sequence log of VIN1A is 0.	00	The expected sequence log of VIN1B is 0.	01	The expected sequence log of VIN1C is 1.
0xD1	SEQ_EXS_EXP[2]	02	The expected sequence log of VIN2A is 2.	00	The expected sequence log of VIN2B is 0.	00	The expected sequence log of VIN2C is 0.
0xD2	SEQ_EXS_EXP[3]	01	The expected sequence log of VIN3A is 1.	00	The expected sequence log of VIN3B is 0.	00	The expected sequence log of VIN3C is 0.
0xD3	SEQ_EXS_EXP[4]	00	The expected sequence log of VIN4A is 0.	00	The expected sequence log of VIN4B is 0.	00	The expected sequence log of VIN4C is 0.
0xD4	SEQ_EXS_EXP[5]	00	The expected sequence log of VIN5A is 0.	00	The expected sequence log of VIN5B is 0.	01	The expected sequence log of VIN5C is 1.
0xD5	SEQ_EXS_EXP[6]	00	The expected sequence log of VIN6A is 0.	03	The expected sequence log of VIN6B is 3.	00	The expected sequence log of VIN6C is 0.

FUNCTIONAL BLOCK DIAGRAM

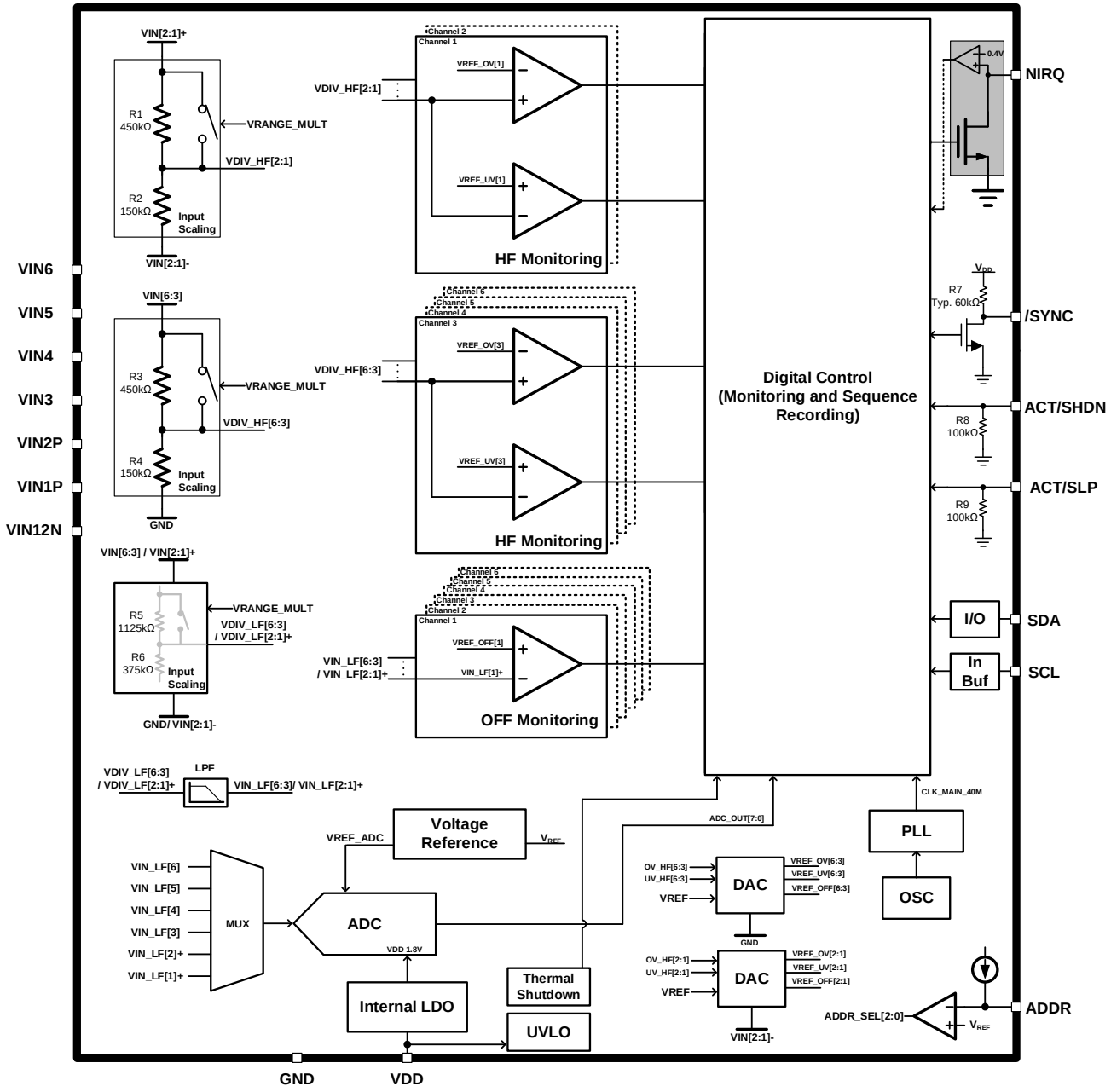


Figure 1: Functional Block Diagram

OPERATION

The MPQ79500FS is a functional safety voltage and sequence monitor. It is engineered for advanced driver assistance systems (ADAS) and autonomous driving platforms. The MPQ79500FS provides the voltage and sequencing monitoring function for the entire platform.

The MPQ79500FS contains six input channels for monitoring. Voltage-level monitoring is implemented to detect high-frequency (HF) and low-frequency (LF) voltage violations. In addition, the device reports the LF voltage level and detects and timestamps when the voltage threshold is reached. The input voltage (V_{IN}) sequence is monitored to determine when the channels transition between states.

For applications containing more than six rails, the sync I/O function is implemented to enable multi-device sequence synchronization and tagging. Low-power mode (LPM) can be selected for an extremely low quiescent current.

The MPQ79500FS's configurability and flexibility enable design reuse across different applications and system-on-chip (SoC) generations. The built-in safety mechanisms such as built-in self-testing (BIST) provide a high diagnostic coverage, which helps a system to achieve an ASIL-D safety rating.

High-Frequency and Low-Frequency Voltage-Level Monitoring

The MPQ79500FS monitors up to six voltage channels with four single-ended channels and two differential channels. Two different monitor scales can be selected via VRANGE_MULT on every input channel, which defines the V_{IN} range (0.2V to 1.475V, or 0.8V to 5.5V). The following voltage-level monitoring functionalities are provided:

1. The real-time, monitored LF voltage level is recorded in the VIN_LVL[x] register, and can be read via the I²C.
2. The HF monitoring faults are detected and reported for over-voltage (OV) and under-voltage (UV) violations down to a 100ns pulse, depending on the debounce time (set via OV_DEB[3:0] and UV_DEB[3:0]).
3. The LF voltage drift is detected and reported for OV and UV violations. The cutoff frequency of the LPF's G(s) can be configured via the FC_LF[x] register.
4. The order of on, off, and sleep entry/exit power sequences are detected and recorded.
5. In LPM, only HF voltage detection works with no debounce time to reduce loss.

Figure 2 shows the voltage monitoring structure in high-power mode (HPM). Figure 3 on page 27 shows this structure in LPM.

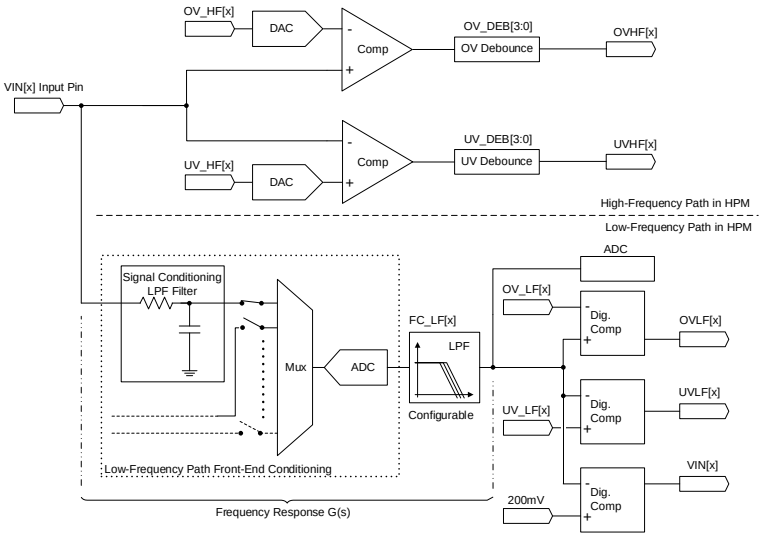


Figure 2: Voltage Monitoring Structure in HPM

Figure 2 on page 26 shows the architecture when SLEEP_PWR is set to 1, and shows the monitoring signal paths in HPM. These are described in greater detail below:

1. The HF path monitors the voltage signal down to 100ns pulse-width. It is adopted to detect voltage signal violations of OV and UV thresholds, defined in the OV_HF[x] and UV_HF [N] registers.
2. An 8-bit analog-to-digital converter (ADC) is designed to support the LF path functionalities. The LF path is used to:
   a. Monitor long-term voltage drifts and erroneous voltage settings, and to detect OV and UV threshold violations (via OV_LF[x] and UV_LF[x]) within the bandwidth set by the FC_LF[x] register.
   b. Measure and log the real-time voltage rails' levels to the host (VIN_LVL[x]).
   c. Timestamp (with t_{SEQ_LSB} resolution) the power sequences for on, off, and sleep exit/entry modes when the monitored voltages cross the UV_LF[x] / OFF thresholds (depending on what is set via OFF_UV[x]).

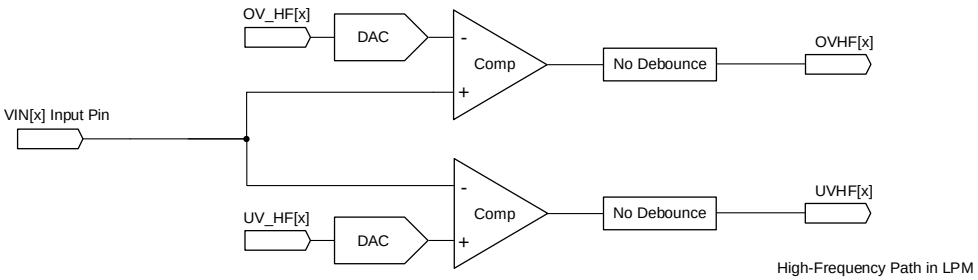


Figure 3: Voltage Monitoring Structure in LPM

Figure 3 shows the architecture when SLEEP_PWR is set to 0, and shows the monitoring signal paths in LPM. These are described in greater detail below:

1. In LPM, the HF path monitors the voltage signal with no debounce time, so the OV and UV flags are reported when there is voltage noise on VIN[x]. The OV and UV thresholds are defined in OV_HF[x] and UV_HF[x], respectively.
2. ADC is inactive in LPM. The value in VIN_LVL[x] remains at the same level that was set before LPM. OVLF and UVLF are inactive as well, even if IEN_OVLF and IEN_UVLF are enabled.

The MPQ79500FS supports up to two differential input channels for high-current applications and four common input channels. The differential input channels (CH1 and CH2) share the same reference (VIN12N). VIN12N, VIN1P, and VIN2P should be connected to GND if the differential input channels are not used.

If the voltage exceeds the channel monitoring limit (1.475V for 1x scaling and 5.5V for 4x scaling), ADC accuracy is no longer guaranteed. Different scale set-ups are allowed for different channels with different input voltages.

Table 6 on page 28 shows the summary of voltage-level monitoring.

Table 6: Voltage-Level Monitoring Summary

State	SLEEP_ PWR	ADC Monitoring	Available Voltage Threshold Monitoring (10)	
			Off Rails	On Rails
Idle	0 (LPM)	Inactive	OVHF (no debounce)	OVHF (no debounce) (in application, there may not be rails that are on in the idle state)
	1 (HPM)	Active	OVHF, OVLF	OVHF, OVLF (in application, there may not be rails that are on in the idle state)
Active	1 (HPM)	Active	OVHF, OVLF (in application, UV threshold monitoring should be disabled by host for the rails that are off in the active state)	OVHF, UVHF, OVLF, UVLF
Sleep	0 (LPM)	Inactive	OVHF (no debounce) (AMSK_ENS should be enabled for rails in sleep mode, while UVHF should be disabled for rails that are off in the sleep state)	OVHF (no debounce), UVHF (no debounce)
	1 (HPM)	Active	OVHF, OVLF (AMSK_ENS should be enabled for rails in sleep mode, while UVHF and UVLF should be disabled for rails that are off in the sleep state)	OVHF, UVHF, OVLF, UVLF

Note:

10) Some of the OV/UV monitoring function do not work if the function is disabled or an auto-mask is applied. For more details, see Table 7 on page 42.

Monitoring Operation

Once the supply voltage (V_{DD}) exceeds $UVLO_{VTH-R}$, the MPQ79500FS turns on. When the device is on, BIST is optionally executed (depending on the AT_POR bit, which is set via the one-time programmable [OTP] memory) and the configuration is loaded from the OTP and non-volatile memory (NVM). This process is assisted by the error-correction code (ECC), supporting single-error correction (SEC) and double-error detection (DED).

After that, the I^2C and fault reporting (through NIRQ) are active. The details of the configuration load, ECC, and BIST results are reported in the TEST_INFO register.

Figure 4 on page 29 shows the MPQ79500FS's state machine as start-up completes.

Normal operation can be divided into several states by two pins: ACT/SHDN and ACT/SLP. In the operation state machine, all of the sequence monitoring states represent functional sequences that are executed while transitioning states. These sequences cannot be interrupted by any input pin (GPI) actions or I^2C commands until SEQ_TOUT expires.

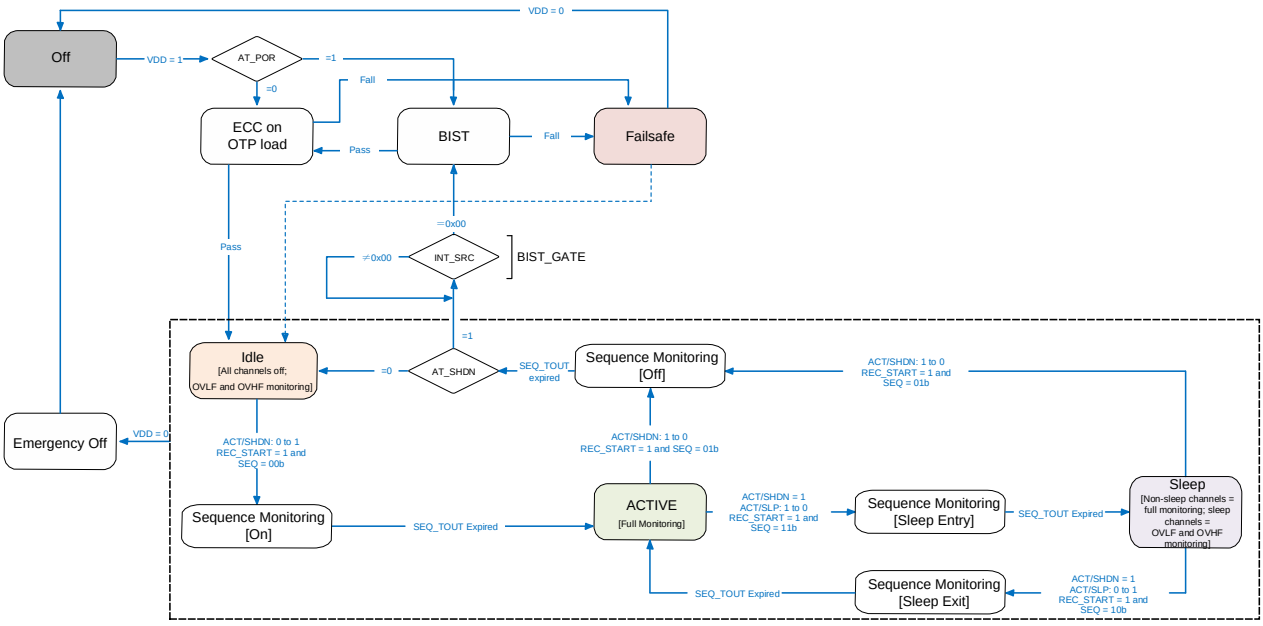


Figure 4: MPQ79500FS State Machine

For active and idle mode, the MPQ79500FS operates at the active or idle state, respectively. For active mode, the input rails are expected to be fully on, while they are off in idle mode. The sleep state is designed for system LPM. This state should be considered a temporary mode during the active state. Sleep mode cannot be activated in the idle state. This means that the ACT/SLP pin is nonfunctional once ACT/SHDN is low.

Different states change at the rising and falling edges of ACT/SHDN and ACT/SLP. When start-up is complete (including the optional BIST), the default state is idle, regardless of whether ACT/SHDN and ACT/SLP are high or low. To enter the active state, a rising edge on ACT/SHDN must be detected. Similarly, the MPQ79500FS cannot enter the sleep state until a falling edge on ACT/SLP is triggered while in the active state.

To support cases where state transitions are required when the pins are not transitioning, there are two ways to trigger state transitions:

1. The ACT/SHDN and ACT/SLP pins change state. The ACT/SHDN pin initiates power on/power off sequences, while the ACT/SLP pin initiates sleep entry/exit sequences. Both pins begin sequence recording for the V_{IN} rails.
2. The SEQ_REC_CTL register changes. Set the REC_START bit to 1 to activate a sequence transmission. The operating state should be defined in the sequence selection bits (SEQ[1:0]), which store the logs (sequence tagging) in the correct registers and perform the proper sequence comparison.

For any control input pin state changes or REC_START bit changes within the sequence timeout time (SEQ_TOUT), additional triggers are ignored. The second sequence is not used or recorded. The sequence logs of the second sequence are not recorded in any register groups. Note the following rules for the MPQ79500FS:

- ACT/SLP is ignored while ACT/SHDN is low. It is ignored until SEQ_TOUT, after the ACT/SHDN pin transitions from 0 to 1.
- Once a sequence recording starts, the sequence triggers (including ACT/SHDN, ACT/SLP, and the SEQ_REC_CTL register) are ignored until the current sequence timer (SEQ_TOUT) is reached. After sequence timeout, a new sequence triggering edge is required to start a new sequence recording.
- When working in LPM, sequence triggering (by SEQ_REC_CTL, ACT/SHDN, or ACT/SLP) is ignored. The MPQ79500FS

remains in the previous state. The IC operates in HPM and executes a sequence transmission until SLEEP_PWR is set to 1. To trigger sequence transition monitoring, the MPQ79500FS must leave LPM and enter HPM.

Built-In Self-Testing (BIST) and Load Configuration

The MPQ79500FS provides BIST for both critical analog and logic functions. BIST is optionally executed when the device starts up, and can be online-complied through the AT_SHDN after off sequence monitoring (see Figure 4 on page 29). However, certain safety items are periodically checked while operating, instead of only being checked once during start-up.

The items that are checked in real time are listed below:

1. I²C protocol PEC: Data transfers through the I²C have an attached packet error checking (PEC) code. The slave device rejects data unless the PEC matches the master device. PEC is an optional function related to EN_PEC and REQ_PEC. See the Packet Error Checking (PEC) section page 52 for more details.
2. /SYNC and NIRQ pin short to power: Short to power conditions are checked when the device pulls the /SYNC pin or NIRQ pin low, instead of checking for these conditions periodically. The fault is reported by the SYNC or NIRQ bit. Note that when NIRQ short to power occurs, the device can no longer show the fault by pulling down the NIRQ pin, and the host must read the NIRQ bit for this information. A pin short is also checked when there have been forced assertions through the FORCE_SYNC and FORCE_NIRQ bits.
3. Thermal warning: The MPQ79500FS offers thermal warning protection. If the thermal shutdown (TSD) bit is enabled and the silicon die temperature exceeds the rising threshold (about 170°C), then this bit reports. Once the temperature drops below the falling threshold (about 150°C), this bit de-asserts. If the TSD bit reports a fault, NIRQ is pulled down, and the fault cannot be cleared until the temperature drops below the falling threshold. In HPM, TSD is level-triggered. In LPM, TSD is edge-triggered. If TSD is reported in LPM, set SEEP_PWR to entry HPM first and clear the TSD flag once the temperature drops below the falling threshold.
4. Runtime VM CRC: When there is no data transferring, a cyclic redundancy check (CRC) continues operating to detect accidental changes to the data.
5. State machine error monitoring: The state machine sequence is checked with one-hot coding, including the system state and several functional states.
6. I²C write back check: The I²C write register map has an automatic readback check.
7. Clock monitoring: In addition to the system clock, there is a reference clock for cross-checking with the system clock to detect clock errors. Both system clock and reference clock failures pull down NIRQ and report the interrupt status in the internal fault. Clock monitoring always works; if a clock failure is detected, a fault is reported via the CLK_FAIL bit. NIRQ latches low and cannot be cleared, since the device might be unpredictable with a damaged system clock. The host reacts according to the response selected by the user.

The items checked during start-up are listed below:

1. NVM ECC: While loading the configuration from the NVM, every 32 bytes of data are attached with 7 bits of ECC to protect against data integrity issues and maximize system availability. 1-bit errors can be self-corrected by the ECC, though double errors can only be detected. If SEC or DED occurs, they are reported. The MPQ79500FS executes ECC again after BIST since registers are reset during BIST.
2. SEC: If SEC occurs, the fault is reported via the ECC_SEC bit, NIRQ is pulled down, and the information is recorded to ECC_SEC. Faults in ECC_SEC can be written to one to be cleared, and NIRQ recovers to high. However, the host can read the error status from ECC_SEC and respond.

The SEC check can be disabled by setting the ECC_SEC bit to 0. If ECC occurs in this situation, then ECC_SEC does not report the fault and NIRQ is not pulled down. However, the host can read the error status from ECC_SEC and respond.

3. DED: If DED occurs, the fault is reported in the ECC_DED bit, the information is recorded in the TEST_INFO register, and NIRQ is pulled down. ECC_DED cannot be written to once to be cleared, NIRQ latches low, or the host reacts accordingly. DED cannot be disabled.
4. Voltage Monitoring (VM) BIST: VM BIST is checked when loading data from the NVM.
5. Analog BIST (ABIST): ABIST typically involves exercising diagnostic circuits into and out of fault scenarios by injecting currents or voltages into the diagnostic circuit. This ensures that the diagnostic circuit can switch to both fault and non-fault states. This means that the analog circuit is controlled by a digital circuit that verifies the correct functionality of the analog safety mechanisms. During this process, all safety-related comparators and monitored HF reference voltages are checked.
6. Logic BIST (LBIST): The logic circuits of the MPQ79500FS are checked during LBIST. If an error is detected in LBIST, NIRQ is pulled down and the error is reported in INT_TEST. The BIST bit is recorded to the TEST_INFO register, and interrupts are recorded to INT_TEST. A BIST caused by LBIST cannot be written to one to be cleared, so NIRQ remains latched, and the host should react accordingly.

If IEN_TEST is set to 1, once BIST is completed, an I_BIST_C (INT_TEST[1]) interrupt is triggered and NIRQ is pulled down to indicate BIST completion (regardless of whether any fault is detected during BIST). Write 1 to clear this interrupt. The default status of IEN_TEST is loaded from the OTP. If this register is set to 0, users can acknowledge the BIST status by reading the ST_BIST_C bit via the I^2C.

For the full safety-related instructions, contact an MPS FAE.

Idle Monitoring

The system is not expected to constantly remain fully active, so the MPQ79500FS is designed with a system idle mode. In the idle state, all of the input channels are assumed to be in the off state (e.g. V_{IN} is below the OFF threshold). Under-voltage (UV) detection is unnecessary under such conditions, so UVLF and UVHF are inactive in the idle state. For enabled channels in the off state, only the OVLF and OVHF thresholds are monitored to ensure the reliability limits are not violated. To monitor OVLF, the ADC keeps working and records V_{IN} in this state.

If a channel that is off suddenly turns on in an idle state, it is not immediately detected by the MPQ79500FS. If there is an over-voltage (OV) detection event, the host can periodically poll the OFF_STAT register for the off status of each rail. In addition, if the voltage rails accidentally turn on in the idle state, this leads to a sequence mismatch once sequence monitoring turns on. In this scenario, a sequence fault interrupt is triggered.

The MPQ79500FS remains in the idle state after power on (and optional BIST) is complete, regardless of whether the ACT/SHDN or ACT/SLP pins are high or low, since these pins are edge-triggered. If an ECC error or BIST fail occurs, the IC enters a failsafe state and reports the fault, then operates as it would in the idle state.

If a falling edge is detected on ACT/SHDN (goes from 1 to 0) while operating in the active or sleep state, the device accesses the idle state.

Once the SLEEP_PWR bit is set to 0 to enter LPM, only OVHF detection is active in the idle state, and other sequence triggers are ignored.

Active Monitoring

The MPQ79500FS complies with full monitoring while in the active state. The device monitors the V_{IN} rails against the UVHF, OVHF, UVLF, and OVLF thresholds to detect V_{IN} violations. V_{IN} is recorded via the ADC and stored in VIN_LVL[x].

All input rails are expected to be on during this state, but the rails can be connected to

channels that are below the OFF threshold (and in an off state).

When the MPQ79500FS is in the active state, the UVLF/UVHF interrupts are normally disabled for the channel in the off state (determined by IEN_UVLF and IEN_UVHF). Once the connected rail turns on, the host can enable the channels' UVLF/UVHF interrupts to activate full monitoring. Similarly, before the rail turns off, the host should disable the channels' UVLF/UVHF interrupts to avoid detecting false UV violations while ramping down.

Other enabled channels can be turned off as a result of ACT/SLP transitioning from 1 to 0. These channels are identified by the AMSK_ENS auto-mask register, which is used to avoid interrupts of UVLF and UVHF. Meanwhile, OVLF and OVHF are still monitored to ensure that reliability limits are not violated. For the operation details, see the Sequence Monitoring Sleep Entry Sequency Monitoring on page 34 and the Sleep Exit section Sequency Monitoring on page 37.

When BIST is complete, the device remains in the idle state, even if ACT/SHDN is 1. The device remains in the idle state until ACT/SHDN goes from 0 to 1, since the ACT/SHDN pin is edge-triggered. The MPQ79500FS can enter the active state from the idle state (by triggering a rising edge on the ACT/SHDN pin or by setting REC_START) or from the sleep state (by triggering the falling edge of the ACT/CLP pin or by setting REC_START).

Sleep Monitoring

Consider conditions when the system operates while some voltage rails are off. During sleep monitoring, the MPQ79500FS allows the system to only monitor some channels (called partial monitoring) instead of enabling full monitoring. In this state, only the OVLF and OVHF thresholds are monitored on the sleep channels, while full monitoring is carried out on the non-sleep channels. The sleep channels can be determined in the AMSK_ENS register. See the Sleep Exit Sequence Monitoring section on page 37 for more details.

The MPQ79500FS enters the sleep monitoring state once sequence monitoring (sleep entry) is complete. Sleep monitoring should be considered a temporary system mode during full monitoring, and it should only be entered from the active state. ACT/SLP cannot be pulled down while in the idle state to enter the sleep state.

Low-Power Mode (LPM)

The MPQ79500FS can operate in LPM in idle and sleep states. LPM is used when the load system is powered down, and the power monitor only maintains the lowest level of protection.

During LPM, most functionalities are masked to reduce the device's quiescent current (I_Q). The ADC and LF protections are automatically disabled in LPM. To protect the system from emergencies, asynchronous HF protection remains activated. This means there is HF protection without any debounce time (for debounce time details, see the High-Frequency and Low-Frequency Voltage-Level Monitoring section on page 26).

While entering LPM in the idle state, all protections are deactivated except for OVHF (without a debounce time). While entering LPM in the sleep state, OVLF and UVLF protections are both disabled. For non-sleep channels, both OVHF and UVHF (without a debounce time) are monitored. For sleep channels, only OVHF works due to the auto-mask. Any OV/UV violation is reported via the corresponding registers as other states (e.g. INT_OVHF[x] and INT_UVHF[x]).

LPM can be initiated by setting the power mode selection bit (SLEEP_PWR) to 0. Its default value is 1. This bit can only be set in idle or sleep states, or be loaded from the NVM; otherwise, the set action is ignored.

In LPM, it is not recommended to change any internal settings for the MPQ79500FS. Only the following registers writes are guaranteed to function normally: OV_HF, UV_HF, SEQ_TOUT, IEN_OVHF, and IEN_UVHF. Other than these registers, all others should be changed before entering LPM. Note that all registers can be read normally via the I^2C.

Figure 5 and Figure 6 on page 33 show the recommended process to enter. It is vital to disable vendor interrupts before writing to

SLEEP_PWR to enter LPM; otherwise, a fault may be reported. I²C transaction is not allowed while the device leaves LPM to enter an idle or sleep state. In this scenario, the host should wait at least 400µs before writing to the next I²C command.

Since transitions are not expected in LPM, certain actions (e.g. toggling ACT/SHDN and ACT/SLP pin or setting the REC_START bit) are invalid and ignored.

In HPM, the voltage threshold monitor is level-triggered, so the fault cannot be cleared until the violation voltage has been removed. In LPM, the voltage threshold monitor is edge-triggered, so the interrupt can be cleared after the rail's edge.

If any voltage threshold fault reported in HPM, the interrupt cannot be cleared after entering LPM, even if the OV/UV violation has been removed after entering LPM. Do not try to enter LPM while there are faults. Rather than disable protections, all faults should be cleared and removed before entering LPM.

Figure 5 shows how to activate LPM from the idle state. Figure 6 shows how to activate LPM from the sleep state.

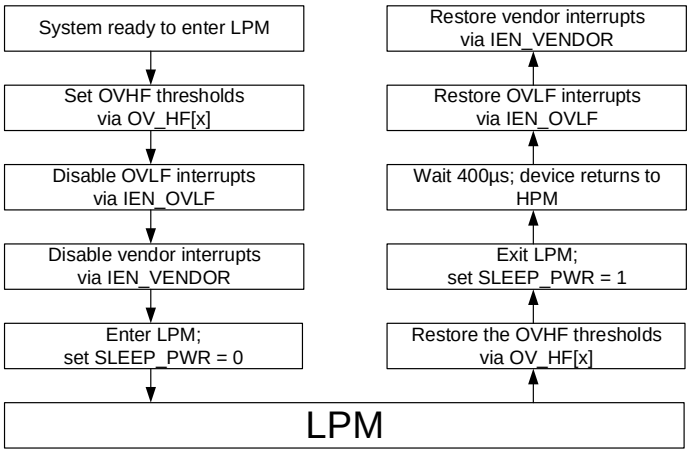


Figure 5: Entering LPM from an Idle State

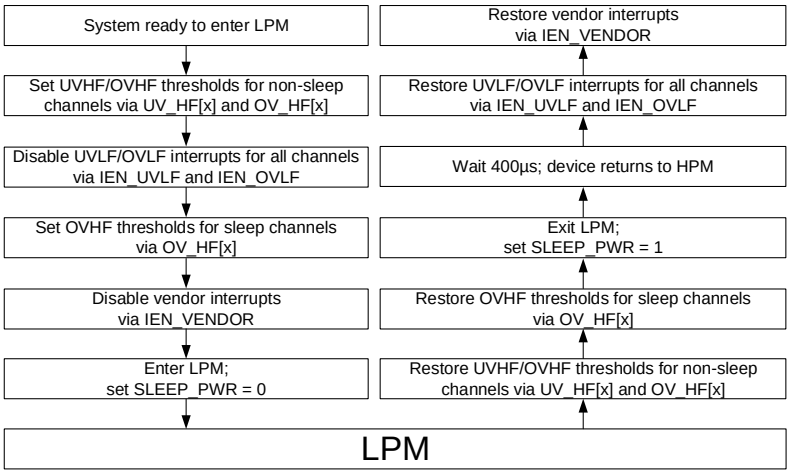


Figure 6: Entering LPM from the Sleep State

On Sequence Monitoring

In addition to voltage monitoring, the MPQ79500FS also monitors the voltage rail sequences while changing states. On sequence monitoring activates under the following conditions:

1. ACT/SHDN transitions from 0 to 1.
2. The host sets REC_START = 1 in the SEQ_REC_CTL register while SEQ[1:0] = 0x00b.

When on sequence monitoring starts, the MPQ79500FS takes several actions:

1. The synchronization counter in register SEQ_ORD_STAT is reset to 0 for the new power sequence recording.
2. The REC_ACTIVE bit is set to 1 to indicate the start of sequence recording.
3. In the SEQ_REC_STAT register, the SEQ[1:0] bits are set to the current sequence (e.g. 00b).
4. If the sequence overwrite bit is enabled (EN_SEQ_OW = 1), then the sequence logging registers (SEQ_ON_LOG[x]) are overwritten with new sequences. If SEQ_ON_RDY = 1, there is data in the register that has not been read by the host. If there was a SEQ_ON_LOG before this data, then the sequence overwrite flag (SEQ_ON_OW) is set to 1 to indicate that the sequence has been overwritten.

   After reading all of the SEQ_ON_LOG registers of each enabled channel, SEQ_ON_RDY and SEQ_ON_OW are set to 0. If SEQ_ON_RDY = 0, then after SEQ_ON, SEQ_ON_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
5. If the timestamp overwrite bit is enabled (EN_TS_OW = 1), then the timestamp logging registers (SEQ_TIME_xSB[x]) are overwritten by the new timestamp. If TS_RDY = 1, then the timestamp overwrite flag (TS_OW) is set to 1 to indicate that the timestamp has been overwritten. If TS_RDY = 0, then after SEQ_ON, TS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
6. If the sequence overwrite bit is disabled (EN_SEQ_OW = 0) and there is data in register SEQ_ON_LOG[x] that has not been read by the host (SEQ_ON_RDY = 1), new data is not written to the registers SEQ_ON_LOG[x]. The sequence overwrite flag (SEQ_ON_OW) is set to 1 to indicate that data cannot be written. If SEQ_ON_RDY = 0, then after SEQ_ON, SEQ_ON_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
7. If the timestamp overwrite bit is disabled (EN_TS_OW = 0) and there was data not yet read by the host (TS_RDY = 1), then the data is not written to the registers. The timestamp overwrite flag (TS_OW) is set to 1 to indicate that data cannot be written. If TS_RDY = 0, then after SEQ ON, TS_RDY is set to 1 to indicate that there is data in the register has not yet been read by the host.
8. The internal sequence timer (re)starts.

For details on the sequence operation and timestamp overwrite function, see the Recorded Data Handling section on page 42.

As each rail crosses the UVLF or OFF voltage threshold, the rising sequence order and timestamp are tagged. Then the following occurs:

1. The tag order is stored in the relevant status register SEQ_ON_LOG[x] if allowed by the overwrite settings and statuses. The event timestamp is stored in registers SEQ_TIME_MSB[x] and SEQ_TIME_LSB[x], depending on the overwrite settings and statuses.
2. The SEQ_ON_LOG[x] register is compared to the expected sequence order value, defined in register SEQ_ON_EXP[x]. If a mismatch is detected, then a SEQ fault interrupt is triggered and NIRQ pulls down. This function is only active when the relevant interrupt enable bit (IEN_SEQ_ON) is set. If the overwrite settings and recording statuses do not allow new data to be written to the logging registers, then the comparison is not performed and an interrupt is not generated.

As each rail passes the UVLF threshold (UV_LF[x]), the relevant UV and OV interrupts are unmasked automatically within 10µs, and enabled/disabled according to the IEN_UVLF, IEN_UVHF, and IEN_OVHF registers. Even though SEQ_UP_THLD uses the OFF threshold rather than UV threshold, auto-masking is still inactive for 10µs after the rail crosses the UVLF threshold.

After a timeout, tagging stops and the following occurs:

1. The REC_ACTIVE bit is cleared automatically to indicate the end of sequence recording.

2. If the rails are up with the correct sequence, the MPQ79500FS enters the active state and starts full monitoring.
3. If any rail has a tag that does not match the value in the relevant SEQ_ON_EXP[x] register, NIRQ asserts. The MPQ79500FS continues active monitoring, and the safety microcontroller (SMCU) reacts to the interrupt request and brings the system to a safe state.

Figure 7 shows the on sequence monitoring process.

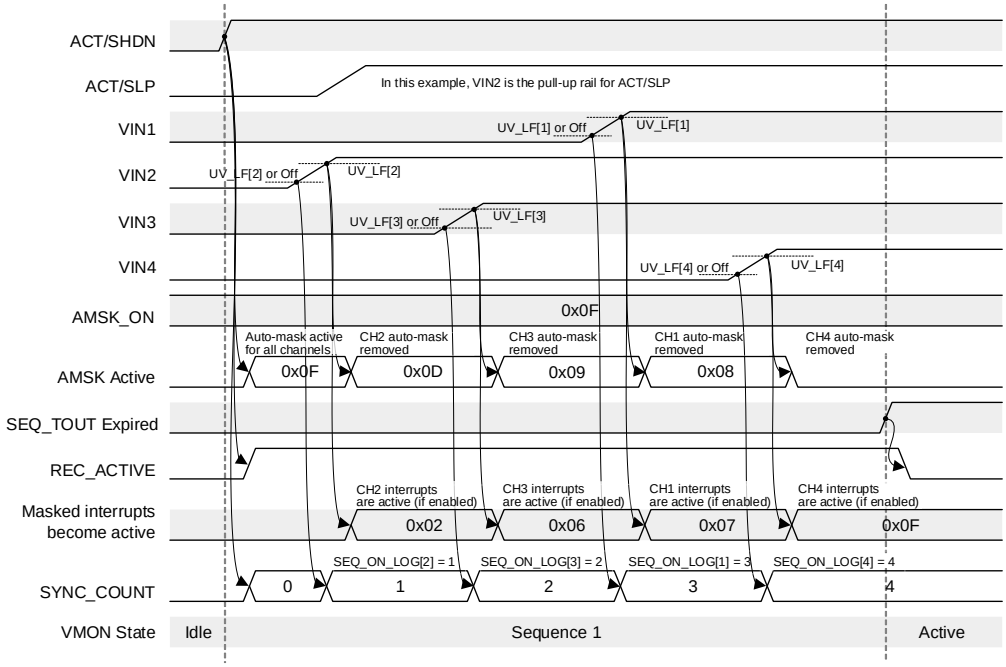


Figure 7: On Sequence Monitoring

Sleep Entry Sequence Monitoring

The MPQ79500FS executes sleep entry sequence monitoring when the device enters the sleep monitoring state. It is expected that some voltage rails turn off, and the system switches to LPM. The following conditions trigger the sleep entry sequence:

1. ACT/SLP transitions from 1 to 0 while ACT/SHDN = 1.
2. The host sets REC_START = 1 in the SEQ_REC_CTL register while SEQ[1:0] = 0x11b.

Sleep entry monitors the power sequence in which the sleep rails turn off. When the device enters sleep mode, the following occurs:

1. The synchronization counter in register SEQ_ORD_STAT is reset to 0 for the new power sequence recording.
2. The REC_ACTIVE bit is set to 1 to indicate the start of sequence recording.
3. In the SEQ_REC_STAT register, the SEQ[1:0] bits are set to 11b to indicate the current recording sequence.
4. If the sequence overwrite bit is enabled (EN_SEQ_OW = 1), then the sequence logging registers (SEQ_ENS_LOG[x]) are overwritten by the new sequence. If SEQ_ENS_RDY = 1, then the sequence overwrite flag (SEQ_ENS_OW) is set to 1 to indicate that the sequence has been overwritten. If SEQ_ENS_RDY = 0, then after sleep entry SEQ_ENS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
5. If the timestamp overwrite bit is enabled (EN_TS_OW = 1), then the timestamp logging registers (SEQ_TIME_xSB[x]) are overwritten by the new timestamp. If TS_RDY = 1, then the timestamp overwrite flag (TS_OW) is set to 1 to indicate that the timestamp has been overwritten. If TS_RDY = 0, then after sleep entry TS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.

6. If the sequence overwrite bit is disabled (EN_SEQ_OW = 0) and data has not yet been read by the host (SEQ_ENS_RDY = 1), then the data is not written to the registers and the sequence overwrite flag (SEQ_ENS_OW) is set to 1 to indicate that data cannot be written. If SEQ_ENS_RDY = 0, then after sleep entry SEQ_ENS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
7. If the timestamp overwrite bit is disabled (EN_TS_OW = 0) and data has not yet been read by the host (TS_RDY = 1), then the data is not written to the registers and the timestamp overwrite flag (TS_OW) is set to 1 to indicate that data cannot be written. If TS_RDY = 0, then after sleep entry TS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
8. The internal sequence timer (re)starts.

As each rail crosses its UVLF or OFF threshold, the falling sequence order and timestamp are tagged. This process is described below:

1. If enabled via the overwrite settings and statues, the tag order is stored in the relevant status register (SEQ_ENS_LOG[x]). The event timestamp is stored in registers SEQ_TIME_MSB[x] and SEQ_TIME_LSB[x], as determined by the overwrite settings and statuses.
2. The SEQ_ENS_LOG[N] register is compared to the expected sequence order value, defined in register SEQ_ENS_EXP[x]. If a sequence mismatch is detected, an interrupt is triggered and NIRQ asserts. This function is only active when the relevant interrupt enable bit (IEN_SEQ_ENS) is set. If the overwrite settings and recording statuses do not allow new data to be written to the logging registers, then the comparison is not performed and an interrupt is not generated.

To define the sleep channels in the sleep monitoring state, the MPQ79500FS inputs the auto-mask register (AMSK_ENS) selections. The interrupts for UVLF and UVHF are masked (disabled). UVLF and UVHF are not reactivated as long as ACT/SLP = 0 and ACT/SHDN = 1. The auto-mask settings can be changed online.

If some rails are in the on sequence and will not be off when entering sleep mode, or will be non-sleep channels, then AMSK_ENS and AMSK_EXS should be set to 0 in order to continue monitoring UVHF and UVLF in sleep mode.

After a timeout, tagging stops and the below actions are carried out:

1. The REC_ACTIVE bit is cleared to indicate the end of sequence recording.
2. If rails go down in the correct sequence, the MPQ79500FS enters the sleep monitoring state.
3. If any rail has a tag that does not match the value configured in the SEQ_ENS_EXP[x] register, then NIRQ asserts. The MPQ79500FS continues sleep monitoring, but the SMCU reacts to the interrupt request and brings the system to a safe state.

Figure 8 on page 37 shows the sleep entry sequence.

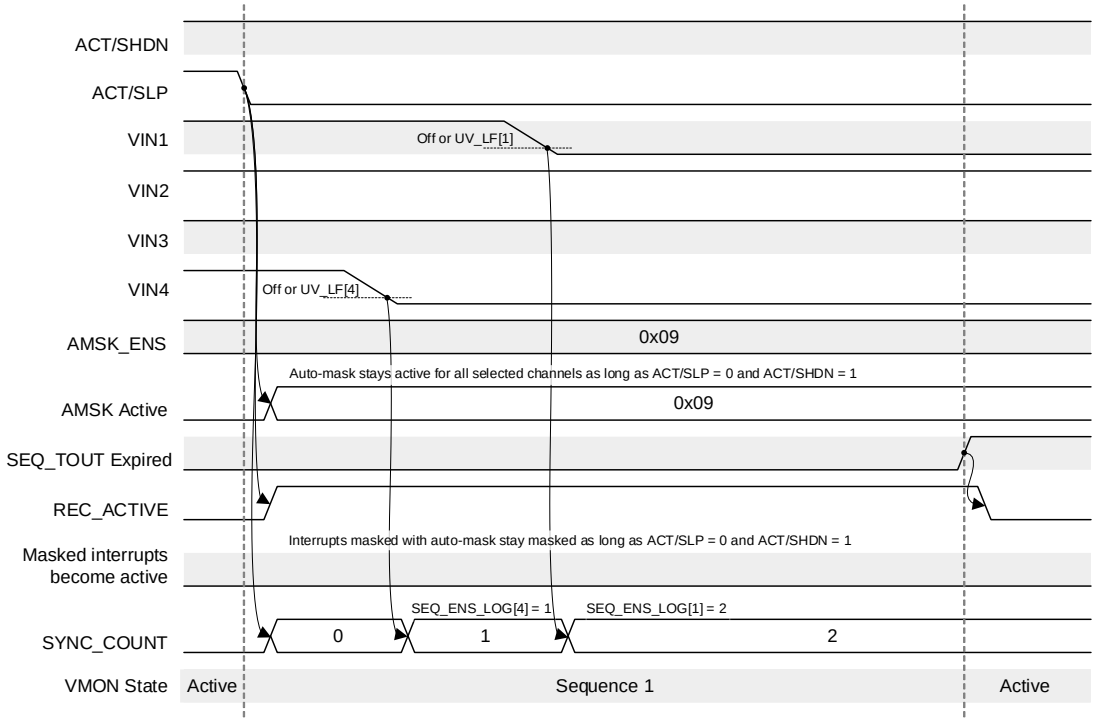


Figure 8: Sleep Entry Sequence Monitoring

Sleep Exit Sequence Monitoring

Sleep exit occurs when the MPQ79500FS transitions from the sleep state to the active state. The following conditions can trigger the device to exit the sleep state:

1. ACT/SLP transitions from 0 to 1 while ACT/SHDN = 1.
2. The host sets REC_START = 1 in the SEQ_REC_CTL register while SEQ[1:0] = = 0x10b.

The turn-on sequence of the sleep channels is monitored while exiting sleep mode. When exiting sleep mode, the following occurs:

1. The synchronization counter in register SEQ_ORD_STAT is reset to 0 for the new power sequence recording.
2. The REC_ACTIVE bit is set to 1 to indicate the start of sequence recording.
3. In the SEQ_REC_STAT register, the SEQ[1:0] bits are set to 10b to indicate the current recording sequence.
4. If the sequence overwrite bit is enabled (EN_SEQ_OW = 1), then the sequence logging registers (SEQ_EXS_LOG[x]) are overwritten by the new sequence. If SEQ_EXS_RDY = 1, then the sequence overwrite flag (SEQ_EXS_OW) is set to 1 to indicate that the sequence has been overwritten. If SEQ_EXS_RDY = 0, then after exiting sleep mode SEQ_EXS_RDY is set to 1 to indicate that data in the register has not yet been read by the host.
5. If the timestamp overwrite bit is enabled (EN_TS_OW = 1), then the timestamp logging registers (SEQ_TIME_xSB[x]) are overwritten by new timestamp. If TS_RDY = 1, then the timestamp overwrite flag (TS_OW) is set to 1 to indicate that the timestamp has been overwritten. If TS_RDY = 0, then after exiting sleep mode the TS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
6. If the sequence overwrite bit is disabled (EN_SEQ_OW = 0) and there is data that has not yet been read by the host (SEQ_EXS_RDY = 1), then data is not written to the registers, and the sequence overwrite flag (SEQ_EXS_OW) is set to 1 to indicate that data cannot be written. If SEQ_EXS_RDY = 0, then after exiting sleep mode SEQ_EXS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.

7. If the timestamp overwrite bit is disabled (EN_TS_OW = 0) and there was data not yet read by the host (TS_RDY = 1), then the data is not written to the registers and the timestamp overwrite flag (TS_OW) is set to 1 to indicate that data cannot be written. If TS_RDY = 0, then after exiting sleep mode TS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
8. The internal sequence timer (re)starts.

As each rail crosses the UVLF or OFF threshold, the rising sequence order and timestamp are tagged. During this process, the following occurs:

1. If enabled via the overwrite settings and statuses, the tag order is stored to the relevant status register (SEQ_EXS_LOG[x]). The timestamp of the event is stored in registers SEQ_TIME_MSB[x] and SEQ_TIME_LSB[x], as determined by the overwrite settings and statuses.
2. The SEQ_EXS_LOG[x] register is compared to the expected sequence order value defined in register SEQ_EXS_EXP[x]. If a mismatch is detected, an interrupt is triggered. This function is active only when the relevant interrupt enable bit (IEN_SEQ_EXS) is set. If the overwrite settings and recording statuses do not allow new data to be written to the logging registers, then the comparison is not performed and an interrupt is not generated.
3. The SEQ_EXS_LOG[x] register is compared to the expected sequence order value, defined in register SEQ_EXS_EXP[x]. If a sequence mismatch is detected, an interrupt is triggered. This function is only active when the relevant interrupt enable bit (IEN_SEQ_EXS) is set. If the overwrite settings and recording statuses do not allow new data to be written to the logging registers, then the comparison is not performed, and an interrupt is not generated.

As each rail reaches the UVLF threshold (UV_LF[x]) or OFF voltage threshold (within 5µs to 10µs), then the relevant UV interrupts are automatically unmasked and enabled/disabled according to the IEN_UVLF and IEN_UVHF registers.

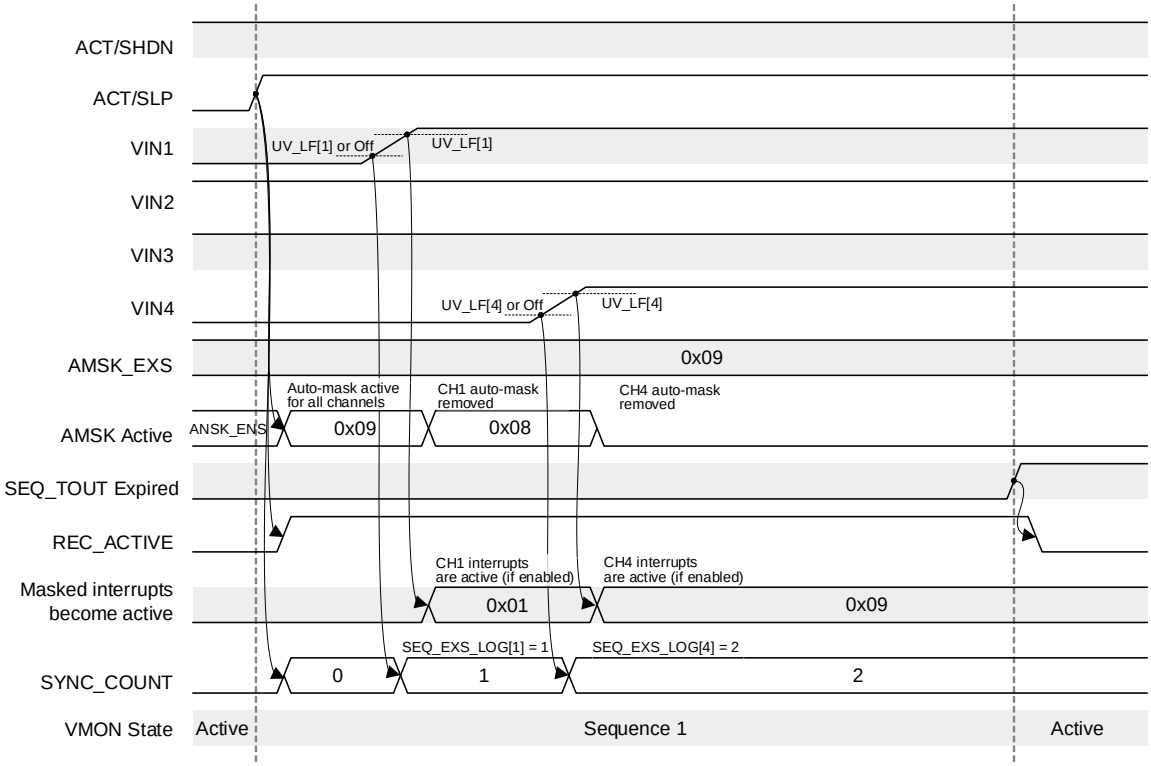


Figure 9: Sleep Exit Sequence Monitoring

After a timeout, tagging stops and the device performs the following actions:

1. The REC_ACTIVE bit is cleared to indicate the end of sequence recording.
2. If the rails are up with the correct sequence, the MPQ79500FS enters an active monitoring state.

If any rail has a tag that does not match the configured value in the SEQ_EXS_EXP[x] register, then NIRQ asserts. The MPQ79500FS continues active monitoring, but the SMCU reacts to the interrupt request and brings the system to a safe state.

Off Sequence Monitoring

As the system shuts down, the MPQ79500FS transmits from an active or sleep state back to the idle state when off sequence monitoring occurs. Unlike the other sequences, the AT_SHDN bit determines whether the device should execute BIST or directly enter the idle state after the timeout expires. The following conditions can trigger off sequence monitoring:

1. ACT/SHDN transitions from 1 to 0.
2. In register SEQ_REC_CTL, the host sets the REC_START bit to 1 and the SEQ bit to 0x01b.

When off sequence monitoring starts, the MPQ79500FS takes several actions:

1. The synchronization counter in register SEQ_ORD_STAT is reset to 0 for the new power sequence recording.
2. The REC_ACTIVE bit is set to 1 to indicate the start of sequence recording.
3. In the SEQ_REC_STAT register, the SEQ[1:0] bits are set to 01b to indicate the current recording sequence.
4. If the sequence overwrite bit is enabled (EN_SEQ_OW = 1), then the sequence logging registers (SEQ_OFF_LOG[x]) are overwritten by the new sequence. If SEQ_OFF_RDY = 1, then the sequence overwrite flag (SEQ_OFF_OW) is set to 1 to indicate that the sequence has been overwritten. If SEQ_OFF_RDY = 0, then after the off sequence SEQ_OFF_RDY is set to 1 to indicate that data in the register has not yet been read by the host.
5. If the timestamp overwrite bit is enabled (EN_TS_OW = 1), then the timestamp logging registers (SEQ_TIME_xSB[x]) are overwritten by the new timestamp. If TS_RDY = 1, then the timestamp overwrite flag (TS_OW) is set to 1 to indicate that the timestamp has been overwritten. If TS_RDY = 0, then after the off sequence TS_RDY is set to 1 to indicate that data in the register has not yet been read by the host.
6. If the sequence overwrite bit is disabled (EN_SEQ_OW = 0) and there was data not yet read by the host (SEQ_OFF_RDY = 1), then data is not written to the registers and the sequence overwrite flag (SEQ_OFF_OW) is set to 1 to indicate that data cannot be written. If SEQ_OFF_RDY = 0, then after the off sequence SEQ_OFF_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
7. If the timestamp overwrite bit is disabled (EN_TS_OW = 0) and there was data not yet read by the host (TS_RDY = 1), then data is not written to the registers and the timestamp overwrite flag (TS_OW) is set to 1 to indicate that data cannot be written. If TS_RDY = 0, then after the off sequence TS_RDY is set to 1 to indicate that there is data in the register that has not yet been read by the host.
8. The internal sequence timer (re)starts.

As each rail crosses the UVLF or OFF threshold, the falling sequence order and timestamp are tagged. This process is described below:

1. If enabled via the overwrite settings and statuses, then the tag order is stored in the relevant status register SEQ_OFF_LOG[x]. The event timestamp is stored in registers SEQ_TIME_MSB[x] and SEQ_TIME_LSB[x], as determined by the overwrite settings and statuses.
2. The SEQ_OFF_LOG[x] register is compared to the expected sequence order value, defined in register SEQ_OFF_EXP[x]. If a sequence mismatch is detected, an interrupt is triggered.

This function is only active when the relevant interrupt enable bit (IEN_SEQ_OFF) is set. If the overwrite settings and recording statues do not allow new data to be written to the logging registers, then the comparison is not performed and an interrupt is not generated.

During this sequence, the interrupts for UVLF and UVHF are disabled on input channels that are set via the AMSK_OFF register. Regardless of whether a channel is auto-masked, the UVLF and UVHF interrupts are disabled once the MPQ79500FS enters the idle state.

After SEQ_TOUT expires, the MPQ79500FS executes the steps listed below:

1. The REC_ACTIVE bit is cleared.
2. The device checks the AT_SHDN bit. If AT_SHDN is disabled, then the device directly enters the idle state (see Figure 10). If AT_SHDN is enabled and AT_POR is not set to 00b, then BIST is executed after SEQ_TOUT expires. Then the device returns to the idle state with a loaded OTP code (see Figure 11).

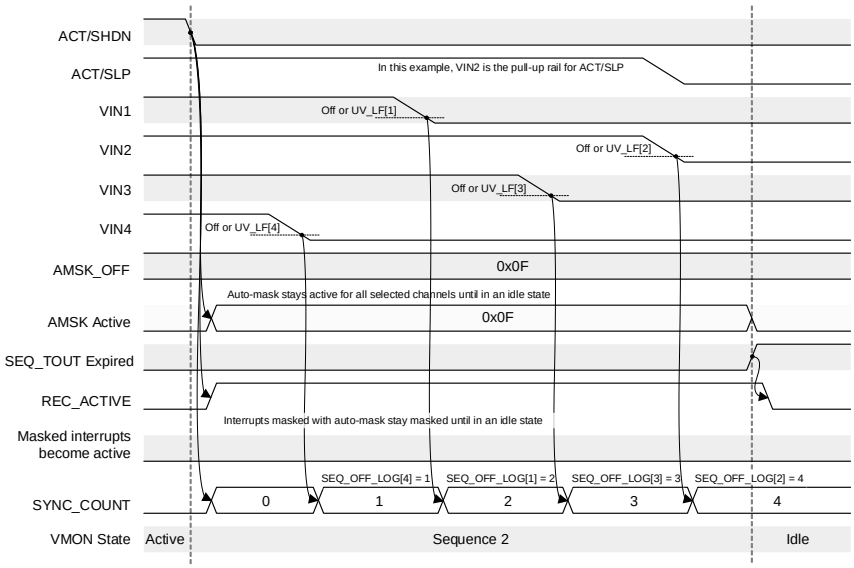


Figure 10: Off Sequence Monitoring (AT_SHDN Disabled)

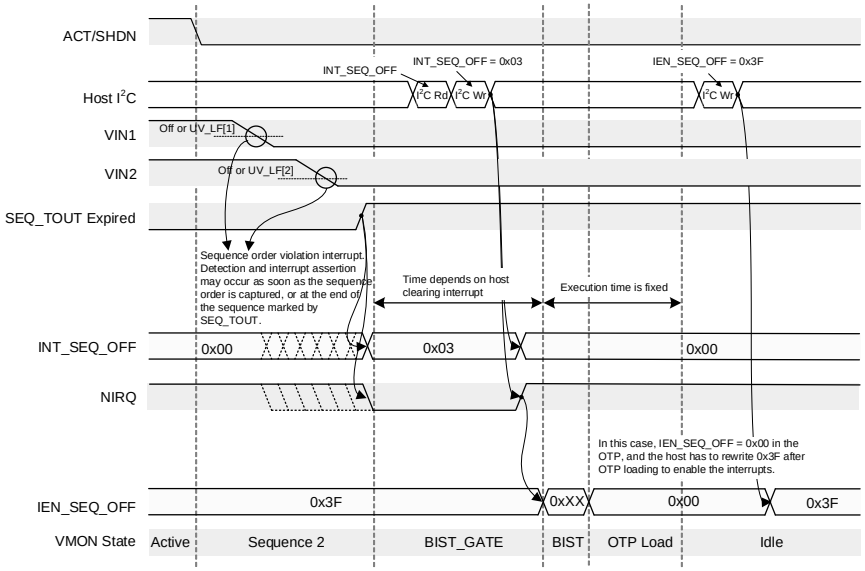


Figure 11: Off Sequence Monitoring (AT_SHDN Enabled)

3. If any rail has a tag that does not match the value in the SEQ_OFF_EXP[x] register (or there is any OV/UV violation, or another fault is reported before SEQ_TOUT expires), then NIRQ asserts. The MPQ79500FS continues to check the AT_SHDN bit, and goes into the BIST gate to block BIST from being executed.

   In the BIST gate, ADC monitoring works as normal. Meanwhile, OVHF and OVLF monitoring re active, but UVHF and UVLF monitoring are inactive, similar to the functionality in the idle state. Toggling the AT/SHDN or ACT/SLP pin cannot exit the BIST gate state. The SMCU is expected to react to the interrupt request and bring the system to a safe state. The I²C is not accessible during BIST, but is accessible via the BIST gate. Once all faults have been cleared by the host, the MPQ79500FS exits BIST gate, runs BIST, reloads the OTP, then enters the idle state (see Figure 11 on page 40).

Interrupt Registers

The interrupt registers show violations related to the voltage rails' threshold, sequence order, memory corruption, and I²C PEC byte, in addition to other interrupts. The interrupt statuses in register INT_SRC consist of four groups of interrupts: INT_MONITOR, INT_CONTROL, INT_TEST, and INT_VENDOR. Any interrupts related to sequence or voltage violations are reported in the INT_MONITOR register. Any interrupts in the INT_SRC register assert the NIRQ pin's signal.

Disabling an interrupt enable bit can prevent a corresponding new fault from being reported. If an interrupt has been reported, then the fault is not cleared automatically by disabling the interrupt enable/disable register, though it can be cleared from W1C via the I²C. Similarly, the temporary interrupt that is disabled via the auto-mask registers during the state transition does not automatically clear the corresponding interrupts in the status register.

Timestamps and Sequence Order

When the input rails cross the UVLF threshold (register UV_LF[x]) or OFF threshold during power on or power off, then the rising or falling sequence and corresponding timestamp are tagged. The triggering threshold is selected via registers SEQ_UP_THLD and SEQ_DN_THLD.

The register groups that tag the rails are listed below:

- SEQ_ON_LOG[x]: Sets the power on sequence order for monitored channels.
- SEQ_OFF_LOG[x]: Sets the power off sequence order for monitored channels.
- SEQ_EXS_LOG[x]: Sets the sleep exit sequence order for monitored channels.
- SEQ_ENS_LOG[x]: Sets the sleep entry sequence order for monitored channels.
- SEQ_TIME_xSB[x]: Sets the timestamp values for monitored channels during the last sequence.

The sequence can be verified by the MPQ79500FS by comparing the actual sequence to the expected sequence (SEQ_xxx_EXP[x] registers). The order can also be read by the host. In addition, timestamp information is recorded for the host to check the sequence. However, the validity of the timestamp is not checked by the MPQ79500FS; this information is only stored for the host.

To prevent falsely triggering a fault due to the rails falling below UVLF or exceeding the noise thresholds for UVHF and OVHF, auto-masks are used during power transitions (ON, ENS, EXS, and OFF sequence transitions) to mask specific channels' interrupts.

During power on scenarios (AMSK_ON and AMSK_EXS), the interrupt enable masks are restored (and auto-mask becomes inactive) when the rail/channel crosses the UVLF threshold (or the sequence timeout expires).

Table 7 on page 42 shows the auto-mask operation for the different ACT/SHDN and ACT/SLP transitions, as well as the transitions by setting the REC_START bits.

If there are rails that are not in the recording sequence that the host would like to turn on, disable the corresponding interrupts of the following registers: IEN_UVHF, IEN_UVLF, IEN_SEQ_ON, IEN_SEQ_OFF, IEN_SEQ_EXS, and IEN_SEQ_ENS.

Table 7: Auto-Mask Summary (11)

Transition	Applied Auto-Mask	Auto-Mask Applies To	Auto-Mask Inactive	Interrupt Active for Channels not in Auto-Mask:
ACT/SHDN = 0 to 1	AMSK_ON	IEN_UVLF, IEN_UVHF	After SEQ_TOUT expires or after the rail crosses UVLF	At ACT/SHDN = 1
ACT/SHDN = 1 to 0	AMSK_OFF	IEN_UVLF, IEN_UVHF	Auto-mask stays active during the transition or until SEQ_TOUT expires (12)	Until SEQ_TOUT expires
ACT/SLP = 0 to 1, ACT/SHDN = 1	AMSK_EXS	IEN_UVLF, IEN_UVHF	After SEQ_TOUT expires or after the rail crosses UVLF	Always active
ACT/SLP = 1 to 0; ACT/SHDN = 1	AMSK_ENS	IEN_UVLF, IEN_UVHF	Auto-mask stays active during the transition or as long as ACT/SLP = 0 and ACT/SHDN = 1	Always active

Notes:

11) The auto-mask result of a transition set by REC_START with I^2C writing is the same as a transition set by the ACT/SHDN or ACT/SLP pin.
12) Once in the idle state (ACT/SHDN = 0 and SEQ_TOUT expires), only the OVLF and OVHF thresholds are monitored in HPM. Although it is not necessary to remove the auto-mask in this case, it is required that AMSK_OFF does not affect any interrupt masking in the idle state. The interrupt masking is handled by the idle state, not by the AMSK_OFF auto-mask.

Recorded Data Handling

Consider when there is sequence/timestamp information stored in the SEQ_xxx_LOG[x] and SEQ_TIME_xSB[x] registers, and this information must be written with new information even if it has not yet been read by the host. For instance, if a sequence mismatch fault is detected and the host has restarted the sequence, then the previous sequence information should be ignored and the register should be overwritten with the new sequence.

The following registers control how the MPQ79500FS handles sequence data recordings:

1. SEQ_REC_STAT: Records sequence recording statuses, including flags (TS_RDY and SEQ_xxx_RDY). It indicates the sequence being recorded and the available data for each recorded data group.
2. SEQ_OW_STAT: This is the sequence recording overwrite status register, including flags (TS_OW and SEQ_xxx_OW). It indicates when a sequence data group has been overwritten, or when new data cannot be written, depending on the overwrite enable configuration from register VMON_MISC.
3. EN_TS_OW: Enables and disables timestamp recording overwrites.
4. EN_SEQ_OW: Enables/disables sequence order recording overwrites.
5. SEQ_REC_CTL: Controls the sequences and includes bits (TS_ACK and SEQ_xxx_ACK) to start recordings, as well as a sequence to indicate the acknowledgment status and allow for overwriting timestamp and/or recorded sequence data.

During sequence monitoring (ON, OFF, ENS, EXS), the MPQ79500FS determines whether the registers should be overwritten by the new timestamp or sequence information, depending on the EN_TS_OW and EN_SEQ_OW bits. The following can occur:

1. If EN_TS_OW and EN_SEQ_OW = 1, then data overwriting is allowed. Once a SEQ_xxx_LOG[x] or SEQ_TIME_xSB[x] register is overwritten with new information, then the TS_OW/SEQ_xxx_OW flag is be set to 1 to indicate that the register has been overwritten. After overwriting, the TS_RDY/SEQ_xxx_RDY flag is set to 1 to indicate that there is new data available for the host. Once this data has been read by the host, TS_RDY/SEQ_xxx_RDY is cleared.

2. If EN_TS_OW and EN_SEQ_OW = 0, then data overwriting is not allowed. Data cannot be written to the SEQ_xxx_LOG[x] and SEQ_TIME_xSB[x] registers unless the TS_OW/SEQ_xxx_OW flag = 0 (data was not overwritten) and the TS_RDY/SEQ_xxx_RDY flag = 0 (there is no new data that has been read by the host, and there is no new data waiting to be read).

   If the host must read data, it can write TS_ACK/SEQ_xxx_ACK to 1 to indicate that the host has acknowledged the timestamp/sequence data. This clears the TS_OW/SEQ_xxx_OW and TS_RDY/SEQ_xxx_RDY flags. If there is new timestamp/sequence data while the TS_RDY/SEQ_xxx_RDY flag = 1 (there is still data in the register that has not yet been read by the host), then TS_OW/SEQ_xxx_OW is set to 1 to indicate that data cannot be written to the register.

When EN_TS_OW and EN_SEQ_OW = 1, the TS_ACK and SEQ_xxx_ACK bits are invalid.

There is a slight difference when the TS_OW and SEQ_xxx_OW bit = 1, and when overwriting is enabled (EN_TS_OW/EN_SEQ_OW = 1) or disabled (EN_TS_OW/EN_SEQ_OW = 0). When EN_TS_OW/EN_SEQ_OW = 1 and TS_OW/SEQ_xxx_OW = 1, the data has been overwritten. When EN_TS_OW/EN_SEQ_OW = 0 and TS_OW/SEQ_xxx_OW = 1, data cannot be written to the register.

Sequence Monitoring with Multiple MPQ79500FS Devices

The MPQ79500FS provides flexibility for applications with more than six voltage rails via the ability to integrate several MPQ79500FS devices. To synchronize the sequence monitoring for supply rails on different devices, the MPQ79500FS features a /SYNC pin. The functions of the /SYNC pin in different scenarios are described below. Figure 12 shows the /SYNC pin's general behavior.

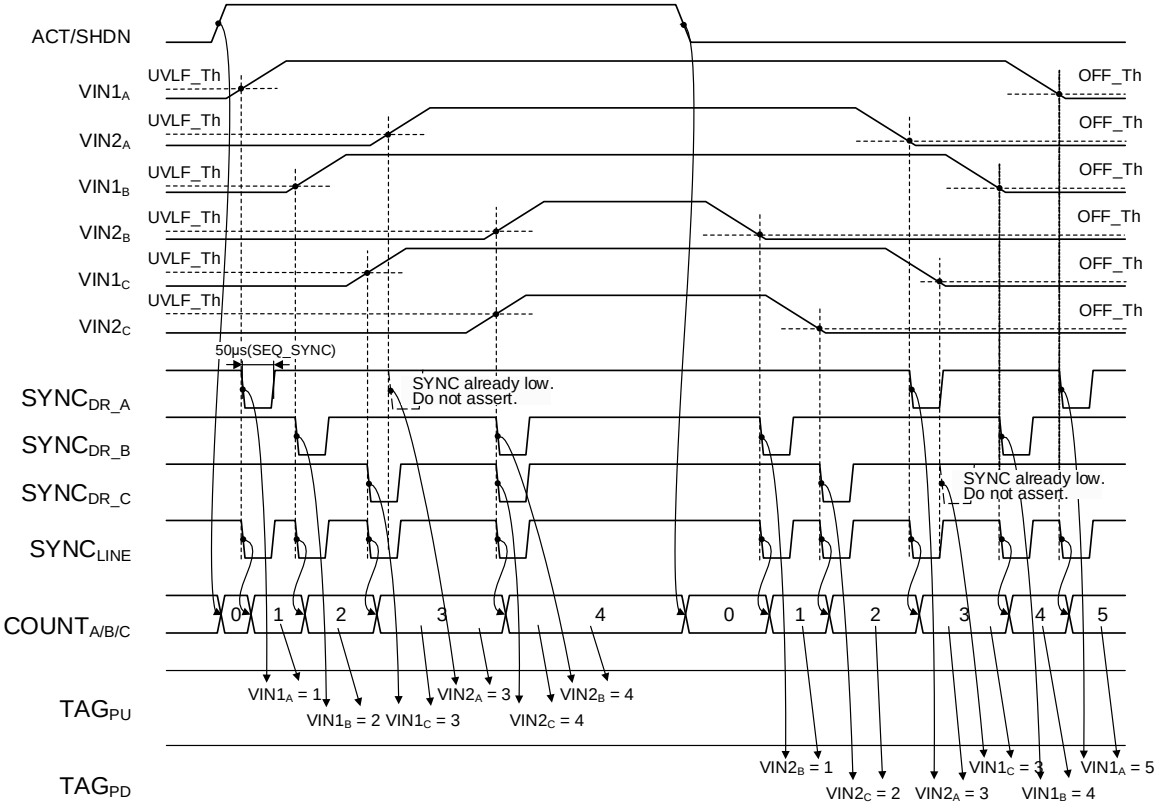


Figure 12: Sequence Monitoring /SYNC Overview with 3 ICs (Transitioning Sequences)

Note the following for the cases and related figures below:

1. Three MPQ79500FS devices (MPQ79500FSA, MPQ79500FSB, and MPQ79500FSC) are depicted.
2. The supply rail being monitored by MPQ79500FSx (where x = A, B, or C) is shown as VIN1/2x.
3. An internal 1MHz clock synchronizes the signals from the external asynchronous domain to the internal synchronous domain. Note that this 1MHz clock only clarifies the time diagram. It does not represent the actual internal clock of the MPQ79500FS.
4. To clarify the function of the /SYNC pin, the clock for different devices are purposely out of phase, with slightly different periods.
5. There are different subscripts for the SYNC signal:
   a. $SYNC_{DR\_X}$ indicates which MPQ79500FSx is driving the SYNC signal.
   b. The SYNC line indicates what an external probe would see on the SYNC line. The subscript denotes which device is being used.
   c. $SYNC_{X\_INTERNAL}$ indicates the SYNC signal in the synchronized internal domain of the MPQ79500FSx. When the MPQ79500FSx is driving SYNC, $SYNC_{DR\_X}$ and $SYNC_{X\_INTERNAL}$ are the same signal, since they are generated by the internal synchronous domain.
6. COUNTx indicates the MPQ79500FSx's internal counter for SYNC high-to-low transitions. The value of this signal should be the same on all MPQ79500FS devices.
7. TAGx_PU/PD is a register assignment. A channel monitored by the MPQ79500FSx is tagged with the counter value when the UVLF or OFF threshold is crossed during a power up/down transition.
8. RespmpTmrX is the timer that sets the safety re-sampling for the SYNC signal if the /SYNC falling edge fails to be detected (see the Case 4: Two Adjacent SYNC Pulses section on page 48 for more details).

For simplification, the sequence tagging thresholds (SEQ_UP_THLD and SEQ_DN_THLD) in the following examples are set to use the UVLF threshold for power on and exiting sleep mode. The OFF threshold is for power off and entering sleep mode.

Case 1: Typical Behavior

In case 1, the SYNC pulses are apart from each other, which is considered typical behavior. Figure 13 on page 45 shows typical behavior for sequence synchronization. Figure 14 on page 45 shows the detailed typical behavior.

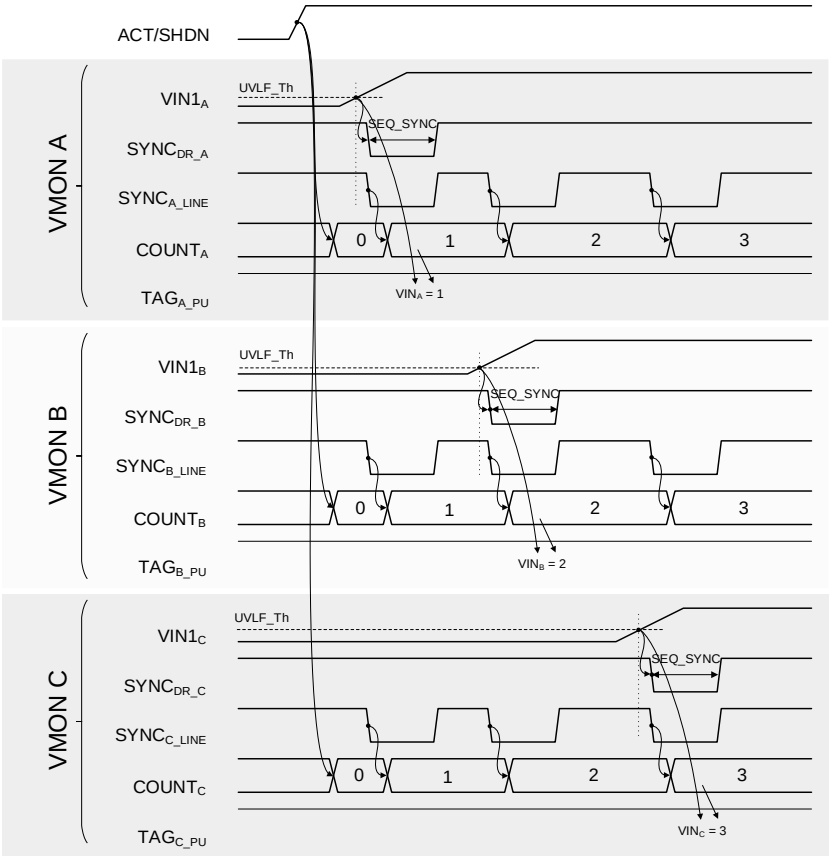


Figure 13: Sequence Synchronization (Typical Behavior)

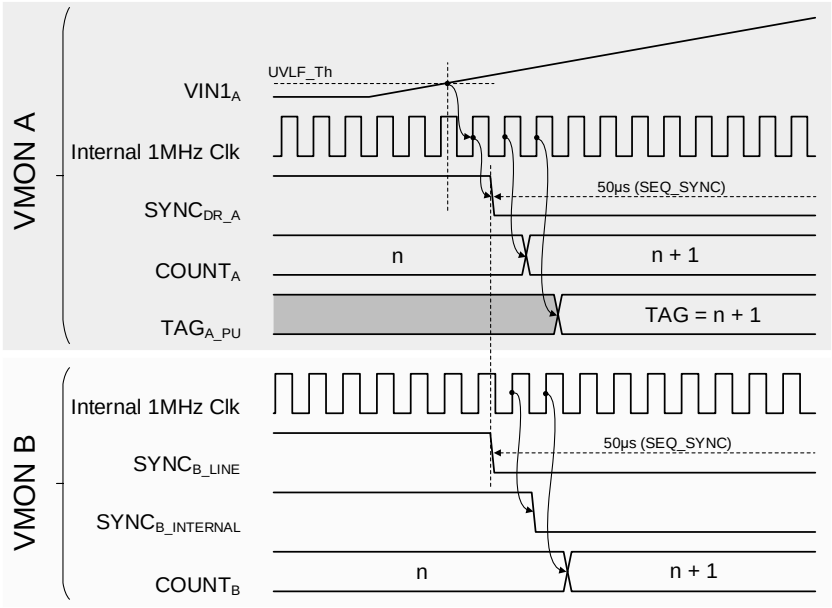


Figure 14: Sequence Synchronization (Typical Behavior Details)

Case 2: Rail Crossing during SYNC

In case 2, one rail crosses the UVLF threshold while a SYNC pulse is already active (due to another rail crossing the UVLF slightly earlier). Figure 15 on page 46 shows rail crossing during the SYNC pulse. Figure 16 on page 46 shows a detailed SYNC pulse.

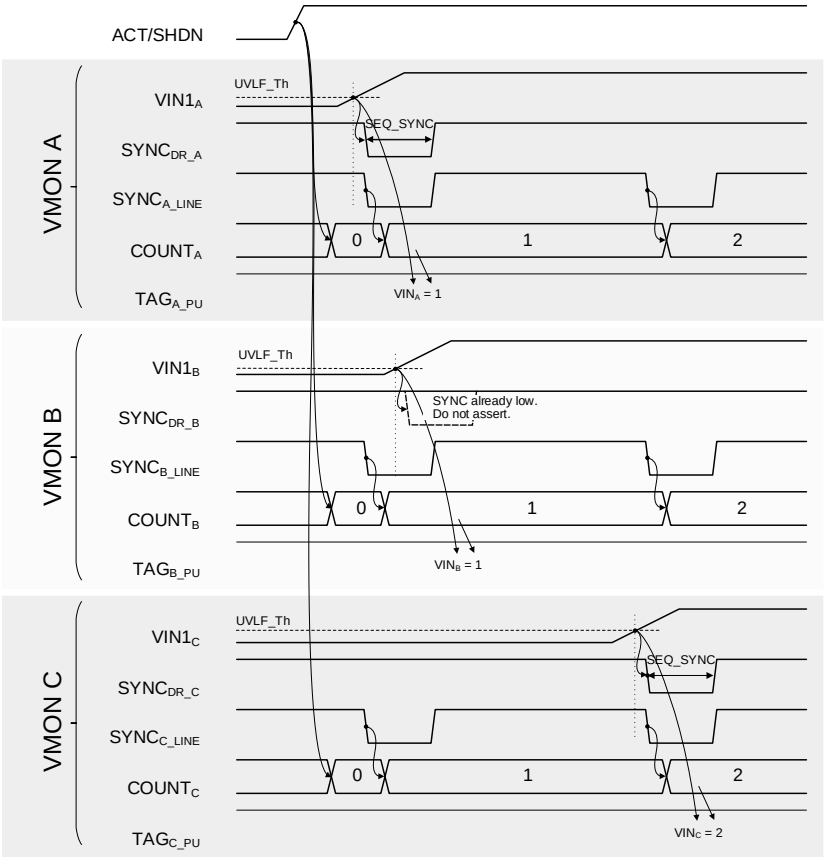


Figure 15: Sequence Synchronization (Rail Crossing During SYNC Pulse)

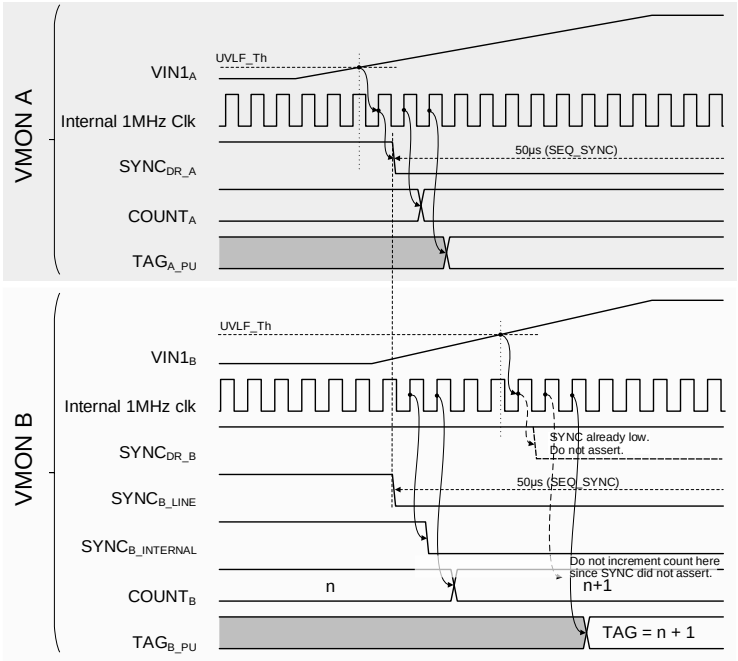


Figure 16: Sequence Synchronization (Detailed: Rail Crossing During SYNC Pulse)

Case 3: Simultaneous Rails

In case 3, two rails (monitored by two separate MPQ79500FS devices) cross the UVLF thresholds almost simultaneously during sequence synchronization.

Figure 17 shows sequence synchronization when two rails reach their UVLF thresholds almost simultaneously. Figure 18 shows a detailed process when two rails reach their UVLF threshold almost simultaneously.

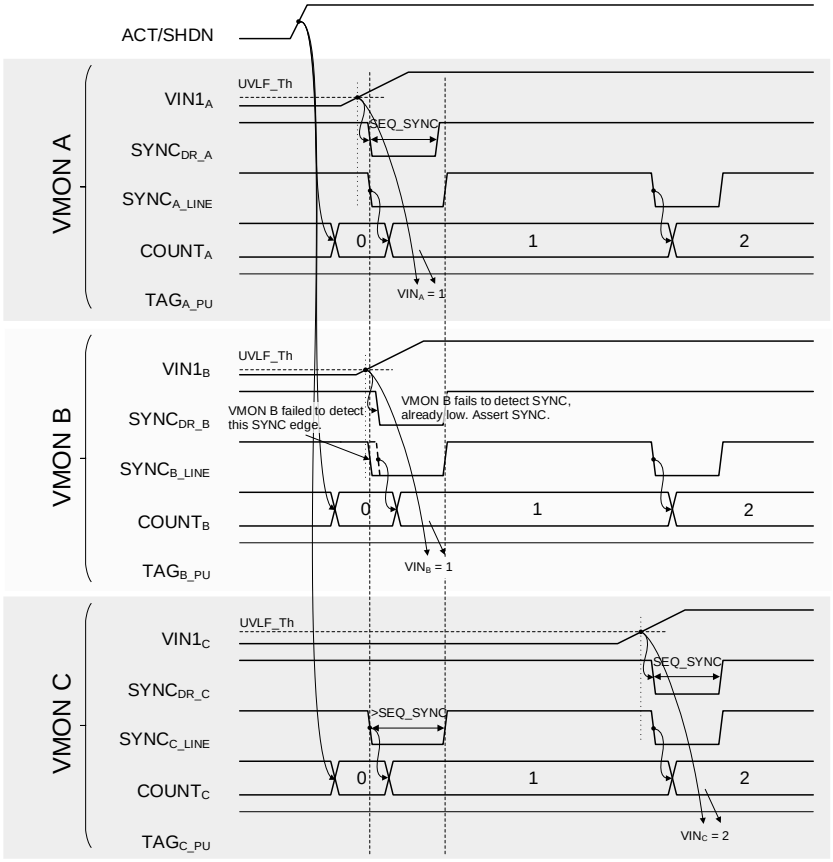


Figure 17: Sequence Synchronization (Two Rails Up Almost Simultaneously)

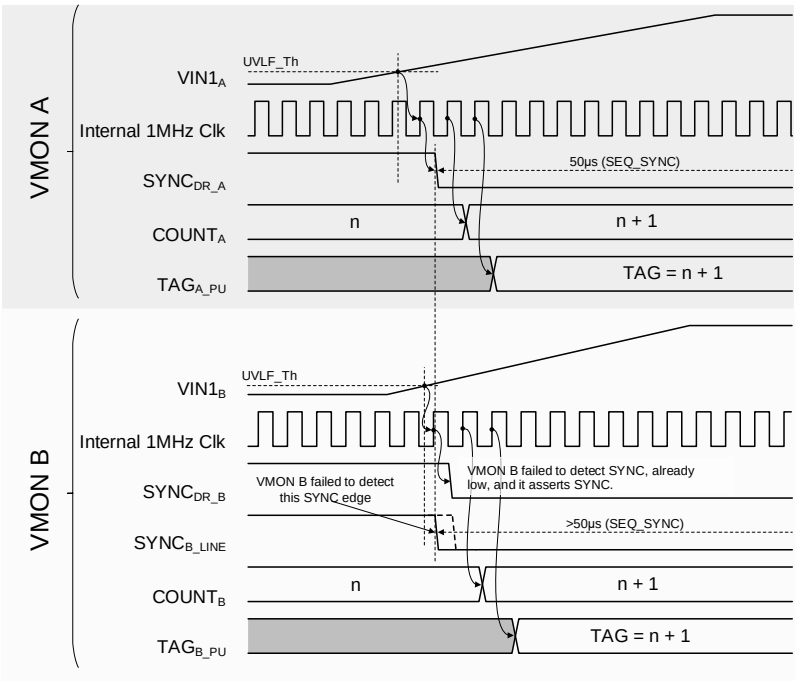


Figure 18: Sequence Synchronization (Details: Two Rails Up Almost Simultaneously)

First, /SYNC drops when the rail of one channel reaches the UVLF threshold. Then another channel should pull down the SYNC line within the time set by PULSE_WIDTH so that the channels share the same SYNC pulse.

Note that during sequence transitions, there is a time from when a rail goes up to when SYNC is pulled low, which varies depending the V_{IN} level, V_{IN} slope, UVLF threshold (or OFF voltage threshold), temperature, clock accuracy, and ADC sampling rate. Even if two rails go up simultaneously, they may not be in the same SYNC pulse, if PULSE_WIDTH is set too short. Adjust PULSE_WIDTH to be long enough for the relevant application conditions.

Case 4: Two Adjacent SYNC Pulses

If two rails are monitored by two separate MPQ79500FS devices and they cross the UVLF threshold within two close SYNC pulses, then the third MPQ79500FS may fail to detect the SYNC low-high-low transition in between. Figure 19 shows when VMON fails to detect consecutive SYNC pulses. Figure 20 on page 49 shows a detailed look at this process.

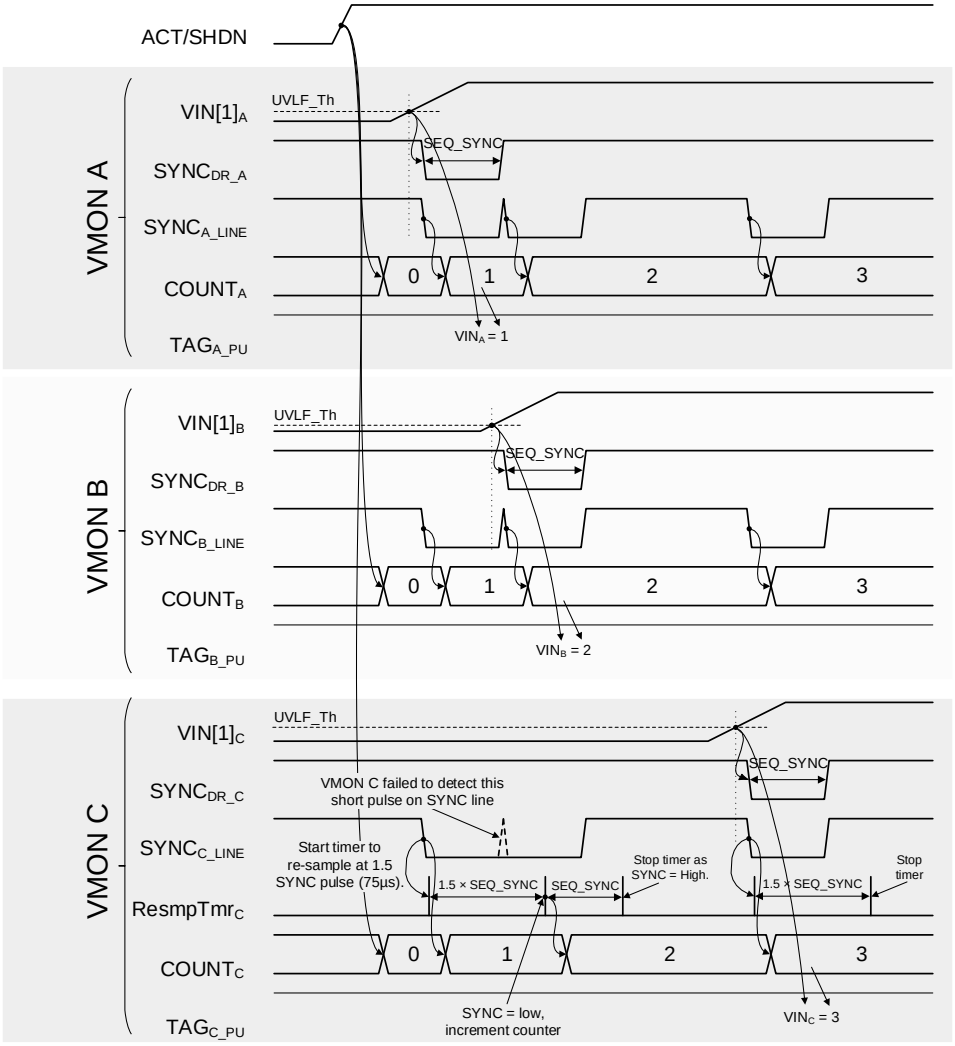


Figure 19: Sequence Synchronization (VMON Fails to Detect Consecutive SYNC Pulses)

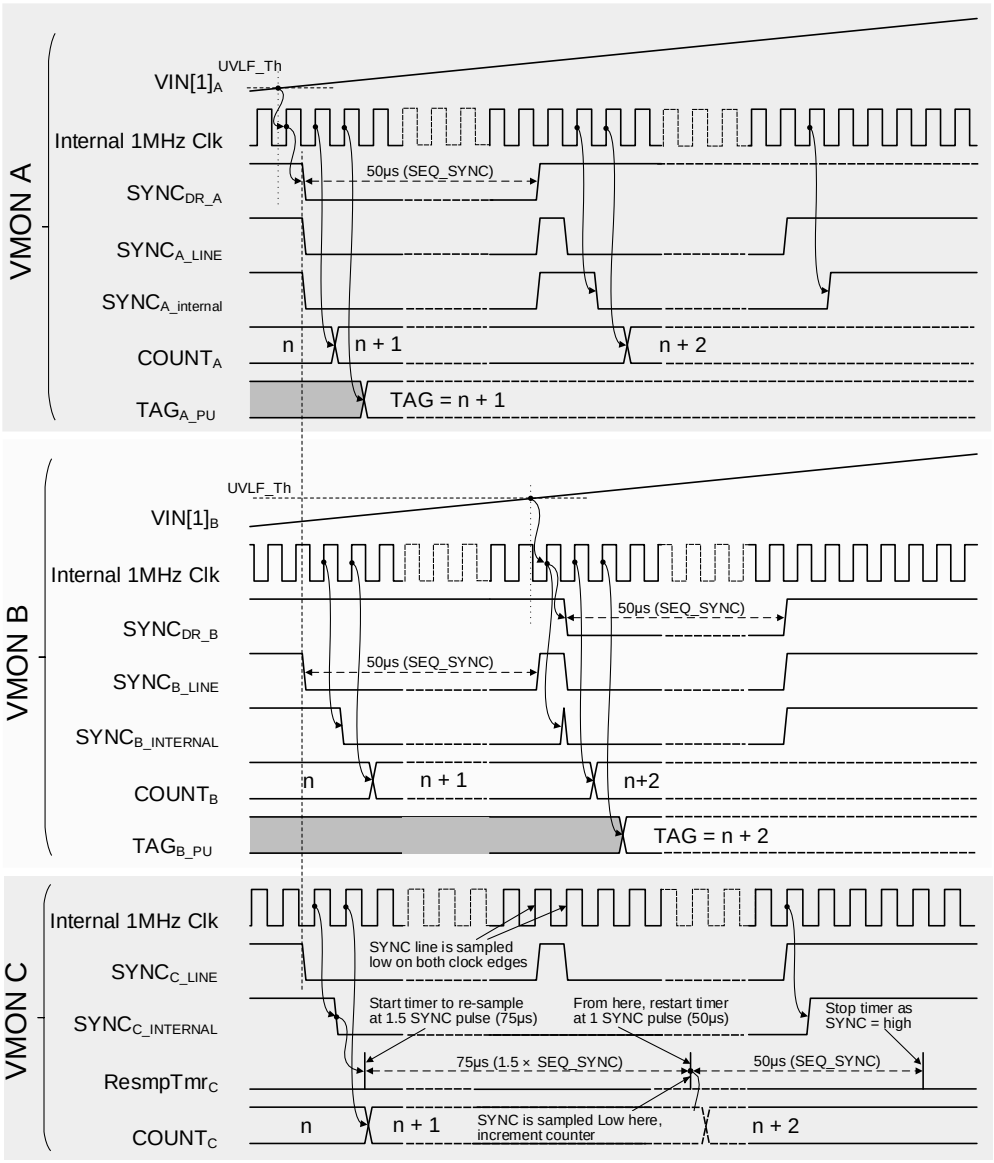


Figure 20: Sequence Synchronization (Details: VMON Fails to Detect Consecutive SYNC Pulses)

I²C INTERFACE

I²C Serial Interface Description

The I²C bus is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. When connected to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MPQ79500FS works as a slave-only device, which supports up to 1Mbs of bidirectional data transfer in fast-mode plus, adding flexibility to the sequencer. Device parameters can be instantaneously controlled via the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on SDA must be stable during the clock's high period. The SDA line's high or low state only changes when the clock signal on the SCL line is low see Figure 21).

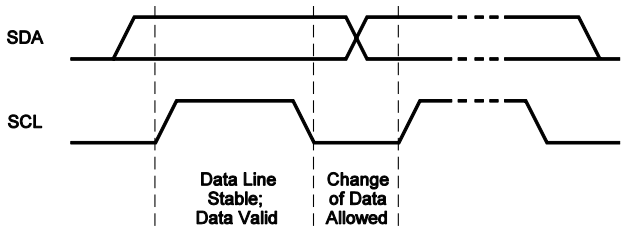


Figure 21: Bit Transfer on the I²C Bus

Start and Stop Commands

Start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while SCL is high. A stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 22).

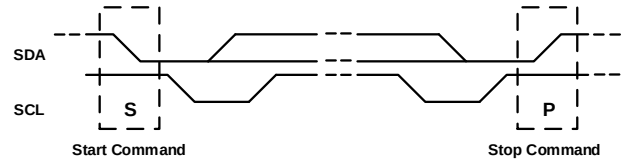


Figure 22: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after a start command. The bus is considered free again after a delay following a stop command.

The bus stays busy if a repeated start (Sr) command is generated instead of a stop command. Start and repeated start commands are functionally identical.

Transfer Data

Every byte put on SDA must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable (low) during the high period of the clock pulse.

Figure 23 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit. The data direction bit determines whether the transmission is a read (R) or write (W). A 0 indicates a write transmission, and a 1 indicates a read (a request for data). A data transfer is always terminated by a stop command generated by the master. However, if the master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

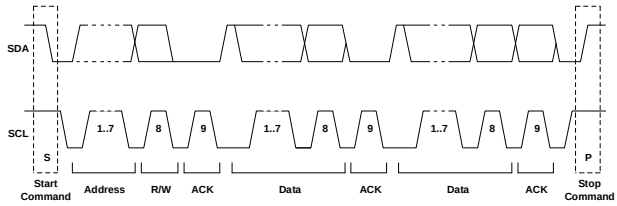


Figure 23: Complete Data Transfer

Write Sequence

The MPQ79500FS I²C supports single and sequential byte writing. If enabled by EN_PEC, single-byte writes have an appended packet error checking (PEC) byte. PEC is not supported on a sequential write.

Figure 24 and Figure 25 on page 51 show the write sequences. The typical MPQ79700FS single-byte write sequence requires a start command from the master, a valid slave address, a register index byte, and a corresponding data byte for a single data update.

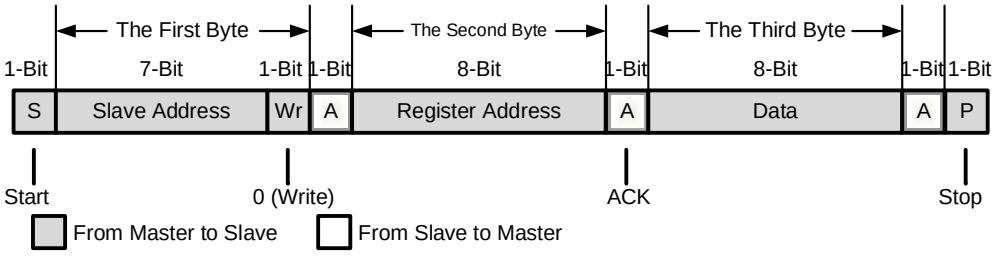


Figure 24: Write Sequence (Single Byte)

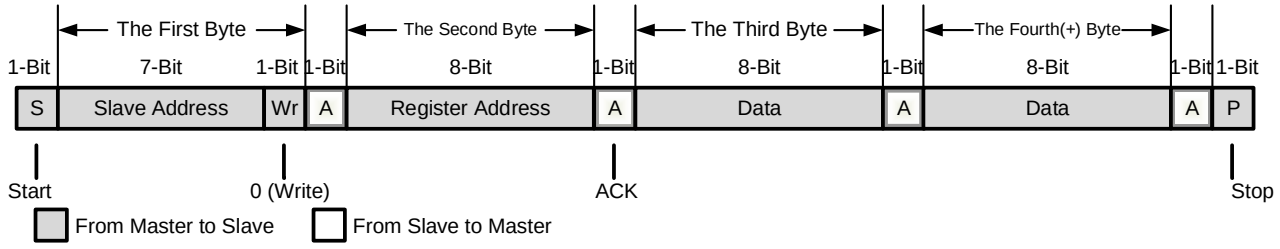


Figure 25: Write Sequence (Sequential Bytes)

After receiving each byte, the MPQ79500FS acknowledges by pulling SDA low during the high period of a single clock pulse. A valid I²C address selects the MPQ79500FS. The MPQ79500FS then performs an update on the falling edge of the LSB byte.

Read Sequence

The MPQ79500FS I²C supports both single and sequential byte reading. If enabled by EN_PEC, 1-byte reads can be appended with a PEC byte. PEC is not supported on a sequential read.

Figure 26 and Figure 27 show the write sequence. The typical MPQ79500FS 1-byte read sequence is 4 bytes long. It begins with a start command from the master, followed by a valid slave address and a register index byte. Unlike with a write sequence, a start command from the master comes again. The bus direction then turns around with the rebroadcast of the slave address, with bit 1 indicating a read cycle. The following 4th byte contains the data being returned by the MPQ79500FS. That byte value in the data byte reflects the value of the register index being queried before.

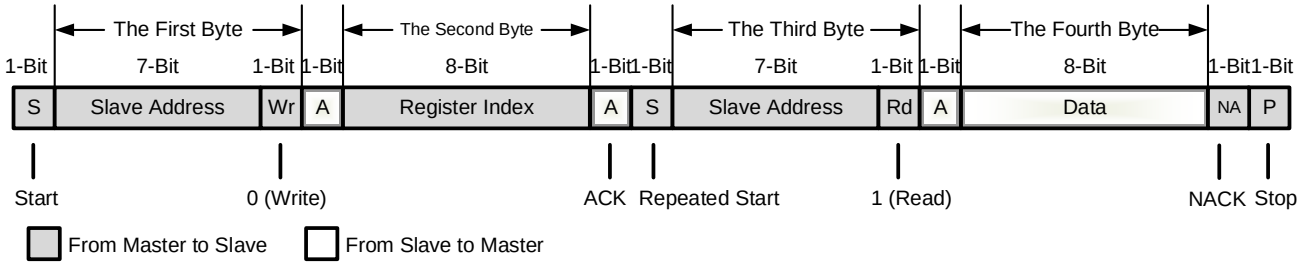


Figure 25: Read Sequence (Single Byte)

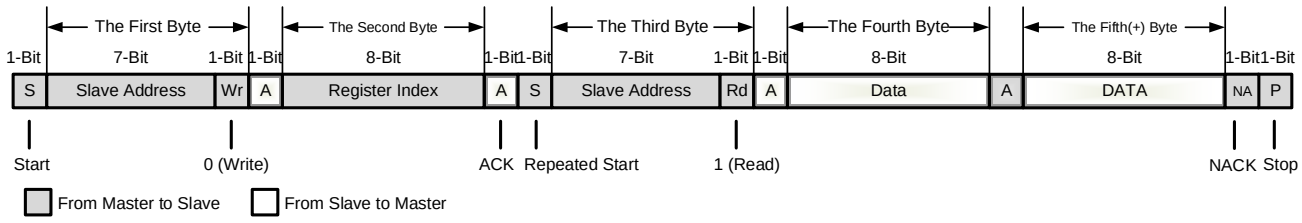


Figure 26: Read Sequence (Sequential Bytes)

Chip Address

The MPQ79500FS supports 127 different addresses (00h~7Fh), which can be preset to register 0xF9 via the I²C bus.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by an 8th data direction bit with a 0 or 1 to indicate a write or read operation, respectively.

Packet Error Checking (PEC)

The MPQ79500FS supports packet error checking (PEC) following the SMBus implementation.

The PEC calculation includes all bytes in the transmission, such as the address, command, and data. The PEC calculation does not include ACK or not acknowledge (NACK) bits, or start, stop, or repeated start commands. This means that the PEC is computed across the entire message from the first start command.

The SMBus must accommodate any combination of devices that support PEC and devices that do not. For this reason, a device that acts as a slave and supports PEC must always be prepared to perform the slave transfer with or without the PEC byte, verify the correctness of the PEC byte if present, and only process the message if the PEC byte is correct.

The I²C master can implement an optional exception for transfers without PEC when PEC is enabled. Such exceptions are controlled by the REQ_PEC bit.

If PEC is enabled by EN_PEC and the PEC byte is present in the write transaction, then the master must NACK and assert NIRQ if the PEC byte is incorrect.

If PEC is enabled by EN_PEC and the PEC byte is not present in the write transaction, then:

- If REQ_PEC = 0, the device behaves as described by the SMBus specifications and NIRQ does not assert.
- If REQ_PEC = 1, the device treats the missing PEC as an incorrect PEC byte and NIRQ asserts.

Figure 27 and Figure 28 show the write and read operations with EN_PEC enabled. For PEC calculations (from the start to stop commands), assume that these transactions are complete as depicted and are not followed by a repeated start command.

Note that when PEC is enabled, the register address auto-increment is disabled. This removes the sequential writes and reads.

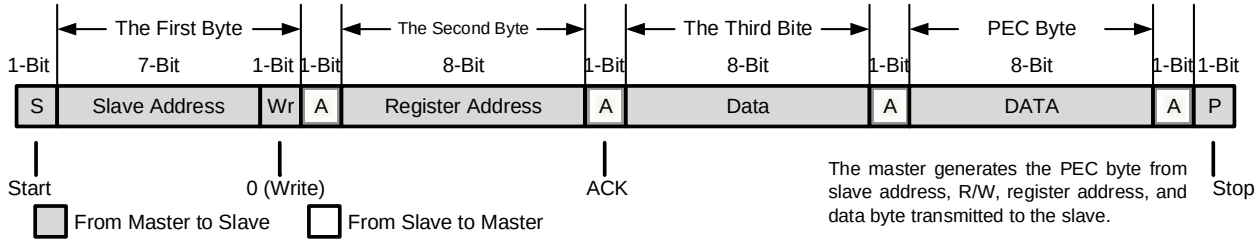


Figure 27: Write Sequence with PEC

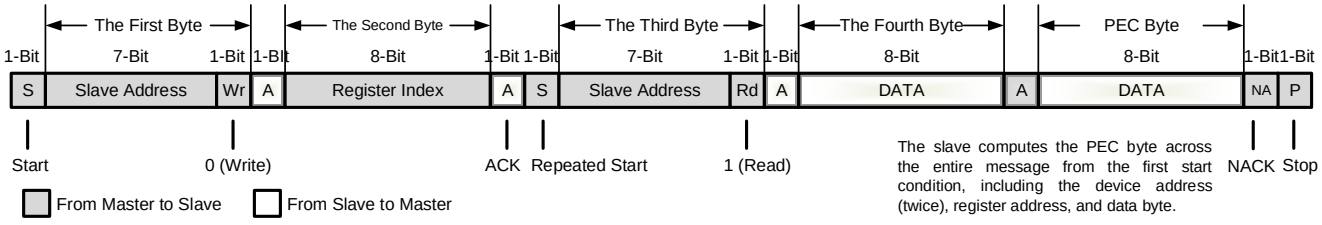


Figure 28: Read Sequence with PEC

Table 8 on page 53 shows the transactional I²C behavior.

Table 8: I²C Transaction Behavior

#	I²C Transaction	Expected Behavior
1	Single-byte write to a valid register with valid data.	Normal condition. Acknowledge the register address byte and data byte. Write byte to register.
2	Single-byte write to an invalid register.	Acknowledge the register address byte and data byte. Ignore the data byte.
3	Single-byte write to protect a register (as per PROT1/2).	Acknowledge the register address byte and data byte. Ignore the data byte.
4	Single-byte write to a valid register with invalid data.	Acknowledge the register address byte and data byte. Ignore the data byte.
5	Single-byte write to a valid register with valid data, but an invalid PEC byte.	Acknowledge the register address byte and data byte. Do not acknowledge the PEC byte + interrupt. Ignore the data byte.
6	Single-byte read from a valid register.	Normal condition. Acknowledge the register address byte. Data is returned.
7	Single-byte read from an invalid register.	Acknowledge the register address byte. 0x00 data is returned.
8	Single-byte read from a protected register (as per PROT1/2).	Normal condition. Acknowledge the register address byte. Data is returned.
9	Single-byte read from a valid register with an invalid PEC byte.	The master must handle an invalid PEC byte for reads.
10	Multi-byte write starting at a valid address and ending at a valid address.	Normal condition. Acknowledge the register address byte and data bytes. Write bytes to registers.
11	Multi-byte write starting at valid address and crossing into an invalid or protected address.	Acknowledge the register address byte and data bytes. Write bytes to valid registers. Ignore data bytes for invalid or protected registers.
12	Multi-byte write starting at a valid address, crossing into an invalid or protected address, then back to valid address.	Acknowledge the register address byte and data bytes. Write bytes to valid registers. Ignore data bytes for invalid or protected registers.
13	Multi-byte read starting at a valid address and ending at a valid address.	Normal condition. Acknowledge the register address byte. Data is returned.
14	Multi-byte read starting at a valid address and crossing into an invalid register.	Acknowledge the register address byte. Data is returned for valid addresses. 0x00 is returned for invalid addresses.
15	Multi-byte read starting at a valid address, crossing into an invalid register, then back to a valid address.	Acknowledge the register address byte. Data is returned for valid addresses. 0x00 is returned for invalid addresses.

REGISTER MAP

Table 9: Back Independent – Common Register Set Summary

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (10)	Group
0x00~0x0F: Device Information												
0x00	VENDOR_ID	R	VENDOR_ID								0x19	
0x01	MODEL_REV	R	MODEL_REV								0x40	
0xF0~0xF7: Bank and Protection Registers												
0xF0	BANK_SEL	R/W	RSVD							BANK	0x00	
0xF1	PROT1	R/W	RSVD	WRKC	WRKS	CFG	IEN	MON		SEQ	0x00	
0xF2	PROT2	R/W	RSVD	WRKC	WRKS	CFG	IEN	MON		SEQ	0x00	
0xF3	PROT_MON1	R/W	RSVD	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]		MON[1]	0x3F	
0xF8~0xFF: Device Configuration Registers												
0xF9	I2CADDR	R	RSVD	ADDR_NVM[3:0]			ADDR_STRAP[2:0]					
0xFA	DEV_CFG	R	RSVD						SOC_IF		0x00	

Table 10: Bank 0 – Status Register Set Summary

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Group
Bank 0: 0x10~0x2F – Interrupt Information Registers												
0x10	INT_SRC	R	VENDOR	RSVD	TEST	CONTROL	MONITOR					
0x11	INT_MONITOR	R	SEQ_ON	SEQ_OFF	SEQ_EXS	SEQ_ENS	OV_LF	OV_ HF	UV_LF	UV_HF		
0x12	INT_UVHF	RW1C	RSVD	RSVD	UVHF[6]	UVHF[5]	UVHF[4]	UVHF [3]	UVHF[2]	UVHF[1]		
0x14	INT_UVLF	RW1C	RSVD	RSVD	UVLF[6]	UVLF[5]	UVLF[4]	UVLF [3]	UVLF[2]	UVLF[1]		
0x16	INT_OVHF	RW1C	RSVD	RSVD	OVHF[6]	OVHF[5]	OVHF[4]	OVHF [3]	OVHF [2]	OVHF [1]		
0x18	INT_OVLF	RW1C	RSVD	RSVD	OVLF[6]	OVLF[5]	OVLF[4]	OVLF [3]	OVLF[2]	OVLF[1]		
0x1A	INT_SEQ_ON	RW1C	RSVD	RSVD	SEQ_ON[6]	SEQ_ON[5]	SEQ_ON[4]	SEQ_ON [3]	SEQ_ON[2]	SEQ_ON[1]		
0x1C	INT_SEQ_OFF	RW1C	RSVD	RSVD	SEQ_OFF[6]	SEQ_OFF[5]	SEQ_OFF[4]	SEQ_OFF[3]	SEQ_OFF[2]	SEQ_O FF[1]		
0x1E	INT_SEQ_EXS	RW1C	RSVD	RSVD	SEQ_EXS[6]	SEQ_EXS[5]	SEQ_EXS[4]	SEQ_EXS[3]	SEQ_EXS[2]	SEQ_EXS[1]		
0x20	INT_SEQ_ENS	RW1C	RSVD	RSVD	SEQ_ENS[6]	SEQ_ENS[5]	SEQ_ENS[4]	SEQ_ENS [3]	SEQ_ENS[2]	SEQ_ENS[1]		
0x22	NT_CONTROL	RW1C	RSVD	RT_CRC	NIRQ	TSD	SYNC	PEC				
0x23	INT_TEST	RW1C	RSVD	ECC_SEC	ECC_DED	I_BIST_C	BIST					
0x24	INT_VENDOR	RW1C	I2C_WR_CHK	RSVD	CLK_FAIL	RSVD	TMR_FAIL	ADC_FAIL	I2C_CONWR_CHK	STATE_FAIL		
Bank 0: 0x30-0x3F – Status Registers (Top Level)												
0x30	VMON_STAT	R	RSVD	ST_BIST_C	RSVD	ST_ACTSLP	ST_ACTSHDN	ST_SYNC	RSVD			

0x31	TEST_ INFO	R	RSVD	ECC_ SEC	ECC_ DED	BIST_VM	BIST_ NVM	BIST_ L	BIST_A			
0x32	OFF_ STAT	R	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]		
0x34	SEQ_REC _STAT	R	REC_ ACTIVE	SEQ [1:0]	TS_RDY	SEQ_ON _RDY	SEQ_ OFF_ RDY	SEQ_ EXS_ RDY	SEQ_ ENS_ RDY			
0x35	SEQ_ OW_STAT	R	RSVD	TS_ OW	SEQ_ ON_OW	SEQ_ OFF_OW	SEQ_ EXS_OW	SEQ_ ENS_ OW				
0x36	SEQ_ ORD_ STAT	R	SYNC_ COUNT [7:0]									
Bank 0: 0x40~0x4F – Status Registers (Channel Voltage-Level Information Registers)												
0x40	VIN_LVL[1]	R	ADC[7:0]									
0x41	VIN_LVL[2]	R	ADC[7:0]									
0x42	VIN_LVL[3]	R	ADC[7:0]									
0x43	VIN_LVL[4]	R	ADC[7:0]									
0x44	VIN_LVL[5]	R	ADC[7:0]									
0x45	VIN_LVL[6]	R	ADC[7:0]									
Bank 0: 0x50~0x5F – Status Registers (Power On (ACT/SHDN = 0 to 1) Sequence Information Registers)												
0x50	SEQ_ON_ LOG[1]	R	ORDER[7:0]									
0x51	SEQ_ON_ LOG[2]	R	ORDER[7:0]									
0x52	SEQ_ON_ LOG[3]	R	ORDER[7:0]									
0x53	SEQ_ON_ LOG[4]	R	ORDER[7:0]									
0x54	SEQ_ON_ LOG[5]	R	ORDER[7:0]									
0x55	SEQ_ON_ LOG[6]	R	ORDER[7:0]									
Bank 0: 0x60~0x6F – Status Registers (Power Off (ACT/SHDN = 1 to 0) Sequence Information Registers)												
0x60	SEQ_OFF _LOG[1]	R	ORDER[7:0]									
0x61	SEQ_OFF _LOG[2]	R	ORDER[7:0]									
0x62	SEQ_OFF _LOG[3]	R	ORDER[7:0]									
0x63	SEQ_OFF _LOG[4]	R	ORDER[7:0]									
0x64	SEQ_OFF _LOG[5]	R	ORDER[7:0]									
0x65	SEQ_OFF _LOG[6]	R	ORDER[7:0]									
Bank 0: 0x70~0x7F – Status Registers (Sleep Exit (ACT/SLP = 0 to 1) Sequence Information Registers)												
0x70	SEQ_EXS _LOG[1]	R	ORDER[7:0]									
0x71	SEQ_EXS _LOG[2]	R	ORDER[7:0]									
0x72	SEQ_EXS _LOG[3]	R	ORDER[7:0]									
0x73	SEQ_EXS _LOG[4]	R	ORDER[7:0]									
0x74	SEQ_EXS _LOG[5]	R	ORDER[7:0]									
0x75	SEQ_EXS _LOG[6]	R	ORDER[7:0]									

Bank 0: 0x80~0x8F – Status Registers (Sleep Entry (ACT/SLP = 1 to 0) Sequence Information Registers)					
0x80	SEQ_ENS_LOG[1]	R	ORDER[7:0]		
0x81	SEQ_ENS_LOG[2]	R	ORDER[7:0]		
0x82	SEQ_ENS_LOG[3]	R	ORDER[7:0]		
0x83	SEQ_ENS_LOG[4]	R	ORDER[7:0]		
0x84	SEQ_ENS_LOG[5]	R	ORDER[7:0]		
0x85	SEQ_ENS_LOG[6]	R	ORDER[7:0]		
Bank 0: 0x90~0xAF – Status Registers (Sequence (Any) Timing Information Registers)					
0x90	SEQ_TIME_MSB[1]	R	CLOCK[7:0]		
0x91	SEQ_TIME_LSB[1]	R	CLOCK[7:0]		
0x92	SEQ_TIME_MSB[2]	R	CLOCK[7:0]		
0x93	SEQ_TIME_LSB[2]	R	CLOCK[7:0]		
0x94	SEQ_TIME_MSB[3]	R	CLOCK[7:0]		
0x95	SEQ_TIME_LSB[3]	R	CLOCK[7:0]		
0x96	SEQ_TIME_MSB[4]	R	CLOCK[7:0]		
0x97	SEQ_TIME_LSB[4]	R	CLOCK[7:0]		
0x98	SEQ_TIME_MSB[5]	R	CLOCK[7:0]		
0x99	SEQ_TIME_LSB[5]	R	CLOCK[7:0]		
0x9A	SEQ_TIME_MSB[6]	R	CLOCK[7:0]		
0x9B	SEQ_TIME_MSB[6]	R	CLOCK[7:0]		

Table 11: Bank 1 – Channels 1–6 Configuration Register Set Summary

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (10)	Group
Bank 1: 0x10~0x1F – Control Registers												
0x10	VMON_CTL	R/W	RSVD		SLEEP_PWR	RSVD	RESET	SYNC_RST	FORCE_SYNC	FORCE_NIRQ	0x20	WRKC
0x11	VMON_MISC	R/W	RSVD				EN_TS_OW	EN_SEQ_OW	REQ_PEC	EN_PEC	0x0F	CFG
0x12	TEST_CFG	RW	RSVD					AT_SHDN	AT_POR[1:0]		0x03	CFG
0x13	IEN_UVHF	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	IEN
0x14	IEN_UVLF	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	IEN
0x15	IEN_OVHF	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	IEN
0x16	IEN_OVLF	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	IEN
0x17	IEN_SEQ_ON	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	IEN
0x18	IEN_SEQ_OFF	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	IEN
0x19	IEN_SEQ_EXS	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	IEN

0x1A	IEN_SEQ_ENS	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	IEN
0x1B	IEN_CONTROL	R/W	RSVD			RT_CRC	RSVD	TSD	SYNC	PEC	0x00	IEN
0x1C	IEN_TEST	R/W	RSVD				ECC_SEC	RSVD	I_BIST_C	BIST	0x01	IEN
0x1D	IEN_VENDOR	R/W	I2C_WR_CHK_INT_EN	RSVD	RSVD	RSVD	TMR_FAIL_INT_EN	ADC_FAIL_INT_EN	I2C_CONWR_CHK_EN	STATE_FAIL_INT_EN	0x00	IEN
0x1E	VIN_CH_EN	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x3F	CFG
0x1F	VRANGE_MULT	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x00	CFG
Bank 1: 0x20~0x2F – Monitor Registers (CH1)												
0x20	UV_HF[1]	R/W	THRESHOLD[7:0]								0x00	MON[1]
0x21	OV_HF[1]	R/W	THRESHOLD[7:0]								0xFF	MON[1]
0x22	UV_LF[1]	R/W	THRESHOLD[7:0]								0x00	MON[1]
0x23	OV_LF[1]	R/W	THRESHOLD[7:0]								0xFF	MON[1]
0x24	FLT_HF[1]	R/W	OV_DEB[3:0]				UV_DEB[3:0]				0x00	MON[1]
0x25	FC_LF[1]	R/W	RSVD					THREEDB[2:0]			0x04	MON[1]
Bank 1: 0x30~0x3F – Monitor Registers (CH2)												
0x30	UV_HF[2]	R/W	THRESHOLD[7:0]								0x00	MON[2]
0x31	OV_HF[2]	R/W	THRESHOLD[7:0]								0xFF	MON[2]
0x32	UV_LF[2]	R/W	THRESHOLD[7:0]								0x00	MON[2]
0x33	OV_LF[2]	R/W	THRESHOLD[7:0]								0xFF	MON[2]
0x34	FLT_HF[2]	R/W	OV_DEB[3:0]				UV_DEB[3:0]				0x00	MON[2]
0x35	FC_LF[2]	R/W	RSVD					THREEDB[2:0]			0x04	MON[2]
Bank 1: 0x40~0x4F – Monitor Registers (CH3)												
0x40	UV_HF[3]	R/W	THRESHOLD[7:0]								0x00	MON[3]
0x41	OV_HF[3]	R/W	THRESHOLD[7:0]								0xFF	MON[3]
0x42	UV_LF[3]	R/W	THRESHOLD[7:0]								0x00	MON[3]
0x43	OV_LF[3]	R/W	THRESHOLD[7:0]								0xFF	MON[3]
0x44	FLT_HF[3]	R/W	OV_DEB[3:0]				UV_DEB[3:0]				0x00	MON[3]
0x45	FC_LF[3]	R/W	RSVD					THREEDB[2:0]			0x04	MON[3]
Bank 1: 0x50~0x5F – Monitor Registers (CH4)												
0x50	UV_HF[4]	R/W	THRESHOLD[7:0]								0x00	MON[4]
0x51	OV_HF[4]	R/W	THRESHOLD[7:0]								0xFF	MON[4]
0x52	UV_LF[4]	R/W	THRESHOLD[7:0]								0x00	MON[4]
0x53	OV_LF[4]	R/W	THRESHOLD[7:0]								0xFF	MON[4]
0x54	FLT_HF[4]	R/W	OV_DEB[3:0]				UV_DEB[3:0]				0x00	MON[4]
0x55	FC_LF[4]	R/W	RSVD					THREEDB[2:0]			0x04	MON[4]
Bank 1: 0x60~0x6F – Monitor Registers (CH5)												
0x60	UV_HF[5]	R/W	THRESHOLD[7:0]								0x00	MON[5]
0x61	OV_HF[5]	R/W	THRESHOLD[7:0]								0xFF	MON[5]
0x62	UV_LF[5]	R/W	THRESHOLD[7:0]								0x00	MON[5]
0x63	OV_LF[5]	R/W	THRESHOLD[7:0]								0xFF	MON[5]
0x64	FLT_HF[5]	R/W	OV_DEB[3:0]				UV_DEB[3:0]				0x00	MON[5]
0x65	FC_LF[5]	R/W	RSVD					THREEDB[2:0]			0x04	MON[5]
Bank 1: 0x70~0x7 – Monitor Registers (CH6)												
0x70	UV_HF[6]	R/W	THRESHOLD[7:0]								0x00	MON[6]
0x71	OV_HF[6]	R/W	THRESHOLD[7:0]								0xFF	MON[6]
0x72	UV_LF[6]	R/W	THRESHOLD[7:0]								0x00	MON[6]
0x73	OV_LF[6]	R/W	THRESHOLD[7:0]								0xFF	MON[6]
0x74	FLT_HF[6]	R/W	OV_DEB[3:0]				UV_DEB[3:0]				0x00	MON[6]
0x75	FC_LF[6]	R/W	RSVD					THREEDB[2:0]			0x04	MON[6]

Table 12: Sequence Registers

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (10)	Group
Bank 1: 0xA0~0xAF – Sequence Registers (Top Level)												
0xA0	SEQ_ REC_CTL	R/W	REC_ START	SEQ[1:0]		TS_ACK	SEQ_ ON_ ACK	SEQ_ OFF_ ACK	SEQ_ EXS_ ACK	SEQ_ ENS_ ACK	0x00	WRKS
0xA1	AMSK_ON	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x3F	IEN
0xA2	AMSK_ OFF	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x3F	IEN
0xA3	AMSK_ EXS	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x3F	IEN
0xA4	AMSK_ ENS	R/W	RSVD	RSVD	VIN[6]	VIN[5]	VIN[4]	VIN[3]	VIN[2]	VIN[1]	0x3F	IEN
0xA5	SEQ_ TOUT_MSB	R/W	MILLISECOND[15:8]								0x00	SEQ
0xA6	SEQ_TOUT _LSB	R/W	MILLISECOND[7:0]								0x31	SEQ
0xA7	SEQ_SYNC	R/W	PULSE_WIDTH[7:0]								0x05	SEQ
0xA8	SEQ_UP_ THLD	R/W	RSVD	RSVD	OFF_UV [6]	OFF_UV [5]	OFF_UV [4]	OFF_UV [3]	OFF_UV [2]	OFF_ UV[1]	0x3F	SEQ
0xA9	SEQ_DN_ THLD	R/W	RSVD	RSVD	OFF_UV [6]	OFF_UV [5]	OFF_UV [4]	OFF_UV [3]	OFF_UV [2]	OFF_ UV[1]	0x00	SEQ
Bank 1: 0xB0~0xBF: Sequence Registers (Power On (ACT/SHDN = 0 to 1) Expected Sequence Order Registers)												
0xB0	SEQ_ON_ EXP[1]	R/W	ORDER[7:0]								0x00	SEQ
0xB1	SEQ_ON_ EXP[2]	R/W	ORDER[7:0]								0x00	SEQ
0xB2	SEQ_ON_ EXP[3]	R/W	ORDER[7:0]								0x00	SEQ
0xB3	SEQ_ON_ EXP[4]	R/W	ORDER[7:0]								0x00	SEQ
0xB4	SEQ_ON_ EXP[5]	R/W	ORDER[7:0]								0x00	SEQ
0xB5	SEQ_ON_ EXP[6]	R/W	ORDER[7:0]								0x00	SEQ
Bank 1: 0xC0~0xCF: Sequence Registers (Power Off (ACT/SHDN = 1 to 0) Expected Sequence Order Registers)												
0xC0	SEQ_OFF_ EXP[1]	R/W	ORDER[7:0]								0x00	SEQ
0xC1	SEQ_OFF_ EXP[2]	R/W	ORDER[7:0]								0x00	SEQ
0xC2	SEQ_OFF_ EXP[3]	R/W	ORDER[7:0]								0x00	SEQ
0xC3	SEQ_OFF_ EXP[4]	R/W	ORDER[7:0]								0x00	SEQ
0xC4	SEQ_OFF_ EXP[5]	R/W	ORDER[7:0]								0x00	SEQ
0xC5	SEQ_OFF_ EXP[6]	R/W	ORDER[7:0]								0x00	SEQ
Bank 1: 0xD0~0xDF: Sequence Registers (Sleep Exit (ACT/SLP = 0 to 1) Expected Sequence Order Registers)												
0xD0	SEQ_EXS_ EXP[1]	R/W	ORDER[7:0]								0x00	SEQ
0xD1	SEQ_EXS_ EXP[2]	R/W	ORDER[7:0]								0x00	SEQ
0xD2	SEQ_EXS_ EXP[3]	R/W	ORDER[7:0]								0x00	SEQ
0xD3	SEQ_EXS_ EXP[4]	R/W	ORDER[7:0]								0x00	SEQ
0xD4	SEQ_EXS_ EXP[5]	R/W	ORDER[7:0]								0x00	SEQ

0xD5	SEQ_EXS_EXP[6]	R/W	ORDER[7:0]	0x00	SEQ
Bank 1: 0xE0~0xEF: Sequence Registers (Sleep Entry (ACT/SLP = 1 to 0) Expected Sequence Order Registers)					
0xE0	SEQ_ENS_EXP[1]	R/W	ORDER[7:0]	0x00	SEQ
0xE1	SEQ_ENS_EXP[2]	R/W	ORDER[7:0]	0x00	SEQ
0xE2	SEQ_ENS_EXP[3]	R/W	ORDER[7:0]	0x00	SEQ
0xE3	SEQ_ENS_EXP[4]	R/W	ORDER[7:0]	0x00	SEQ
0xE4	SEQ_ENS_EXP[5]	R/W	ORDER[7:0]	0x00	SEQ
0xE5	SEQ_ENS_EXP[6]	R/W	ORDER[7:0]	0x00	SEQ

Note:

10) The default code is the “-0000” version. The default value is the initial configurations for the MPQ79500FS-0000 registers. These values can be redefined if the OTP function is available.

REGISTER DESCRIPTION

VENDOR_ID (0x00) – Bank Independent

Access: Read-only

POR: Load from the OTP

The VENDOR_ID command returns the vendor ID.

Bits	Name	Description
D[7:0]	VENDOR_ID	Returns the vendor information.

MODEL_REV (0x01) – Bank Independent

Access: Read-only

POR: Load from the OTP

The MODEL_REV command returns the model revision information.

Bits	Name	Description
D[7:0]	MODEL_REV	Returns the model revision information

INT_SRC (0x10) – Bank 0

Access: Read-only

POR: N/A

The INT_SRC command reports global interrupt source status information. INT_SRC represents the reason for a NIRQ assertion. When the host processor receives a NIRQ signal, it may read this register to determine the source of the interrupt. This register is cleared if NIRQ was not asserted by the MPQ79500FS.

Bits	Name	Description
D[7]	VENDOR	Reports a vendor-specific internal fault. The details are reported in INT_VENDOR. This bit represents the ORed value for all bits in INT_VENDOR. 0: No fault was reported in INT_VENDOR 1: A fault was reported in INT_VENDOR
D[6:3]	RSVD	Reserved.
D[2]	TEST	Reports an internal test or configuration load fault. The details are reported in INT_TEST. This bit represents the ORed value for all bits in INT_TEST. 0: No test/configuration fault has been detected 1: A test/configuration fault has been detected
D[1]	CONTROL	Reports a control status or communication fault. The details are reported in INT_CONTROL. This bit represents the ORed value for all bits in INT_CONTROL. 0: No status or communication fault has been detected 1: A status or communication fault has been detected
D[0]	MONITOR	Reports a voltage or sequence monitor fault. The details are reported in INT_MONITOR. This bit represents the ORed value for all bits in INT_MONITOR. 0: No voltage or sequence fault has been detected 1: A voltage or sequence fault has been detected

INT_MONITOR (0x11) – Bank 0

Access: Read-only

POR: N/A

The INT_MONITOR command reports the voltage and sequence monitor interrupt statuses.

Bits	Name	Description
D[7]	SEQ_ON	Reports a power on sequence fault. The details are reported in INT_SEQ_ON. This bit represents the ORed value for all bits in INT_SEQ_ON. If the contents of the SEQ_ON_LOG[x] register do not match the values defined in the SEQ_ON_EXP[x] register, a power on sequence fault occurs. 0: No power on sequence fault has been detected 1: A power on sequence fault has been detected
D[6]	SEQ_OFF	Reports a power off sequence fault. The details are reported in INT_SEQ_OFF. This bit represents the ORed value for all bits in INT_SEQ_OFF. If the contents of the SEQ_OFF_LOG[x] register do not match the values defined in the SEQ_OFF_EXP[x] register, a power off sequence fault occurs. 0: No power off sequence fault has been detected 1: A power off sequence fault has been detected
D[5]	SEQ_EXS	Reports a sleep exit sequence fault. The details are reported in INT_SEQ_EXS. This bit represents the ORed value for all bits in INT_SEQ_EXS. If the contents of the SEQ_EXS_LOG[N] register do not match the values defined in the SEQ_EXS_EXP[x] register, a sleep exit sequence fault occurs. 0: No sleep exit sequence fault has been detected 1: A sleep exit sequence fault has been detected
D[4]	SEQ_ENS	Reports a sleep entry sequence fault. The details are reported in INT_SEQ_ENS. This bit represents the ORed value for all bits in INT_SEQ_ENS. If the contents of the SEQ_ENS_LOG[N] register do not match the values defined in the SEQ_ENS_EXP[x] register, a sleep entry sequence fault occurs. 0: No sleep entry sequence fault has been detected 1: A sleep entry sequence fault has been detected
D[3]	OV_LF	Reports an over-voltage low-frequency (OVLF) fault. The details are reported in INT_OVLF. This bit represents the ORed value for all bits in INT_OVLF. 0: No OVLF fault has been detected 1: An OVLF fault has been detected
D[2]	OV_HF	Reports an over-voltage high-frequency (OVHF) fault. The details are reported in INT_OVHF. This bit represents the ORed value for all bits in INT_OVHF. 0: No OVHF fault has been detected 1: An OVHF fault has been detected
D[1]	UV_LF	Reports an under-voltage low-frequency (UVLF) fault. The details are reported in INT_UVLF. This bit represents the ORed value for all bits in INT_UVLF. 0: No UVLF fault has been detected 1: A UVLF fault has been detected
D[0]	UV_HF	Reports an under-voltage high-frequency (UVHF) fault. The details are reported in INT_UVHF. This bit represents the ORed value for all bits in INT_UVHF. 0: No UVHF fault has been detected 1: A UVHF fault has been detected

INT_UVHF (0x12) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_UVHF command reports the high-frequency (HF) channel under-voltage (UV) interrupt statuses.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	UVHF[N]	Reports an under-voltage high-frequency (UVHF) fault for channel x (where x = 1–6). If the channel's HF signal drops below the value set by UV_HF[x], this fault is triggered. 0: No UVHF fault has been detected (or the interrupt is disabled in the IEN_UVHF register) 1: A UVHF fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear only clears the bit if the UVHF fault condition is also removed in HPM (the HF signal exceeds the value set by UV_HF[x]).

INT_UVLF (0x14) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_UVLF command reports the low-frequency (LF) channel under-voltage (UV) interrupt statuses.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	UVLF[N]	Reports an under-voltage low-frequency (UVLF) fault for channel x (where x = 1–6). If the channel's LF signal drops below the value set by UV_LF[x], this fault is triggered. 0: No UVLF fault has been detected (or the interrupt is disabled in the IEN_UVLF register) 1: A UVLF fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear only clears the bit if the UVLF fault condition is also removed in HPM (the LF signal exceeds the value set by UV_LF[x]).

INT_OVHF (0x16) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_OVHF command reports the high-frequency (HF) channel over-voltage (OV) interrupt statuses.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] **(where x = 1–6)**	OVHF[N]	Reports an over-voltage high-frequency (OVHF) fault for channel x (where x = 1–6). If the channel's HF signal exceeds the value set by OV_HF[x], this fault is triggered. 0: No OVHF fault has been detected (or the interrupt is disabled in the IEN_OVHF register) 1: An OVHF fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear only clears the bit if the OVHF fault condition is also removed in HPM (the HF signal drops below the value set by OV_HF[x]).

INT_OVLF (0x18) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_OVLF command reports the low-frequency (LF) channel over-voltage (OV) interrupt statuses.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	OVLF[N]	Reports an over-voltage low-frequency (OVLF) fault for channel x (where x = 1–6). If the channel's LF signal exceeds the value set by OV_LF[x], this fault is triggered. 0: No OVLF fault has been detected (or the interrupt is disabled in the IEN_OVLF register) 1: An OVLF fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear only clears the bit if the OVLF fault condition is also removed in HPM (the LF signal drops below the value set by OV_LF[x]).

INT_SEQ_ON (0x1A) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_SEQ_ON command reports the power on sequence (ACT/SHDN = 0 to 1) interrupt statuses.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	SEQ_ON[N]	Reports a power on sequence fault for channel x (where x = 1–6). If the channel's power on sequence counter in the SEQ_ON_LOG[x] register does not match the value defined in the SEQ_ON_EXP[x] register, this fault is triggered. 0: No power on sequence fault has been detected (or the interrupt is disabled in the IEN_SEQ_ON register) 1: A power on sequence fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during next sequence.

INT_SEQ_OFF (0x1C) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_SEQ_OFF command reports the power off sequence (ACT/SHDN = 1 to 0) interrupt statuses.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	SEQ_OFF[N]	Reports a power off sequence fault for channel x (where x = 1–6). If the channel's power off sequence counter in the SEQ_OFF_LOG[x] register does not match the value defined in the SEQ_OFF_EXP[x] register, this fault is triggered. 0: No power off sequence fault has been detected (or the interrupt is disabled in the IEN_SEQ_OFF register) 1: A power off sequence fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during next sequence.

INT_SEQ_EXS (0x1E) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_SEQ_EXS command reports the sleep exit sequence (ACT/SLP = 0 to 1) interrupt statuses.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	SEQ_EXS[N]	Reports a sleep exit sequence fault for channel x (where x = 1–6). Iif the channel's recorded sleep exit sequence counter in the SEQ_EXS_LOG[x] register does not match the value defined in the SEQ_EXS_EXP[x] register, this fault is triggered. 0: No sleep exit sequence fault has been detected (or the interrupt is disabled in the IEN_SEQ_EXS register) 1: A sleep exit sequence fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during next sequence.

INT_SEQ_ENS (0x20) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_SEQ_ENS command reports the sleep entry sequence (ACT/SLP = 1 to 0) interrupt statuses.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	SEQ_EXS[N]	Reports an sleep entry sequence fault for channel x (where x = 1–6). If the channel's recorded sleep entry sequence counter in the SEQ_ENS_LOG[x] register does not match the value defined in the SEQ_ENS_EXP[x] register, this fault is triggered. 0: No sleep entry sequence fault has been detected (or the interrupt is disabled in the IEN_SEQ_ENS register) 1: A sleep entry sequence fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during next sequence.

INT_CONTROL (0x22) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_CONTROL command reports the control and communication interrupt statuses.

Bits	Name	Description
D[7:5]	RSVD	Reserved
D[4]	RT_CRC	Reports a runtime register CRC fault. 0: No CRC fault has been detected (or RT_CRC is disabled) 1: A register CRC fault has been detected The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during the next register CRC.

D[3]	NIRQ	Reports an interrupt pin fault (this fault bit always enabled; no enable bit is available). This fault is only detected when the MPQ79500FS drives NIRQ low. 0: No fault has been detected on NIRQ pin 1: A Low resistance path to the supply has been detected on the NIRQ pin The recovery of this fault condition does not clear the bit. This bit can only be cleared by the host with a write-1-to-clear. Write-1-to-clear is only effective if the NIRQ fault condition is also removed.
D[2]	TSD	Reports a thermal shutdown (TSD) fault. 0: No TSD fault has been detected (or TSD is disabled) 1: A TSD fault has been detected The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear is only effective if the TSD condition is also removed.
D[1]	SYNC	Reports a /SYNC pin fault. This fault is only detected when the MPQ79500FS drives the /SYNC pin low. 0: No fault detected has been detected on the /SYNC pin (or SYNC is disabled) 1: A low resistance path to the supply has been detected on the /SYNC pin The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear is only effective if the SYNC fault condition is also removed.
D[0]	PEC	Reports a PEC fault. 0: No PEC mismatch has occurred (or PEC is disabled) 1: A PEC mismatch has occurred, or REQ_PEC = 1 and the PEC is missing in a write transaction The recovery of the fault condition does not clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during the next I^2C transaction.

INT_TEST (0x23) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_TEST command reports the internal test and configuration load interrupt statuses.

Bits	Name	Description
D[7:4]	RSVD	Reserved.
D[3]	ECC_SEC	Reports whether an ECC single-error has been detected an corrected on the OTP configuration load. 0: No single-error has been corrected (or ECC_SEC is disabled) 1: A Single-error has been corrected Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during the next OTP configuration load.
D[2]	ECC_DED	Reports whether an ECC double-error has been detected on the OTP configuration load. The fault bit is always enabled (there is no associated interrupt enable bit). 0: No double-error has been detected on the OTP load 1: A Double-error has been detected on the OTP load Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during the next OTP configuration load. Once ECC_DED occurs, NIRQ is pulled down and the interrupt cannot be cleared. The host reacts accordingly.

D[1]	I_BIST_C	Indicates whether built-in self-testing (BIST) is complete. 0: BIST is not complete (or BIST_C is disabled) 1: BIST is complete Write-1-to-clear clears the bit. After completing the next BIST execution, this bit is set again.
D[0]	BIST	Reports a BIST fault. 0: No BIST fault has been detected (or BIST is disabled) 1: A BIST fault has been detected Write-1-to-clear clears the bit. If the same fault is detected, the bit is set again during the next BIST execution. If a BIST fault is caused by logic BIST, NIRQ is pulled down and cannot be cleared, even if the BIST bit is cleared. The host reacts accordingly.

INT_VENDOR (0x24) – Bank 0

Access: Read and write-1-to-clear. Writing 0 has no effect; writing 1 to a bit that is already set to 0 has no effect.

POR: N/A

The INT_VENDOR command reports vendor-specific internal interrupt statuses.

Bits	Field Name	Description
D[7]	I2C_WR_CHK	Reports the I^2C write back check fault status. 0: No I^2C write back fault has been detected. 1: The I^2C write back check failed
D[6]	RSVD	Reserved.
D[5]	CLK_FAIL	Reports the internal reference clock and system clock check. Clock monitoring always works. If a clock failure is detected, the fault is reported, then NIRQ latches low and cannot be cleared. 0: No clock fault has been detected 1: An internal reference clock is lost or the system clock is lost
D[4]	RSVD	Reserved.
D[3]	TMR_FAIL	Reports the internal triple voting check for important logic circuits not covered by LBIST. 0: No TMR failure has been detected. 1: Internal triple voting failed
D[2]	ADC_FAIL	Reports the ADC check. Can only be cleared if the fault has been removed. 0: No ADC fault has been detected 1: There is an ADC or reference voltage failure
D[1]	I2C_CONWR_CHK	Reports the I^2C continuous write check. When PEC is enabled, only single-byte write is allowed and continuous write is checked. 0: No continuous write has been detected 1: Continuous write has been detected
D[0]	STATE_FAIL	Reports the state machine check. 0: No state machine error has been detected 1: An error has been detected during one-hot coding

VMON_STAT (0x30) – Bank 0

Access: Read-only

POR: N/A

The VMON_STAT command reports the status of internal operations and other non-critical conditions.

Bits	Name	Description
D[7]	RSVD	Reserved.
D[6]	ST_BIST_C	Reports the built-in self-testing (BIST) status. 0: Not complete 1: Complete
D[5:4]	RSVD	Reserved.
D[3]	ST_ACTSLP	Reports the current state of the ACT/SLP input. 0: The ACT/SLP pin is driven low (SLP) by the system 1: The ACT/SLP pin is driven high (ACT) by the system
D[2]	ST_ACTSHDN	Reports the current state of the ACT/SHDN input. 0: The ACT/SHDN pin is driven low (SHDN) by the system 1: The ACT/SHDN pin is driven high (ACT) by the system
D[1]	ST_SYNC	Reports the current state of the /SYNC pin. 0: /SYNC is low 1: /SYNC is high
D[0]	RSVD	Reserved.

TEST_INFO (0x31) – Bank 0

Access: Read-only

POR: N/A

The TEST_INFO command reports the internal self-testing and ECC information.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[5]	ECC_SEC	Reports the status of ECC SEC on the OTP configuration load. 0: No error correction has been applied 1: A single error correction has been applied
D[4]	ECC_DED	Reports the status of ECC DED on the OTP configuration load. 0: No double error has been detected 1: A double error has been detected
D[3]	BIST_VM	Reports the status of the volatile memory test output from BIST. 0: Pass 1: Fail
D[2]	BIST_NVM	Reports the status of the NVM test output from BIST. 0: Pass 1: Fail
D[1]	BIST_L	Reports the status of the logic test output from BIST. 0: Pass 1: Fail

D[0]	BIST_A	Reports the status of the analog test output from BIST. 0: Pass 1: Fail

OFF_STAT (0x32) – Bank 0

Access: Read-only

POR: N/A

The OFF_STAT command reports the channel's off status.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Reports the off status for each channel. 0: Not off 1: Off

SEQ_REC_STAT (0x34) – Bank 0

Access: Read-only

POR: N/A

The SEQ_REC_STAT command reports the sequence recording statuses.

Bits	Field Name	Description
D[7]	REC_ACTIVE	Indicates the status of sequence logging (recording). 0: No sequence recording is active 1: ACT/SHDN, ACT/SLP, or REC_START initiated a power sequence and recording is active
D[6:5]	SEQ[1:0]	Reports the current sequence being recorded. 00b: Power on (ACT/SHDN = 0 to 1) 01b: Power off (ACT/SHDN = 1 to 0) 10b: Sleep exit (ACT/SLP = 0 to 1) 11b: Sleep entry (ACT/SLP = 1 to 0)
D[4]	TS_RDY	Reports the timestamp data availability in the SEQ_TIME_xSB registers. 0: No new data is available (or data is already read) 1: New data is available (data still needs to be read) If EN_TS_OW = 0, this bit is cleared when TS_ACK is written to 1 by the host. If EN_TS_OW = 1, this bit is cleared when all the SEQ_TIME_xSB[x] registers for the enabled channels (in the VIN_CH_EN register) are read. If the bit is set and REC_ACTIVE is also set, then the data in the SEQ_TIME_xSB registers are being overwritten.
D[3]	SEQ_ON_RDY	Reports the power on sequence data availability in the SEQ_ON_LOG registers: 0: No new data is available (or data is already read) 1: New data is available (data still needs to be read) If EN_SEQ_OW = 0, this bit is cleared when SEQ_ON_ACK is written to 1 by the host. If EN_SEQ_OW = 1, this bit is cleared when all the SEQ_ON_LOG registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set, REC_ACTIVE is set, and SEQ[1:0] = 00b, then the data in the SEQ_ON_LOG registers is being overwritten.

D[2]	SEQ_OFF_RDY	Reports the power off sequence data availability in the SEQ_OFF_LOG registers: 0: No new data is available (or data is already read) 1: New data is available (data still needs to be read) If EN_SEQ_OW = 0, this bit is cleared when SEQ_OFF_ACK is written to 1 by the host. If EN_SEQ_OW = 1, this bit is cleared when all the SEQ_OFF_LOG registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set, REC_ACTIVE is set, and SEQ[1:0] = 01b, then the data in the SEQ_OFF_LOG registers is being overwritten.
D[1]	SEQ_EXS_RDY	Reports the sleep exit sequence data availability in the SEQ_EXS_LOG registers: 0: No new data is available (or data is already read) 1: New data is available (data still needs to be read) If EN_SEQ_OW = 0, this bit is cleared when SEQ_EXS_ACK is written to 1 by the host. If EN_SEQ_OW = 1, this bit is cleared when all the SEQ_EXS_LOG registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set, REC_ACTIVE is set, and SEQ[1:0] = 10b, then the data in the SEQ_EXS_LOG registers is being overwritten.
D[0]	SEQ_ENS_RDY	Reports the sleep entry sequence data availability in the SEQ_ENS_LOG registers. 0: No new data is available (or data is already read) 1: New data is available (data still needs to be read) If EN_SEQ_OW = 0, this bit is cleared when SEQ_ENS_ACK is written to 1 by the host. If EN_SEQ_OW = 1, this bit is cleared when all the SEQ_ENS_LOG registers for the enabled channels (in VIN_CH_EN register) are read. If the bit is set, REC_ACTIVE is set, and SEQ[1:0] = 11b, then the data in the SEQ_ENS_LOG registers is being overwritten.

SEQ_OW_STAT (0x35) – Bank 0

Access: Read-only

POR: N/A

The SEQ_OW_STAT command reports the sequence recording overwrite statuses.

Bits	Name	Description
D[7:5]	RSVD	Reserved.
D[4]	TS_OW	Indicates whether timestamp data was overwritten. 0: No data was overwritten 1: Data was overwritten (if EN_TS_OW = 1), or data could not be written (if EN_TS_OW = 0) For more details, see the Recorded Data Handling section on page 42.
D[3]	SEQ_ON_OW	Indicates whether power on sequence data was overwritten. 0: No data was overwritten 1: Data was overwritten (if EN_SEQ_OW = 1), or data could not be written (if EN_SEQ_OW = 0) For more details, see the Recorded Data Handling section on page 42.
D[2]	SEQ_OFF_OW	Indicates whether power off sequence data was overwritten. 0: No data was overwritten 1: Data was overwritten (if EN_SEQ_OW = 1), or data could not be written (if EN_SEQ_OW = 0) For more details, see the Recorded Data Handling section on page 42.
D[1]	SEQ_EXS_OW	Indicates whether sleep exit sequence data was overwritten. 0: No data was overwritten 1: Data was overwritten (if EN_SEQ_OW = 1), or data could not be written (if EN_SEQ_OW = 0) For more details, see the Recorded Data Handling section on page 42.

D[0]	SEQ_ENS_OW	Indicates whether sleep entry sequence data was overwritten. 0: No data was overwritten 1: Data was overwritten (if EN_SEQ_OW = 1), or data could not be written (if EN_SEQ_OW = 0) For more details, see the Recorded Data Handling section on page 42.

SEQ_ORD_STAT (0x36) – Bank 0

Access: Read-only

POR: N/A

The SEQ_ORD_STAT command returns the sequencing and /SYNC counter (rail order) value.

Bits	Field Name	Description
D[7:0]	SYNC_COUNT[7:0]	Returns the counter value during a power/sleep sequence. It corresponds to the number of detected SYNC falling edges, and is used as tag value for the monitored channels.

VIN_LVL[x] (0x40~0x45) – Bank 0

Access: Read-only

POR: N/A

The VIN_LVL[x] (where x = 1–6) command stores the channel's V_{IN} voltage level (8-bit ADC).

Bits	Field Name	Description
D[7:0]	ADC[7:0]	Represents the 8-bit voltage level of channel N. The 8-bit value interpretation depends on the scaling setting via the VRANGE_MULT register. 1x scaling: the 8-bit value represents the range 0.2V to 1.475V, where 1 LSB = 5mV 4x scaling: the 8-bit value represents the range 0.8V to 5.9V, where 1 LSB = 20mV

SEQ_ON_LOG[x] (0x50~0x55) – Bank 0

Access: Read-only

POR: N/A

The SEQ_ON_LOG[x] (where x = 1–6) command stores the channel's power on sequence order value (ACT/SHDN = 0 to 1).

Bits	Field Name	Description
D[7:0]	ORDER[7:0]	Stores the power on sequence order value for the channel. The sequence order value is the tag assigned to the channel when the sequence is triggered by ACT/SHDN. The tag is assigned when the voltage rising level exceeds SEQ_UP_THLD. The tag value is SYNC_ORD_COUNT at the time when the threshold is crossed.

SEQ_OFF_LOG[x] (0x60~0x65) – Bank 0

Access: Read-only

POR: N/A

The SEQ_OFF_LOG[x] (where x = 1–6) command stores the channel's power off sequence order value (ACT/SHDN = 1 to 0).

Bits	Name	Description
D[7:0]	ORDER[7:0]	Stores the power off sequence order value for the channel. The sequence order value is the tag assigned to the channel when the sequence is triggered by ACT/SHDN. The tag is assigned when the voltage falling level drops below SEQ_DN_THLD. The tag value is SYNC_ORD_COUNT at the time when the threshold is crossed.

SEQ_EXS_LOG[x] (0x70~0x75) – Bank 0

Access: Read-only

POR: N/A

The SEQ_EXS_LOG[x] (where x = 1–6) command stores the channel's sleep exit sequence order value (ACT/SLP = 0 to 1).

Bits	Name	Description
D[7:0]	ORDER[7:0]	Stores the sleep exit sequence order value for the channel. The sequence order value is the tag assigned to the channel when the sequence is triggered by ACT/SLP. The tag is assigned when the voltage rising level exceeds the SEQ_UP_THLD value. The tag value is SYNC_ORD_COUNT at the time when the threshold is crossed.

SEQ_ENS_LOG[x] (0x80~0x85) – Bank 0

Access: Read-only

POR: N/A

The SEQ_EXS_LOG[x] (where x = 1–6) command stores the channel's sleep entry sequence order value (ACT/SLP = 1 to 0).

Bits	Name	Description
D[7:0]	ORDER[7:0]	This register stores the sleep entry sequence order value for the channel. The sequence order value is the tag assigned to the channel when the sequence is triggered by ACT/SLP. The tag is assigned when the voltage falling level drops below SEQ_DN_THLD. The tag value is SYNC_ORD_COUNT at the time when the threshold is crossed.

SEQ_TIME_MSB[x] and SEQ_TIME_LSB[x] (0x90~0x9B) – Bank 0

MSB: 0x90 + (2x - 2), where x = 1–6

LSB: 0x91 + (2x - 2), where x = 1–6

Access: Read-only

POR: N/A

The SEQ_TIME_MSB[x] and SEQ_TIME_LSB[x] command stores the channel's sequence timestamp value for the MSB and LSB (for all sequences).

Bits	Name	Description
D[7:0]	CLOCK[7:0]	Stores the MSB and LSB of the sequence timestamp for the channel. The sequence timer value is the time assigned to the channel when the sequence is triggered by ACT/SHDN or ACT/SLP. The timestamp is stored when the voltage rising level exceeds the UV_LF[x] threshold for the power on and sleep exit sequences (ACT/SHDN = 0 to 1 or ACT/SLP = 0 to 1). The timestamp is stored when the voltage falling level drops below the OFF threshold (200mV) for the power off and sleep entry sequences (ACT/SHDN = 1 to 0 or ACT/SLP = 1 to 0). The least significant bit corresponds to 50µs (equal to t_{SEQ_LSB}). See the Timestamps and Sequence Order section on page 41 for more details.

VMON_CTL (0x10) – Bank 1

Access: Read/write. Read-only if the WRKC group is protected.

POR: Load from the OTP

The VMON_CTL command controls the VMON device.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.

D[5]	SLEEP_PWR	Selects the power mode. Low-power mode (LPM) can be initiated through this bit in the idle/sleep state. Setting this bit to something other than the idle/sleep state is invalid. There is no WRKC protection on this bit. 0: LPM 1: High-power mode (HPM)
D[4]	RSVD	Reserved.
D[3]	RESET	Resets the protection keys. 0: Always read 0 1: Reset the protection keys
D[2]	SYNC_RST	Resets the SYNC counter (SYNC_COUNT). 0: Always read 0 1: Reset the SYNC counter
D[1]	FORCE_SYNC	Force SYNC assertion. 0: The /SYNC pin is de-asserted and controlled by the sequence monitoring logic 1: The /SYNC pin is forced to assert (low)
D[0]	FORCE_NIRQ	Force NIRQ assertion. 0: NIRQ pin is de-asserted and controlled by the interrupt registers faults 1: The NIRQ pin is forced to assert (low)

VMON_MISC (0x11) – Bank 1

Access: Read/write. Read-only if CFG group is protected.

POR: Load from the OTP

The VMON_MISC command sets miscellaneous monitor configurations.

Bits	Field Name	Description
D[7:4]	RSVD	Reserved.
D[3]	EN_TS_OW	Enables the timestamp recording to be overwritten. 0: Disabled. If sequence timestamp data is available in the SEQ_TIME_xSB[x] registers and the TS_RDY bit is set (data not read yet), then a new sequence does not overwrite the existing data 1: Enabled (default). The sequence timestamp data is overwritten with a new sequence, regardless of the TS_RDY bit For more details, see the Recorded Data Handling section on page 42.
D[2]	EN_SEQ_OW	Enables the sequence order recording to be overwritten. 0: Disabled. If sequence order data is available in the SEQ_ON_LOG[x], SEQ_OFF_LOG[x], SEQ_EXS_LOG[x], or SEQ_ENS_LOG[x] registers and the related bits are set (data not read yet), then a new sequence does not overwrite the existing data 1: Enabled (default). The sequence order data is overwritten with a new sequence, regardless of the SEQ_ON_RDY, SEQ_OFF_RDY, SEQ_EXS_RDY, or SEQ_ENS_RDY bits For more details, see the Recorded Data Handling section on page 42.
D[1]	REQ_PEC	Require PEC byte (valid only if EN_PEC is 1). 0: A missing PEC byte is treated as a good PEC 1: A missing PEC byte is treated as a bad PEC and triggers a fault
D[0]	EN_PEC	Enables PEC. 0: Disabled (default) 1: Enabled

TEST_CFG (0x12) – Bank 1

Access: Read/write. Read-only if the CFG group is protected.

Default: Load from the OTP (only AT_POR[1:0])

The TEST_CFG command configures the built-in self-test (BIST) execution. See the Built-In Self-Testing (BIST) and Load Configuration section on page 30 for more details.

Bits	Name	Description
D[7:3]	RSVD	Reserved.
D[2]	AT_SHDN	Runs BIST when exiting an ACTIVE state due to ACT/SHDN transitioning from 1 to 0. The device is ready after t_{CFG_WB}. This bit cannot be set in the OTP/NVM. Always defaults to 0 when loading configurations from the OTP/NVM.
D[1:0]	AT_POR[1:0]	Determines whether to run the BIST at power-on reset (POR). The device is ready after t_{CFG_WB}. 00b: For a valid OTP configuration, skip BIST at POR 01b: For a corrupt OTP configuration, run BIST at POR 10b: For a corrupt OTP configuration, run BIST at POR 11b: For a valid OTP configuration, run BIST at POR These bits can be set in OTP/NVM, and they are read-only from the host while the CFG group is protected.

IEN_UVHF (0x13) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_UVHF command enables under-voltage high-frequency (UVHF) interruption. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Enables under-voltage high-frequency (UVHF) fault interruption for the respective channel. 0: Disabled 1: Enabled

IEN_UVLF (0x14) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_UVLF command enables under-voltage low-frequency (UVLF) interruption. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Enables under-voltage low-frequency (UVLF) fault interruption for the respective channel. 0: Disabled 1: Enabled

IEN_OVHF (0x15) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_OVHF command enables over-voltage high-frequency (OVHF) fault interruption. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Enables over-voltage high-frequency (OVHF) fault interruption for the respective channel. 0: Disabled **1: Enabled**

IEN_OVLF (0x16) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_OVLF command enables over-voltage low-frequency (OVLF) fault interruption. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Enables over-voltage low-frequency (OVLF) fault interruption for the respective channel. 0: Disabled 1: Enabled

IEN_SEQ_ON (0x17) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_SEQ_ON command enables the power on sequence (ACT/SHDN = 0 to 1) fault interruption. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Enables power on sequence fault interruption for the respective channel. 0: Disabled 1: Enabled

IEN_SEQ_OFF (0x18) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_SEQ_OFF command enables power off sequence (ACT/SHDN = 1 to 0) fault interruption. Note that clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Enables power off sequence fault interruption for the respective channel. 0: Disabled 1: Enabled

IEN_SEQ_EXS (0x19) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_SEQ_EXS command enables sleep exit sequence (ACT/SLP = 0 to 1) fault interruption. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Enables sleep exit sequence fault interruption for the respective channel. 0: Disabled 1: Enabled

IEN_SEQ_ENS (0x1A) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_SEQ_ENS command enables sleep entry sequence (ACT/SLP = 1 to 0) fault interruption. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Enables sleep entry sequence fault interruption for the respective channel. 0: Disabled 1: Enabled

IEN_CONTROL (0x1B) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_CONTROL command enables the control and communication fault interruptions. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Field Name	Description
D[7:5]	RSVD	Reserved.
D[4]	RT_CRC	Enables the runtime register CRC fault interruption. 0: Disabled 1: Enabled
D[3]	RSVD	Reserved.
D[2]	TSD	Enables thermal shutdown fault interruption. 0: Disabled 1: Enabled
D[1]	SYNC	Enables /SYNC pin fault (short to supply or ground detected on the /SYNC pin) interruption. 0: Disabled 1: Enabled
D[0]	PEC	Enables PEC fault (mismatch) interruption. 0: Disabled 1: Enabled

IEN_TEST (0x1C) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_TEST command enables internal test and configuration load fault interruptions. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Name	Description
D[7:4]	RSVD	Reserved.
D[3]	ECC_SEC	Enables ECC SEC fault (on OTP load) interruption. 0: Disabled 1: Enabled
D[2]	RSVD	Reserved.
D[1]	BIST_C	Enables BIST completion interruption. 0: Disabled 1: Enabled
D[0]	BIST	Enables BIST fault interruption. 0: Disabled 1: Enabled Generally, this function should always be enabled. If there is an LBIST failure, the interrupt is directly reported to the NIRQ pin, and it is not controlled by the enable function.

IEN_VENDOR (0x1D) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The IEN_VENDOR command enables vendor-specific internal interruption. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Field Name	Description
D[7]	I2C_WR_CHK_INT_EN	Enables I^2C write with automatic readback check fault interruption. It is recommend to execute an I^2C write back check in the system instead of using this function. 0: Disabled 1: Enabled
D[6]	RSVD	Reserved.
D[5]	RSVD	Reserved.
D[4]	RSVD	Reserved.
D[3]	TMR_FAIL_INT_EN	Enables the internal triple voting fail for important logics not covered by LBIST. 0: Disabled 1: Enabled
D[2]	ADC_FAIL_INT_EN	0: Disabled 1: Enabled
D[1]	I2C_CONWR_CHK_EN	0: Disabled 1: Enabled
D[0]	STATE_FAIL_INT_EN	0: Disabled 1: Enabled

VIN_CH_EN (0x1E) – Bank 1

Access: Read/write. Read-only if the CFG group is protected.

POR: Load from the OTP

The VIN_CH_EN command enables voltage monitoring for channels 1–6. For disabled channels, OV and UV detection, 4x scale voltage monitoring, and sequence transition order faults are also disabled. Clearing the enable registers does not clear the fault flags. Fault clearing only supports W1C.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[N]	Enables voltage monitoring for the respective channel. 0: Disabled 1: Enabled

VRANGE_MULT (0x1F) – Bank 1

Access: Read/write. Read-only if the CFG group is protected.

POR: Load from the OTP

The VRANGE_MULT command sets the voltage monitoring range/scale for channels 1-6.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Sets the V_{IN} voltage monitoring range/scale for the respective channel. 0: 1x scaling (0.2V to 1.475V, with 5mV steps) 1: 4x scaling (0.8V to 5.9V, with 20mV steps)

UV_HF[x] (0x20 + (x - 1) x 0x10, where x = channel number (1–6)) – Bank 1

Access: Read/write. Read-only if the MON group is protected and MON[x] = 1.

POR: Load from the OTP

The UV_HF[x] command sets the channel's high-frequency (HF) under-voltage (UV) threshold. For more details, see the High-Frequency and Low-Frequency Voltage-Level Monitoring section on page 26, Figure 2 on page 26, and Figure 3 on page 27.

Bits	Name	Description
D[7:0]	THRESHOLD[7:0]	Sets the under-voltage (UV) threshold for the monitor's channel's high-frequency (HF) component. The 8-bit value interpretation depends on the value set by VRANGE_MULT. 1x scaling: the 8-bit value represents the range 0.2V to 1.475V where 1 LSB = 5mV 4x scaling: the 8-bit value represents the range 0.8V to 5.9V, where 1 LSB = 20mV

OV_HF[x] (0x21 + (x - 1) x 0x10, where x = channel number (1–6)) – Bank 1

Access: Read/write. Read-only if the MON group is protected and MON[x] = 1.

POR: Load from the OTP

The OV_HF[x] command sets the channel's high-frequency (HF) over-voltage (OV) threshold. For more details, see the High-Frequency and Low-Frequency Voltage-Level Monitoring section on page 26, Figure 2 on page 26, and Figure 3 on page 27.

Bits	Name	Description
D[7:0]	THRESHOLD[7:0]	Sets the over-voltage (OV) threshold for the monitor's channel's high-frequency (HF) component. The 8-bit value interpretation depends on the value set by VRANGE_MULT. 1x scaling: the 8-bit value represents the range 0.2V to 1.475V where 1 LSB = 5mV 4x scaling: the 8-bit value represents the range 0.8V to 5.9V, where 1 LSB = 20mV

UV_LF[x] (0x22 + (x - 1) x 0x10, where x = channel number (1–6)) – Bank 1

Access: Read/write. Read-only if the MON group is protected and MON[x] = 1.

POR: Load from the OTP

The UV_LF[x] command sets the channel's low-frequency (LF) under-voltage (UV) threshold. For more details, see the High-Frequency and Low-Frequency Voltage-Level Monitoring section on page 26, and Figure 2 on page 26.

Bits	Field Name	Description
D[7:0]	THRESHOLD[7:0]	Sets the under-voltage (UV) threshold for the monitor's channel's low-frequency (HF) component. The 8-bit value interpretation depends on the value set by VRANGE_MULT. 1x scaling: the 8-bit value represents the range 0.2V to 1.475V where 1 LSB = 5mV 4x scaling: the 8-bit value represents the range 0.8V to 5.9V, where 1 LSB = 20mV

OV_LF[x] (0x23 + (x - 1) x 0x10, where x = channel number (1–6)) – Bank 1

Access: Read/write. Read-only if the MON group is protected and MON[x] = 1.

POR: Load from the OTP

The OV_LF[x] command sets the channel's low-frequency (LF) over-voltage (OV) threshold. For more details, see the High-Frequency and Low-Frequency Voltage-Level Monitoring section on page 26, and Figure 2 on page 26.

Bits	Name	Description
D[7:0]	THRESHOLD[7:0]	Sets the over-voltage (OV) threshold for the monitor's channel's low-frequency (HF) component. The 8-bit value interpretation depends on the value set by VRANGE_MULT. 1x scaling: the 8-bit value represents the range 0.2V to 1.475V where 1 LSB = 5mV 4x scaling: the 8-bit value represents the range 0.8V to 5.9V, where 1 LSB = 20mV

FLT_HF[x] (0x24 + (x - 1) x 0x10, where x = channel number (1–6)) – Bank 1

Access: Read/write. Read-only if the MON group is protected and MON[x] = 1.

POR: Load from the OTP

The FLT_HF[x] command Channel N UV and OV debouncing for High Frequency thresholds comparator output. For more details, see the High-Frequency and Low-Frequency Voltage-Level Monitoring section on page 26, and Figure 2 on page 26.

Bits	Name	Description
D[7:4]	OV_DEB[3:0]	Sets the over-voltage (OV) comparator output debounce time (asserts when the voltage crosses the threshold for longer than the debounce time) for the high-frequency (HF) monitoring path. 0000b: 0.1µs 0001b: 0.2µs 0010b: 0.4µs 0011b: 0.8µs 0100b: 1.6µs 0101b: 3.2µs 0110b: 6.4µs 0111b: 12.8µs 1000b: 25.6µs 1001b: 51.2µs 1010b: 102.4µs 1011b: 102.4µs 1100b: 102.4µs 1101b: 102.4µs 1110b: 102.4µs 1111b: 102.4µs

D[3:0]	UV_DEB[3:0]	Sets the under-voltage (UV) comparator output debounce time (asserts when the voltage crosses the threshold for longer than the debounce time) for the high-frequency (HF) monitoring path. 0000b: 0.1µs 0001b: 0.2µs 0010b: 0.4µs 0011b: 0.8µs 0100b: 1.6µs 0101b: 3.2µs 0110b: 6.4µs 0111b: 12.8µs 1000b: 25.6µs 1001b: 51.2µs 1010b: 102.4µs 1011b: 102.4µs 1100b: 102.4µs 1101b: 102.4µs 1110b: 102.4µs 1111b: 102.4µs

FC_LF[x] (0x25 + (x - 1) x 0x10, where x = channel number (1–6)) – Bank 1

Access: Read/write. Read-only if the MON group is protected and MON[x] = 1.

POR: Load from the OTP

The FC_LF[x] command sets the channel's low-frequency (LF) path G(s), which is implemented as a digital low-pass filter (LPF). G(s) has the same transfer function as a first-order RC filter. Setting FC_LF[x] makes G(s) meet different cutoff frequencies (defined at the -3dB point). The corresponding cutoff frequency and time constant (τ) are listed below.

Bits	Name	Description
D[7:3]	RSVD	Reserved.
D[2:0]	THREEDB[2:0]	000b: Invalid 001b: Invalid 010b: 250Hz, τ = 636µs 011b: 500Hz, τ = 318µs 100b: 1kHz, τ = 159µs (default) 101b: 2kHz, τ = 80µs 110b: 4kHz, τ = 40µs 111b: Invalid

SEQ_REC_CTL (0xA0) – Bank 1

Access: Read/write. Read-only if the WRKS group is protected.

POR: 0x00

The SEQ_REC_CTL command sets the sequence control parameters.

Bits	Name	Description
D[7]	REC_START	Initiates the software to start sequence logging (recording). 0: Always reads as 0 1: Initiate power sequence (selected by SEQ[1:0]) recording
D[6:5]	SEQ[1:0]	Sequence to record (and compare for faults to corresponding expected sequence order registers): 00b: Power on (same as ACT/SHDN = 0 to 1) 01b: Power off (ACT/SHDN = 1 to 0) 10b: Sleep exit (ACT/SLP = 0 to 1) 11b: Sleep entry (ACT/SLP = 1 to 0)

D[4]	TS_ACK	Allows the timestamp data to be overwritten. Valid and used only if EN_TS_OW = 0. 0: Always reads as 0 1: Acknowledge the timestamp data and allow overwriting. TS_RDY and TS_OW are cleared For more details, see the Recorded Data Handling section on page 42.
D[3]	SEQ_ON_ACK	Allows the power on sequence data to be overwritten. Valid and used only if EN_SEQ_OW = 0. 0: Always reads as 0 1: Acknowledge the power on sequence data and allow overwriting. SEQ_ON_RDY and SEQ_ON_OW are cleared For more details, see the Recorded Data Handling section on page 42.
D[2]	SEQ_OFF_ACK	Allows the power off sequence data to be overwritten. Valid and used only if EN_SEQ_OW = 0. 0: Always reads as 0 1: Acknowledge the power off sequence data and allow overwriting. SEQ_OFF_RDY and SEQ_OFF_OW are cleared For more details, see the Recorded Data Handling section on page 42.
D[1]	SEQ_EXS_ACK	Allows the sleep exit sequence data to be overwritten. Valid and used only if EN_SEQ_OW = 0. 0: Always reads as 0 1: Acknowledge the sleep exit sequence data and allow overwriting. SEQ_EXS_RDY and SEQ_EXS_OW are cleared For more details, see the Recorded Data Handling section on page 42.
D[0]	SEQ_ENS_ACK	Allows the sleep entry sequence data to be overwritten. Valid and used only if EN_SEQ_OW = 0. 0: Always reads as 0 1: Acknowledge the sleep entry sequence data and allow overwriting. SEQ_ENS_RDY and SEQ_ENS_OW are cleared For more details, see the Recorded Data Handling section on page 42.

AMSK_ON (0xA1) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The AMSK_ON command sets the auto-mask UVLF and UVHF interrupts for ACT/SHDN = 0 to 1 transitions.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Sets the auto-mask for ACT/SHDN = 0 to 1 transitions for IEN_UVLF and IEN_UVHF for V_{IN} channels 1–6. 0: Channel interrupts are not auto-masked 1: Channel interrupts auto-masked

AMSK_OFF (0xA2) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The AMSK_OFF command sets the auto-mask UVLF and UVHF interrupts for ACT/SHDN = 1 to 0 transitions.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Sets the auto-mask for ACT/SHDN = 1 to 0 transitions for IEN_UVLF and IEN_UVHF for V_{IN} channels 1–6. 0: Channel interrupts are not auto-masked 1: Channel interrupts auto-masked

AMSK_EXS (0xA3) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The AMSK_EXS command sets the auto-mask UVLF and UVHF interrupts for ACT/SLP = 0 to 1 transitions.

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Sets the auto-mask for ACT/SLP = 0 to 1 transitions for IEN_UVLF and IEN_UVHF for V_{IN} channels 1–6. 0: Channel interrupts are not auto-masked 1: Channel interrupts auto-masked If certain rails are in the on sequence, they do not turn off when entering sleep mode, or become non-sleep channels. AMSK_ENS and AMSK_EXS should be set to 0 to continue monitoring UVHF and UVLF in sleep mode.

AMSK_ENS (0xA4) – Bank 1

Access: Read/write. Read-only if the IEN group is protected.

POR: Load from the OTP

The AMSK_ENS command sets the auto-mask UVLF, UVHF, and OVHF interrupts for ACT/SLP = 1 to 0 transitions.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	VIN[x]	Sets the auto-mask for ACT/SLP = 1 to 0 transitions for IEN_UVLF and IEN_UVHF for V_{IN} channels 1–6. 0: Channel interrupts are not auto-masked 1: Channel interrupts auto-masked If certain rails are in the on sequence, they do not turn off when entering sleep mode, or become non-sleep channels. AMSK_ENS and AMSK_EXS should be set to 0 to continue monitoring UVHF and UVLF in sleep mode.

SEQ_TOUT 0xA5 (MSB), 0xA6 (LSB) – Bank 1

Access: Read/write. Read-only if the SEQ group is protected.

POR: Load from the OTP

The SEQ_TOUT command sets the sequence timeout.

Bits	Field Name	Description
D[15:0]	MILLISECOND [15:0]	Sets the ACT/SHDN and ACT/SLP transition sequence timeout. After the timeout, the auto-masks (AMSK_xxx) are released and the IEN_xVxF interrupts become active. 0x0000: 1ms 0x0001: 2ms … While the maximum value is not specified, it is recommended to be able to set this timeout up to 4s, and at least 256ms (using only the lower byte at address 0xA6). SEQ_TOUT should be set to a value greater that at which the last rail's DC voltage reaches UVLF threshold or OFF threshold according to the configuration. There is a 16-bits timestamp for each channel. The maximum recordable timestamp is 2^{16} x 50µs = 3.2768s, so it is recommended to set SEQ_TOUT under 3.2768s.

SEQ_SYNC (0xA7) – Bank 1

Access: Read/write. Read-only if the SEQ group is protected.

POR: Load from the OTP

The SEQ_SYNC command sets the sequence SYNC pulse duration.

Bits	Name	Description
D[7:0]	PULSE_WIDTH[7:0]	Sets the pulse width for the SYNC synchronization pulse. 00000000b: 50µs 00000001b: 60µs 00000010b: 70µs … 11111101b: 2580µs 11111110b: 2590µs 11111111b: 2600µs

SEQ_UP_THLD (0xA8) – Bank 1

Access: Read/Write. Read-only if the SEQ group is protected.

POR: Load from the OTP

The SEQ_UP_THLD command selects the threshold for up sequence tagging (0 to 1 transitions for ACT/SHDN and ACT/SLP).

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	OFF_UV[x]	Selects the OFF (200mV) or UV (UV_LF[x] register) threshold for power on and sleep exit sequence tagging. 0: Use the OFF threshold (200mV) 1: Use the UV threshold (UV_LF[x] register)

SEQ_DN_THLD (0xA9) – Bank 1

Access: Read/write. Read-only if the SEQ group is protected.

POR: Load from the OTP

The SEQ_DN_THLD command selects the threshold for down sequence tagging (1 to 0 transitions for ACT/SHDN and ACT/SLP).

Bits	Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	OFF_UV[x]	Selects the OFF (200mV) or UV (UV_LF[x] register) threshold for power off and enter sleep sequence tagging. 0: Use the OFF threshold (200mV) 1: Use the UV threshold (UV_LF[x] register)

SEQ_ON_EXP[x] (0xB0~0xB5) – Bank 1

Access: Read/write. Read-only if the SEQ group is protected.

POR: 0x00

The SEQ_ON_EXP[x] command sets the channel's expected power on sequence order (ACT/SHDN = 0 to 1).

Bits	Field Name	Description
D[7:0]	ORDER[7:0]	Sets the expected power on sequence order value for the respective channel. This sequence order value is compared to the channel's SEQ_ON_LOG[x] register when the sequence is triggered by ACT/SHDN.

SEQ_OFF_EXP[x] (0xC0~0xC5) – Bank 1

Access: Read/write. Read-only if the SEQ group is protected.

POR: 0x00

The SEQ_OFF_EXP[x] command sets the channel's expected power off sequence order (ACT/SHDN = 1 to 0).

Bits	Name	Description
D[7:0]	ORDER[7:0]	Sets the expected power off sequence order value for the respective channel. This sequence order value is compared to the channel's SEQ_OFF_LOG[x] register when the sequence is triggered by ACT/SHDN.

SEQ_EXS_EXP[x] (0xD0~0xD5) – Bank 1

Access: Read/write. Read-only if the SEQ group is protected.

POR: 0x00

The SEQ_EXS_EXP[x] command sets the channel's expected sleep exit sequence order (ACT/SLP = 0 to 1).

Bits	Name	Description
D[7:0]	ORDER[7:0]	Sets the expected sleep exit sequence order value for the respective channel. This sequence order value is compared to the channel's SEQ_EXS_LOG[x] register when the sequence is triggered by ACT/SLP.

SEQ_ENS_EXP[x] (0xE0~0xE5) – Bank 1

Access: Read/write. Read-only if the SEQ group is protected.

POR: 0x00

The SEQ_ENS_EXP[x] command sets the channel's expected sleep entry sequence order (ACT/SLP = 1 to 0).

Bits	Field Name	Description
D[7:0]	ORDER[7:0]	Sets the expected sleep entry sequence order value for the respective channel. This sequence order value is compared to the channel's SEQ_ENS_LOG[x] register when the sequence is triggered by ACT/SLP.

BANK_SEL (0xF0) – Bank Independent

Access: Read/write

POR: 0x00

The BANK_SEL command selects the register bank.

Bits	Field Name	Description
D[7:1]	RSVD	Reserved.
D[0]	BANK	Selects the register bank number. Only bank 0 or 1 can be selected.

PROT1 (0xF1) and PROT2 (0xF2) – Bank Independent

Access: Read/write

POR: 0x00

The PROT1 and PROT2 commands selects protections. To write-protect a register group, the host must set the relevant bit in both registers. For security, these registers must have a POR value = 0x00. They become read-only once they are set, until power is cycled. Once any bit is set to 1, it cannot be cleared to 0 by the host. It can only be cleared (and allow writing to different configuration registers) by executing one of the following:

- Cycling power on the device
- Initiate a reset through the VMON_CTL register
- Execute BIST executed when exiting the off sequence (if AT_SHDN = 1)

RESET is in the WRKC group. If WEKC is protected, the only way to clear the protection is to cycle the power on the MPQ79500FS or execute BIST while exiting the off sequence (if AT_SHDN = 1).

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[5]	WRKC	0: The control working (WRKC) registers are writeable 1: Writes to the WRKC registers are ignored
D[4]	WRKS	0: The sequence working (WRKS) registers are writeable 1: Writes to the WRKS registers are ignored
D[3]	CFG	0: The configuration (CFG) registers are writeable 1: Writes to the CFG registers are ignored
D[2]	IEN	0: The interrupt enable (IEN) registers are writeable 1: Writes to the IEN registers are ignored
D[1]	MON	0: The monitor (MON[x]) registers are writeable 1: Writes to the monitor registers selected in the PROT_MON1 register are ignored
D[0]	SEQ	0: The sequence (SEQ) registers are writeable 1: Writes to the SEQ registers are ignored

PROT_MON1 (0xF3) – Bank Independent

Access: Read/write. Read-only if the MON group is protected.

POR: Load from the OTP

The PROT_MON1 command sets the configuration protections of monitored channels.

Bits	Field Name	Description
D[7:6]	RSVD	Reserved.
D[x - 1] (where x = 1–6)	MON[N]	Selects the monitor channels configurations that are protected once the PROT1 and PROT2 registers are written to protect the MON group. 0: The monitor configuration registers for the respective channel are writeable 1: Writes to the monitor configuration registers for are ignored for the respective channel

I2CADDR (0xF9) – Bank Independent

Access: Read-only

POR: From the strap and OTP

The I2CADDR command sets the I^2C address.

Bits	Field Name	Description
D[7]	RSVD	Reserved.
D[6:3]	ADDR_NVM[3:0]	Sets the I^2C address for the four most significant bits (MSB). Set in the NVM (default = 0110b).
D[2:0]	ADDR_STRAP[2:0]	Sets the I^2C address for the three least significant bits (LSB). Set by the strap level detected on the ADDR pin (from 000b to 111b under different resistors).

DEV_CFG (0xFA) – Bank Independent

Access: Read-only

POR: Load from the OTP

The PROT_MON1 command configures some device options.

Bits	Name	Description
D[7:1]	RSVD	Reserved.
D[0]	SOC_IF	Sets the host SoC interface (including I^2C, ACT/SHDN, ACT/SLP, and SYNC). 0: 3.3V 1: 1.2V/1.8V Although SYNC is not currently a SoC interface signal, it is included for consistency across interface and control signals.

APPLICATION INFORMATION

Figure 29 shows a typical application circuit for the MPQ79500FS.

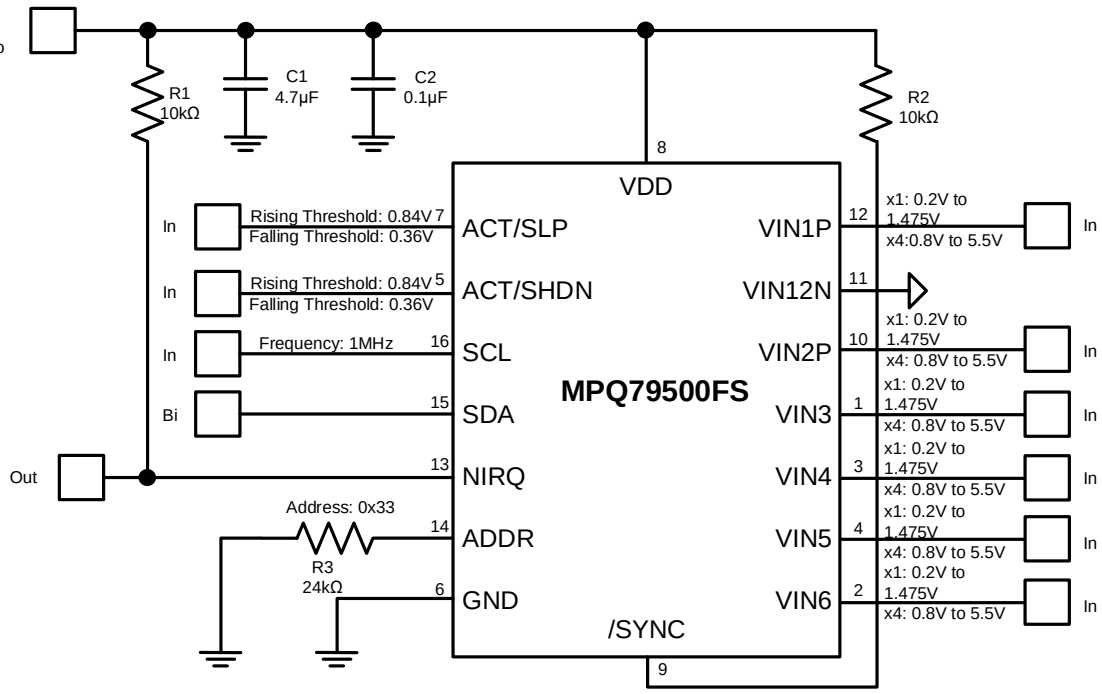


Figure 29: Typical Application Circuit of a Single MPQ79500FS

Table 13: Design Guide Index

Pin No.	Pin Name	Component	Design Guide Index
1, 2, 3, 4	VIN3, VIN6, VIN4, VIN5	-	Connecting to the Monitored Voltage (VIN3, Pin 1; VIN6, Pin 2; VIN4, Pin 3; VIN5, Pin 4)
5	ACT/SHDN	-	ACT/SHDN and ACT/SLP Input Control (ACT/SHDN, Pin 5; ACT/SLP, Pin 7)
6	GND	-	Setting the GND Connection (GND, Pin 6)
7	ACT/SLP	-	ACT/SHDN and ACT/SLP Input Control (ACT/SHDN, Pin 5; ACT/SLP, Pin 7)
8	VDD	C1, C2	Selecting the Input Capacitors (VDD, Pin 8)
9	SYNC	R2	Setting the Internal or External Pull-Up (/SYNC, Pin 9)
10, 12	VIN2P, VIN1P	-	Connecting to the Monitored Voltage (VIN2P, Pin 10; VIN1P, Pin 12)
11	VIN12N	-	Connecting to the Monitored Voltage (VIN12N, Pin 11)
13	NIRQ	R1	Setting the Active-Low Signal (NIRQ, Pin 13)
14	ADDR	R3	Selecting the Resistor to GND (ADDR, Pin 14)
15	SDA	-	Setting the I^2C Interface (SDA, Pin 15; SCL, Pin 16)
16	SCL	-	

Connecting to the Monitored Voltage (VIN3, Pin 1; VIN6, Pin 2; VIN4, Pin 3; VIN5, Pin 4)

VIN3, VIN6, VIN4, and VIN 5 are four single-ended monitor inputs. It is recommended to connect these input pins directly to the monitored voltage to ensure ADC accuracy.

Two kinds of scaling can be selected for the monitor input. When a channel is set for 1x scaling, the monitored voltage range is between 0.2V and 1.475V. When a channel is set for 4x scaling, the monitored voltage range is between 0.8V and 5.5V. The ADC is only guaranteed to work within this range, and a channel with 1x scaling cannot be forced to operate at 4x scaling voltages. Note that OV/UV monitoring

continues to work even when a voltage is beyond its range.

For the channel set for 1x scaling via the OTP, its voltage must be below V_{DD}. Connect the VINx pin to GND if it is not used.

For voltages in the LF margin, a 2LSB offset may be implemented, and it may cause UVLF and OVLF to be falsely triggered. In this scenario, the recommended voltage ranges are between 0.215V and 1.46V for 1x scaling, and 0.86V and 5.5V for 4x scaling.

ACT/SHDN and ACT/SLP Input Control (ACT/SHDN, Pin 5; ACT/SLP, Pin 7)

The ACT/SLP and ACT/SHDN pins are digital control pins. Both ACT/SHDN and ACT/SLP do not require an external pull-up resistor to be connected to the signal source. The signal source voltage level can be either above or below V_{DD}.

ACT/SHDN or ACT/SLP can also be connected to a voltage source through an external pull-up resistor. An internal 100kΩ resistor is separately connected from ACT/SHDN and ACT/SLP to GND. ACT/SHDN and ACT/SLP are pulled low when they are floating.

Setting the GND Connection (GND, Pin 6)

See the PCB Layout Guidelines section on page 89 for more details.

Selecting the Input Capacitors (VDD, Pin 8)

For VDD, it is required to use 4.7µF and 100nF input capacitors. Higher input voltages may require a 10µF (or greater) capacitor. Place the capacitor as close as possible to the VDD pin. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their small temperature coefficients.

Setting the Internal or External Pull-Up (/SYNC, Pin 9)

Float the /SYNC pin or connect it to VDD with a pull-up resistor. A minimum 10kΩ pull-up is recommended to ensure that V_{OL} does not exceed 0.1V. The /SYNC pin cannot be pulled up to an external voltage with a level that is different from V_{DD}.

For multiple IC sequence functions, the /SYNC pins should be connected together. Route the /SYNC pin away from the PCB trace or solder pads with a large voltage jump.

Connecting to the Monitored Voltage (VIN2P, Pin 10; VIN1P, Pin 12)

VIN1P and VIN2P are two differential monitor inputs. Connect these pins directly to the monitored voltage. When a channel is set for 1x scaling, the monitored voltage range is between 0.2V and 1.475V. When a channel is set for 4x scaling, the monitored voltage range is between 0.8V and 5.5V.

The ADC is only guaranteed to work within this range, and a channel with 1x scaling cannot be forced to operate at 4x scaling voltages. Note that OV/UV monitoring continues to work even when a voltage is beyond its range.

For the channel set for 1x scaling via the OTP, its voltage must be below V_{DD}.

For voltages in the min/max LF margin, a 2LSB offset may be implemented, and it may cause UVLF and OVLF to be falsely triggered. In this scenario, the recommended voltage ranges are between 0.215V and 1.46V for 1x scaling, and 0.86V and 5.5V for 4x scaling.

The positive terminal of the differential input pin (VIN1P or VIN2P) cannot be lower than the negative terminal (VIN12N).

Connect this pin to GND if it is not used.

Connecting to the Monitored Voltage (VIN12N, Pin 11)

For high-current applications, the VIN12N pin's voltage cannot exceed 0.05V. Do not float this pin. If there is no remote voltage sensing, connect this pin to GND with short, direct, and wide traces. Then the VIN1P and VIN2P pins work similar to the single-ended input pins.

Setting the Active-Low Signal (NIRQ, Pin 13)

NIRQ is an active-low signal. Any interrupts in INT_SRC register pull down the NIRQ pin's signal. Connect this pin to an external power supply (or VDD) with a pull-up resistor. A minimum 10kΩ pull-up is recommended to ensure that V_{OL} does not exceed 0.1V. Route the NIRQ pin away from the PCB trace or solder pads with a large voltage jump.

Selecting the Resistor to GND (ADDR, Pin 14)

Table 14 on page 88 shows the I^2C addresses, which can be selected with different resistor

values. It is recommended to use a resistor with 1% accuracy.

Table 14: I²C Addresses

Resistor	Address (Bits)						
	6	5	4	3	2	1	0
0Ω to GND	Load from the OTP				0	0	0
8.06kΩ to GND	Load from the OTP				0	0	1
16kΩ to GND	Load from the OTP				0	1	0
24kΩ to GND	Load from the OTP				0	1	1
32.4kΩ to GND	Load from the OTP				1	0	0
40.2kΩ to GND	Load from the OTP				1	0	1
47.5kΩ to GND	Load from the OTP				1	1	0
0Ω to VDD	Load from the OTP				1	1	1

The MPQ79500FS provides an OTP function to set custom default parameters.

MPS provides a graphic user interface (GUI) and I²C tool to configure the MPQ79500FS during the development process. To configure the device in application, contact an MPS FAE for more details.

Setting the I²C Interface (SDA, Pin 15; SCL, Pin 16)

The MPQ79500FS works as a slave-only device. It supports up to 1Mbs of bidirectional data transfer in fast-mode plus, which adds flexibility to the power sequencer application and provides advanced diagnoses. See the I²C Interface section on page 50 for more details.

If the I²C interface is not used, it is recommended to connect these pins to the VDD pin through a resistor (e.g. 100kΩ).

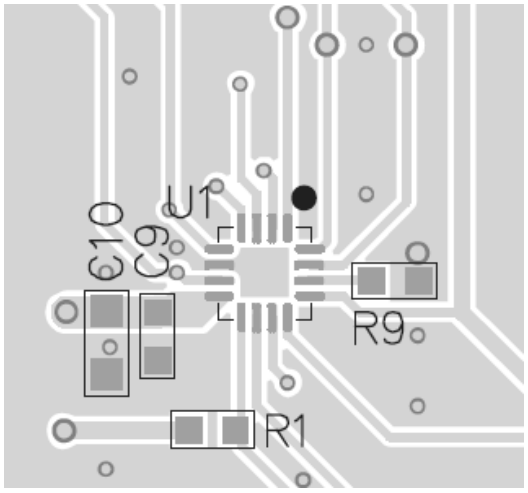
PCB Layout Guidelines (11)

Efficient PCB layout (especially for the input capacitor placement) is critical for stable operation. A 4-layer layout is recommended. For the best results, refer to Figure 30 and follow the guidelines below:

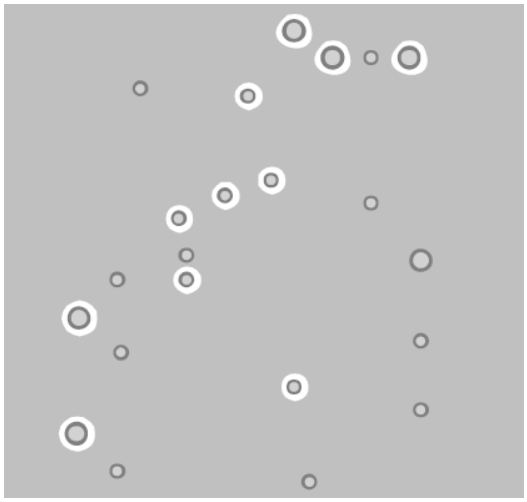
1. Place the ceramic input capacitors, especially the small package size (0603) bypass capacitor, as close to the VDD and GND pins as possible to minimize high-frequency noise.
2. Connect the GND pin to GND with short, direct, and wide traces. Use a large ground plane to connect directly to GND.
3. If the bottom layer is a ground plane, add vias near GND.
4. Ensure that the VINx pin has direct and short traces that are routed away from the high-frequency paths and paths with a large voltage jump.
5. Route the SYNC and NIRQ pin away from the high-frequency paths and paths with a large voltage jump.
6. Use multiple vias to connect the power planes to the internal layers.

Notes:

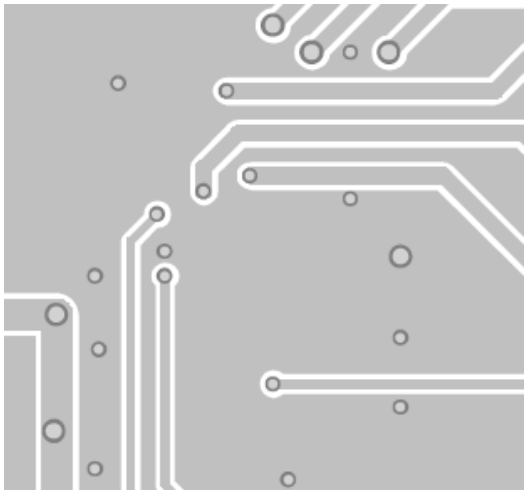
11) The recommended PCB layout is based on the typical application circuit (see Figure 31 on page 90).



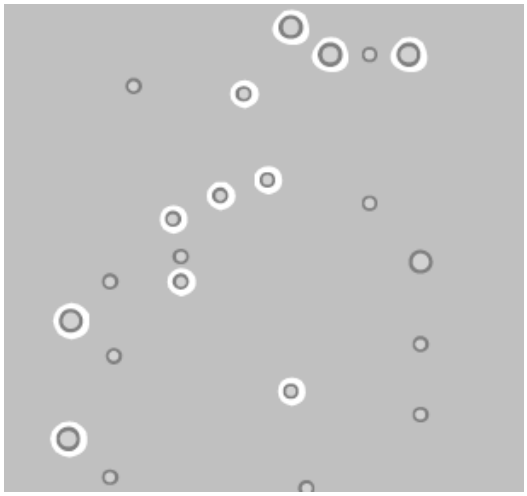
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 30: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

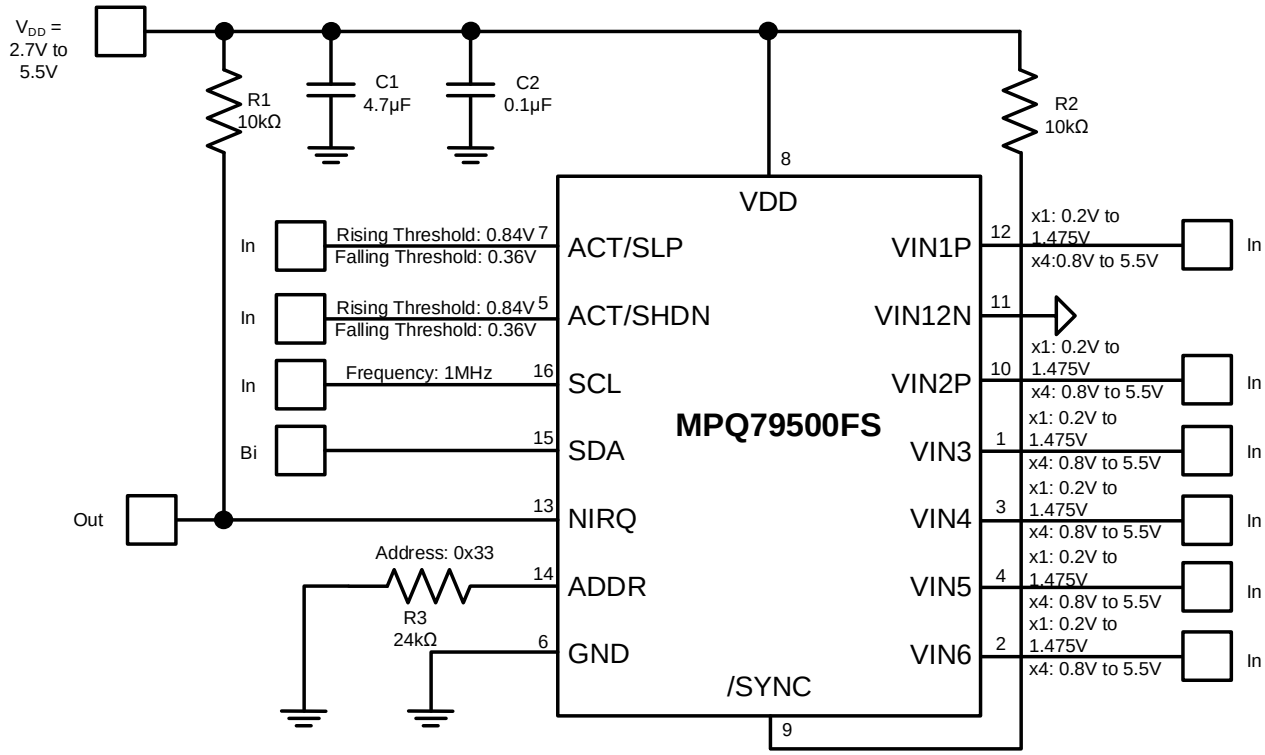


Figure 31: Typical Application Circuit of a Single MPQ79500FS

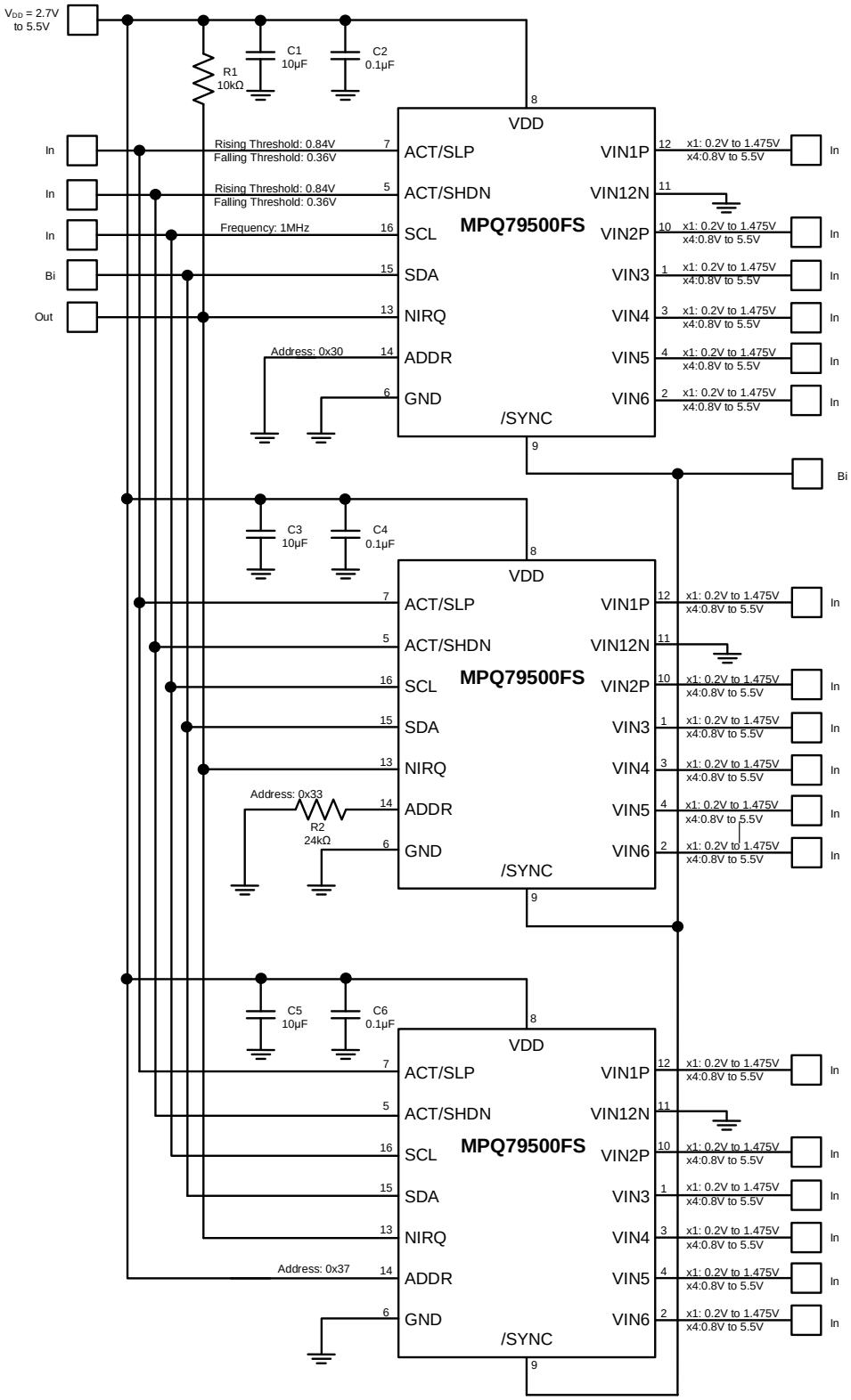


Figure 32: Typical Application Circuit of Three MPQ79500FS Devices

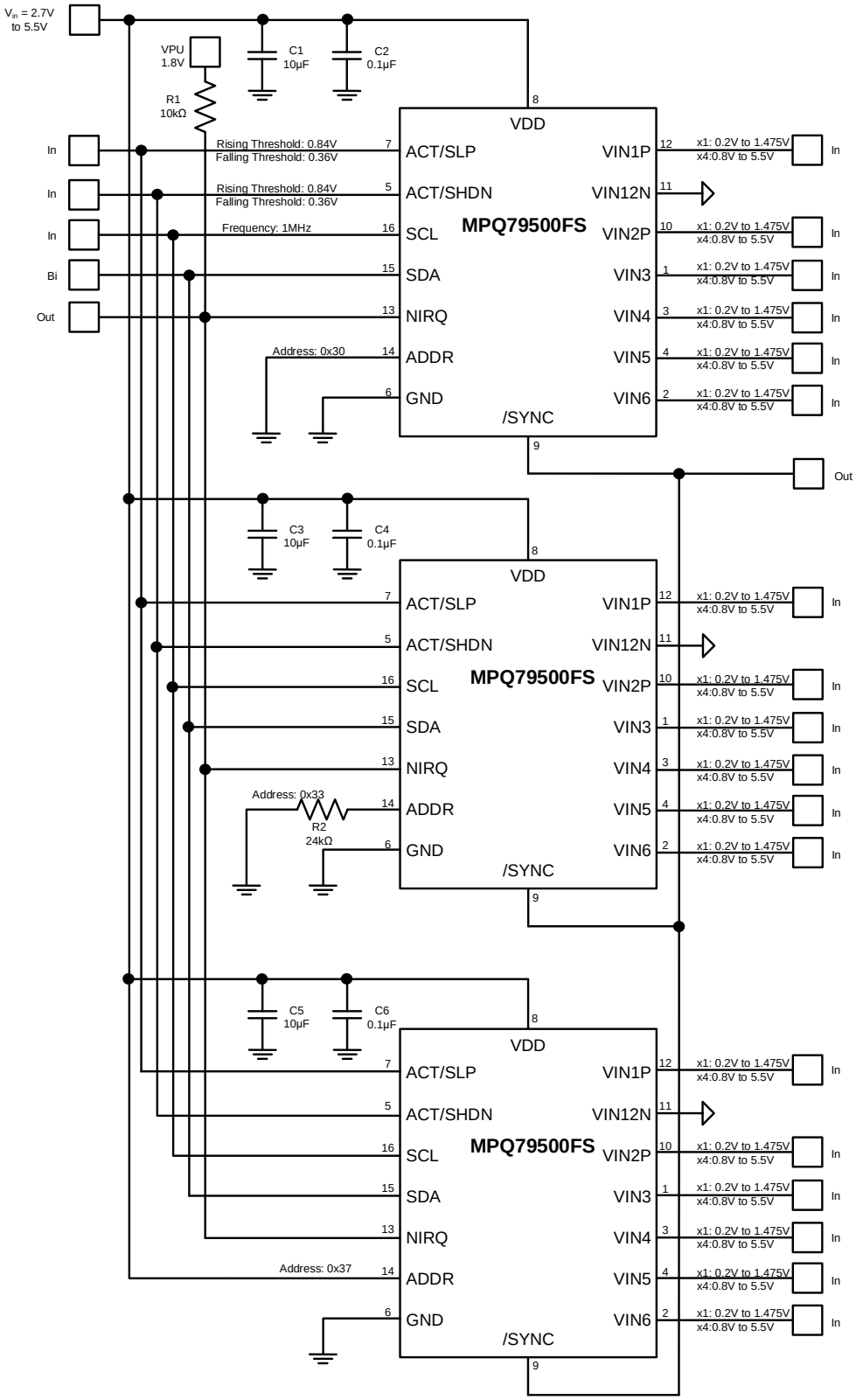
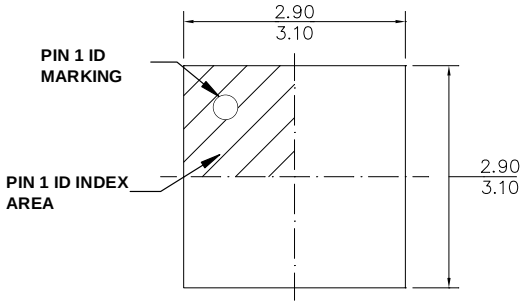


Figure 33: Three MPQ79500FS Devices (NIRQ Powered by External Source)

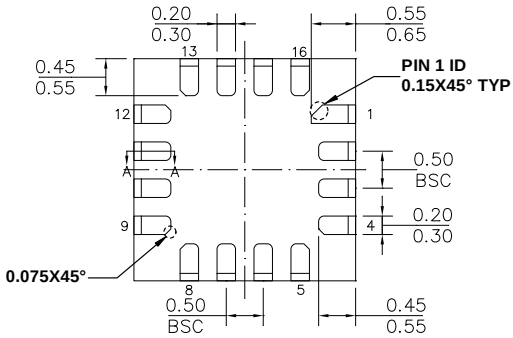
PACKAGE INFORMATION

QFN-16 (3mmx3mm)

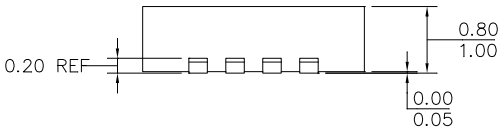
Wettable Flank



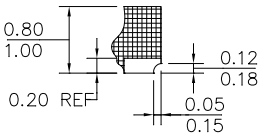
TOP VIEW



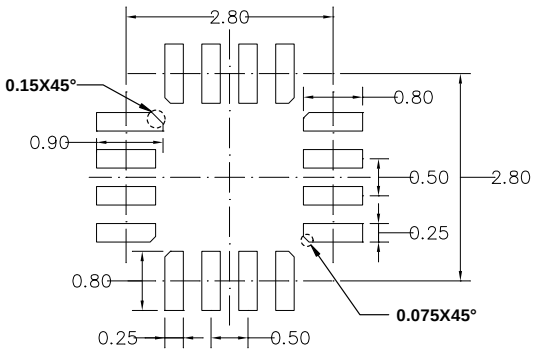
BOTTOM VIEW



SIDE VIEW



SECTION A-A

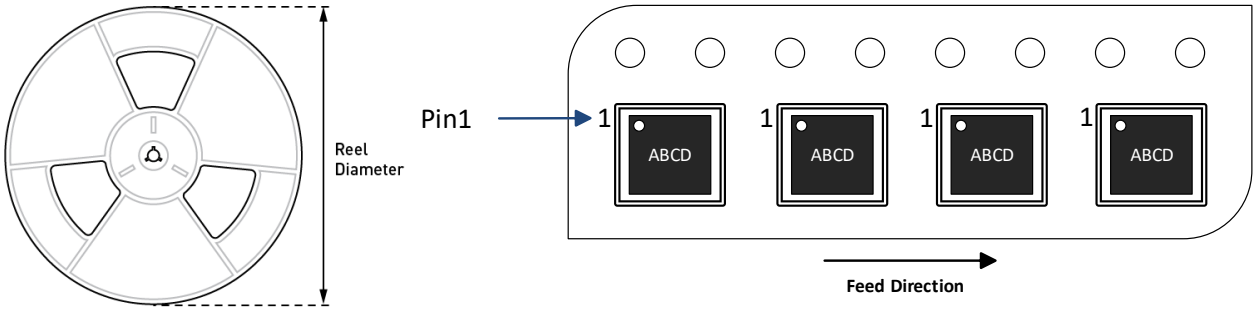


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ79500FSGQE-xxxx-AEC1-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/10/2022	Initial Release	-