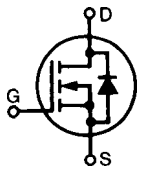
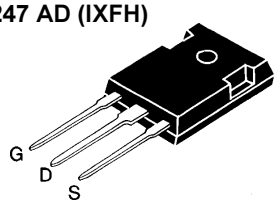
HiPerFET™ Power MOSFETs

N-Channel Enhancement Mode
High dv/dt, Low t_{rr}, HDMOS™ Family

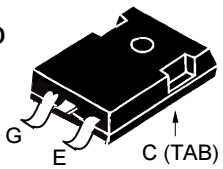
	V_{DSS}	I_{D25}	$R_{DS(on)}$	t_{rr}
IXFH/IXFM35N30	300 V	35 A	100mΩ	200 ns
IXFH40N30	300 V	40 A	85mΩ	200 ns
IXFM40N30	300 V	40 A	88mΩ	200 ns



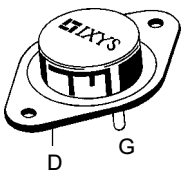
TO-247 AD (IXFH)



TO-247 SMD
("S" Suffix)
(Note 1)



TO-204 AE (IXFM)



G = Gate, D = Drain,
S = Source, TAB = Drain

Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		300	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		300	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	35N30	35	A
		40N30	40	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	35N30	140	A
		40N30	160	A
I_{AR}	T_C = 25°C	35N30	35	A
		40N30	40	A
E_{AR}	T_C = 25°C		30	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		300	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
M_d	Mounting torque		1.13/10	Nm/lb.in.
Weight			TO-204 = 18 g, TO-247 = 6 g	
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s			300	°C

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)		Characteristic Values min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 μA		300			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA		2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$	T_J = 25°C			200	μA
	V_{GS} = 0 V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5\ I_{D25}$	35N30			0.100	Ω
		FH40N30			0.085	Ω
		FM40N30			0.088	Ω
	Pulse test, t ≤ 300 μs, duty cycle δ ≤ 2 %					

Features
- International standard packages
- Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic Rectifier

Applications
- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls
- Low voltage relays

Advantages
- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- Space savings
- High power density

91523E (10/95)

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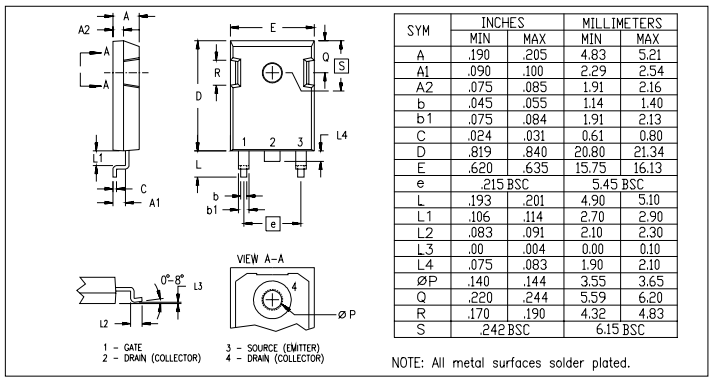
Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 I_{D25}, pulse test	22	25		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4800		pF
C_{oss}			745		pF
C_{rss}			280		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 I_{D25} R_G = 2 Ω (External)		20	30	ns
t_r			60	90	ns
$t_{d(off)}$			75	100	ns
t_f			45	90	ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 I_{D25}		177	200	nC
Q_{gs}			28	50	nC
Q_{gd}			78	105	nC
R_{thJC}				0.42	K/W
R_{thCK}			0.25		K/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)		min.	typ.	max.	
I_S	V_{GS} = 0	35N30			35	A
		40N30			40	A
I_{SM}	Repetitive; pulse width limited by T_{JM}	35N30			140	A
		40N30			160	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle δ ≤ 2 %				1.5	V
t_{rr}	I_F = I_S, -di/dt = 100 A/μs, V_R = 100 V	T_J = 25°C			200	ns
		T_J = 125°C			350	ns

Note 1: Add "S" suffix for TO-247 SMD PACKAGE OPTION (EX: IXFH40N30S)

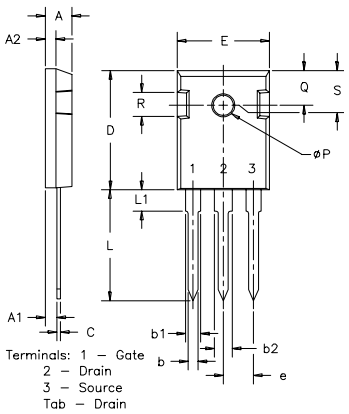
TO-247 SMD Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.193	.201	4.90	5.10
L1	.106	.114	2.70	2.90
L2	.083	.091	2.10	2.30
L3	.00	.004	0.00	0.10
L4	.075	.083	1.90	2.10
ØP	.140	.144	3.55	3.65
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.242 BSC		6.15 BSC	

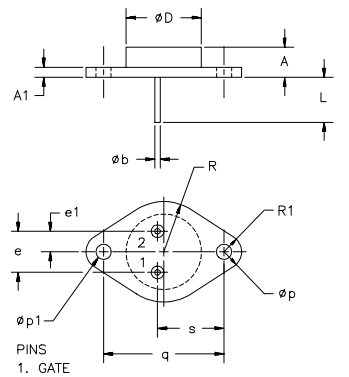
NOTE: All metal surfaces solder plated.

TO-247 AD (IXFH) Outline



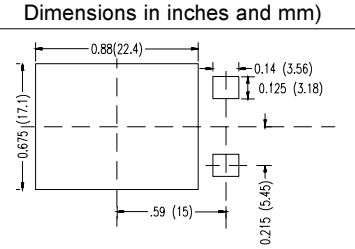
SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.7	5.3
A1	.087	.102	2.2	2.54
A2	.059	.098	2.2	2.6
b	.040	.055	1.0	1.4
b1	.065	.084	1.65	2.13
b2	.113	.123	2.87	3.12
C	.016	.031	.4	.8
D	.819	.845	20.80	21.46
E	.610	.640	15.75	16.26
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1		.177		4.50
ØP	.140	.144	3.55	3.65
Q	.212	.244	5.4	6.2
R	.170	.216	4.32	5.49
S	.242 BSC		6.15 BSC	

TO-204AE (IXFM) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.250	.450	6.4	11.4
A1	.060	.135	1.53	3.42
Øb	.057	.063	1.45	1.60
ØD		.875		22.22
e	.420	.440	10.67	11.17
e1	.205	.225	5.21	5.71
L	.440	.480	11.18	12.19
Øp	.151	.165	3.84	4.19
Øp1	.151	.165	3.84	4.19
q	1.187 BSC		30.15 BSC	
R	.495	.525	12.58	13.33
R1	.131	.188	3.33	4.77
s	.655	.675	16.64	17.14

Min. Recommended Footprint
Dimensions in inches and mm)



IXYS reserves the right to change limits, test conditions, and dimensions.

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Fig.1. Output Characteristics

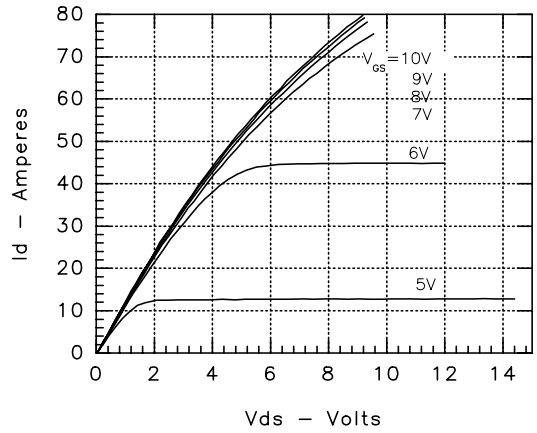

Fig. 2. Input Admittance

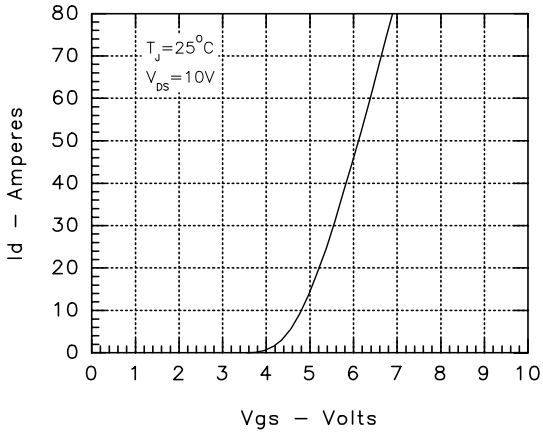

Fig. 3. Rds(on) vs. Drain Current

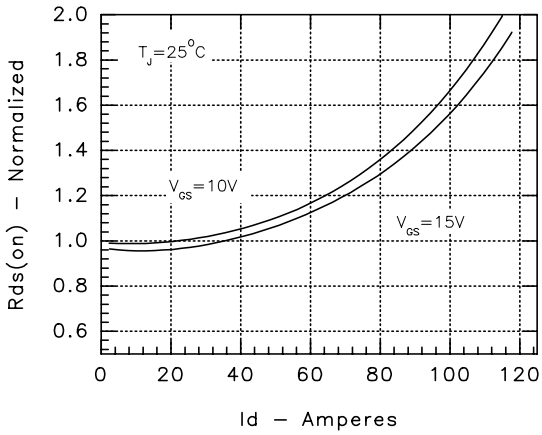

Fig. 4. Temperature Dependence of Drain to Source Resistance

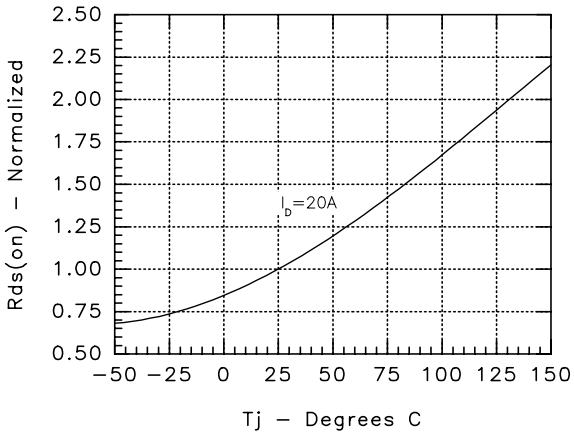

Fig. 5. Drain Current vs. Case Temperature

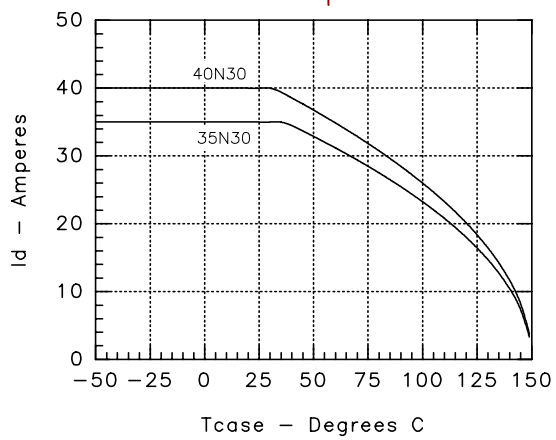

Fig. 6. Temperature Dependence of Breakdown Voltage and Threshold Voltage

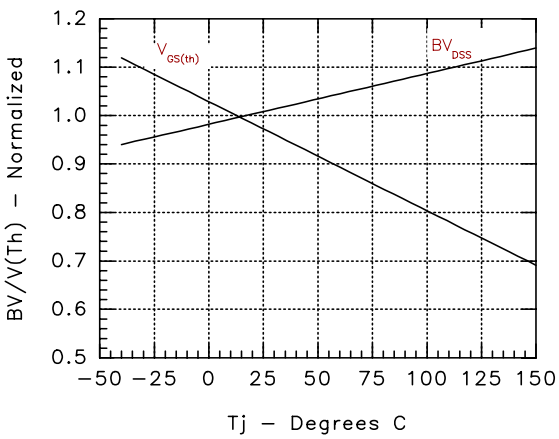

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Fig. 7. Gate Charge

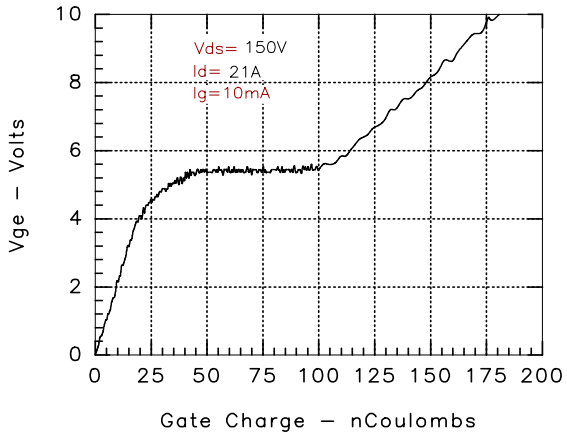


Fig. 8. Forward Bias Safe Operating Area

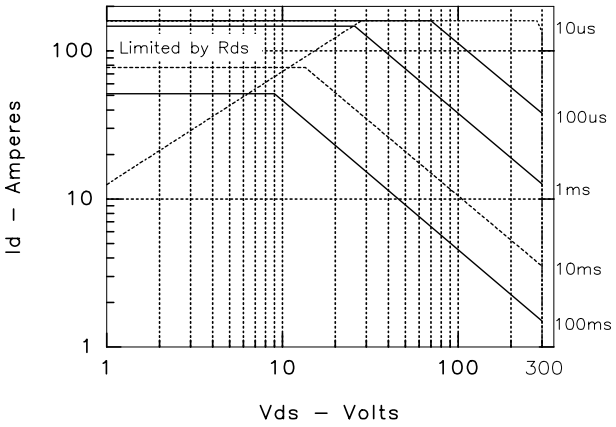


Fig. 9. Capacitance Curves

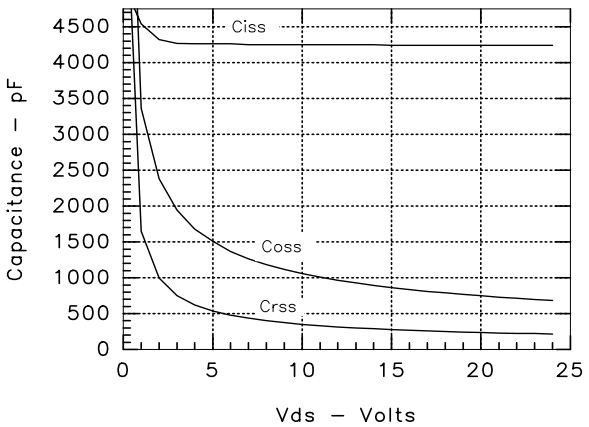


Fig. 10. Source Current vs. Source to Drain Voltage

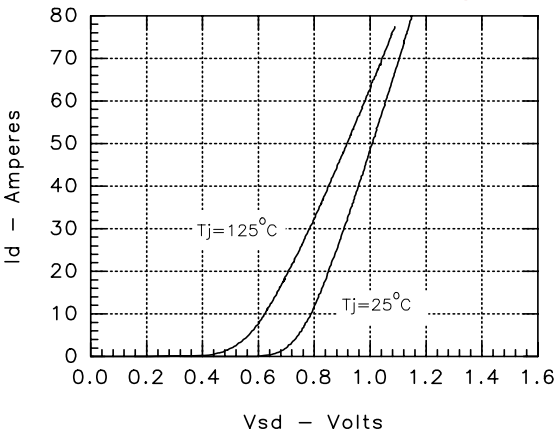
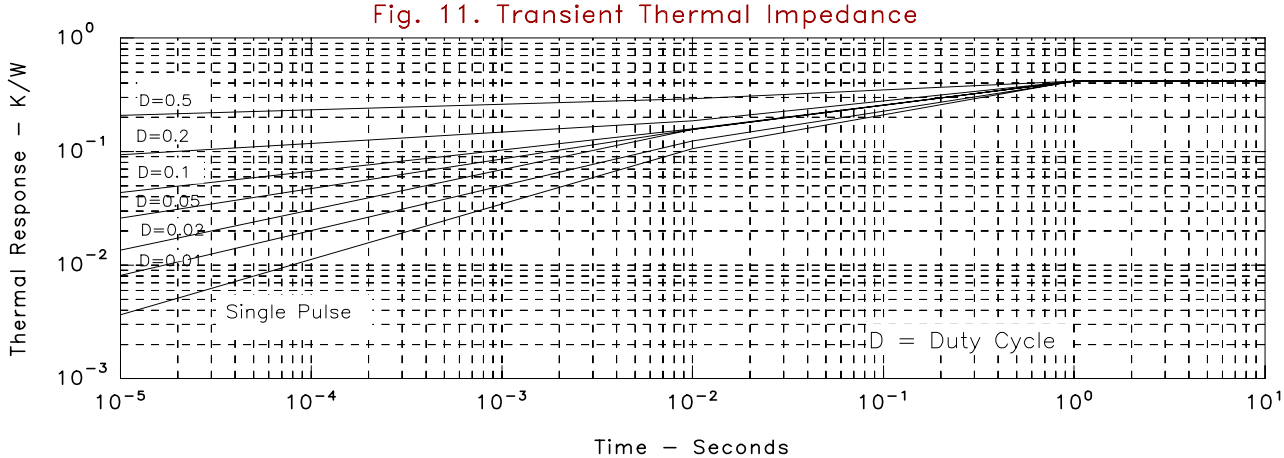


Fig. 11. Transient Thermal Impedance



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