Product Specification TYPE NUMBER : M T M 9 8 2 4 0 0 B B F *1	Prepared by S.Miyata	Checked by M.Fujisawa	Applied by K.Hagi	Established by H. Shidouka

Type	Silicon Field Effect Transistors		
Application	Switching		
Structure	N-Channel MOS Type		
Outline	SO8-F1-B	Marking	CA

Absolute Maximum Ratings	VDSS	VGSS	ID	IDp	PD*2	Tch	Tstg
	40	±20	7	28	2	150	-55 to +150
	(V)	(V)	(A)	(A)	(W)	(°C)	(°C)

Electrical characteristics (Ta = 25 °C ±3 °C)

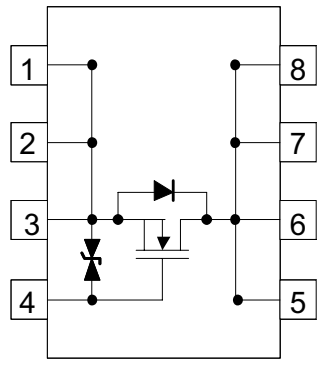
Item	Symbol	Measuring condition	Limit min.	Limit typ.	Limit max.	Unit
Drain-Source Voltage	VDSS	ID = 1mA, VGS = 0V	40			V
Drain-Source Cutoff Current	IDSS	VDS = 40V, VGS = 0V			10	μA
Gate-Source Cutoff Current	IGSS	VGS = ±16V, VDS = 0V			±10	μA
Gate Threshold Voltage	Vth	ID = 1.0mA, VDS = 10.0V	1.0		2.5	V
Drain Resistance (ON) *3	RDS(ON)	ID = 7A, VGS = 10V		16	23	mΩ
Drain Resistance (ON) *3	RDS(ON)	ID = 3.5A, VGS = 5.0V		29	40	mΩ
Forward Transfer Admittance *3	|Yfs|	ID = 7A, VDS = 10V	4			S
Small-Signal Short-Circuit Imput Capacitance	Ciss	VDS = 10V, VGS = 0V, f = 1MHz		1750		pF
Small-Signal Short-Circuit Output Capacitance	Coss	VDS = 10V, VGS = 0V, f = 1MHz		150		pF
Small-Signal Reverse Transfer Capacitance	Crss	VDS = 10V, VGS = 0V, f = 1MHz		90		pF
Turn-on Delay Time *3,4	td(on)	VDD = 25V, VGS = 0 to 10V, ID = 3.5A		17		ns
Rise Time *3,4	tr	VDD = 25V, VGS = 0 to 10V, ID = 3.5A		9		ns
Turn-off Delay Time *3,4	td(off)	VDD = 25V, VGS = 10 to 0V, ID = 3.5A		94		ns
Fall Time *3,4	tf	VDD = 25V, VGS = 10 to 0V, ID = 3.5A		33		ns

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Packing
Embossed type (thermo-compressioon sealing)
*2 Measuring on ceramic board at 50×50×1.0mm.
*3 Pulse test
*4 See test circuit

Internally connected circuit

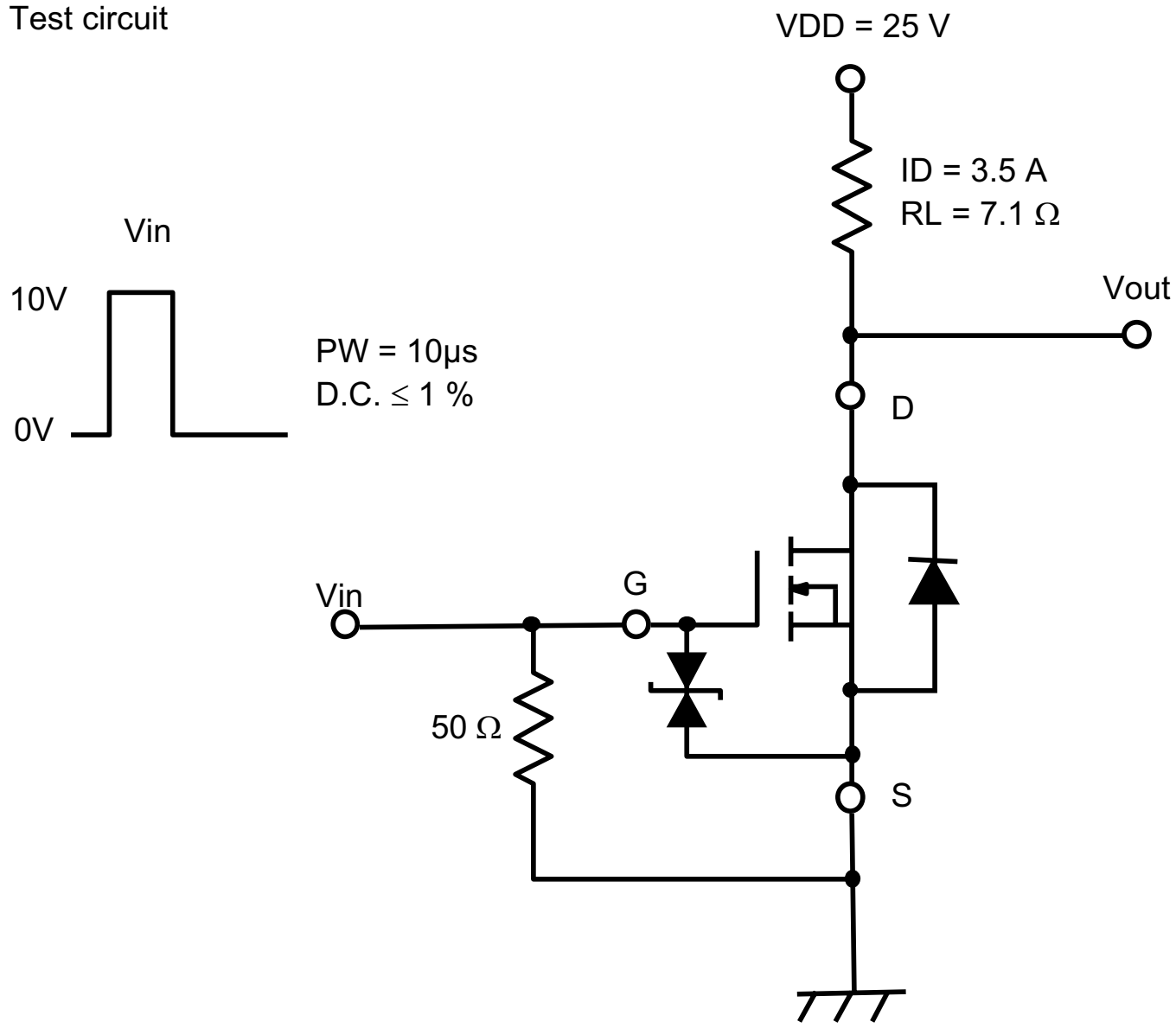
1.Source
2.Source
3.Source
4.Gate
5.Drain
6.Drain
7.Drain
8.Drain



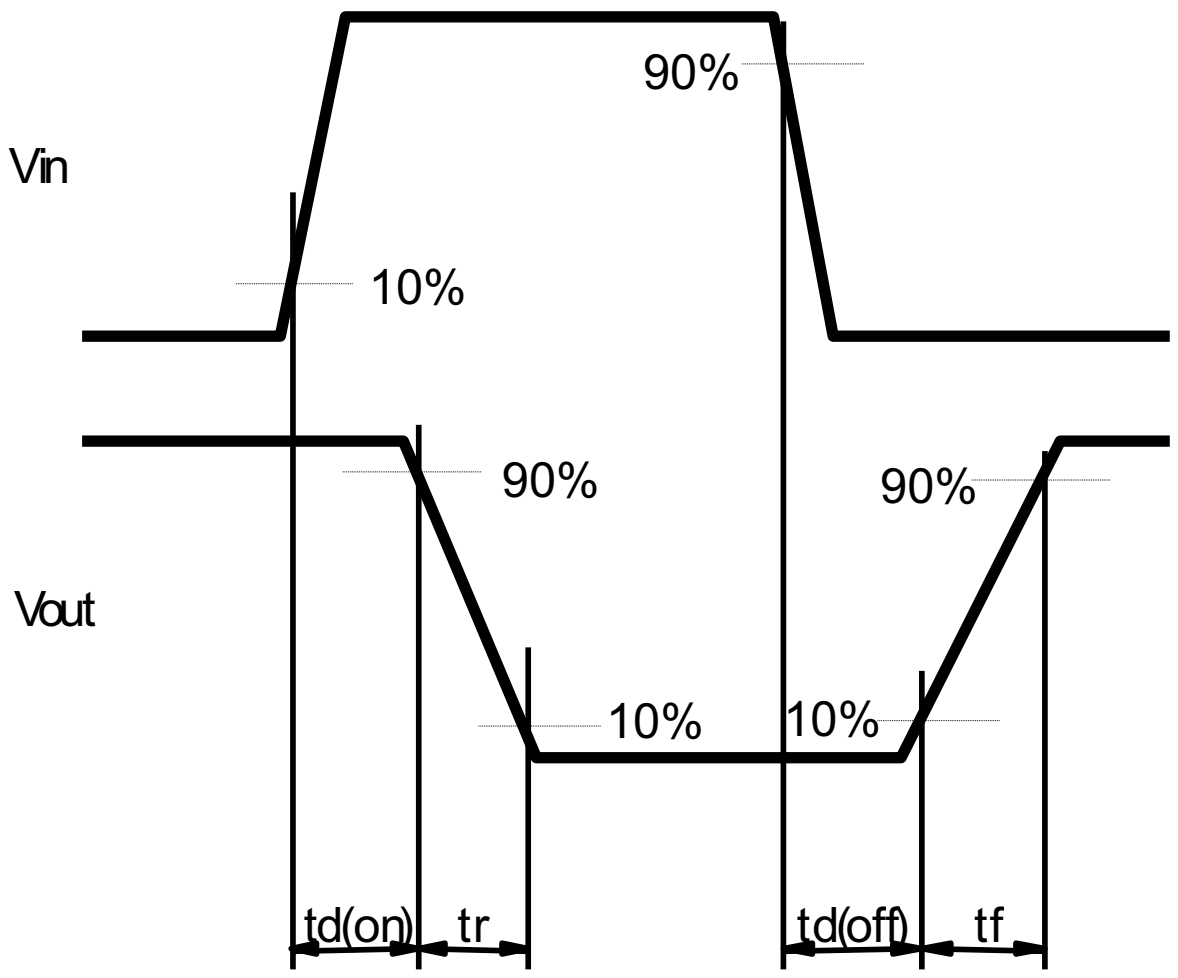
2009.4.27	
Established	Revised

Product Specification Type Number : M T M 9 8 2 4 0 0 B B F *1	

Test circuit



PW = 10μs
D.C. ≤ 1 %

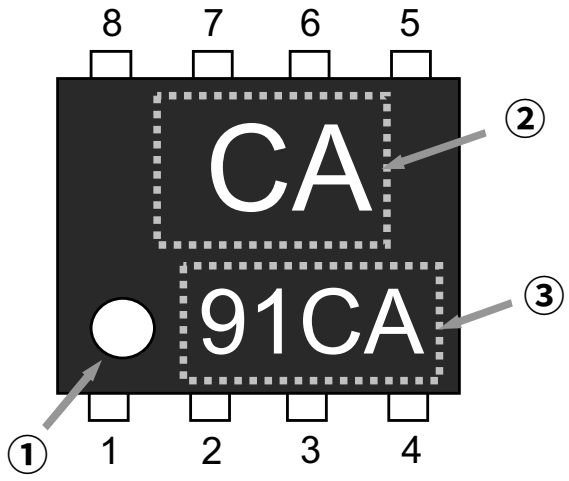


2009.4.27	
Established	Revised

Product Specification
Type Number : M T M 9 8 2 4 0 0 [B] B F
Mark Indication *1)

<Mark Indication>
① No.1 pin Indication
② Product mark (Abbreviation)
③ Date code Indication

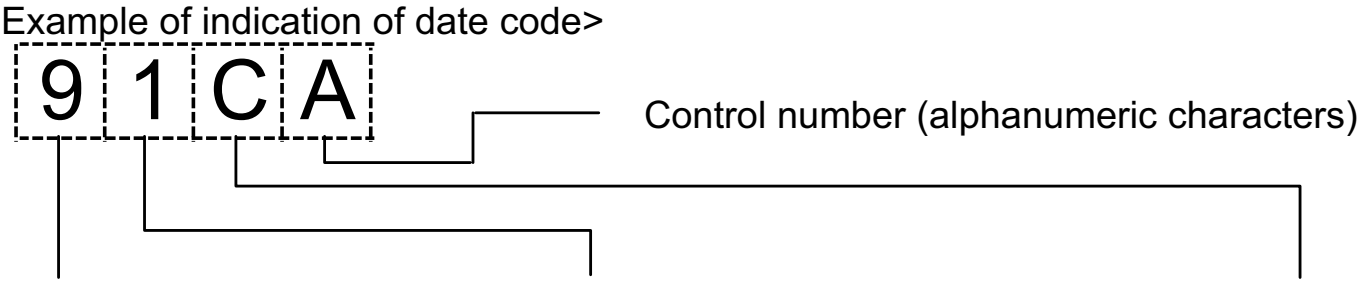
Note.
The actual font of symbol mark may differ slightly from the font shown in this specification.



Connection

1.Source	5.Drain
2.Source	6.Drain
3.Source	7.Drain
4.Gate	8.Drain

<Example of indication of date code>



AD2009 → 9
AD2010 → 0
AD2011 → 1
AD2012 → 2

Jan. to Sep. → 1 to 9
Oct. → O
Nov. → N
Dec. → D

Day	Symbol	Day	Symbol	Day	Symbol
1	1	11	A	21	M
2	2	12	B	22	N
3	3	13	C	23	P
4	4	14	D	24	R
5	5	15	E	25	S
6	6	16	F	26	T
7	7	17	H	27	U
8	8	18	J	28	V
9	9	19	K	29	W
10	0	20	L	30	X
				31	Y

<Factory distinction mark>

JAPAN	-	-	-
SO8-F1-B	-	-	-
CA	-	-	-

∗ White parts are treated by laser mark.

2009.4.27	
Established	Revised

Semiconductor Company, Panasonic Corporation

PACKAGE STANDARDS

Package Code	SO8-F1-B

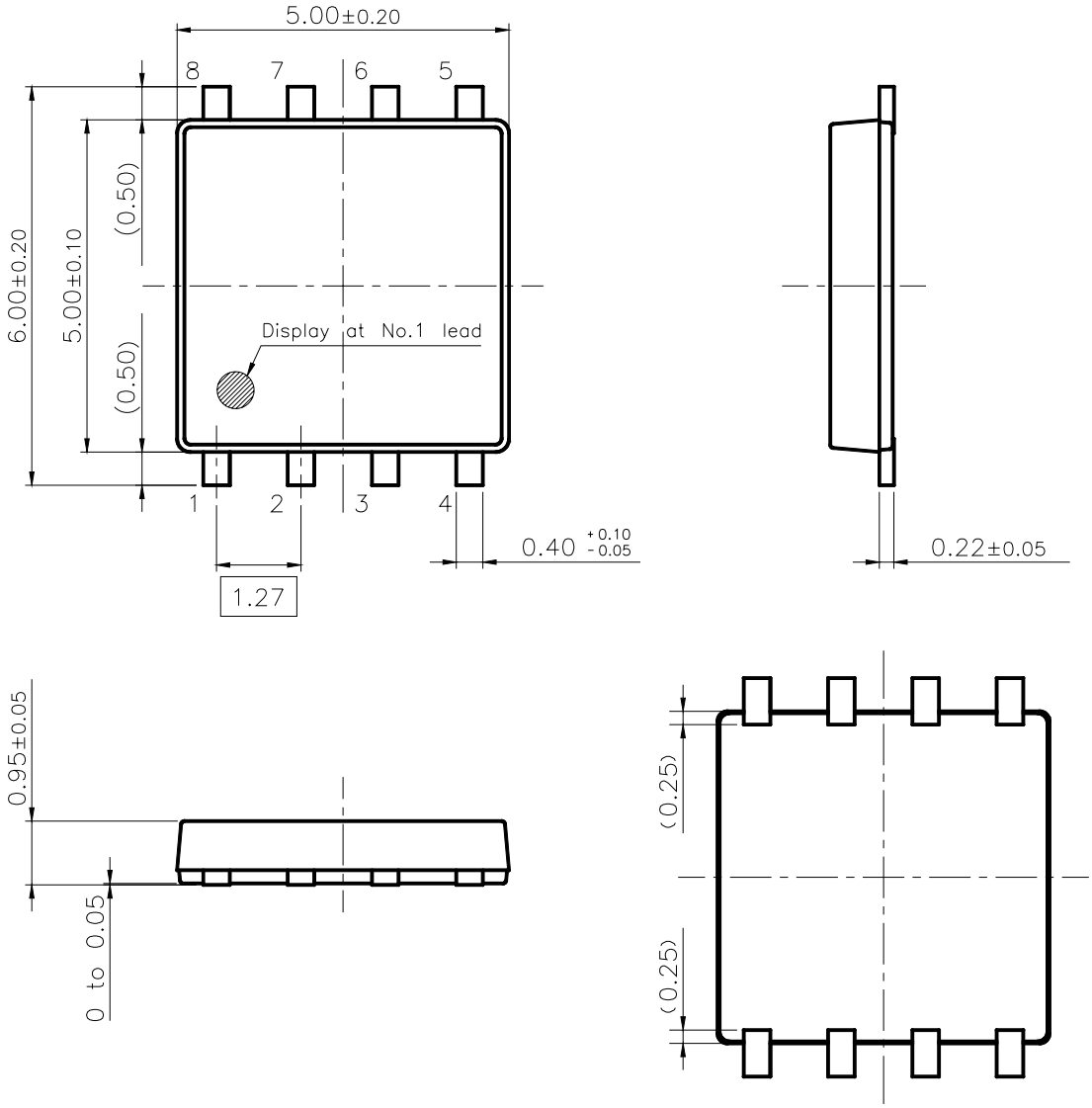
Semiconductor Company
Panasonic Corporation

Established by	Applied by	Checked by	Prepared by
H.Shidooka	H.Yoshida	M.Okajima	M.Kametaka

Established: 2007-01-18
Revised : 2009-01-23

1. Outline Drawing

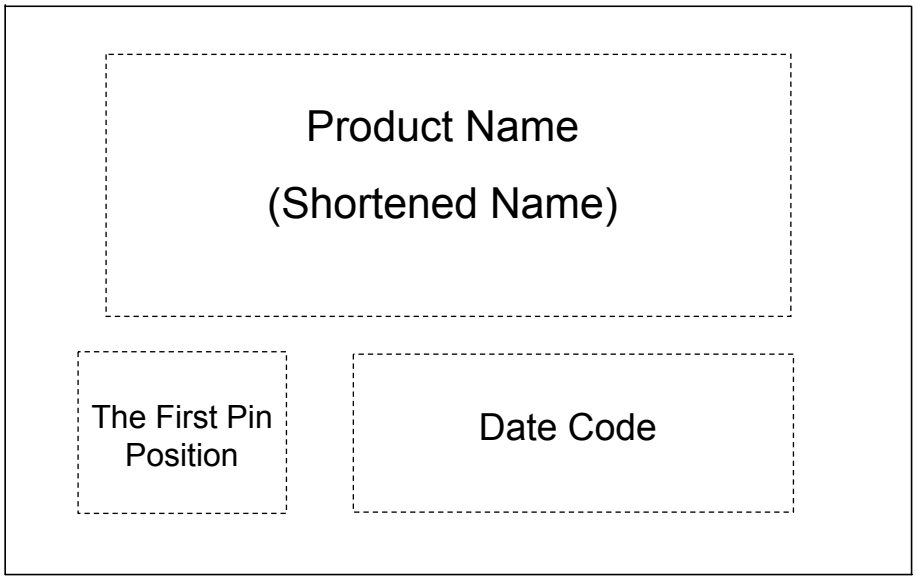
Unit:mm



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	SnBi Plating

Established: 2007-01-18
Revised : 2009-01-23

3. Mark Drawing



Established: 2007-01-18
Revised : 2009-01-23