

GENERAL DESCRIPTION

The XRT85L61 is an integrated E1, T1, 64KHz Centralized Clock interface for T1 (1.544Mbps) 100Ω, E1 (2.048Mbps) 75Ω or 120Ω applications.

The XRT85L61 extracts either 2048kHz or 1544 kHz clock signals from an E1 (2.048 MHz), T1 (1.544 Mhz) inputs respectively or 64 KHz, 8kHz or 400 Hz clock signals from the 64kHz reference clock input.

The XRT85L61 includes an on-chip crystal-less jitter attenuator with 32 bit FIFO that can either be enabled or disabled.

FEATURES

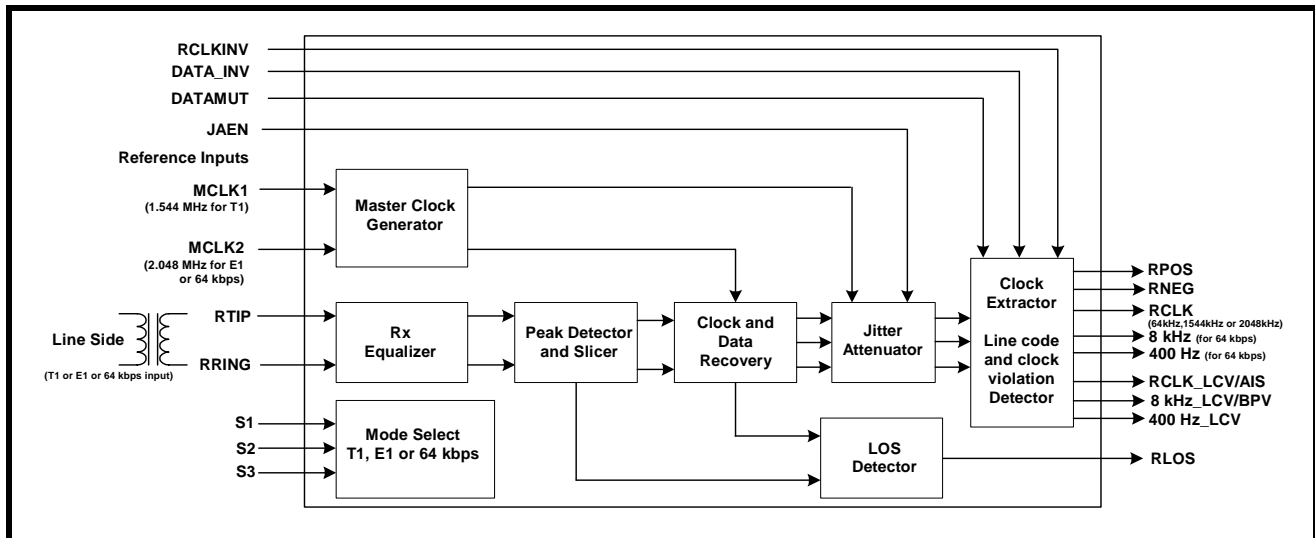
- Fully integrated single chip solution for E1,T1 or 64 kHz clock synchronization applications.
- Extracts 2048 kHz, 1544 kHz clock and data components
- Extracts 64 KHz and 8 kHz, 400 Hz clock information
- Line Code Violation alarms
- On-chip digital clock recovery circuit

- Supports 75Ω and 120Ω (E1), 100Ω (T1) applications.
- Crystal-less digital jitter attenuator with 32-bit FIFO that can either be enabled or disabled
- Receive loss of signal (RLOS) output
- Meets Telcordia GR-1244-CORE Section 3.4.1 R3-27 specification
- Meets or exceeds T1 and E1 specifications in ITU G.703, G.775
- Single +3.3V Supply Operation
- Logic inputs accept either 3.3 V or 5 V levels
- 28 pin TSSOP package

APPLICATIONS

- Universal Clock Synchronization for G.703 Telecom Formats
- T1/E1 Line Receiver with Clock and Data Recovery
- DSLAM

FIGURE 1. BLOCK DIAGRAM OF THE XRT85L61



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT85L61IG	28 Lead TSSOP	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT85L61

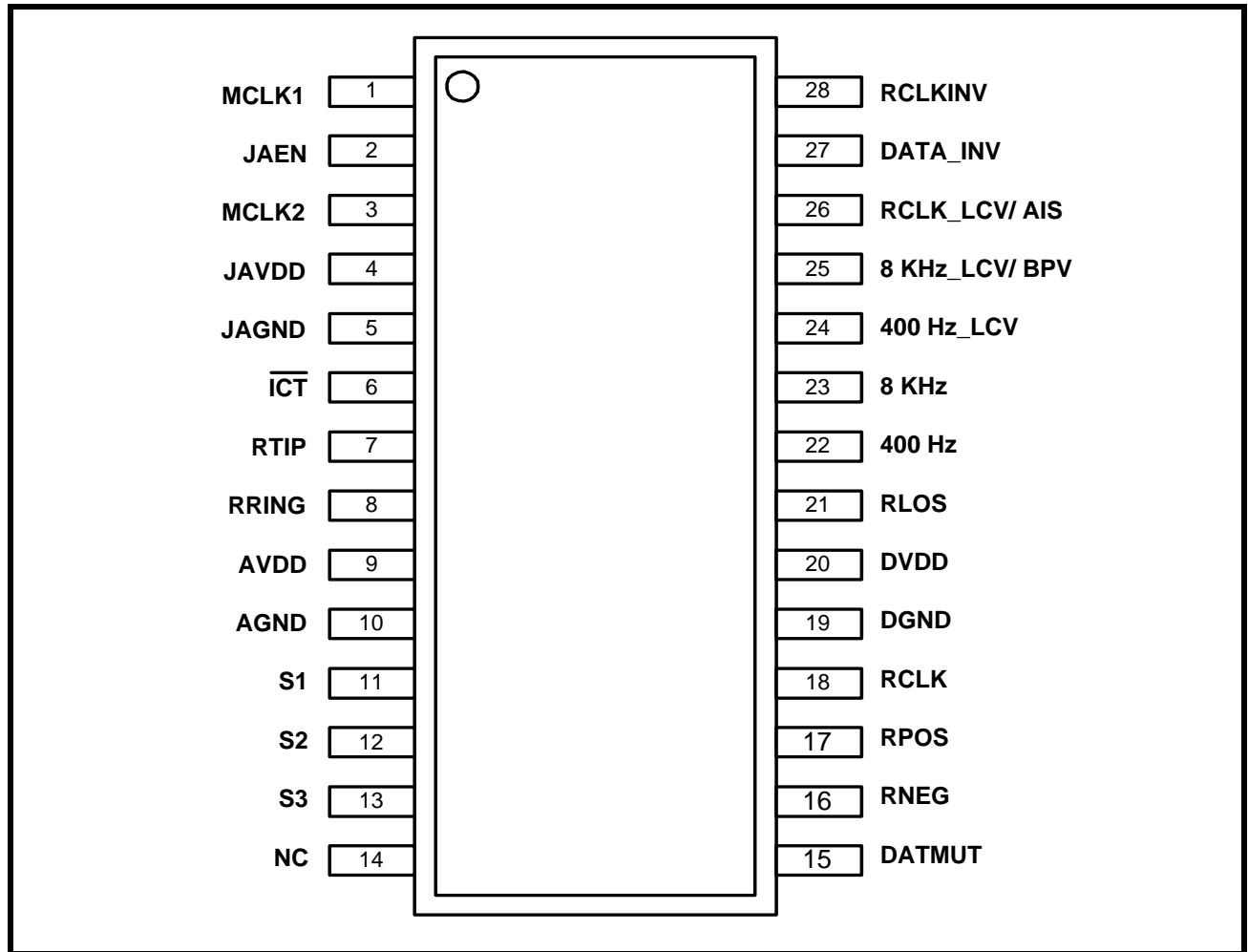


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PIN DESCRIPTIONS

PIN #	SYMBOL	TYPE	DESCRIPTION
1	MCLK1	I	<p>Reference T1 Clock input: This signal is an independent 1544 kHz clock with accuracy better than ± 32 ppm and duty cycle within 40% to 60%. This clock provides timing source for the PLL clock recovery circuit in T1 mode.</p> <p>NOTE: <i>If T1 mode is not used, this clock is not necessary for the device to operate.</i></p>
2	JAEN	I	<p>Jitter Attenuator Enable: Tie this pin "High" to enable the Jitter Attenuator. When enabled, a 32 bit FIFO is included in the data path for all modes of operation.</p> <p>NOTE: <i>Internally Pulled down with 50 kΩ resistor</i></p>
3	MCLK2	I	<p>Reference E1 and 64 kHz Clock Input: This signal is an independent 2048 kHz clock with accuracy better than ± 50 ppm and duty cycle within 40% to 60%. This clock provides timing source for the PLL clock recovery circuit in E1 and 64 kHz mode.</p> <p>NOTE: <i>To reduce intrinsic jitter when the JA is enabled, it is recommended to have a reference clock with an accuracy of ± 25 ppm or better. If E1 mode or 64 kHz mode is not used, this clock is not necessary for the device to operate.</i></p>
4	JAVDD	***	VDD for Jitter Attenuator (3.3V \pm 5%)
5	JAGND	***	Jitter Attenuator Ground
6	$\overline{\text{ICT}}$	I	<p>In circuit Testing When this pin is grounded, all output pins are Tri-stated for testing purposes.</p> <p>NOTE: <i>Internally Pulled up with 50 kΩ resistor</i></p>
7	RTIP	I	Receive Positive Input
8	RRING	I	Receive Negative Input
9	AVDD	***	Analog VDD (3.3V \pm 5%)
10	AGND	***	Analog Ground

PIN DESCRIPTIONS

PIN #	SYMBOL	TYPE	DESCRIPTION																																				
11	S1	I	<p>Mode Select</p> <table border="1"> <thead> <tr> <th>S1</th> <th>S2</th> <th>S3</th> <th>MODE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>64 kHz + 8 kHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>64kHz+8kHz+400Hz</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>E1 RZ</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>E1 NRZ</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>T1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>T1 (output full width data)</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>E1 (output full width data)</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table> <p><i>NOTE: T1 NRZ or E1 NRZ means the output data at RPOS and RNEG are 1 RCLK wide.</i></p>	S1	S2	S3	MODE	0	0	0	64 kHz + 8 kHz	0	0	1	64kHz+8kHz+400Hz	0	1	0	E1 RZ	0	1	1	E1 NRZ	1	0	0	T1	1	0	1	T1 (output full width data)	1	1	0	E1 (output full width data)	1	1	1	Reserved
S1	S2	S3	MODE																																				
0	0	0	64 kHz + 8 kHz																																				
0	0	1	64kHz+8kHz+400Hz																																				
0	1	0	E1 RZ																																				
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1	0	1	T1 (output full width data)																																				
1	1	0	E1 (output full width data)																																				
1	1	1	Reserved																																				
12	S2	I	Mode Select																																				
13	S3	I	Mode Select																																				
14	NC	***	This pin must be grounded for normal operation																																				
15	DATMUT	I	<p>Data Muting: Connect this pin “High” to mute data output to “Low” state at RPOS/ RNEG. The RLOS pin can be connected to this pin to mute the output when RLOS occurs. <i>NOTE: Internally Pulled down with 50 kΩ resistor</i></p>																																				
16	RNEG	O	<p>Receive Negative Data Output: The data is half clock cycle wide.</p>																																				
17	RPOS	O	<p>Receive Positive Data Output: The data is half clock cycle wide</p>																																				
18	RCLK	O	<p>Receive Clock Output Outputs either 1.544 MHz or 2.048 MHz or 64 kHz clock</p>																																				
19	DGND	***	Digital Supply Ground																																				
20	DVDD	***	Digital Supply Voltage (3.3V ± 5%)																																				
21	RLOS	O	Receive Loss of Signal Output																																				
22	400Hz	O	400 Hz Clock output for 64 kHz Operation																																				
23	8 kHz	O	8 kHz clock output for 64 kHz Operation																																				
24	400Hz_LCV	O	<p>Line Code Violation for 400 Hz This pin will stay “High” when 400 Hz is not in sync.</p>																																				

PIN DESCRIPTIONS

PIN #	SYMBOL	TYPE	DESCRIPTION
25	8 kHz_LCV/ BPV	O	<p>Line Code Violation for 8 kHz in 64 kHz operation</p> <p>Bipolar Violation: In E1RZ or T1 mode, every Bipolar violation valid or not valid is indicated at this pin. This pin will stay "High" when 8 kHz is not in sync.</p>
26	RCLK_LCV/AIS	O	<p>Receive Clock Violation. In 64 kbps operation, every missing pulse will cause this pin to go "High" for half the clock cycle</p> <p>AIS Indication In E1RZ or T1 mode, this output serves as an AIS indicator. AIS will stay "High" for 250 μs in E1 RZ mode, and in T1 mode, AIS will stay "High" for 3 ms.</p>
27	DATA_INV	I	<p>Data Invert: Connect this pin "High" to output active "Low" data at RPOS/RNEG. NOTE: Internally Pulled down with 50 kΩ resistor</p>
28	RCLK_INV	I	<p>Receive Clock Invert: Connect this pin "High" to align the data to change at the falling edge of RCLK. NOTE: Internally Pulled down with 50 kΩ resistor</p>

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	- 65°C to + 150°C
Operating Temperature	- 40°C to + 85°C
Supply Voltage Range	-0.5V to +6.0V
ESD	2000 V
Theta-JA	68°C/W
Theta-JC	13°C/W

ELECTRICAL CHARACTERISTICS (Ta = 25°C, VDD = 3.3 V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DC Electrical Characteristics					
V _{DDD}	DC Supply Voltage (Digital)	3.135	3.3	3.465	V
V _{DDA}	DC Supply Voltage (Analog)	3.135	3.3	3.465	V
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage	2.0		V _{DD}	V
V _{OL}	Output Low Voltage, IO _{UT} = -4.0mA	0		0.4	V
V _{OH}	Output High Voltage, IO _{UT} = 4.0mA	2.4		V _{DD}	V
I _L	Input Leakage Current*			±10	µA
C _I	Input Capacitance		5		pF
C _L	Output Load Capacitance			25	pF

NOTE: * Not applicable to pins with pull-down resistors.

FUNCTIONAL DESCRIPTION

The XRT85L61 is an integrated BITS (Building Integrated Timing Supply) Clock Generator. Simplified block diagram of the chip is shown in Figure 1.

The XRT85L61 extracts the clock signals from the following synchronization lines:

- Balanced 100 Ω lines with 1544 kbps DS1 pattern.
- Balanced 120 Ω or unbalanced 75 Ω lines with 2048 kbps RZ pattern.
- Balanced 120 Ω or unbalanced 75 Ω line with 2048 kbps NRZ pattern.
- Balanced 110 Ω line with 64 kbps having 8 kHz violations; a “64 kHz + 8 kHz sync pattern.
- Balanced 110 Ω line with a 64 kbps pattern having both 8 kHz and 400 Hz violations; a “64 kHz + 8 kHz + 400 Hz” sync pattern.

1.0 OPERATING MODE:

The operating mode for the XRT85L61 is shown in Table 1.

TABLE 1: OPERATING MODE SELECTION

S1	S2	S3	MODE	DATA OUTPUT AT RPOS / RNEG
0	0	0	64 kHz + 8 kHz	RZ
0	0	1	64 kHz + 8 kHz + 400 Hz	RZ
0	1	0	E1RZ	RZ
0	1	1	E1NRZ	RZ
1	0	0	T1	RZ
1	0	1	T1 (full width)	
1	1	0	E1 (full width)	
1	1	1	Reserved	

1.1 64 kHz Clock Mode:

The XRT85L61 receives the 64 kbps ternary RZ signal. Two modes of 64 kHz operation is possible by selecting S1, S2 and S3 as shown in Table 1.

TABLE 2: G.703 SPECIFICATION FOR THE 64 KHZ CLOCK SIGNAL AT INPUT PORT

FREQUENCY	(A) 64 kHz + 8 kHz OR (B) 64 kHz + 8 kHz + 400 Hz
Signal Format	(a) AMI with 8 kHz Bipolar Violation (b) AMI with 8 kHz Bipolar Violation removed at every 400 Hz.
Alarm Condition	Alarm should not occur against the amplitude range from 0.63 V to 1.1 V

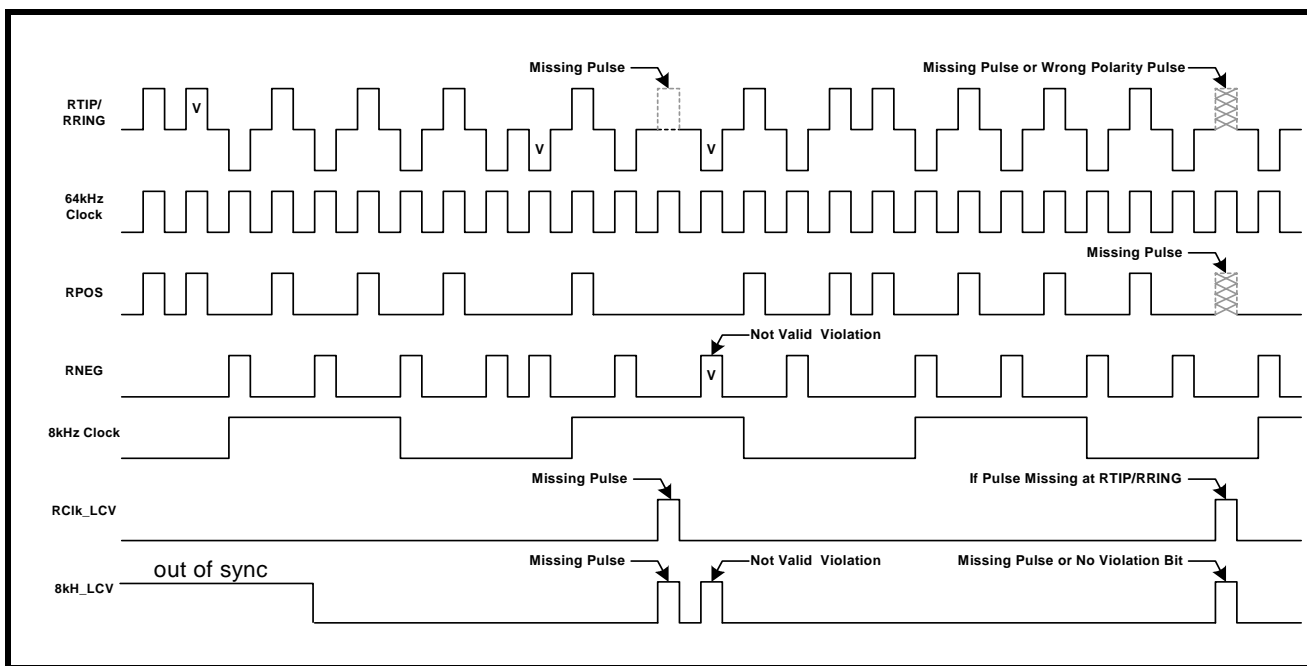
TABLE 3: G.703 SPECIFICATION FOR THE 64 KHz CLOCK SIGNAL AT OUTPUT PORT

FREQUENCY	(A) 64 KHz + 8 KHz OR (B) 64 KHz + 8 KHz + 400 Hz
Load Impedance	110 Ω resistive
Transmission Media	Symmetric Pair Cable
Pulse Width (FWHM)	< 7.8 ± 0.78 μs
Amplitude	< 1 V ± 0.1 V

1.1.1 64 kHz + 8 kHz Clock Extraction

The input data is shown in Figure 3. The 64 kHz clock signal consist of AMI code with 8 kHz Bipolar Violation. Both the 64 kHz and 8 kHz components are extracted from the composite received signal and presented at the 64 kHz and 8 kHz output pins.

FIGURE 3. INPUT DATA 64 KHz + 8 KHz OPERATION (s1 = 0, s2 = 0, s3 = 0)

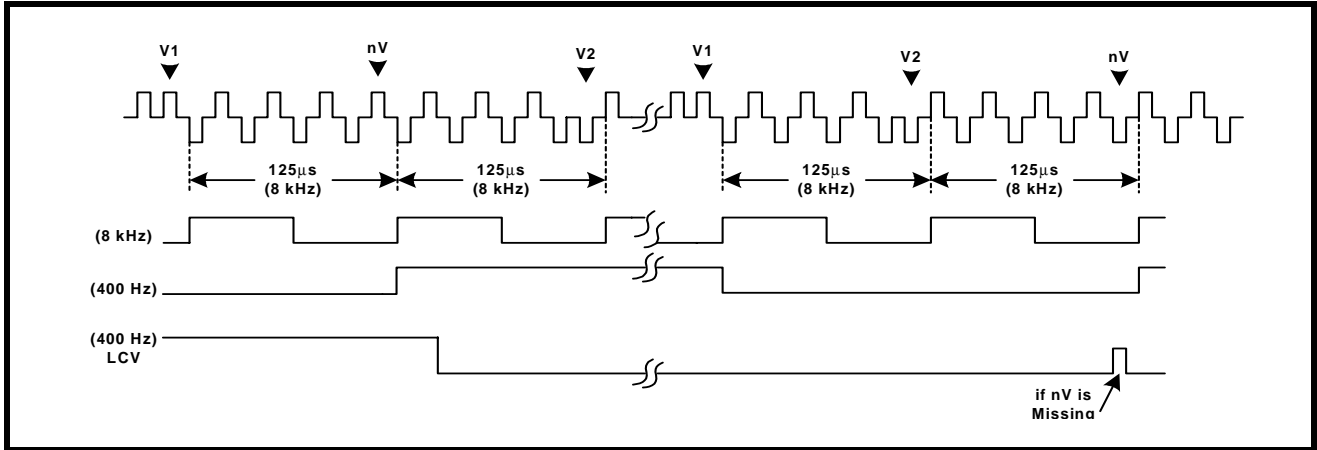


1.1.2 64 kHz + 8 kHz + 400 Hz Clock Extraction

Figure 4 shows the input data for this mode. The 64 kHz clock signal consist of AMI code with 8 kHz Bipolar Violation removed every 400 Hz. The 64 kHz, 8 kHz and 400 Hz components are extracted from the composite received signal and presented at the RCik, 8 kHz and 400 Hz output pins.

NOTE: The inputs are not aligned with all output signals. The above diagram is used to depict the output activity when the input signals have errors.

FIGURE 4. INPUT DATA 64 KHz + 8 KHz + 400 Hz OPERATION (s1 = 0, s2 = 0, s3 = 1)



NOTES:

1. V1 and V2 indicate AMI code-rule violations, and give the 8kHz timing.
2. V1 and V2 have different violation polarity with respect to each other.
3. nV indicates no violation (violation stealing) and gives the 400 Hz timing.

1.2 2048 kHz RZ E1 Mode

In this mode, the XRT85L61 receives a standard E1 signal as shown in Figure 5. Table 4 gives the details of the E1 pulse.

FIGURE 5. E1 PULSE MASK (G.703)

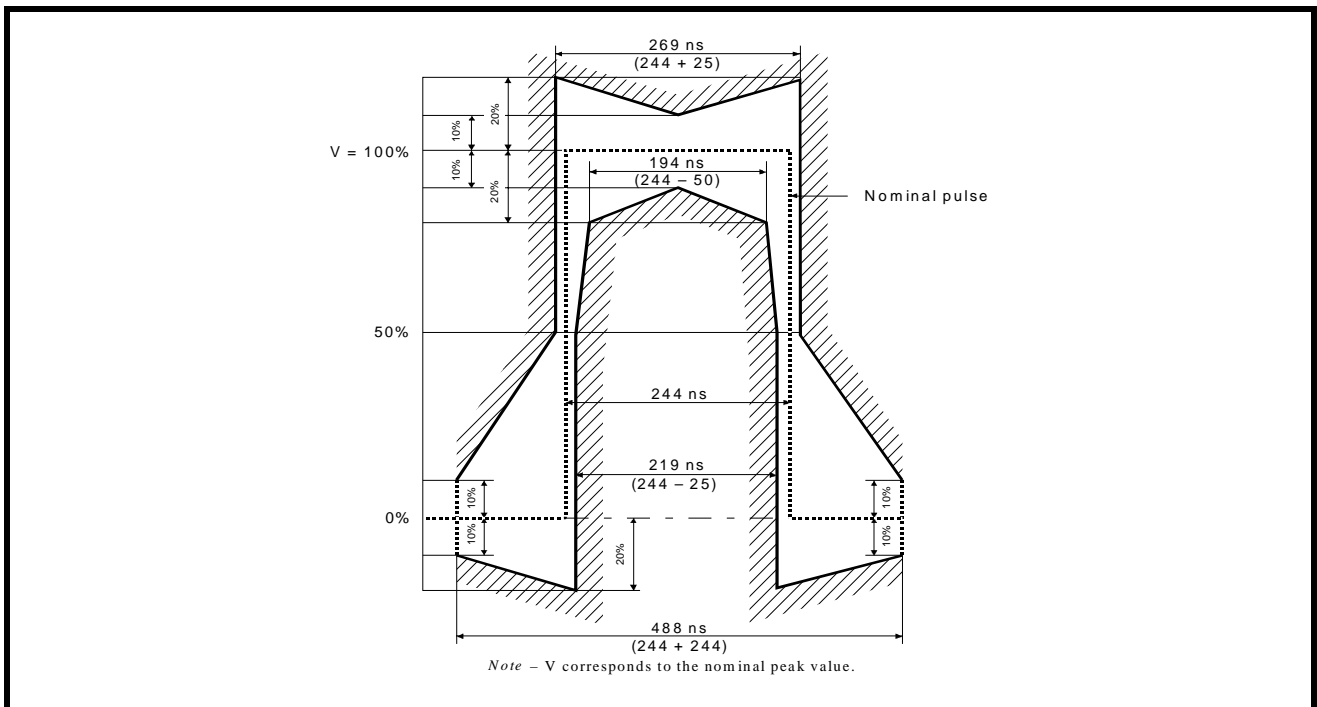


TABLE 4: G.703 SPECIFICATION E1

PULSE	INTERFACE	
Pulse Shape (nominally rectangular)	All Marks of a valid signal must conform with the mask irrespective of the sign. The value V corresponds to the nominal peak value.	
Pair(s) in each direction	One coaxial pair	One symmetrical pair
Test Load Impedance	75 Ω Resistive	120 Ω Resistive
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 \pm 0.237 V	0 \pm 0.3 V
Nominal Pulse Width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	
Maximum peak to peak jitter at an output port	Refer to ITU-T G.823 specification	

1.3 2048 kHz NRZ Mode

In this mode, XRT85L61 receives 2048 kbps synchronization signal as shown in Figure 6.

FIGURE 6. E1 CLOCK SIGNAL WAVE SHAPE - G.703

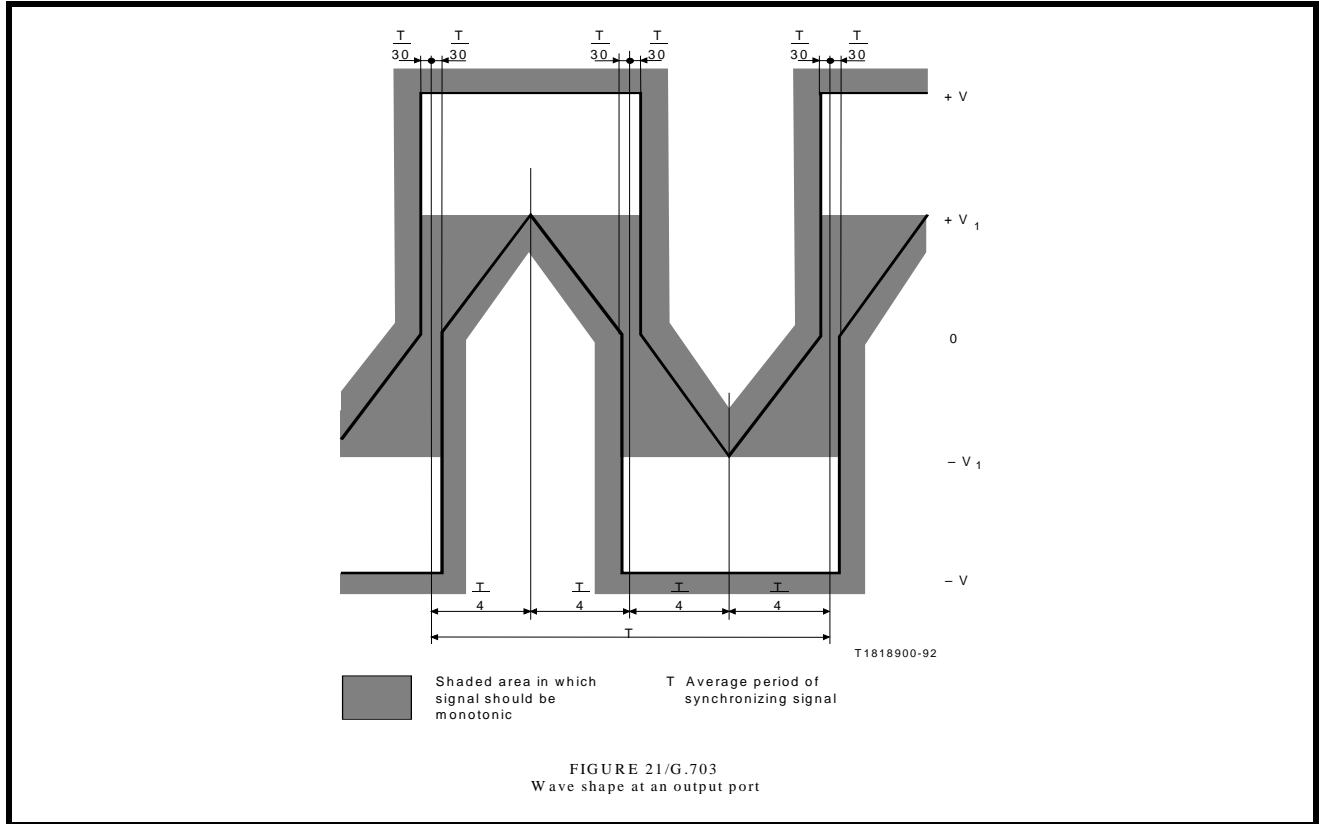


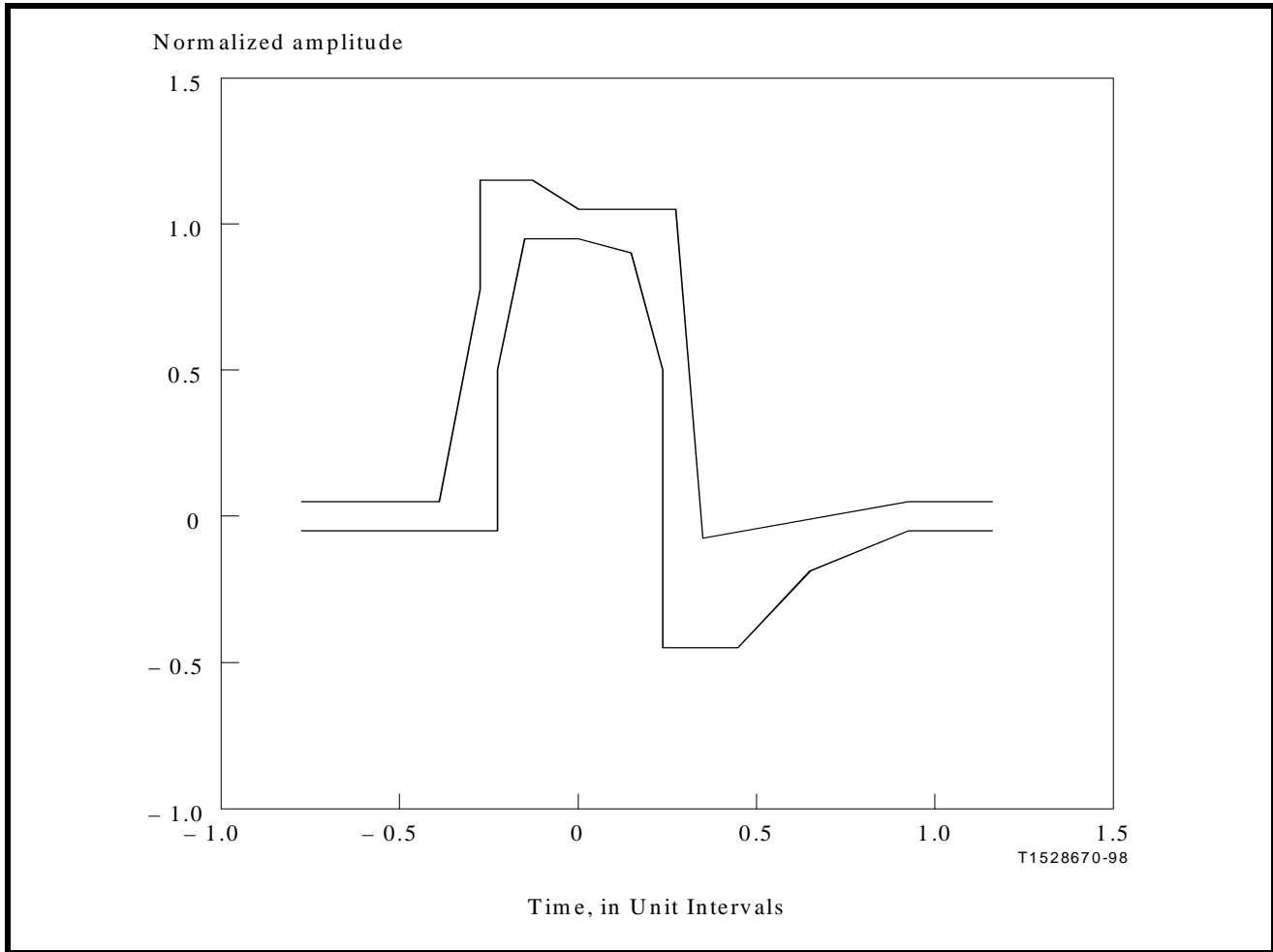
TABLE 5: G.703 2048 kHz CLOCK INTERFACE

PULSE	INTERFACE	
Frequency	2048 kHz ± 50 ppm	
Pulse Shape	The signal must conform with the mask. The value V corresponds to maximum peak value The value V ₁ corresponds to minimum peak value	
Pair(s) in each direction	Coaxial pair	Symmetrical pair
Test Load Impedance	75 Ω Resistive	120 Ω Resistive
Maximum peak value (V _{op})	1.5	1.9
Minimum peak value (V _{op})	0.75	1.0
Maximum jitter at an output port	0.05 UI peak to peak measured within the frequency range f ₁ = 20 Hz to f ₄ = 100 kHz NOTE: This value is valid for network timing distribution equipment. Other values may be specified for timing output ports of digital links carrying the network timing.	

1.4 1544 kHz T1 Mode

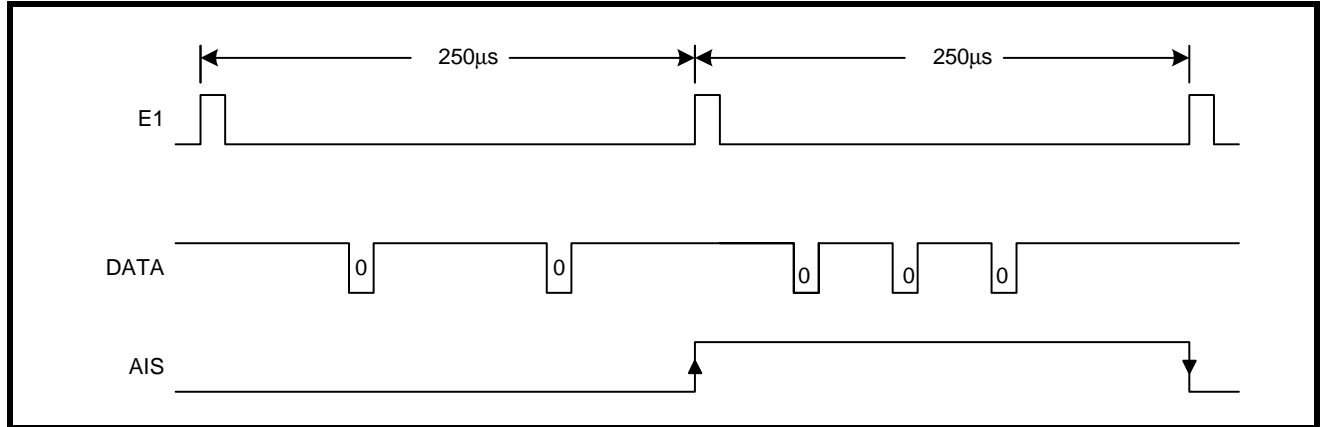
In this mode, the XRT85L61 receives a standard DS1 signal as shown in Figure 7.

FIGURE 7. G.703 DS1 WAVE FORM

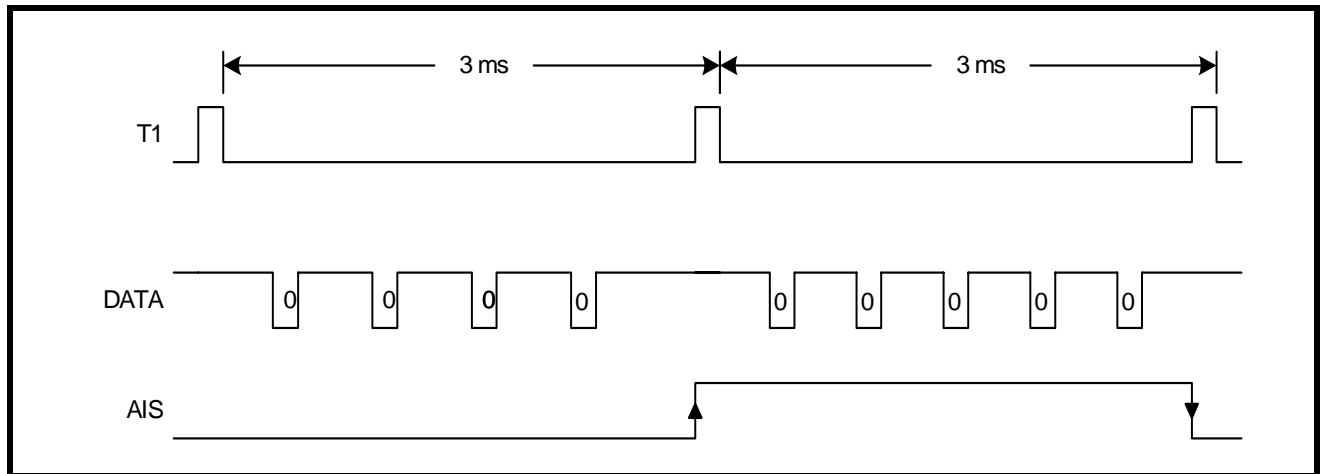


2.0 AIS DETECTION TIMING

In E1 mode, AIS is set when the incoming signal has 2 or less Zeros in sequence of 512 bits. AIS will stay "High" for 250 μ s and AIS is cleared upon receiving three or more zeros in the subsequent 512 bits (250 μ s) time-frame. Figure 8 shows the AIS timing.

FIGURE 8. AIS DETECTION FOR E1 MODE

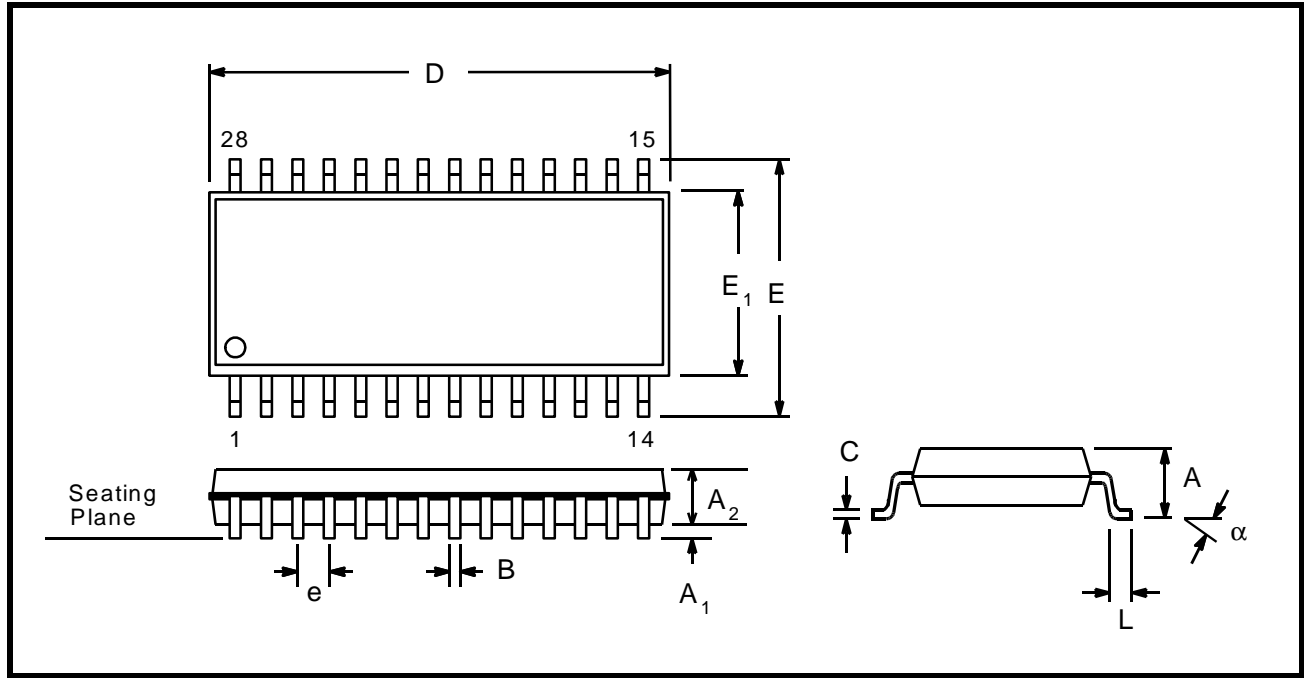
In T1 mode, AIS is cleared when 5 or more zeros is detected in the subsequent 4632 bits (3 ms) time-frame. Figure 9 shows the AIS timing for T1 mode.

FIGURE 9. AIS DETECTION FOR T1 MODE

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT85L61IG	28 Lead TSSOP	-40°C to +85°C

PACKAGE OUTLINE DRAWING



Note: The control dimension is in the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.033	0.047	0.85	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.378	0.386	9.60	9.80
E	0.248	0.260	6.30	6.60
E1	0.169	0.177	4.30	4.50
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°



REVISION HISTORY

REVISION #	DATE	CHANGES
P1.0.1	August 2002	original
P1.0.2	November 2002	Edits to text
P1.0.3	December 2002	Ordering information changed from XRT85L61IV to XRT85L61IG
1.0.0	January 2004	Final Release
1.0.1	February 2004	Added description for MCLK1 and MCLK2.

NOTICE

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