

Structure Silicon monolithic integrated circuit
 Product High-Side Switch
 Type **BD6513F**
 Feature 100mΩ (VDD=5V, Typ.) Dual High-Side Switch
 Over current detector, Thermal shutdown, Under voltage lockout
 Control Logic : Active Low

◇ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{DD}	-0.3 ~ 6.0	V
CTRL voltage	V _{CTRL}	-0.3 ~ V _{DD} + 0.3	V
Flag voltage	V _{FLAG}	-0.3 ~ 6.0	V
Output voltage	V _{OUT}	-0.3 ~ V _{DD} + 0.3	V
Storage Temperature	T _{STG}	-55 ~ 150	°C
Power Dissipation *1	Pd	560	mW

*1 This value decreases 4.48mW/°C above 25°C.

- * Resistance radiation design is not doing.
- * Operation is not guaranteed.

◇ Operating Conditions (Ta=-25°C~85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	V _{DD}	3.0	5.0	5.5	V

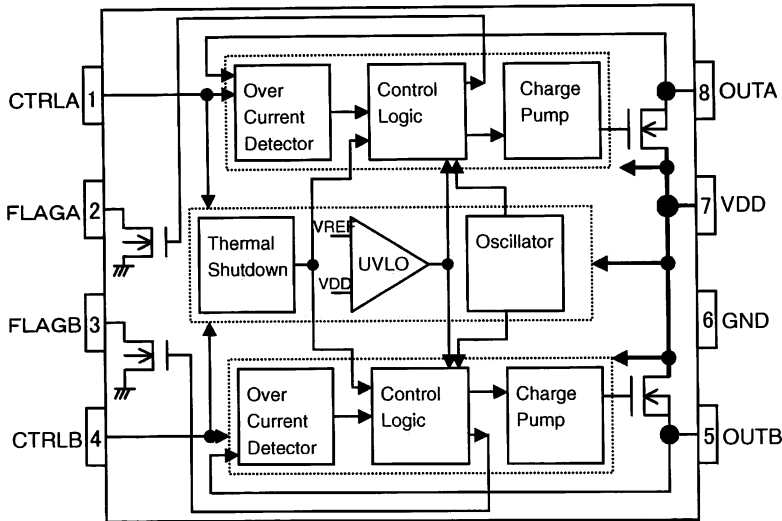
Application example

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◇Electrical Characteristics (Unless otherwise specified, VDD = 5V, Ta = 25°C)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Current	I _{DD}	-	85	120	μA	V _{CTRL} =0V OUT=OPEN
		-	0.01	2	μA	V _{CTRL} =5V OUT=OPEN
Control Input Voltage	V _{CTRL}	-	-	0.7	V	CTRL Low Level Input
		2.5	-	-	V	CTRL High Level Input
Control Input Current	I _{CTRL}	-1	0.01	1	μA	V _{CTRL} = 0V or 5V
On Resistance	R _{ON}	-	100	130	mΩ	V _{DD} = 5V, I _{OUT} = 500mA
		-	120	160	mΩ	V _{DD} = 3.3V, I _{OUT} = 500mA
Turn on Delay	T _{RD}	100	600	2000	μs	RL=10Ω "V _{CTRL} =H→L" → V _{OUT} =50%
Turn On Rise Time	T _R	200	1500	6000	μs	RL=10Ω V _{OUT} =10% → 90%
Turn Off Delay	T _{FD}	-	3	20	μs	RL=10Ω "V _{CTRL} =L→H" → V _{OUT} =50%
Turn Off Fall Time	T _F	-	1	20	μs	RL=10Ω V _{OUT} =90% → 10%
UVLO Threshold Voltage	V _{UVLOH}	2.3	2.5	2.7	V	V _{DD} increasing
	V _{UVLOL}	2.1	2.3	2.5	V	V _{DD} decreasing
Thermal Shutdown Threshold	T _{TS}	-	135	-	°C	
Over Current Limit Threshold Level	I _{THLIM}	1.25	1.65	2.20	A	
Over Current Limit Level	I _{LIM}	0.6	1.1	1.6	A	
Flag Output Resistance	R _{FLAG}	-	16	40	Ω	I _{FL} = 10mA
Flag Off Current	I _{FLAG}	-	0.01	1	μA	

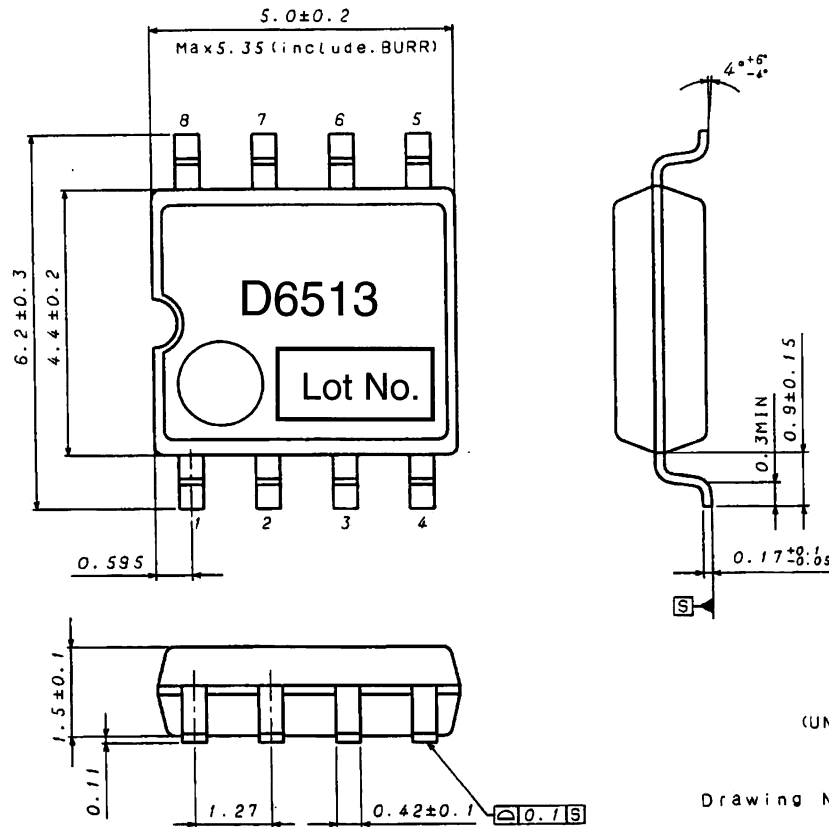
◇ Block Diagram



◇ Pin Description

Pin Number	Pin name	Pin Function
1 4	CTRLA CTRLB	Enable Input
2 3	FLAGA FLAGB	Fault Flag Output
5 8	OUTA OUTB	Switch Output
6	GND	Ground
7	VDD	Supply Input

◇ Package Outline



SOP 8 (Unit : mm)

(UNIT: mm)
Drawing No. EX112-5002

◇Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become 135°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

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