ACPL-H342 and ACPL-K342

2.5 Amp Output Current IGBT Gate Drive Optocoupler with Active Miller Clamp, Rail-to-Rail Output Voltage and UVLO in Stretched SO8

Data Sheet

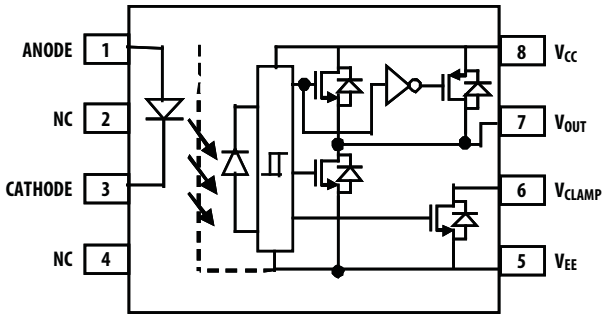
Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available; -xxxE denotes a lead-free product

Description

The ACPL-H342/ACPL-K342 contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving IGBT with ratings up to 1200V/150A. For IGBTs with higher ratings, the ACPL-H342/ACPL-K342 can be used to drive a discrete power stage which drives the IGBT gate. The ACPL-H342 and ACPL-K342 have the highest insulation voltage of V_{IORM} = 891Vpeak and 1140Vpeak respectively in the IEC/ EN/DIN EN 60747-5-5.

Functional Diagram



Note: Design Note: A 1 µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	$V_{CC} - V_{EE}$ "POSITIVE GOING" (i.e., TURN-ON)	$V_{CC} - V_{EE}$ "NEGATIVE GOING" (i.e., TURN-OFF)	V_O	V_{CLAMP}
OFF	0 – 30V	0 – 30V	LOW	LOW
ON	0 – 10V	0 – 9V	LOW	LOW
ON	10 – 13.5V	9 – 12V	TRANSITION	TRANSITION
ON	13.5 – 30V	12 – 30V	HIGH	Hi-Z

Features

- 2.5 A Maximum Peak Output Current
- 2.0A Minimum Peak Output Current
- Built-in Active Miller Clamp
- Rail-to-Rail Output Voltage
- Fast Propagation Delay to minimize Dead Time
- $t_{PHL} < t_{PLH}$ to provide "Anti-Cross" Conduction
- LED input threshold current hysteresis
- I_{CC} = 2.5 mA Maximum Supply Current to allow boot-strap power supply
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- 40 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- Wide Operating V_{CC} Range: 15 to 30 Volts
- Industrial Temperature Range: -40°C to 105°C
- Safety Approval:
  - UL Recognized 3750/5000 V_{RMS} for 1min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 891/1140 Vpeak

Applications

- IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Renewable Energy Inverters
- Industrial Inverters
- Switching Power Supplies

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-H342 is UL Recognized with 3750 V_{RMS} for 1 minute per UL1577.

ACPL-K342 is UL Recognized with 5000 V_{RMS} for 1 minute per UL1577.

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 V_{RMS} /1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-H342	-000E	Stretched SO-8	X				80 per tube
	-500E		X	X			1000 per reel
	-060E		X			X	80 per tube
	-560E		X	X		X	1000 per reel
ACPL-K342	-000E	Stretched SO-8	X		X		80 per tube
	-500E		X	X	X		1000 per reel
	-060E		X		X	X	80 per tube
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-H342-560E to order product of Stretched SO-8 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliant.

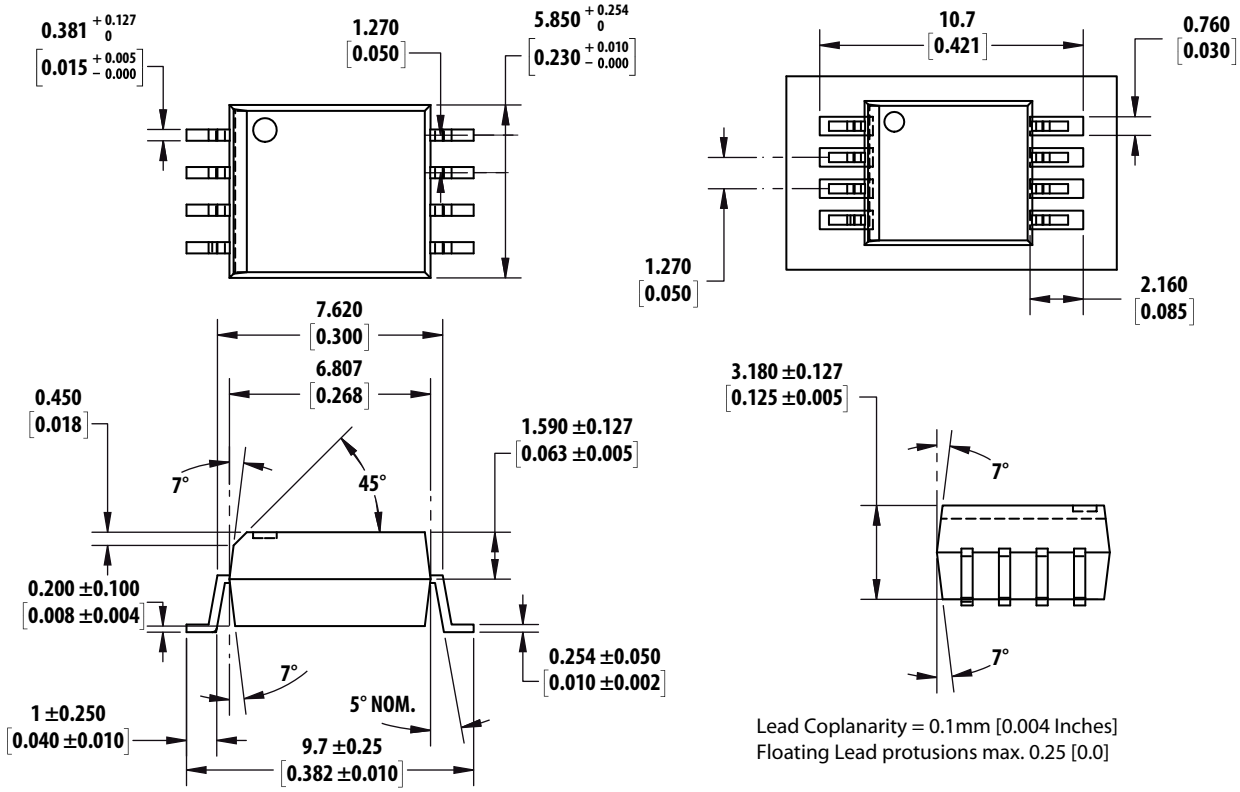
Example 2:

ACPL-K342-000E to order product of Stretched SO-8 Surface Mount package in Tube packaging with UL 5000 V_{RMS}/1 minute and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

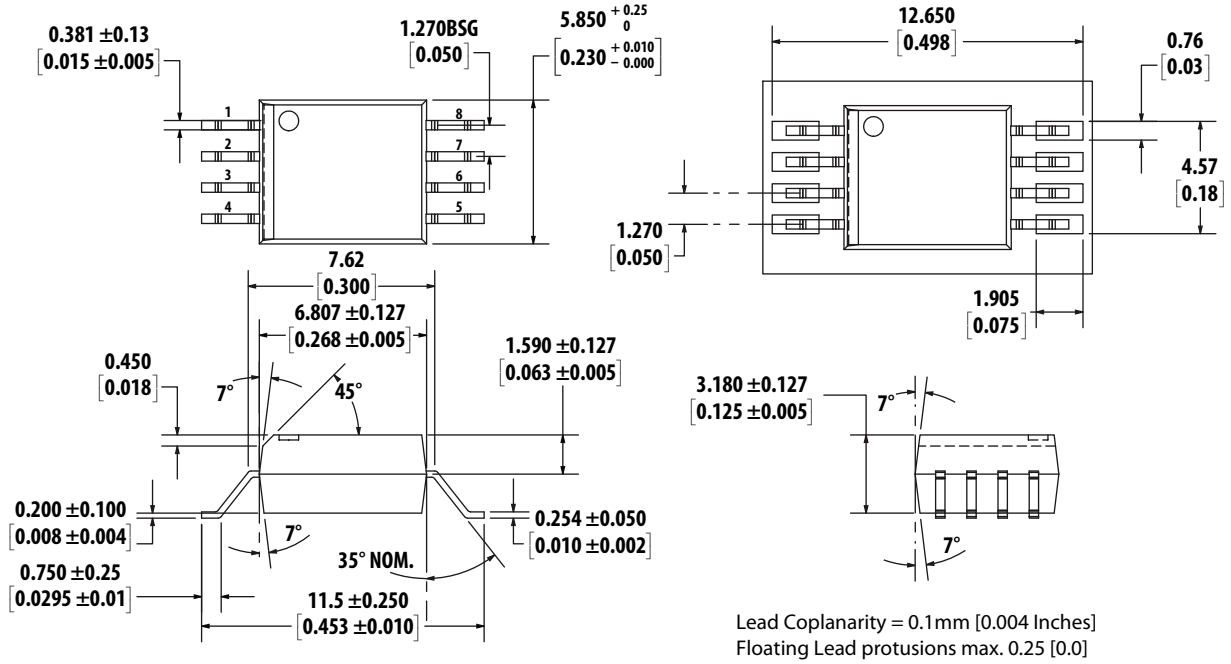
ACPL-H342 Outline Drawing



Lead Coplanarity = 0.1mm [0.004 Inches]
Floating Lead protusions max. 0.25 [0.0]

Dimensions in Millimeters [Inches]

ACPL-K342 Outline Drawing



Lead Coplanarity = 0.1mm [0.004 Inches]
Floating Lead protusions max. 0.25 [0.0]

Dimensions in Millimeters [Inches]

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-H342 / ACPL-K342 is approved by the following organizations:

UL

Recognized under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} (ACPL-H342) and V_{ISO} = 5000 V_{RMS} (ACPL-K342), File 55361

CSA

CSA Component Acceptance Notice #5, File CA 88324

IEC/EN/DIN EN 60747-5-5 (ACPL-H342/K342 Option 060 Only)

Maximum Working Insulation Voltage Viorm = 891V_{peak} (ACPL-H342) and Viorm = 1140 V_{peak}(ACPL-K342)

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (ACPL-H342 / ACPL-K342 Option 060)

Description	Symbol	ACPL-H342 Option 060	ACPL-K342 Option 060	Unit
Installation classification per DIN VDE 0110/1.89, Table 1				
for rated mains voltage ≤ 150 V_{rms}		I – IV	I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	I – IV	
for rated mains voltage ≤ 450 V_{rms}		I – III	I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – III	I – IV	
for rated mains voltage ≤ 1000 V_{rms}			I – III	
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1671	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1426	1824	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure, also see Figure 37.				
Case Temperature	T_S	175	175	°C
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

Note:
These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-H342	ACPL-K342	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Notes:

1. All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Output IC Junction Temperature	T_J		125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 μs pulse width, 300pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	2
Peak Clamp Sink Current	I_{CLAMP}		2.5	A	2
Total Output Supply Voltage	$(V_{CC} - V_{EE})$	0	35	V	
Input Current (Rise/Fall Time)	$t_{r(IN)} / t_{f(IN)}$		500	ns	
Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC}	V	
Output IC Power Dissipation	P_O		210	mW	3
Total Power Dissipation	P_T		255	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	- 40	105	°C	
Output Supply Voltage	$(V_{CC} - V_{EE})$	15	30	V	
Input Current (ON)	$I_{F(ON)}$	7	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.6	0.8	V	

Table 5. Electrical Specifications (DC)

Unless otherwise noted, all typical values are at T_A = 25°C, V_{CC} - V_{EE} = 30 V, V_{EE} = Ground; all Minimum/Maximum specifications are at Recommended Operating Conditions (T_A = -40 to 105°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Peak Output Current	I_{OH}	-0.5	-1.2		A	$V_O = V_{CC} - 4$	3, 4, 23	5
		-2.0			A	$V_O = V_{CC} - 15$		2
Low Level Peak Output Current	I_{OL}	0.5	2.7		A	$V_O = V_{EE} + 2.5V$	6, 7, 24	5
		2.0			A	$V_O = V_{EE} + 15V$		2
High Output Transistor RDS(ON)	$R_{DS,OH}$		2.6	5.0	Ω	I_{OH} = -2.0A	8	
Low Output Transistor RDS(ON)	$R_{DS,OL}$		0.8	2.0	Ω	I_{OL} = 2.0A	9	
Clamp Output Peak Current	I_{CLAMP}	1.0	2.5		A	$V_O = V_{EE} + 2.5$	14, 16, 27	2
Clamp Pin Threshold	V_{tCLAMP}		2.3		V		15,16, 28	
Clamp Output Transistor RDS(ON)	$R_{DS,CLAMP}$		0.8	2.0	Ω	I_{CLAMP} = 1.5 A		
High Level Output Voltage	V_{OH}	V_{CC}-2.0	V_{CC}-0.80		V	I_O = -100 mA	2, 4, 25	6, 7
High Level Output Voltage	V_{OH}		V_{CC}		V	I_O = 0 mA , I_F=10 mA	1	
Low Level Output Voltage	V_{OL}		0.07	0.25	V	I_O = 100 mA	5, 7, 26	
High Level Supply Current	I_{CCH}		1.68	2.5	mA	R_g = 10Ω, C_g = 25 nF, I_F = 10 mA,	10, 11	
Low Level Supply Current	I_{CCL}		2.0	2.5	mA	R_g = 10Ω, C_g = 25 nF, I_F = 0 mA		
Threshold Input Current Low to High	I_{FLH}	0.5	1.5	4.0	mA	R_g = 10Ω, C_g = 25 nF, V_O > 5 V	12, 13, 29	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.55	1.95	V	I_F = 10 mA	22	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		-1.7		mV/°C			
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 100 μA		
Input Capacitance	C_{IN}		70		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	10.0	12.3	13.5	V	V_O > 5 V, I_F = 10 mA	30	
	V_{UVLO-}	9.0	10.7	12.0				
UVLO Hysteresis	$UVLO_{HYS}$		1.4					

Table 6. Switching Specifications (AC)

Unless otherwise noted, all typical values are at T_A = 25°C, V_{CC} - V_{EE} = 30 V, V_{EE} = Ground; all Minimum/Maximum specifications are at Recommended Operating Conditions (T_A = -40 to 105°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.100	0.260	0.350	µs	R_g = 10Ω, C_g = 25 nF, f = 20 kHz , Duty Cycle = 50%, I_F = 7 mA to 16 mA, V_{CC} = 15 V to 30V	17, 18, 19, 20, 21, 31	15
Propagation Delay Time to Low Output Level	t_{PHL}	0.050	0.145	0.250	µs			
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})	-0.010	-0.100	-0.200	µs		39, 40	11
Rise Time	t_R		22		ns	V_{CC} = 30V	31	
Fall Time	t_F		18		ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	40	50		kV/µs	T_A = 25°C, I_F = 10 mA, V_{CC} = 30 V, V_{CM} = 1500 V with split resistors	32	12, 13
		25	35			T_A = 25°C, I_F = 10 mA, V_{CC} = 30 V, V_{CM} = 1000 V without split resistors		
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	40	50		kV/µs	T_A = 25°C, V_F = 0 V, V_{CC} = 30 V, V_{CM} = 1500 V with split resistors,	32	12, 14
		25	35			T_A = 25°C, V_F = 0 V, V_{CC} = 30 V, V_{CM} = 1000 V without split resistors		

Table 7. Package Characteristics

Unless otherwise noted, all typical values are at T_A = 25°C; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	ACPL-H342	3750			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		8,10
		ACPL-K342	5000			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		9,10
Input-Output Resistance	R_{I-O}			$>50^{12}$		Ω	V_{I-O} = 500 V_{DC}		10
Input-Output Capacitance	C_{I-O}			0.2		pF	f =1 MHz		
LED-to-Ambient Thermal Resistance	R_{11}		311			°C/W	Thermal Model in Application Notes Below		
LED-to-Detector Thermal Resistance	R_{12}, R_{21}		111						
Detector-to-Ambient Thermal Resistance	R_{22}		168						

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:
1. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10µs
3. Derate linearly above 85°C free-air temperature at a rate of 5.5 mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 6.3 mW/°C. The maximum LED junction temperature should not exceed 125°C.
5. Maximum pulse width = 50 µs.
6. In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms.
8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤5 µA).
9. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥6000 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤5 µA).
10. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
11. The difference between t_{PHL} and t_{PLH} between any two ACPL-H342 parts under the same test condition.
12. Pins 2 and 4 need to be connected to LED common.
13. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15.0 V).
14. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V).
15. This load condition approximates the gate load of a 1200V/150A IGBT.

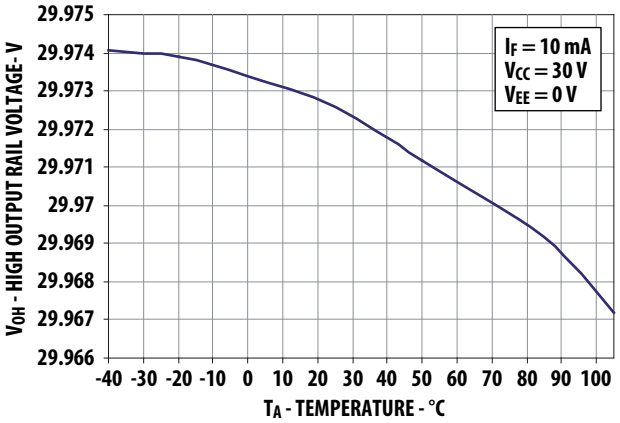


Figure 1. High Ouput Rail Voltage vs. Temperature.

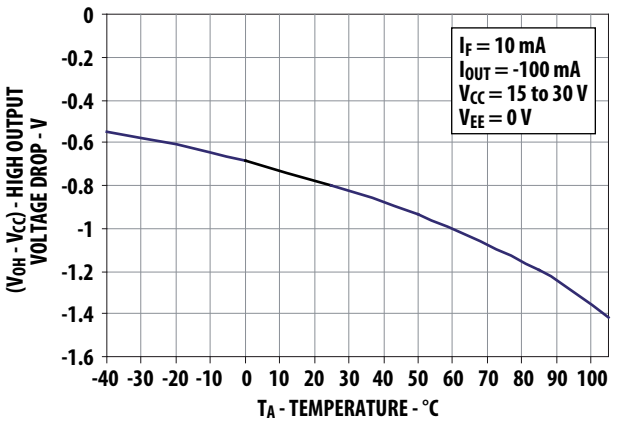


Figure 2. V_{OH} vs. temperature.

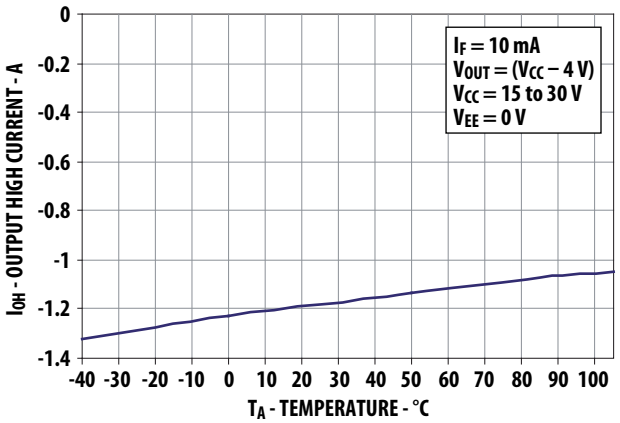


Figure 3. I_{OH} vs. temperature.

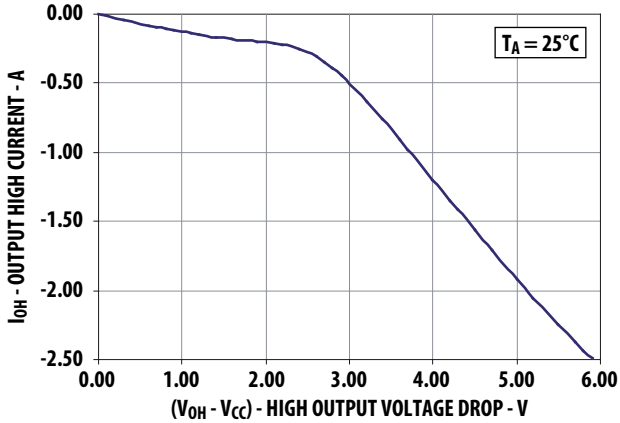


Figure 4. I_{OH} vs. V_{OH}.

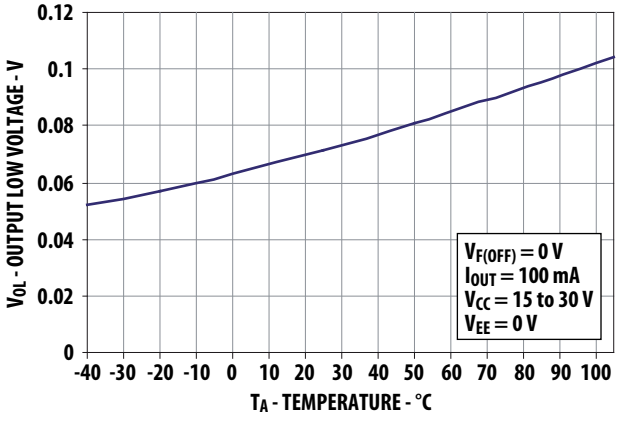


Figure 5. V_{OL} vs. temperature.

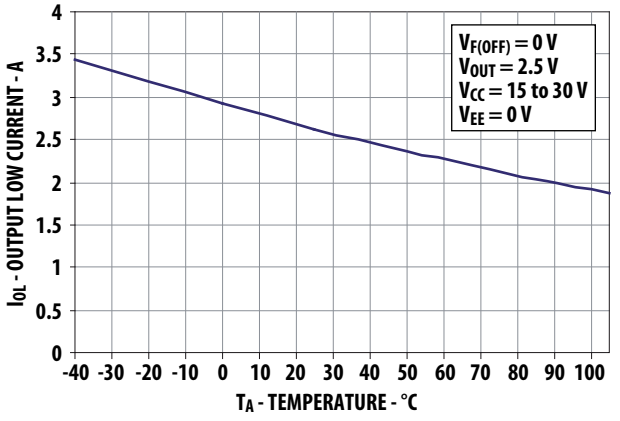


Figure 6. I_{OL} vs. temperature.

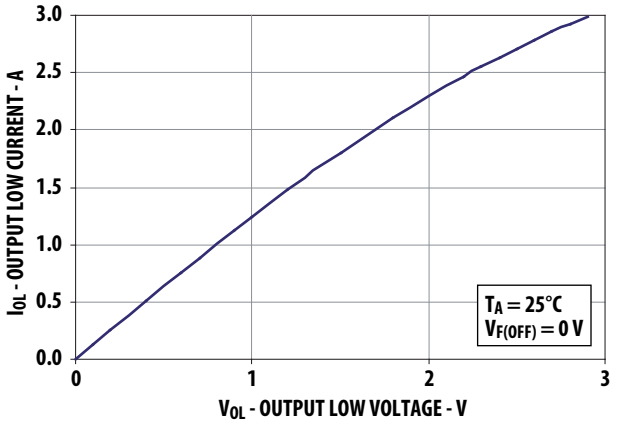


Figure 7. I_{OL} vs. V_{OL}

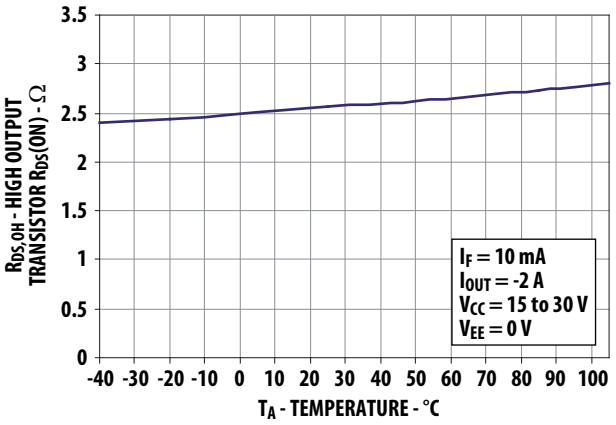


Figure 8. $R_{DS,OH}$ vs. temperature.

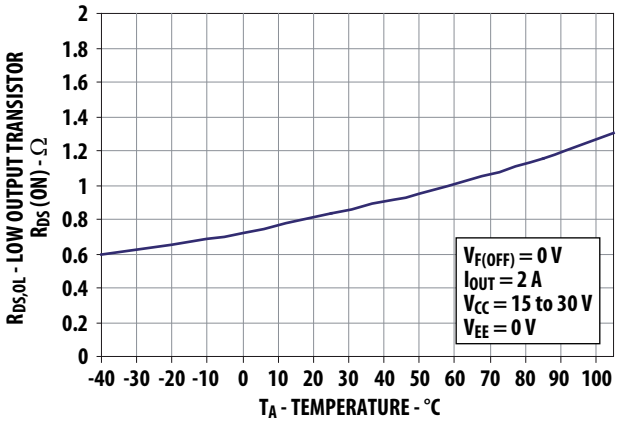


Figure 9. $R_{DS,OL}$ vs. temperature.

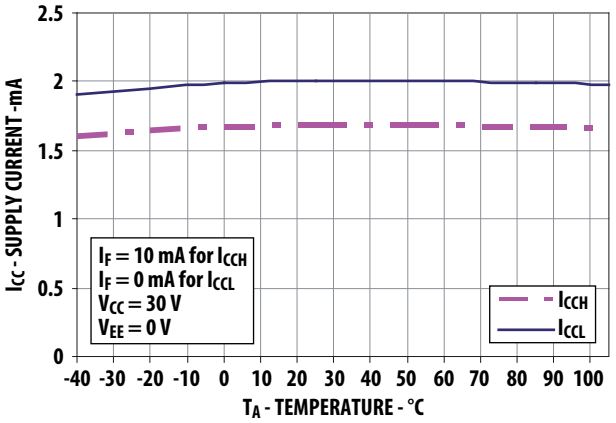


Figure 10. I_{CC} vs. temperarure.

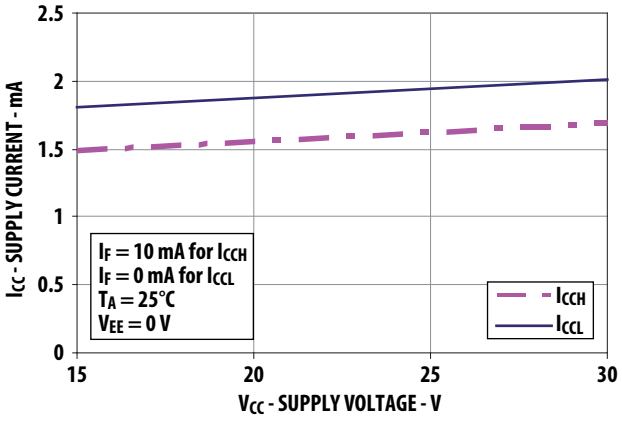


Figure 11. I_{CC} vs. V_{CC}.

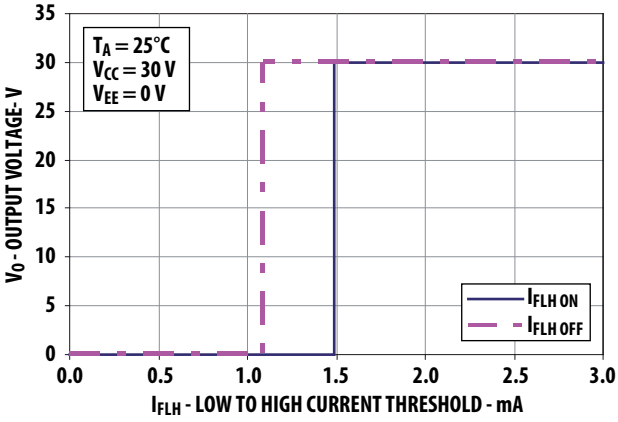


Figure 12. I_{FLH} hysteresis.

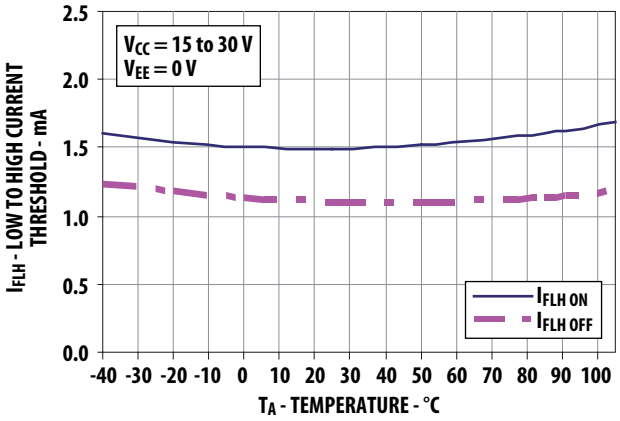


Figure 13. I_{FLH} vs. temperature.

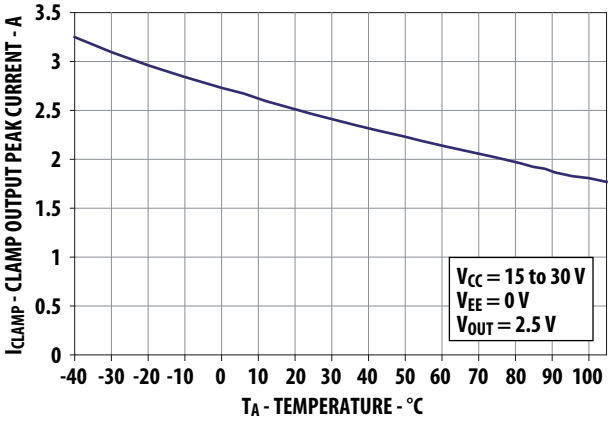


Figure 14. I_{CLAMP} vs. temperature.

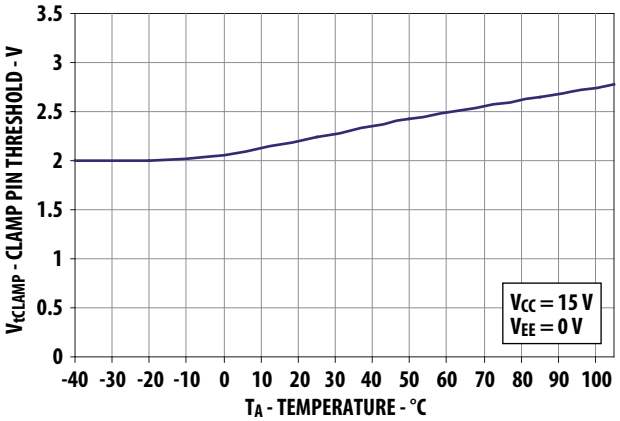


Figure 15. V_{tCLAMP} vs. temperature.

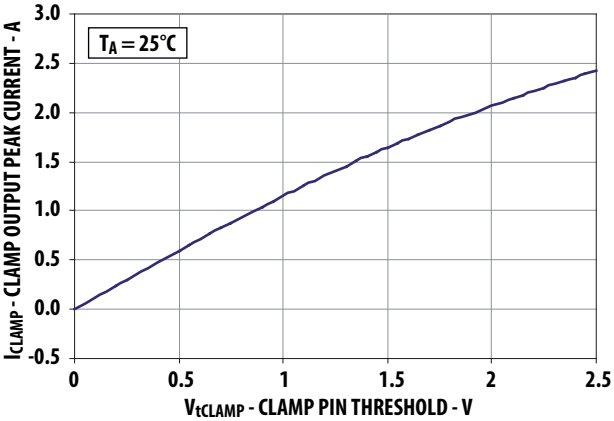


Figure 16. I_{CLAMP} vs. V_{tCLAMP}.

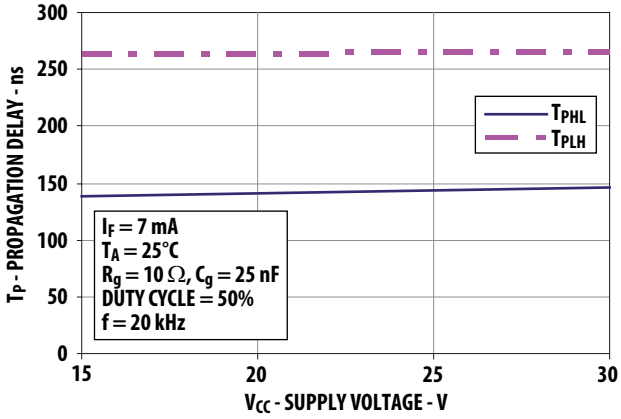


Figure 17. Propagation delay vs. V_{CC}.

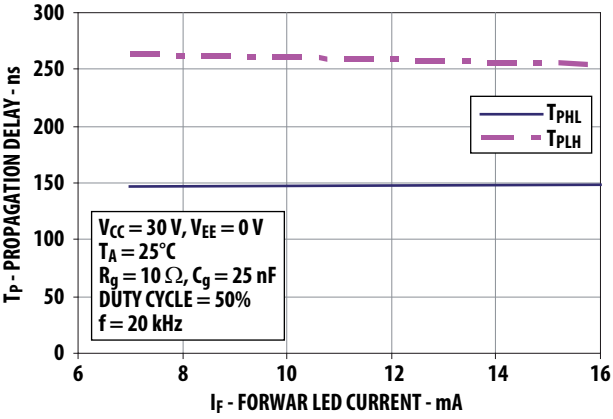


Figure 18. Propagation delay vs. I_F.

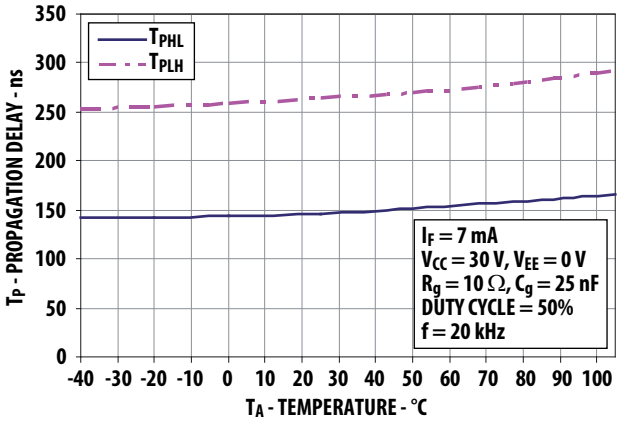


Figure 19. Propagation delay vs. temperature.

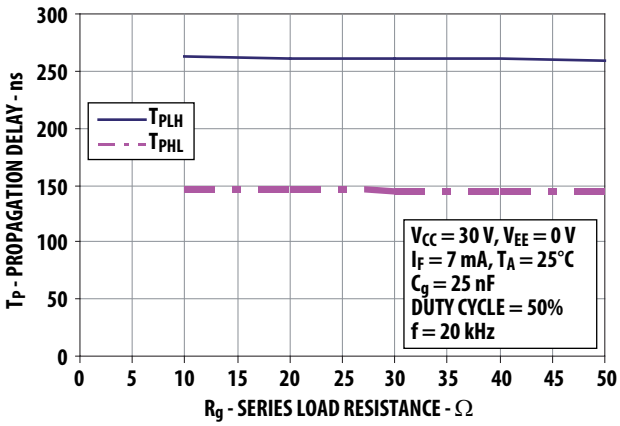


Figure 20. Propagation delay vs. Rg.

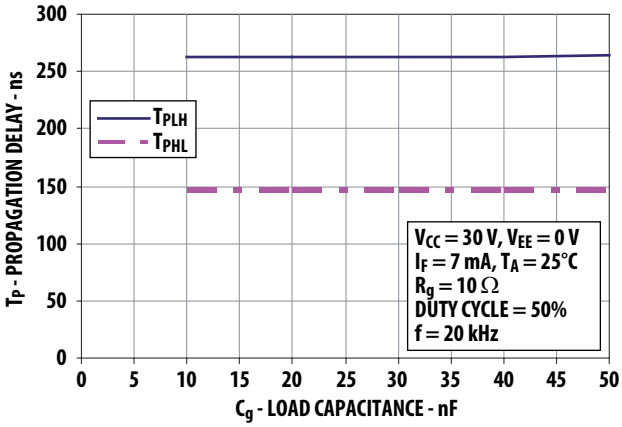


Figure 21. Propagation delay vs. Cg.

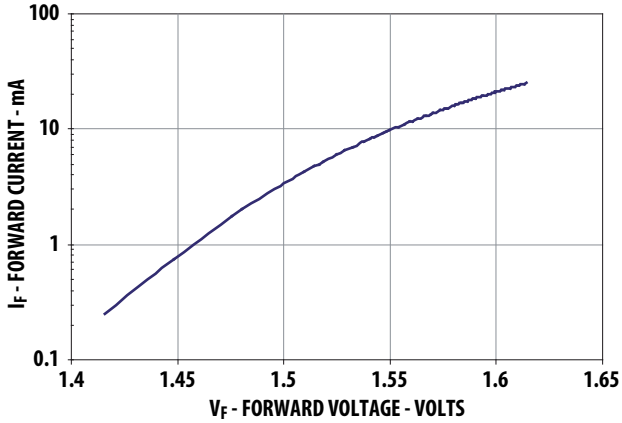


Figure 22. Input current vs. forward voltage.

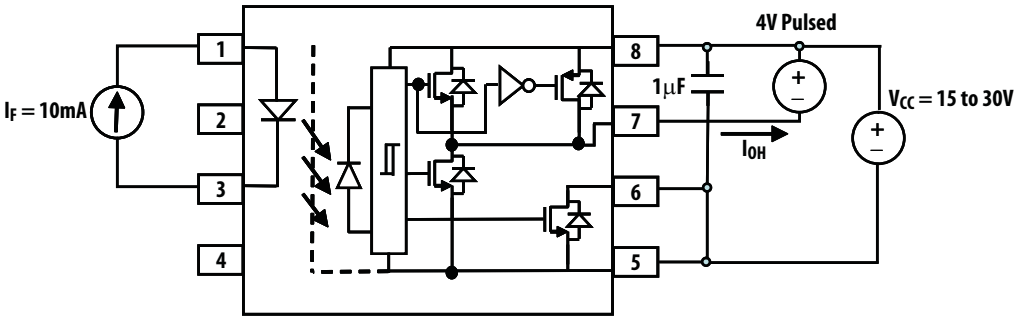


Figure 23. I_{OH} test circuit.

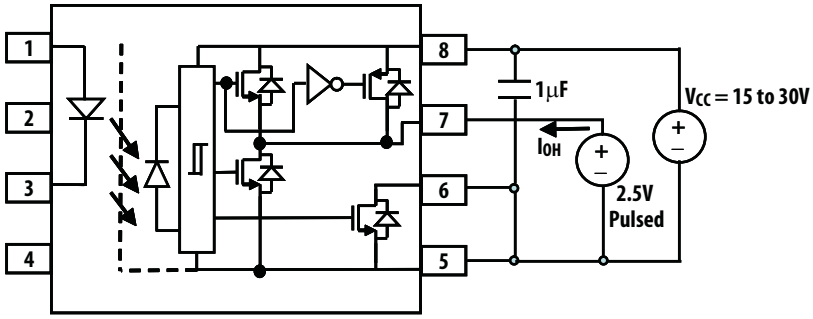


Figure 24. I_{OL} test circuit.

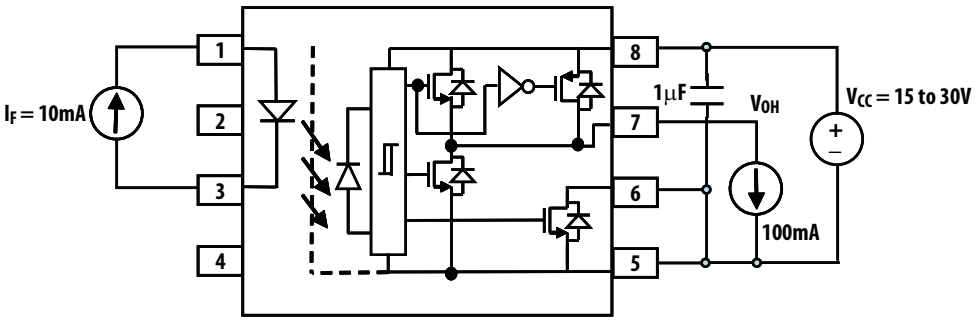


Figure 25. V_{OH} test circuit.

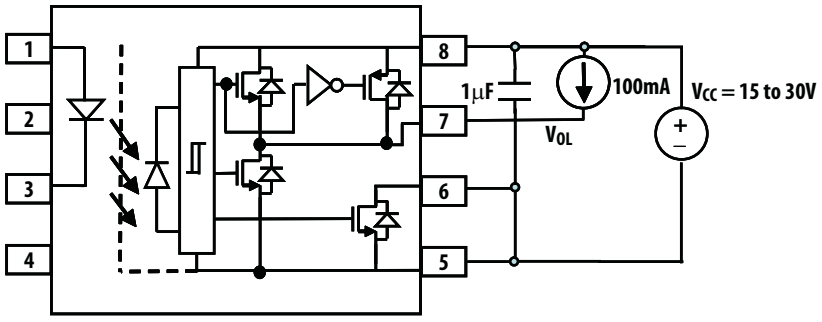


Figure 26. V_{OL} test circuit.

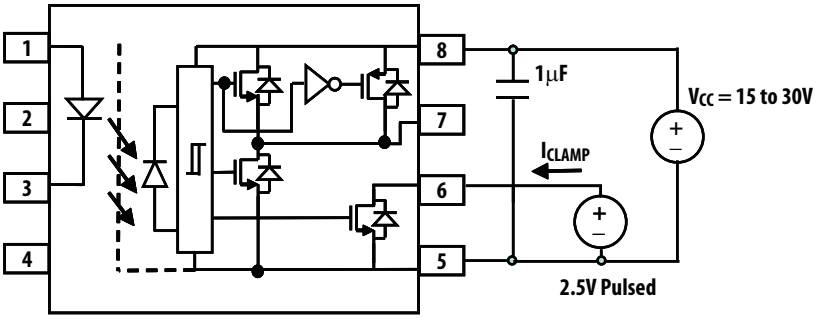


Figure 27. I_{CLAMP} test circuit.

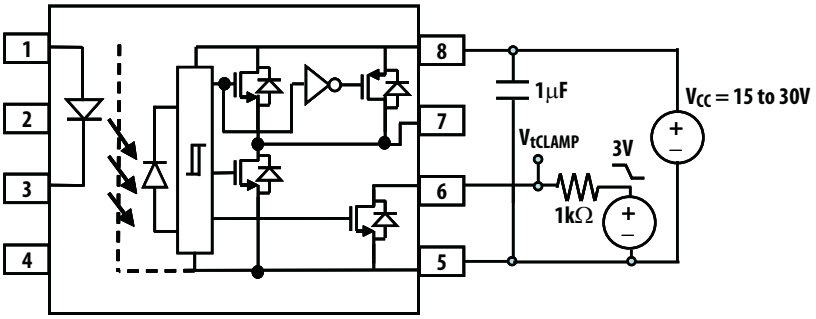


Figure 28. V_{tCLAMP} test circuit.

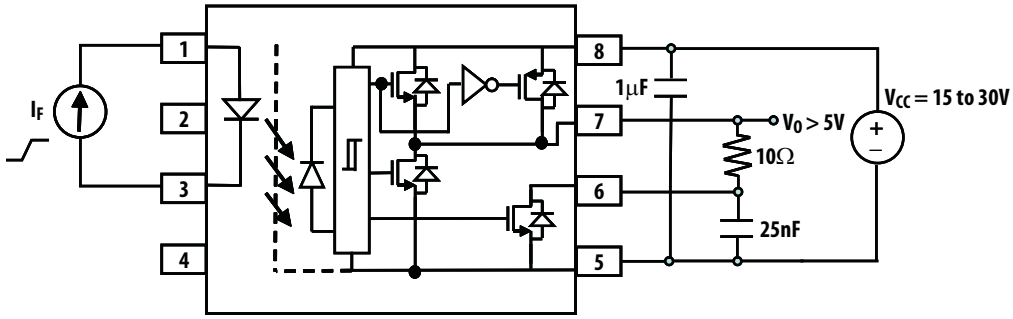


Figure 29. I_{FLH} test circuit.

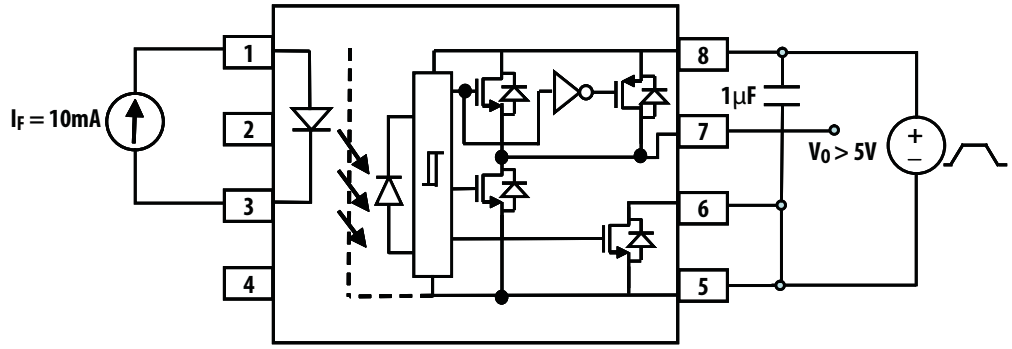


Figure 30. UVLO test circuit.

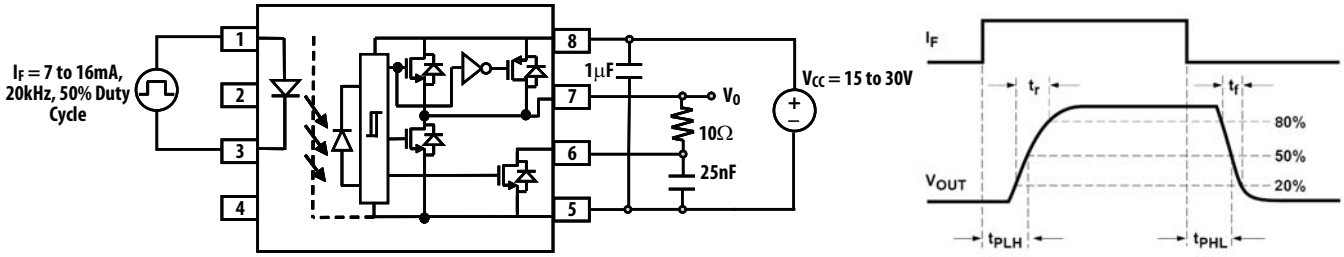


Figure 31. t_{PLH}, t_{PHL}, t_r and t_f test circuit and waveforms.

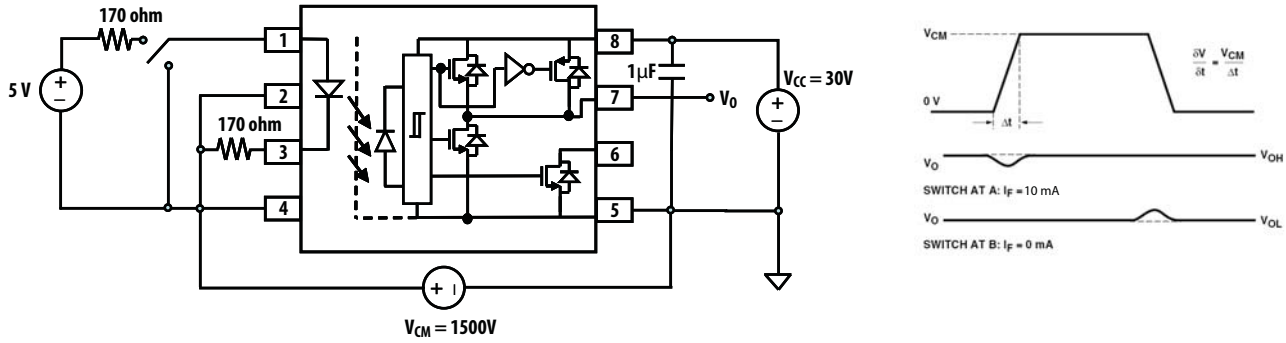


Figure 32. CMR test circuit with split resistors network and waveforms.

Application Information

Product Overview Description

The ACPL-H342/K342 is an optically isolated power output stage capable of driving IGBTs of up to 150 A and 1200 V. It has very high CMR rating which allows the microcontroller and the IGBT to operate at very large common mode noise found in industrial motor drives and other power switching applications. And to achieve better system reliability in such noisy environment, this power control device incorporates new features like Active Miller clamp, Rail-to-Rail output voltage, Anti-cross conduction and LED input current hysteresis.

Active Miller clamp function eliminates the need of negative gate drive in most application and allows the use of simple bootstrap supply for high side driver. Rail-to-Rail output voltage ensures that the IGBT's gate voltage is driven to the optimum intended level with no power loss across IGBT. Anti-cross conduction prevents current shoot through between the high and low side of half bridge IGBT configuration. This will help to simplify the controller design in terms of having to account for the delay needed at the LED input. And lastly, the LED input current hysteresis prevents output oscillation if insufficient LED driving current is applied. This will eliminates the need of additional Schmitt trigger circuit at the input LED.

This feature rich IGBT gate driver is designed to increase the performance and reliability of a motor drive without the cost, size, and complexity of external circuitry or control.

Recommended Application Circuit

The recommended application circuit shown in Figure 33 illustrates a typical gate drive implementation using the ACPL-H342. The following describes about driving IGBT. However, it is also applicable to MOSFET. Designers will need to adjust the V_{CC} supply voltage, depending on the MOSFET or IGBT gate threshold requirements (Recommended V_{CC} = 18V for IGBT and 12V for MOSFET).

The supply bypass capacitors (1 µF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (2.5mA) power supply will be enough to power the device. The split resistors across the LED will provide a high CMR response by providing a balanced resistance network across the LED.

The gate resistor R_G serves to limit gate charge current and controls the IGBT collector voltage rise and fall times.

In PC board design, care should be taken to avoid routing the IGBT collector or emitter traces close to the ACPL-H342 input as this can result in unwanted coupling of transient signals into ACPL-H342 and degrade performance.

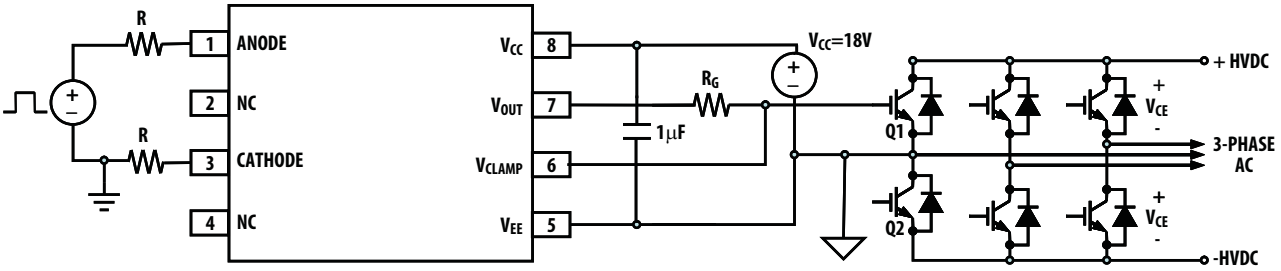


Figure 33. Recommended application circuit with split resistors LED drive and active Miller Clamp.

Active Miller Clamp

A Miller clamp allows the control of the Miller current during a high dV/dt situation. And it can also eliminate the use of a negative supply voltage by quickly discharging the large gate capacitance of IGBT to low level without affecting the IGBT turn-off characteristics. During turn-off, the gate voltage is monitored and the clamp output is activated when gate voltage goes below 2.3V (relative to V_{EE}). The clamp voltage is V_{OL}+2.5V typ for a Miller current up to 2.5 A. The clamp is disabled when the LED input is triggered again.

AN5314 application note describes how the clamp reduces the parasitic turn-on effect due to the Miller capacitor and at the same time eliminates the need of a negative power supply.

The Miller pin should be connected to V_{EE} when not in use.

Rail-to-Rail Output

Figure 34 shows a typical gate driver's high current output stage with 3 bipolar transistors in darlington configuration. During the output high transition, the output voltage rises rapidly to within 3 diode drops of V_{CC}. To ensure the V_{OUT} is at V_{CC} in order to achieve IGBT rated $V_{CE(ON)}$ voltage. The level of V_{CC} will be need to be raised to beyond V_{CC}+3(V_{BE}) to account for the diode drops. And to limit the output voltage to V_{CC}, a pull-down resistor, $R_{PULL-DOWN}$ between the output and V_{EE} is recommended to sink a static current while the output is high.

ACPL-H342 uses a power NMOS follower stage to deliver the initial large current and a smaller PMOS to pull it to V_{CC} to achieve Rail-to-Rail output voltage as shown in Figure 35. This ensures that the IGBT's gate voltage is driven to the optimum intended level with no power loss across IGBT even when an unstable power supply is used.

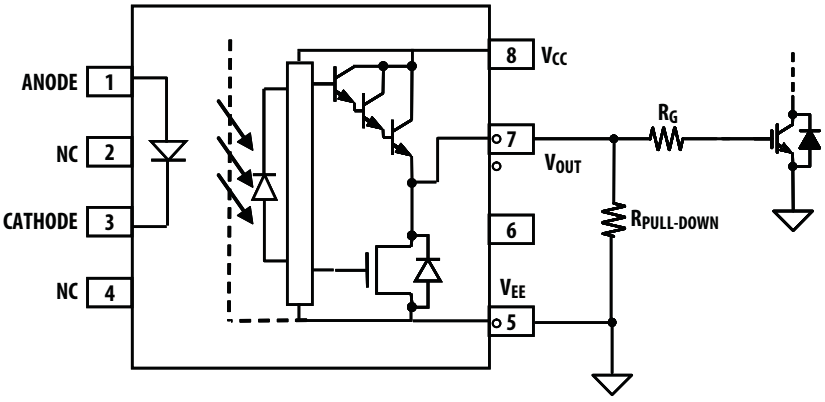


Figure 34. Typical gate driver with output stage in darlington configuration

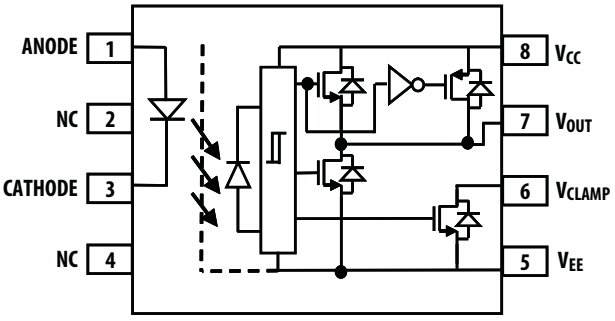


Figure 35. ACPL-H342 with NMOS and PMOS output stage for Rail-to-Rail output voltage

Selecting the Gate Resistor (Rg)

Step 1: Calculate Rg minimum from the IOL peak specification. The IGBT and Rg in Figure 33 can be analyzed as a simple RC circuit with a voltage supplied by ACPL-H342/K342.

$$Rg \geq \frac{V_{CC} - V_{EE} - V_{OL}}{I_{OLPEAK}}$$

$$= \frac{18V - 0V - 2.3V}{2.5A}$$

$$= 6.28\Omega \approx 7\Omega$$

The V_{OL} value of 2.3V in the previous equation is the V_{OL} at the peak current of 2.5A (see Figure 7).

Step 1: Check the ACPL-H342/K342 power dissipation and increase Rg if necessary. The ACPL-H342/K342 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$P_T = P_E + P_O$

$P_E = I_F \cdot V_F \cdot \text{Duty Cycle}$

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$

$= I_{CC} \cdot (V_{CC}-V_{EE}) + E_{SW}(Rg;Qg) \cdot f$

Using I_F(worst case) = 16mA, Rg = 7Ω, Max Duty Cycle = 80%, Qg = 500nC, f = 25kHz and T_A max = 85°C:

$P_E = 16mA \cdot 1.95V \cdot 0.8 = 32mW$

$P_O = 2.5mA \cdot 18V + 4\mu J \cdot 25\ kHz$

$= 45mW + 100mW$

$= 145mW < 210mW\ (P_{O(MAX)} @ 85°C)$

The value of 2.5mA for I_{CC} in the previous equation is the maximum I_{CC} over the entire operating temperature range.

Since P_O is less than $P_{O(MAX)}$, Rg = 7Ω is alright for the power dissipation.

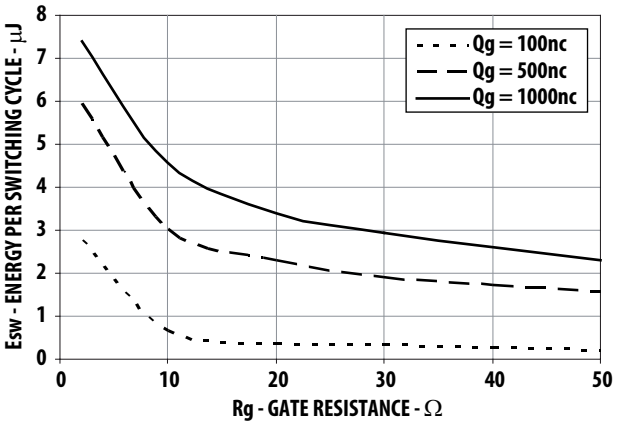
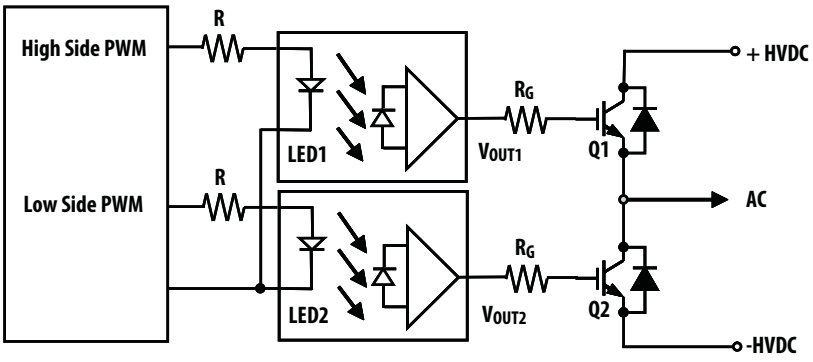


Figure 36. Energy Dissipated in the ACPL-H342/K342 for each IGBT switching cycle.

Anti-Cross Conduction to Prevent Current Shoot Through and Determining Dead Time

The ACPL-H342 includes a Propagation Delay Difference (PDD = $t_{PHL} - t_{PLH}$) specification to help prevent both the high(Q1) and low(Q2) side power transistors from turning on at the same time. This "Anti-Cross" conduction feature prevents large currents from flowing through the power transistors by ensuring t_{PHLMAX} is faster than t_{PLHMIN}. In another words, the "Anti-Cross" feature will ensure one power transistor is turned off before the other is turned on.

A gate driver without Anti-Cross feature will for example has a PDD_{MIN} of -350ns and a PDD_{MAX} of 350ns. A positive PDD_{MAX} of 350ns would mean one transistor will be turn on before the other is off since t_{PHLMAX} is longer than t_{PLHMIN}. This is shown in Figure 37. To prevent this and the shoot through current, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, Q1 has just turned off when Q2 turns on. The amount of delay to achieve this condition is equal to PDD_{MAX} as shown in Figure 38.



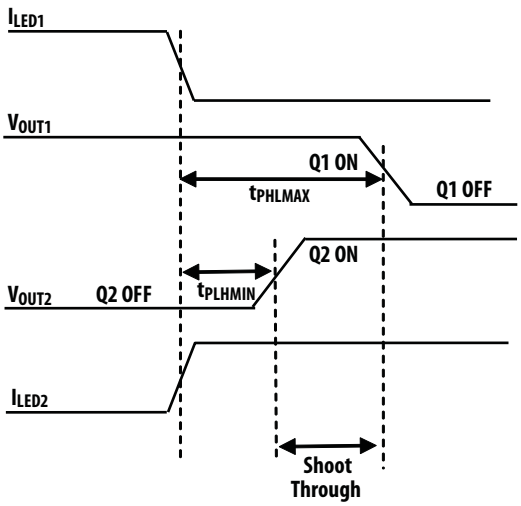


Figure 37. Current shoot through without Anti-Cross feature

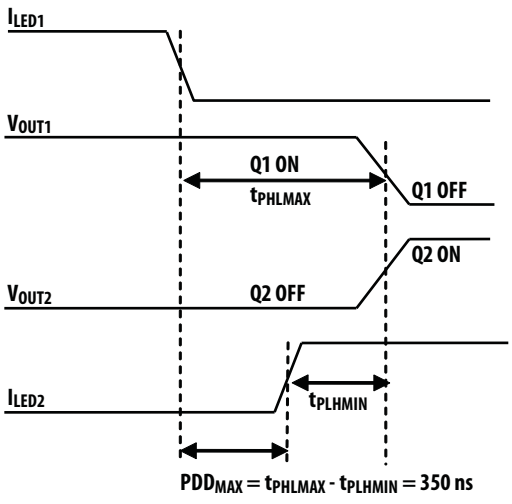


Figure 38. Adding delay to prevent shoot through

The ACPL-H342 with the Anti-Cross feature has a PDD_{MIN} of -10ns and a PDD_{MAX} of -200ns. Since the PDD is always a negative value, the t_{PHLMAX} is always faster than t_{PLHMIN}. Thus this simplified the design without having to add any amount of delay for the input LEDs as shown in Figure 39.

Symbol	Min.	Typ.	Max.	Units
t_{PLH}	0.100	0.260	0.350	µs
t_{PHL}	0.050	0.145	0.250	µs
PDD (t_{PHL} - t_{PLH})	-0.010	-0.100	-0.200	µs

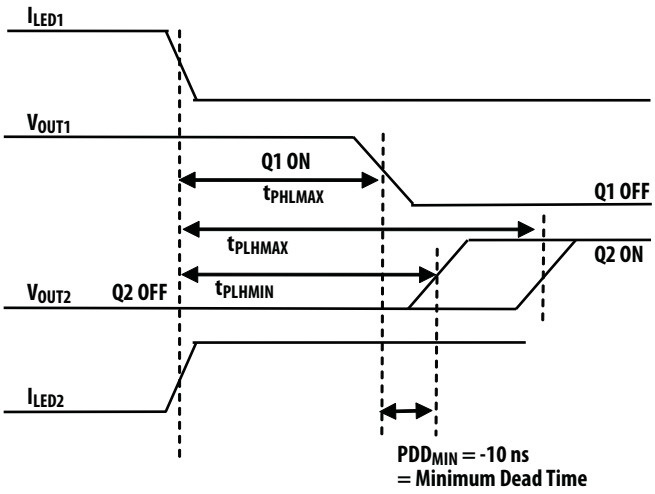


Figure 39. Anti-Cross to prevent shoot through

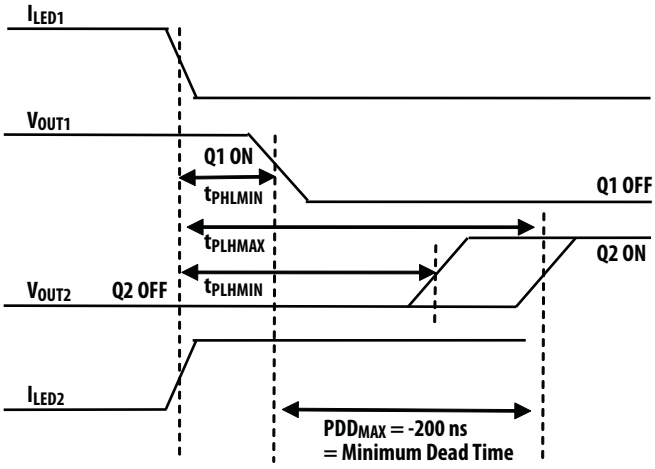


Figure 40. Determining maximum dead time

Dead time is the time period during which both the high(Q1) and low(Q2) side transistor are off. During this time, no work is done and this reduces the efficiency of the inverter or motor drive. The minimum and maximum dead time is shown in Figure 39 and 40 and is equivalent to the PDD_{MIN} and PDD_{MAX} . Due to the smaller PDD and skewed propagation delay configuration, ACPL-H342 shows a smaller maximum dead time as compared to its predecessor, HCPL-3120 as shown in figure 41 and hence an improve in efficiency. Note that the propagation delays used to calculate PDD and dead time are taken at equal temperature and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

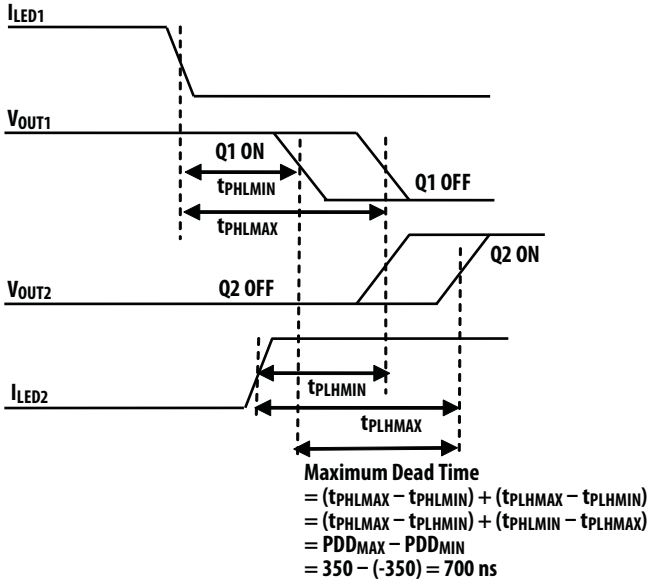


Figure 41. HCPL-3120 maximum dead time

LED Input Current Hysteresis

The detector has optical receiver input stage with built in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The hysteresis (Figure 12) provides differential mode noise immunity and minimizes the potential for output signal chatter.

Under Voltage Lockout

The ACPL-H342 Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the ACPL-H342 output low during power-up. IGBTs typically require gate voltages of 15 V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 13 V typically, the $V_{CE(ON)}$ voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10 V), the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply (V_{CC}) is applied. Once V_{CC} exceeds V_{UVLO+} (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals.

Thermal Model for ACPL-H342/K342 Stretched SO8 Package Optocoupler

Definitions:

R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED

R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)

R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

P_1: Power dissipation of LED (W).

P_2: Power dissipation of Detector / Output IC (W).

T_1: Junction temperature of LED (°C).

T_2: Junction temperature of Detector (°C).

T_A: Ambient temperature.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25cm above optocoupler at ~23°C in still air

Thermal Resistance	°C/W
R_{11}	311
R_{12}, R_{21}	111
R_{22}	168

This thermal model assumes that an 8-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB) per JEDEC standards. The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$T_1 = (R_{11} * P_1 + R_{12} * P_2) + T_A \quad (1)$$

$$T_2 = (R_{21} * P_1 + R_{22} * P_2) + T_A \quad (2)$$

Using the given thermal resistances and thermal model formula in this datasheet, we can calculate the junction temperature for both LED and the output detector. Both junction temperature should be within the absolute maximum rating.

For example, given P_1 = 45 mW, P_2 =210 mW, Ta = 85°C:

LED junction temperature,

$T_1 = (R_{11} * P_1 + R_{12} * P_2) + T_A$
$= (311 * 0.045 + 111 * 0.210) + 85$
$= 122°C$

Output IC junction temperature,

$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_A$
$= (111 * 0.045 + 168 * 0.210) + 85$
$= 125°C$

T_1 and T_2 should be limited to 125°C based on the board layout and part placement.

Related Application Noted

AN5336 – Gate Drive Optocoupler Basic Design for IGBT/MOSFET

AN1043 – Common-Mode Noise: Sources and Solutions

AN02-0310EN – Plastics Optocouplers Product ESD and Moisture Sensitivity

AV02-2526EN - June 11, 2010