

MTM86128

Silicon P-channel MOS FET

For DC-DC converter circuits

For switching circuits

■ Overview

MTM86128 is the P-channel MOS FET that is highly suitable for DC-DC converter and other switching circuits.

■ Features

- Low ON resistance: $R_{on} = 300 \text{ m}\Omega$ (typ.) ($V_{GS} = 4.0 \text{ V}$)
- Low short-circuit input capacitance (common source): $C_{iss} = 80 \text{ pF}$ (typ.)
- Small surface mounting halogen-free package: WSSMini6-F1 (1.6 mm × 1.6 mm × 0.5 mm)

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	-20	V
Gate-source surrender voltage	V_{GSS}	± 12	V
Drain current	I_D	-1.0	A
Peak drain current	I_{DP}	-4.0	A
Power dissipation	P_{D1}^{*1}	540	mW
	P_{D2}^{*2}	150	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note) *1: Glass epoxy board: 25.4 mm × 25.4 mm × t 0.8 mm
 Copper foil of the drain portion should have a area of 300 mm² or more
 *2: Stand-alone (without the board)

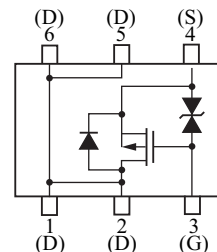
■ Package

- Code
WSSMini6-F1
- Pin Name

1: Drain	4: Source
2: Drain	5: Drain
3: Gate	6: Drain

■ Marking Symbol: ML

■ Internal Connection



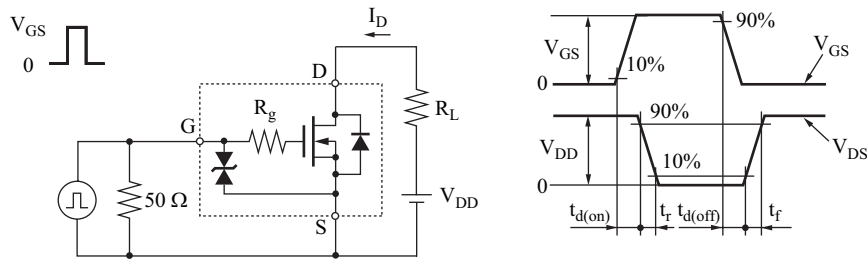
■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

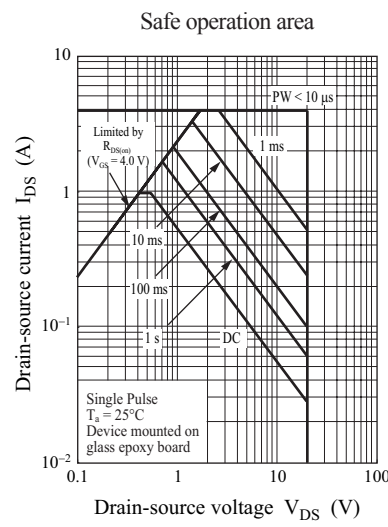
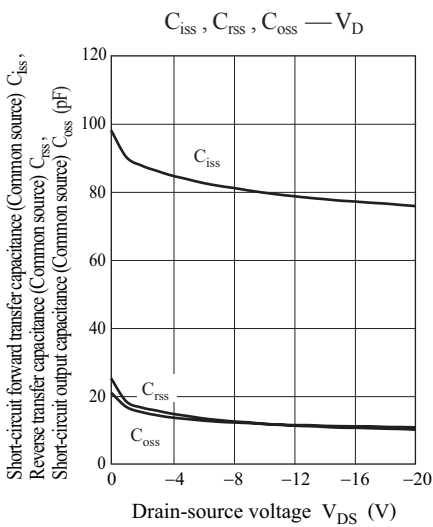
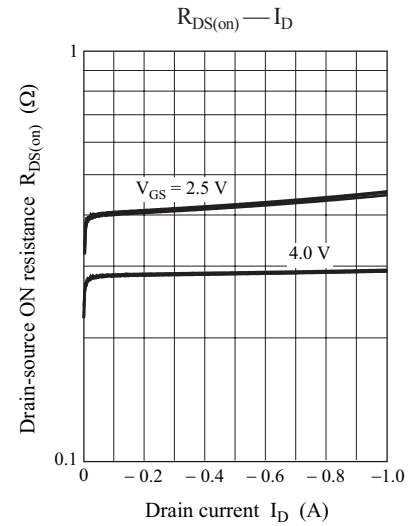
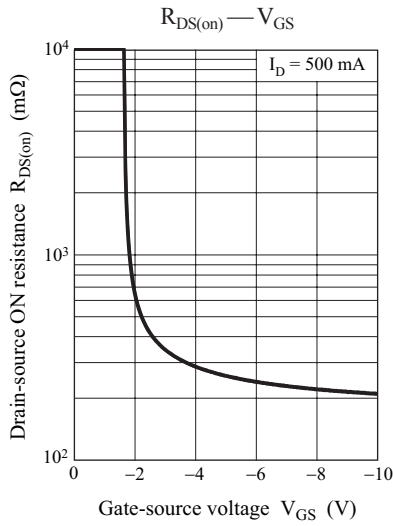
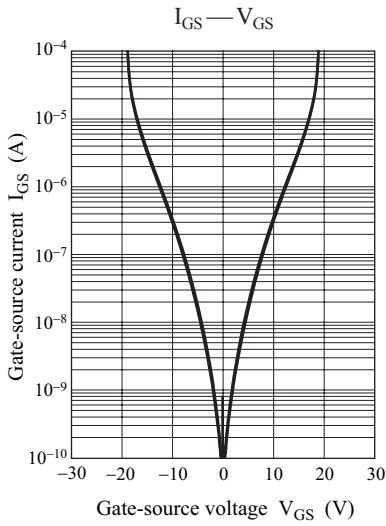
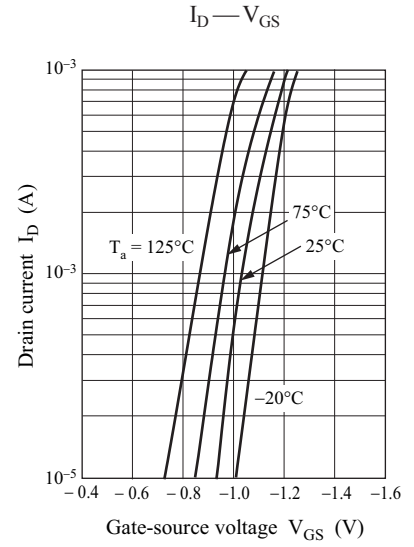
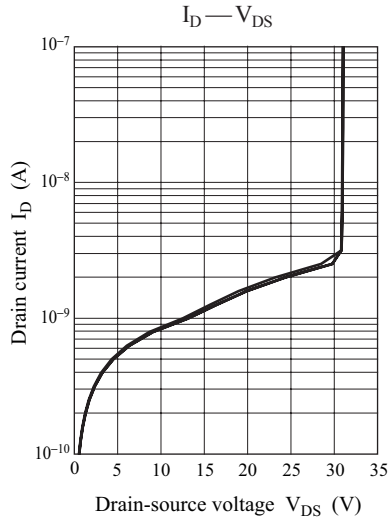
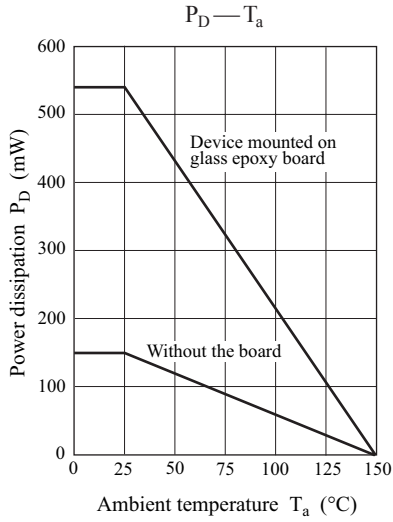
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	$I_D = -1.0 \text{ mA}, V_{GS} = 0$	-20			V
Drain-source cutoff current	I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0$			-1.0	μA
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$			± 10	μA
Gate threshold voltage	V_{TH}	$I_D = -1.0 \text{ mA}, V_{DS} = -10 \text{ V}$	-0.45	-1.0	-1.5	V
Drain-source ON resistance	$R_{DS(on)1}$	$I_D = -0.5 \text{ A}, V_{GS} = -4.0 \text{ V}$		300	420	$\text{m}\Omega$
	$R_{DS(on)2}$	$I_D = -0.5 \text{ A}, V_{GS} = -2.5 \text{ V}$		420	560	$\text{m}\Omega$
Forward transfer admittance ^{*1}	$ Y_{fs} $	$I_D = -0.5 \text{ A}, V_{DS} = -10 \text{ V}$	1.0	2.0		S
Short-circuit input capacitance (Common source)	C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		80		pF
Short-circuit output capacitance (Common source)	C_{oss}			12		pF
Reverse transfer capacitance (Common source)	C_{rss}			12		pF
Turn-on delay time ^{*1, 2}	$t_{d(on)}$				12	
Rise time ^{*1, 2}	t_r	$V_{DD} = -15 \text{ V}, V_{GS} = -4.0 \text{ V},$ $I_D = -0.5 \text{ A}, R_L = 30 \Omega$		6		ns
Turn-off delay time ^{*1, 2}	$t_{d(off)}$			17		ns
Fall time ^{*1, 2}	t_f			10		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *1: $t = 10 \mu\text{s}$, Duty cycle < 1%

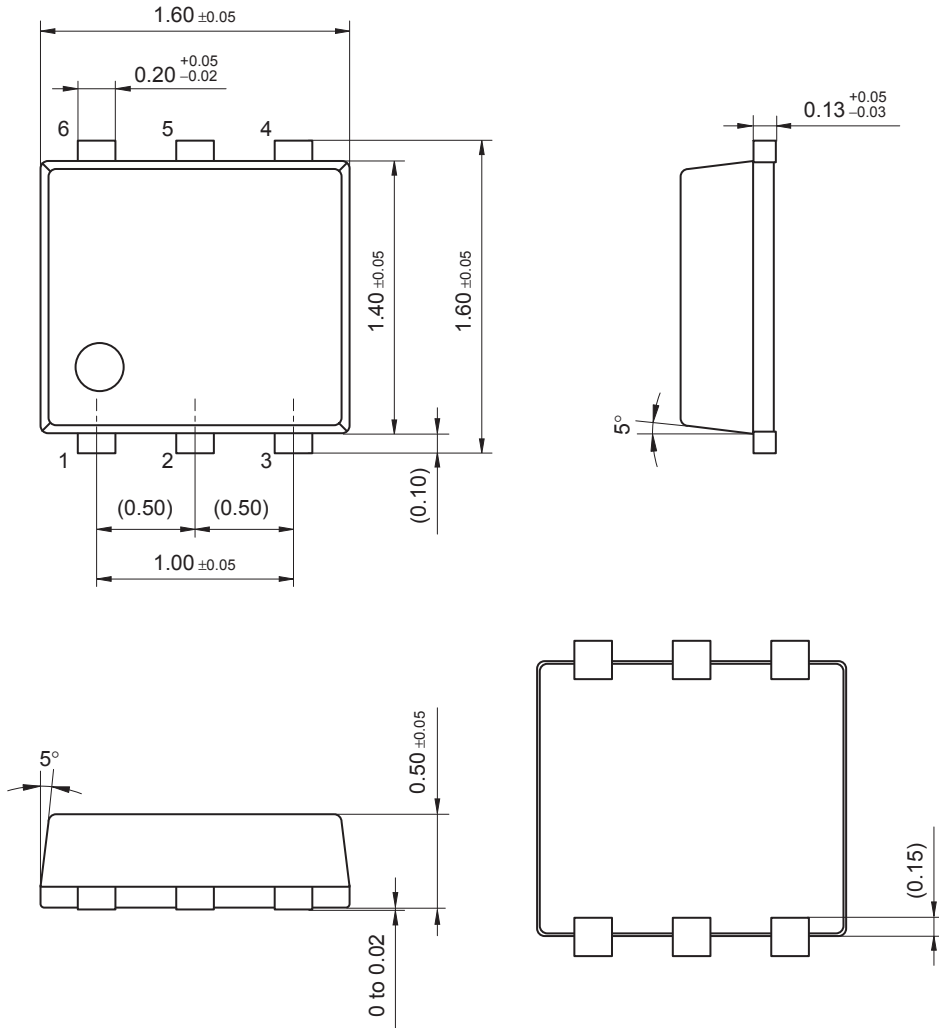
*2: Test circuit





WSSMini6-F1

Unit: mm



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