TelCom Semiconductor, Inc.

**TC7126**
**TC7126A**

# 3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS

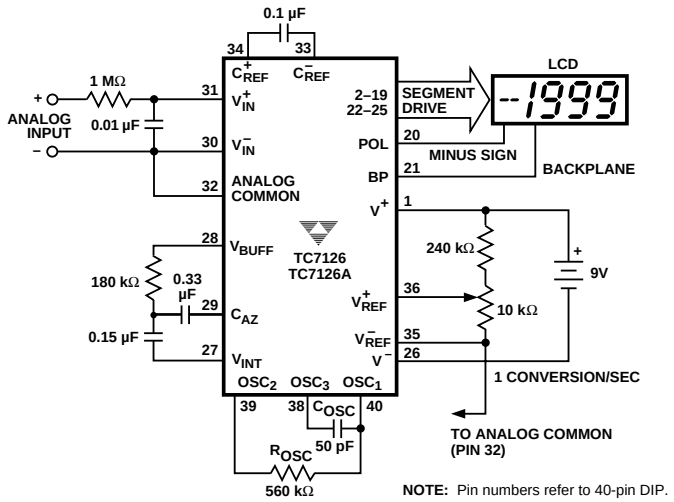
## FEATURES

- **Low Temperature Drift Internal Reference**
  - **TC7126 ..... 80 ppm/°C Typ.**
  - **TC7126A ..... 35 ppm/°C Typ.**
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise ..... 15$\mu V_{P-P}$**
- **High Resolution ..... 0.05%**
- **Low Input Leakage Current ..... 1pA Typ. 10pA Max**
- **Precision Null Detectors With True Polarity at Zero**
- **High-Impedance Differential Input**
- **Convenient 9V Battery Operation With Low Power Dissipation ..... 500$\mu$W Typ. 900$\mu$W Max**

## TYPICAL APPLICATIONS

- **Thermometry**
- **Bridge Readouts: Strain Gauges, Load Cells, Null Detectors**
- **Digital Meters and Panel Meters — Voltage/Current/Ohms/Power, pH**
- **Digital Scales, Process Monitors**

### TYPICAL OPERATING CIRCUIT




**NOTE:** Pin numbers refer to 40-pin DIP.

## GENERAL DESCRIPTION

The TC7126A is a 3-1/2 digit CMOS analog-to-digital converter (ADC) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, digit and polarity drivers, voltage reference, and clock circuit are integrated on-chip. The TC7126A directly drives a liquid crystal display (LCD), and includes a backplane driver.

A low-cost, high-resolution indicating meter requires only a display, four resistors, and four capacitors. The TC7126A's extremely low power drain and 9V battery operation make it ideal for portable applications.

The TC7126A reduces linearity error to less than 1 count. Roll-over error (the difference in readings for equal magnitude but opposite polarity input signals) is below ±1 count. High-impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The 15 $\mu V_{P-P}$ noise performance guarantees a "rock solid" reading, and the auto-zero cycle guarantees a zero display reading with a 0V input.

The TC7126A features a precision, low-drift internal voltage reference and is functionally identical to the TC7126. A low-drift external reference is not normally required with the TC7126A.

## ORDERING INFORMATION

**PART CODE** **TC7126X X XXX**

**A or blank*** —

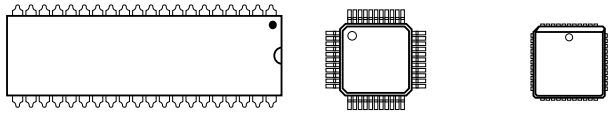
**R (reversed pins) or blank (CPL pkg only)** —

* "A" parts have an improved reference TC

**Package Code** (see below): —

| Package Code | Package | Temperature Range |
|---|---|---|
| CKW | 44-Pin PQFP | 0°C to +70°C |
| CLW | 44-Pin PLCC | 0°C to +70°C |
| CPL | 40-Pin PDIP | 0°C to +70°C |
| IPL | 40-Pin PDIP (non-A only) | – 25°C to +85°C |

### AVAILABLE PACKAGES



**40-Pin Plastic DIP** | **44-Pin Plastic Quad Flat Package Formed Leads** | **44-Pin Plastic Chip Carrier PLCC**

# TC7126
# TC7126A

## ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ($V^+$ to $V^-$) ..... +15V
Analog Input Voltage (Either Input) (Note 1) ..... $V^+$ to $V^-$
Reference Input Voltage (Either Input) ..... $V^+$ to $V^-$
Clock Input ..... TEST to $V^+$
Operating Temperature Range
- C Devices ..... 0°C to +70°C
- I Devices ..... – 25°C to +85°C

Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Power Dissipation ($T_A \leq 70°C$) (Note 2)
- 44-Pin PQFP ..... 1.00W
- 44-Pin PLCC ..... 1.23W
- 40-Pin PDIP ..... 1.23W

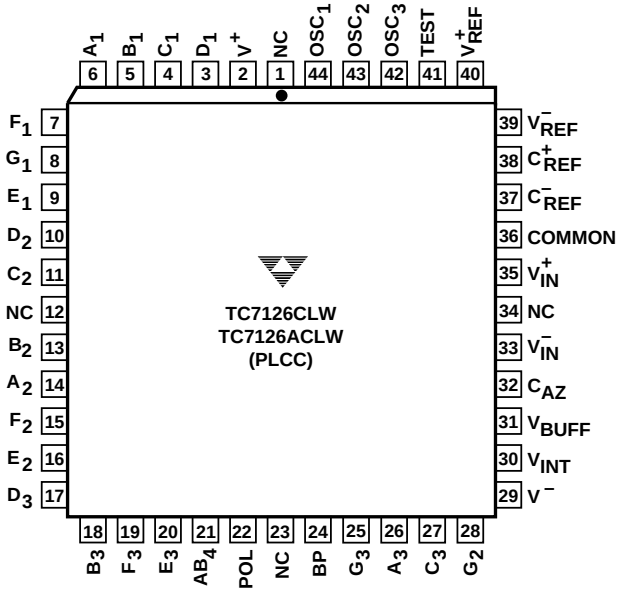
*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

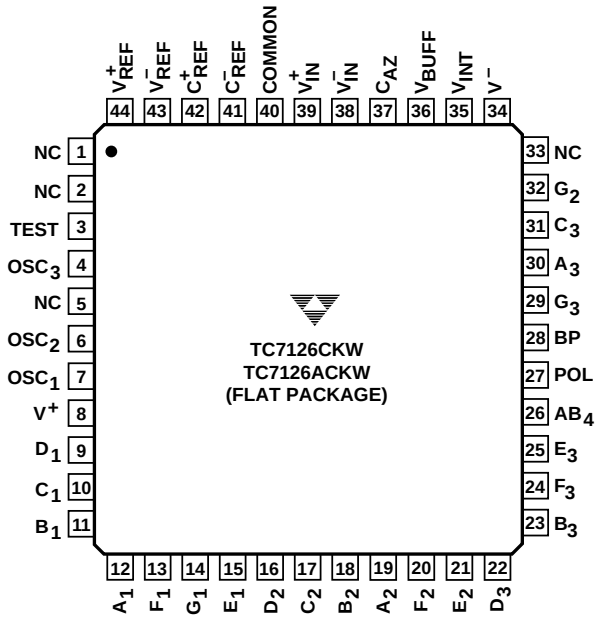
## ELECTRICAL CHARACTERISTICS: $V_S$ = +9V, $f_{CLK}$ = 16kHz, and $T_A$ = +25°C, unless otherwise noted.

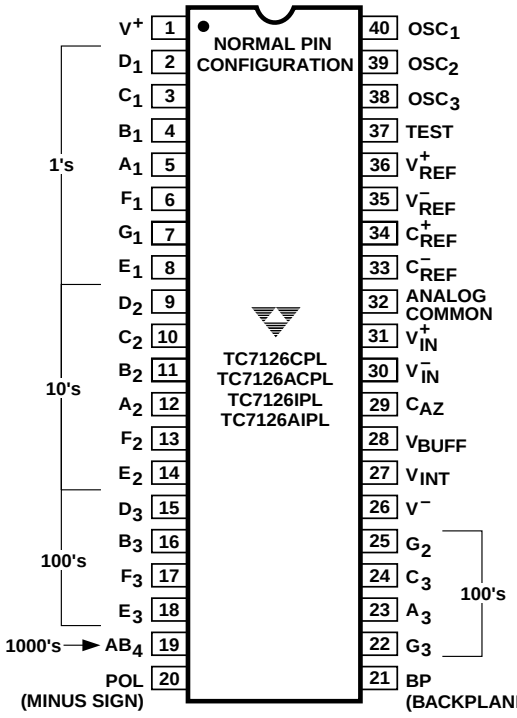
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| | Zero Input Reading | $V_{IN}$ = 0V<br>Full Scale = 200mV | –000.0 | ±000.0 | +000.0 | Digital Reading |
| | Zero Reading Drift | $V_{IN}$ = 0V, 0°C ≤ $T_A$ ≤ +70°C | — | 0.2 | 1 | µV/°C |
| | Ratiometric Reading | $V_{IN}$ = $V_{REF}$, $V_{REF}$ = 100mV | 999 | 999/1000 | 1000 | Digital Reading |
| NL | Linearity Error | Full Scale = 200mV or 2V<br>Max Deviation From Best Fit Straight Line | – 1 | ±0.2 | 1 | Count |
| | Roll-Over Error | $-V_{IN}$ = $+V_{IN}$ ≈ 200mV | | – 1 | ±0.2 | 1 Count |
| $e_N$ | Noise | $V_{IN}$ = 0V, Full Scale = 200mV | — | 15 | — | $\mu V_{P-P}$ |
| $I_L$ | Input Leakage Current | $V_{IN}$ = 0V | — | 1 | 10 | pA |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = ±1V, $V_{IN}$ = 0V,<br>Full Scale = 200mV | — | 50 | — | µV/V |
| | Scale Factor Temperature Coefficient | $V_{IN}$ = 199mV, 0°C ≤ $T_A$ ≤ +70°C<br>Ext Ref Temp Coeff = 0ppm/°C | — | 1 | 5 | ppm/°C |
| **Analog Common** | | | | | | |
| $V_{CTC}$ | Analog Common Temperature Coefficient | 250kΩ Between Common and $V^+$ | — | — | — | — |
| | | 0°C ≤ $T_A$ ≤ +70°C ("C" Devices): | — | — | — | — |
| | | TC7126 | — | 80 | — | ppm/°C |
| | | TC7126A | — | 35 | 75 | ppm/°C |
| | | – 25°C ≤ $T_A$ ≤ +85°C ("I" Device): | | | | |
| | | TC7126A | — | 35 | 100 | ppm/°C |
| $V_C$ | Analog Common Voltage | 250kΩ Between Common and $V^+$ | 2.7 | 3.05 | 3.35 | V |
| **LCD Drive** | | | | | | |
| $V_{SD}$ | LCD Segment Drive Voltage | $V^+$ to $V^-$ = 9V | 4 | 5 | 6 | $V_{P-P}$ |
| $V_{BD}$ | LCD Backplane Drive Voltage | $V^+$ to $V^-$ = 9V | 4 | 5 | 6 | $V_{P-P}$ |
| **Power Supply** | | | | | | |
| $I_S$ | Power Supply Current | $V_{IN}$ = 0V, $V^+$ to $V^-$ = 9V (Note 6) | — | 55 | 100 | µA |

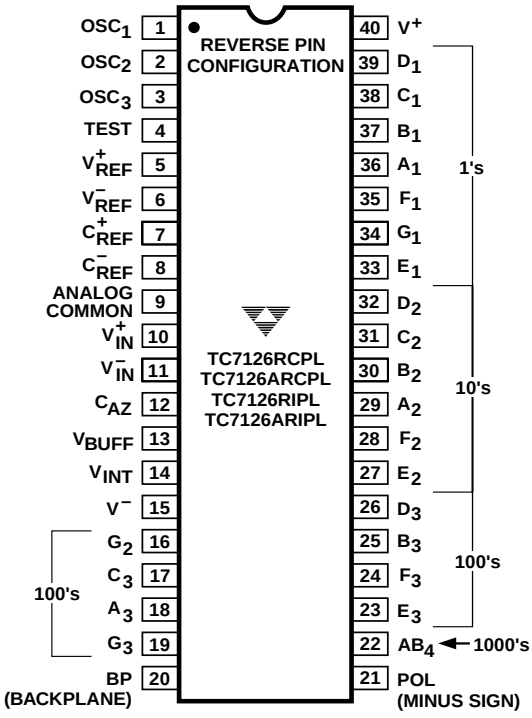
**NOTES:**
1. Input voltage may exceed supply voltages when input current is limited to 100µA.
2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
3. Refer to "Differential Input" discussion.
4. Backplane drive is in-phase with segment drive for "OFF" segment and 180° out-of-phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
5. See "Typical Operating Circuit."
6. During auto-zero phase, current is 10–20 µA higher. A 48kHz oscillator increases current by 8µA (typical). Common current not included.

## PIN CONFIGURATIONS




NC = NO INTERNAL CONNECTION

## PIN DESCRIPTION

| Pin No. 40-Pin PDIP Normal | (Reverse) | Name | Description |
|---|---|---|---|
| 1 | (40) | $V^+$ | Positive supply voltage. |
| 2 | (39) | $D_1$ | Activates the D section of the units display. |
| 3 | (38) | $C_1$ | Activates the C section of the units display. |
| 4 | (37) | $B_1$ | Activates the B section of the units display. |
| 5 | (36) | $A_1$ | Activates the A section of the units display. |
| 6 | (35) | $F_1$ | Activates the F section of the units display. |
| 7 | (34) | $G_1$ | Activates the G section of the units display. |
| 8 | (33) | $E_1$ | Activates the E section of the units display. |
| 9 | (32) | $D_2$ | Activates the D section of the tens display. |
| 10 | (31) | $C_2$ | Activates the C section of the tens display. |
| 11 | (30) | $B_2$ | Activates the B section of the tens display. |
| 12 | (29) | $A_2$ | Activates the A section of the tens display. |
| 13 | (28) | $F_2$ | Activates the F section of the tens display. |
| 14 | (27) | $E_2$ | Activates the E section of the tens display. |
| 15 | (26) | $D_3$ | Activates the D section of the hundreds display. |
| 16 | (25) | $B_3$ | Activates the B section of the hundreds display. |
| 17 | (24) | $F_3$ | Activates the F section of the hundreds display. |
| 18 | (23) | $E_3$ | Activates the E section of the hundreds display. |
| 19 | (22) | $AB_4$ | Activates both halves of the 1 in the thousands display. |
| 20 | (21) | POL | Activates the negative polarity display. |
| 21 | (20) | BP | Backplane drive output. |
| 22 | (19) | $G_3$ | Activates the G section of the hundreds display. |
| 23 | (18) | $A_3$ | Activates the A section of the hundreds display. |
| 24 | (17) | $C_3$ | Activates the C section of the hundreds display. |
| 25 | (16) | $G_2$ | Activates the G section of the tens display. |
| 26 | (15) | $V^-$ | Negative power supply voltage. |
| 27 | (14) | $V_{INT}$ | The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance buildup will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 µF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See "Integrating Capacitor" section for additional details. |
| 28 | (13) | $V_{BUFF}$ | Integration resistor connection. Use a 180 kΩ resistor for a 200 mV full-scale range and a 1.8 MΩ resistor for a 2V full-scale range. |
| 29 | (12) | $C_{AZ}$ | The size of the auto-zero capacitor influences system noise. Use a 0.33 µF capacitor for 200 mV full scale, and a 0.033 µF capacitor for 2V full scale. See paragraph on auto-zero capacitor for more details. |
| 30 | (11) | $V_{IN}^-$ | The low input signal is connected to this pin. |
| 31 | (10) | $V_{IN}^+$ | The high input signal is connected to this pin. |
| 32 | (9) | ANALOG COMMON | This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on analog common for more details. It also acts as a reference voltage source. |
| 33 | (8) | $C^-_{REF}$ | See pin 34. |

## PIN DESCRIPTION (Cont.)

| Pin No. 40-Pin PDIP Normal | (Reverse) | Name | Description |
|---|---|---|---|
| 34 | (7) | $C^+_{REF}$ | A 0.1µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the $V_{IN}^-$ pin is not at analog common), and a 200mV scale is used, a 1µF capacitor is recommended and will hold the roll-over error to 0.5 count. |
| 35 | (6) | $V^-_{REF}$ | See pin 36. |
| | (5) | $V^+_{REF}$ | The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on reference voltage. |
| 36 | (4) | TEST | Lamp test. When pulled HIGH (to $V^+$), all segments will be turned ON and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under test for additional information. |
| 37 | (3) | $OSC_3$ | See pin 40. |
| 38 | (2) | $OSC_2$ | See pin 40. |
| 40 | (1) | $OSC_1$ | Pins 40, 39 and 38 make up the oscillator section. For a 48kHz clock (3 readings 39 per second), connect pin 40 to the junction of a 180kΩ resistor and a 50pF capacitor. The 180kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38. |

## GENERAL THEORY OF OPERATION

*(All Pin Designations Refer to the 40-Pin DIP)*

### Dual-Slope Conversion Principles

The TC7126A is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7126A operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period ($t_{SI}$), measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal ($t_{RI}$).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

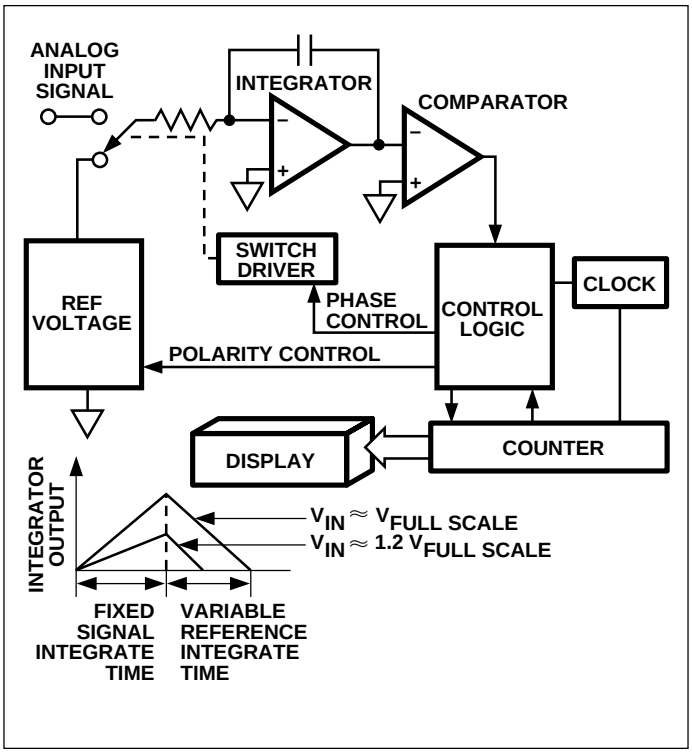



**Figure 1. Basic Dual-Slope Converter**

where:

$V_R$ = Reference voltage

$t_{SI}$ = Signal integration time (fixed)

$t_{RI}$ = Reference voltage integration time (variable).

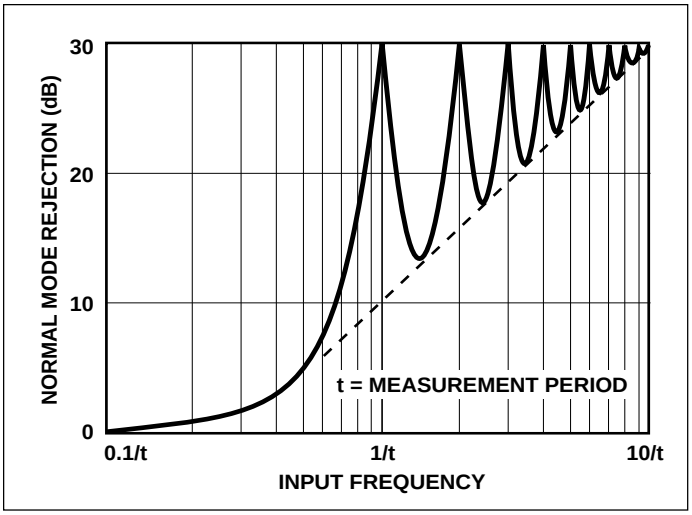



**Figure 2. Normal-Mode Rejection of Dual-Slope Converter**

For a constant $V_{IN}$:

$$V_{IN} = V_R \left( \frac{t_{RI}}{t_{SI}} \right).$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50Hz/60Hz power line period.

## ANALOG SECTION

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC7126A design incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three phases:

(1) Auto-zero phase

(2) Signal integrate phase

(3) Reference integrate phase

### Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on $C_{AZ}$ compensates for device offset voltages. The auto-zero phase residual is typically 10 μV to 15 μV.

The auto-zero cycle length is 1000 to 3000 clock periods.

### Signal Integration Phase

The auto-zero loop is entered and the internal differential inputs connect to $V_{IN}^+$ and $V_{IN}^-$. The differential input signal is integrated for a fixed time period. The TC7126A signal integration period is 1000 clock periods, or counts. The externally-set clock frequency is ÷4 before clocking the internal counters. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where $f_{OSC}$ = external clock frequency.

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, $V_{IN}^-$ should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

### Reference Integrate Phase

The third phase is reference integrate, or deintegrate. $V_{IN}^-$ is internally connected to analog common and $V_{IN}^+$ is connected across the previously-charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is:

$$1000 \frac{V_{IN}}{V_{REF}}$$

## DIGITAL SECTION

The TC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD. An LCD backplane driver is included. The backplane frequency is the external clock frequency ÷ 800. For 3 conversions per second the backplane frequency is 60Hz with a 5V nominal amplitude.

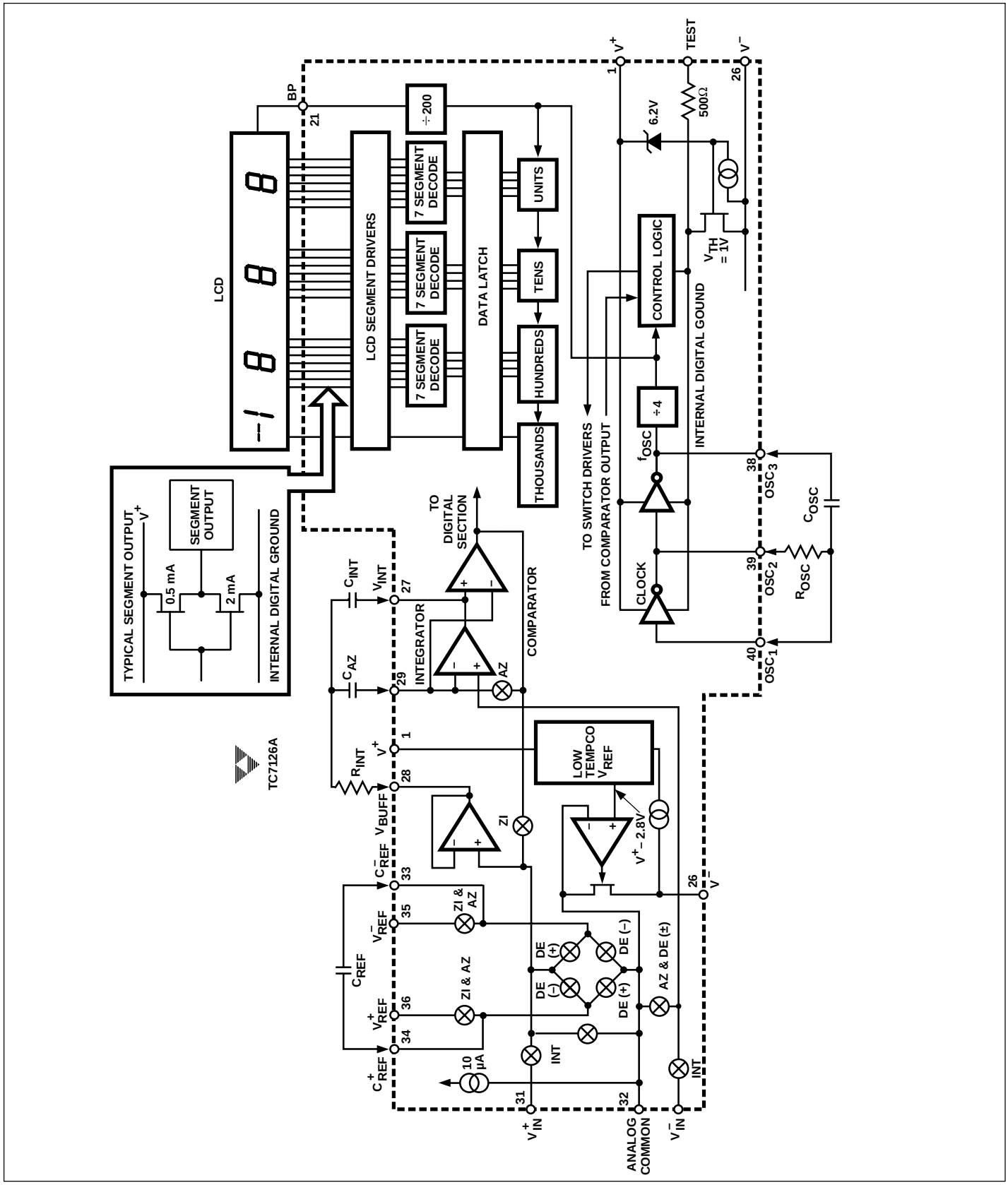



**Figure 3. TC7126A Block Diagram**

When a segment driver is in-phase with the backplane signal, the segment is OFF. An out-of-phase segment drive signal causes the segment to be ON, or visible. This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is ON for negative analog inputs. If $V_{IN}^{+}$ and $V_{IN}^{-}$ are reversed, this indicator would reverse.

On the TC7126A, when the TEST pin is pulled to $V^{+}$, all segments are turned ON. The display reads –1888. During this mode, LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES; LCDS MAY BE DESTROYED IF OPERATED WITH DC LEVELS FOR EXTENDED PERIODS.

The display font and segment drive assignment are shown in Figure 4.

## System Timing

The oscillator frequency is ÷4 prior to clocking the internal decade counters. The three-phase measurement cycle takes a total of 4000 counts (16,000 clock pulses). The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

(1) Auto-zero phase: 1000 to 3000 counts
(4000 to 12,000 clock pulses)

For signals less than full scale, the auto-zero phase is assigned the unused reference integrate time period.

(2) Signal integrate: 1000 counts
(4000 clock pulses)

This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right],$$

where $f_{OSC}$ is the externally-set clock frequency.

(3) Reference integrate: 0 to 2000 counts
(0 to 8000 clock pulses)

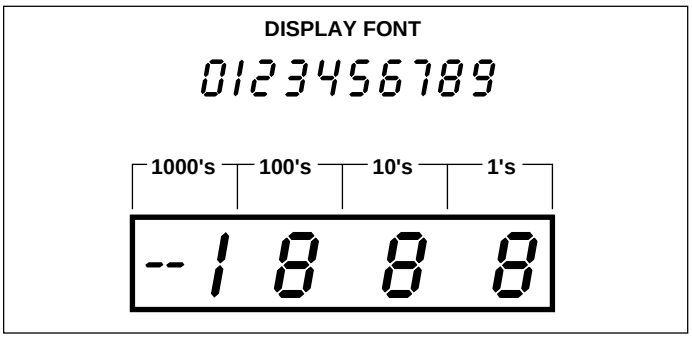



**Figure 4. Display Font and Segment Assignment**

The TC7126A is a drop-in replacement for the TC7126 and ICL7126 that offers a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

## COMPONENT VALUE SELECTION

### Auto-Zero Capacitor ($C_{AZ}$)

The $C_{AZ}$ size has some influence on system noise. A 0.33µF capacitor is recommended for 200mV full-scale applications where 1 LSB is 100µV. A 0.033µF capacitor is adequate for 2V full-scale applications. A Mylar-type dielectric capacitor is adequate.

### Reference Voltage Capacitor ($C_{REF}$)

The reference voltage, used to ramp the integrator output voltage back to zero during the reference integrate phase, is stored on $C_{REF}$. A 0.1µF capacitor is acceptable when $V_{REF}^{-}$ is tied to analog common. If a large common-mode voltage exists ($V_{REF}^{-} \neq$ analog common) and the application requires a 200 mV full scale, increase $C_{REF}$ to 1 µF. Roll-over error will be held to less than 0.5 count. A Mylar-type dielectric capacitor is adequate.

### Integrating Capacitor ($C_{INT}$)

$C_{INT}$ should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TC7126A's superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case, a ±2V full-scale integrator output swing is satisfactory. For 3 readings per second ($f_{OSC}$ = 48 kHz), a 0.047µF value is suggested. For 1 reading per second, 0.15 µF is recommended. If a different oscillator frequency is used, $C_{INT}$ must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for $C_{INT}$ is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}},$$

where: $f_{OSC}$ = Clock frequency at pin 38
$V_{FS}$ = Full-scale input voltage
$R_{INT}$ = Integrating resistor
$V_{INT}$ = Desired full-scale integrator output swing.

At 3 readings per second, a 750Ω resistor should be placed in series with $C_{INT}$. This increases accuracy by compensating for comparator delay. $C_{INT}$ must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

## Integrating Resistor ($R_{INT}$)

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6μA. The integrator and buffer can supply 1μA drive current with negligible linearity errors. $R_{INT}$ is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200mV full scale, $R_{INT}$ is 180kΩ. A 2V full scale requires 1.8MΩ.

| Component Value | Nominal Full-Scale Voltage | |
|---|---|---|
| | 200 mV | 2V |
| $C_{AZ}$ | 0.33 μF | 0.033 μF |
| $R_{INT}$ | 180 kΩ | 1.8 MΩ |
| $C_{INT}$ | 0.047 μF | 0.047 μF |

**NOTE:** $f_{OSC}$ = 48kHz (3 readings per sec).

## Oscillator Components

$C_{OSC}$ should be 50pF; $R_{OSC}$ is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$ .

For a 48 kHz clock (3 conversions per second), R = 180kΩ.

Note that $f_{OSC}$ is ÷4 to generate the TC7126A's internal clock. The backplane drive signal is derived by dividing $f_{OSC}$ by 800.

To achieve maximum rejection of 60Hz noise pickup, the signal integrate period should be a multiple of 60Hz. Oscillator frequencies of 24kHz, 12kHz, 80kHz, 60kHz, 40kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 20kHz, 100kHz, 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings per second) will reject both 50Hz and 60Hz.

## Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

| Required Full-Scale Voltage* | $V_{REF}$ |
|---|---|
| 20 mV | 100mV |
| 2V | 1V |

*$V_{FS}$ = 2 $V_{REF}$.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000lb/in.$^2$ is 400mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

The differential reference can also be used where a digital zero reading is required when $V_{IN}$ is not equal to zero. This is common in temperature-measuring instrumentation. A compensating offset voltage can be applied between analog common and $V_{IN}^-$. The transducer output is connected between $V_{IN}^+$ and analog common.

## DEVICE PIN FUNCTIONAL DESCRIPTION

(Pin Numbers Refer to 40-Pin DIP)

### Differential Signal Inputs

#### $V_{IN}^+$ (Pin 31), $V_{IN}^-$ (Pin 30)

The TC7126A is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range ($V_{CM}$). Typical range is $V^+$ – 1V to $V^-$+1V. Common-mode voltages are removed from the system when the TC7126A operates from a battery or floating power source (isolated from measured system), and $V_{IN}^-$ is connected to analog common ($V_{COM}$). (See Figure 5.)

In systems where common-mode voltages exist, the TC7126A's 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large positive $V_{CM}$ exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with $V_{CM}$ (see Figure 6.) For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of $V^+$ or $V^-$ without increased linearity error.

### Differential Reference

#### $V_{REF}^+$ (Pin 36), $V_{REF}^-$ (Pin 35)

The reference voltage can be generated anywhere within the $V^+$ to $V^-$ power supply range.

To prevent roll-over type errors being induced by large common-mode voltages, $C_{REF}$ should be large compared to stray node capacitance.

The TC7126A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage, suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35 ppm/°C for the TC7126A and 80 ppm/°C for the TC7126.

#### ANALOG COMMON (Pin 32)

The analog common pin is set at a voltage potential approximately 3V below $V^+$. The potential is guaranteed to be between 2.7V and 3.35V below $V^+$. Analog common is tied internally to an N-channel FET capable of sinking 100μA. This FET will hold the common line at 3V should an

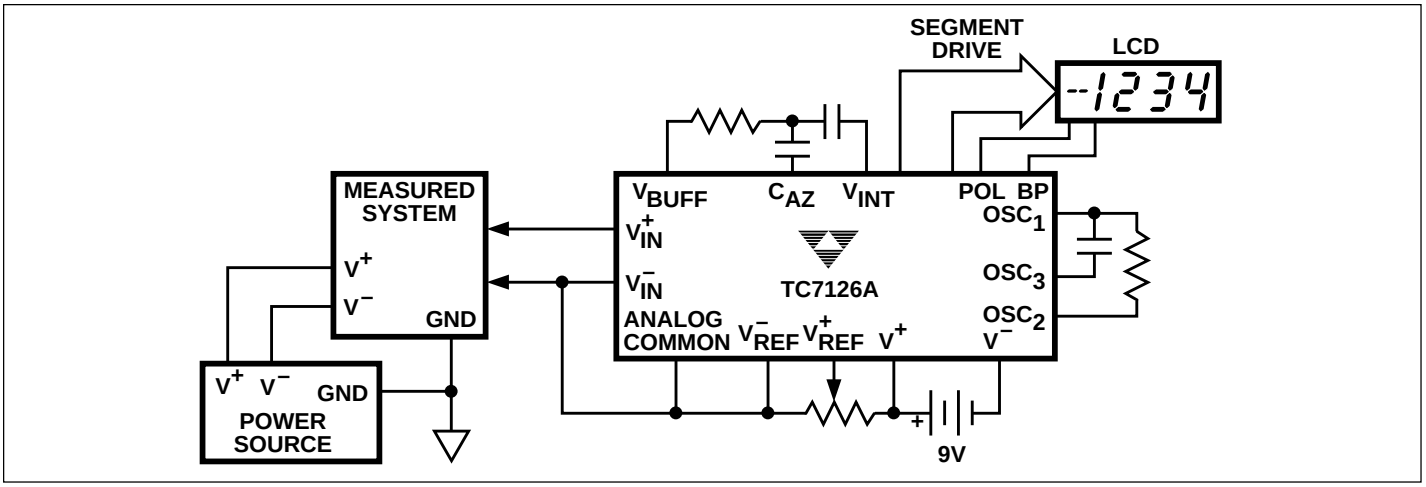



**Figure 5. Common-Mode Voltage Removed in Battery Operation With $V_{IN}$ = Analog Common**

external load attempt to pull the common line toward $V^+$. Analog common source current is limited to 1µA. Therefore, analog common is easily pulled to a more negative voltage (i.e., below $V^+ - 3V$).

The TC7126A connects the internal $V_{IN}^+$ and $V_{IN}^-$ inputs to analog common during the auto-zero phase. During the reference-integrate phase, $V_{IN}^-$ is connected to analog common. If $V_{IN}^-$ is not externally connected to analog common, a common-mode voltage exists, but is rejected by the converter's 86 dB common-mode rejection ratio. In battery operation, analog common and $V_{IN}^-$ are usually connected, removing common-mode voltage concerns. In systems where $V_{IN}^-$ is connected to power supply ground or to a given voltage, analog common should be connected to $V_{IN}^-$.

The analog common pin serves to set the analog section reference, or common point. The TC7126A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7126A's power source. The analog common potential of $V^+ - 3V$ gives a 7V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7V$), analog common is a very stable potential with excellent temperature stability (typically 35ppm/°c). This potential can be used to generate the TC7126A's reference voltage. An external voltage reference will be unnecessary in most cases because of the 35ppm/°C temperature coefficient. See "TC7126A Internal Voltage Reference" discussion.

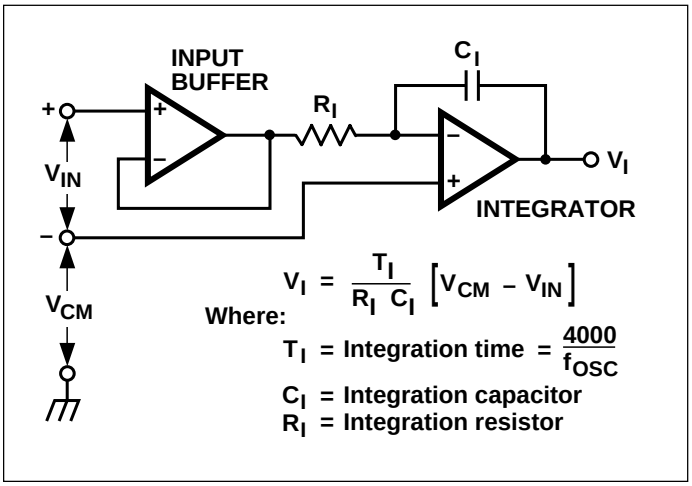



**Figure 6. Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)**

**TEST (Pin 37)**

The TEST pin potential is 5V less than $V^+$. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally-generated negative logic supply through a 500Ω resistor. The TEST pin load should not be more than 1 mA. See "Digital Section" for additional information on using TEST as a negative digital logic supply.

If TEST is pulled HIGH (to $V^+$), all segments plus the minus sign will be activated. DO NOT OPERATE IN THIS MODE FOR MORE THAN SEVERAL MINUTES. With TEST= $V^+$, the LCD segments are impressed with a DC voltage which will destroy the LCD.

## TC7126A Internal Voltage Reference

The TC7126A's analog common voltage temperature stability has been significantly improved (Figure 7). The "A" version of the industry-standard TC7126 device allows users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 10 shows analog common supplying the necessary voltage reference for the TC7126A.

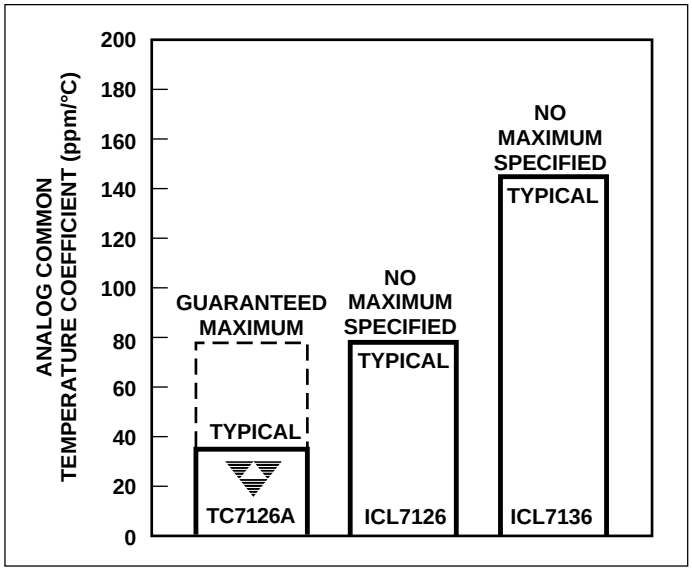



**Figure 7. Analog Common Temperature Coefficient**

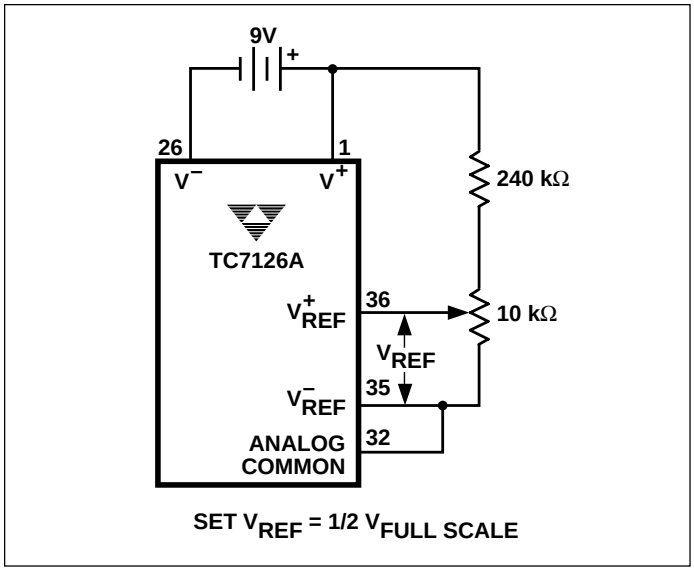



**Figure 8. TC7126A Internal Voltage Reference Connection**

## APPLICATIONS INFORMATION

### Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7126A 3-1/2 digit analog-to-digital converter.

| Manufacturer | Address/Phone | Representative Part Numbers* |
|---|---|---|
| Crystaloid Electronics | 5282 Hudson Dr., Hudson, OH 44236 216-655-2429 | C5335, H5535, T5135, SX440 |
| AND | 720 Palomar Avenue Sunnyvale, CA 94086 408-523-8200 | FE 0801, FE 0203 |
| VGI, Inc. | 1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878 | I1048, I1126 |
| Hamlin, Inc. | 612 E. Lake St., Lake Mills, WI 53551 414-648-2361 | 3902, 3933, 3903 |

*__NOTE:__ Contact LCD manufacturer for full product listing/specifications.

### Decimal Point and Annunciator Drive

The TEST pin is connected to the internally-generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the TEST pin: its potential is approximately 5V below $V^+$.

### Flat Package

The TC7126A is available in an epoxy 64-pin formed-lead flat package. A test socket for the TC7126ACBQ device is available:

Part No. IC 51-42
Manufacturer: Yamaichi
Distribution: Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94043
(415) 856-9332

### Ratiometric Resistance Measurements

The TC7126A's true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately-defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000.$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

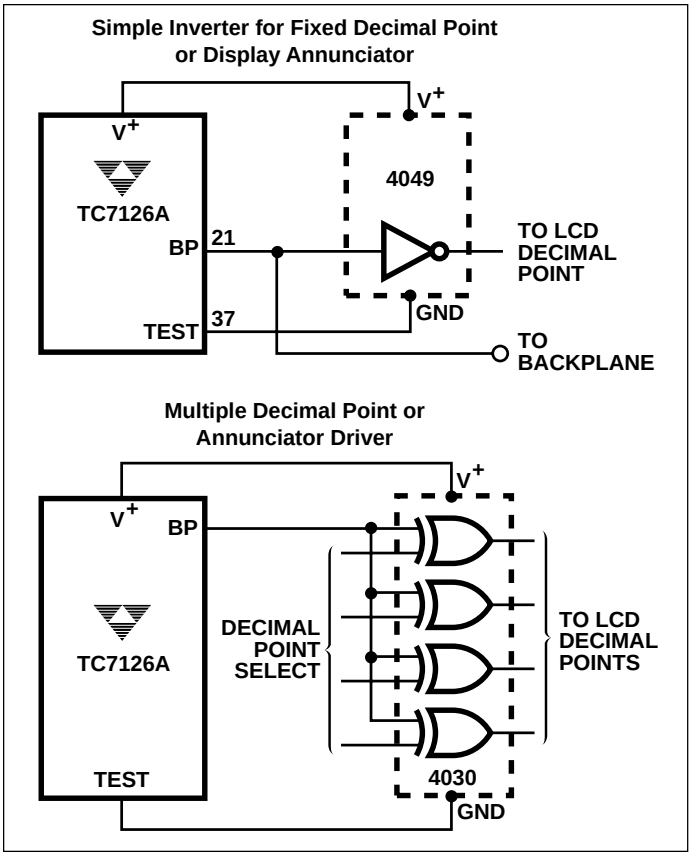



Figure 9. Decimal Point and Annunciator Drives

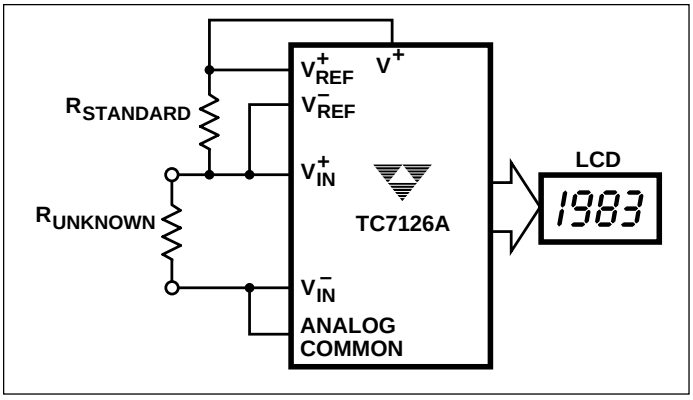



Figure 10. Low Parts Count Ratiometric Resistance Measurement

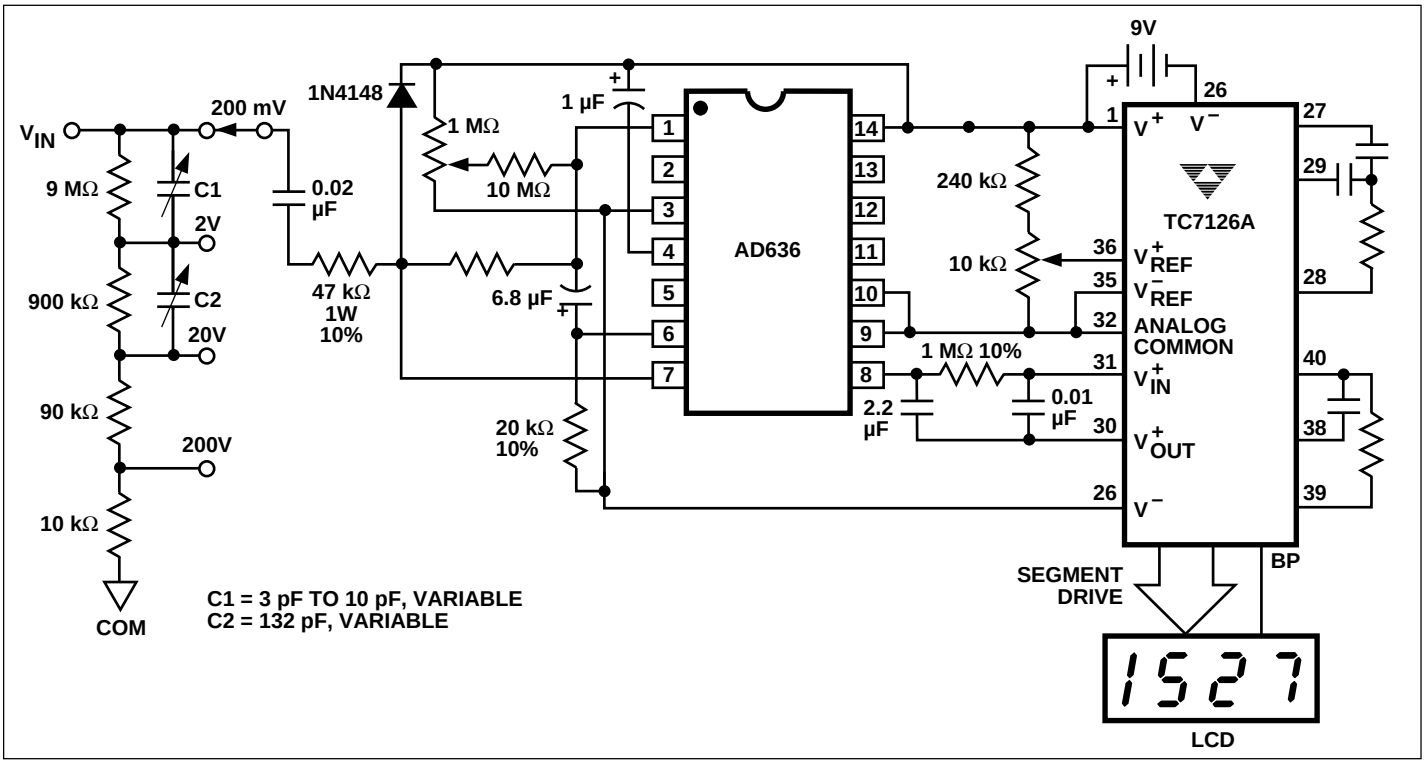



Figure 11. 3-1/2 Digit True RMS AC DMM

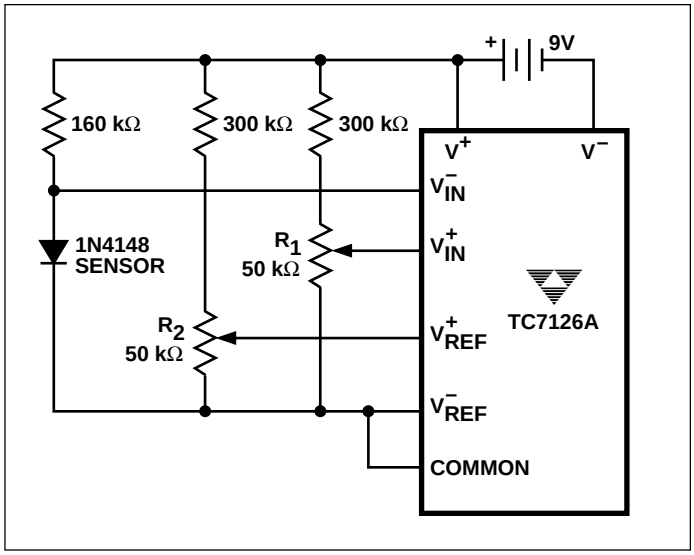



Figure 12. Temperature Sensor

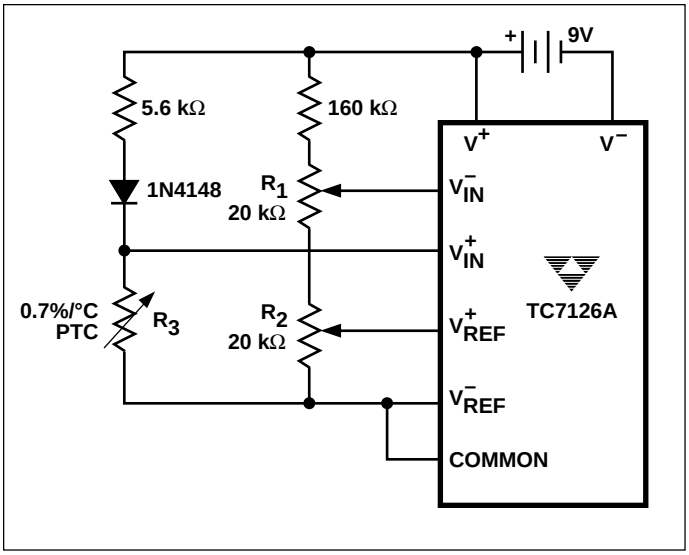



Figure 13. Positive Temperature Coefficient Resistor Temperature Sensor

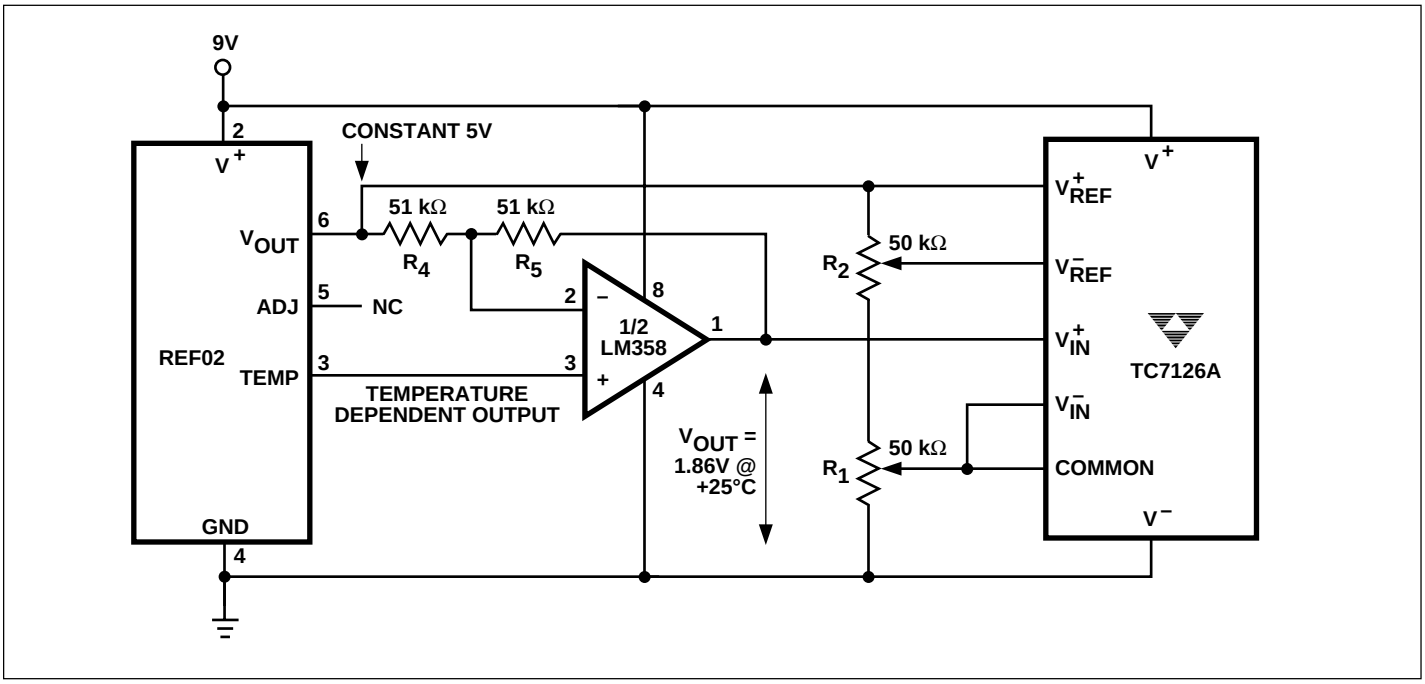
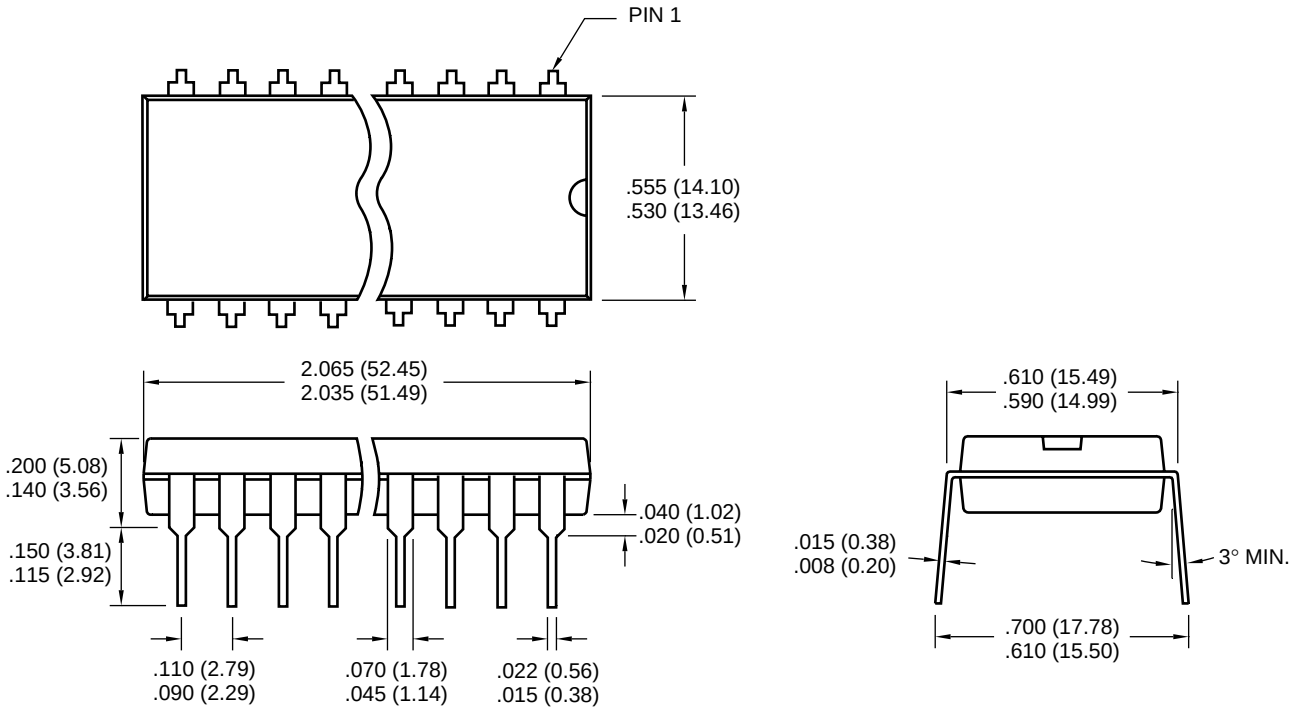



Figure 14. Integrated Circuit Temperature Sensor

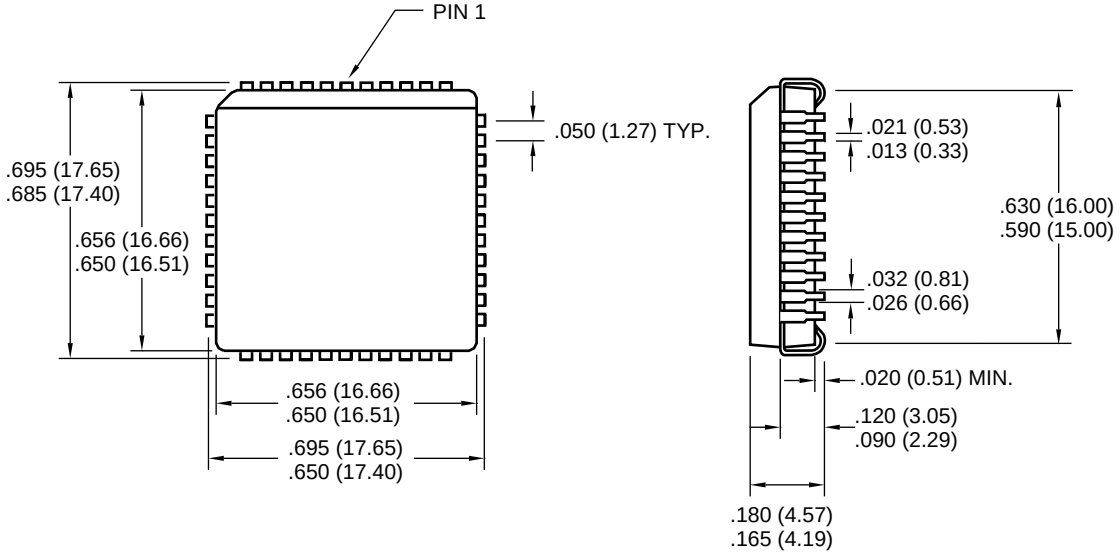
# TC7126
# TC7126A

## PACKAGE DIMENSIONS

### 40-Pin PDIP



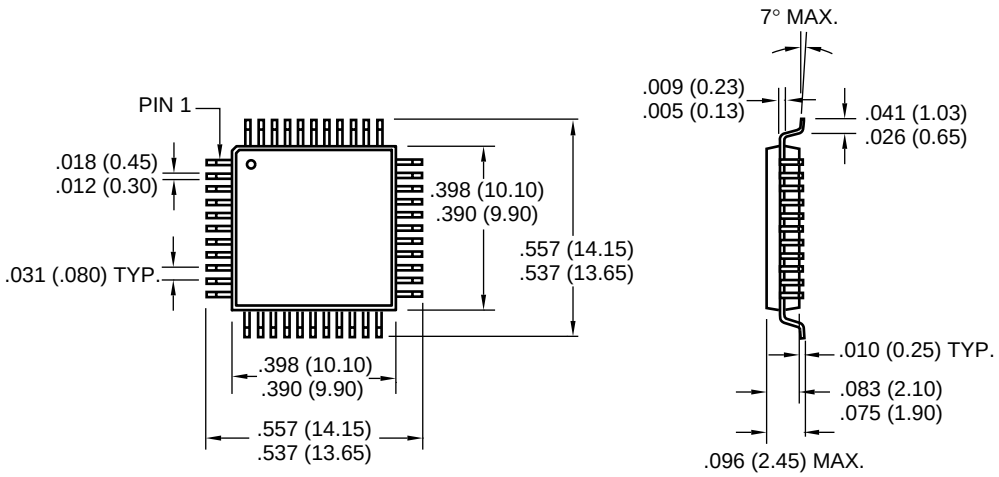

### 44-Pin PLCC




Dimensions: inches (mm)

**PACKAGE DIMENSIONS** (Cont.)

**44-Pin PQFP**




Dimensions: inches (mm)

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