# AS1364

**DataSheet**

## 1A, Low-Dropout Linear Voltage Regulator

## 1 General Description

The AS1364 is a low-dropout linear regulator (LDO) designed to operate from 2V to 5.5V input, that delivers a wide range of highly accurate (±0.75%) factory-trimmed output voltages as well as adjustable output voltages (using an external resistor-divider network).

The ultra-low dropout device requires only 140mV drop-out voltage while delivering a guaranteed 1A load current and is therefore perfectly suited for battery-operated portable applications.

Additionally the AS1364 offers extremly low 10µVRMS (100Hz to 100kHz) or 45µVRMS (10Hz to 1MHz) output voltage noise.

*Table 1. Standard Products*

| Model | Output Type | BYP | SET |
|---|---|---|---|
| AS1364-AD | Adjustable | No | Yes |
| AS1364-_ _ | Fixed | Yes | No |

The device features an internal PMOS pass transistor (for a low supply current of only 35µA), reset output, a low-power shutdown mode, and protection from short-circuit and thermal-overload conditions.

The AS1364 is available in an 8-pin TDFN 3x3mm package.

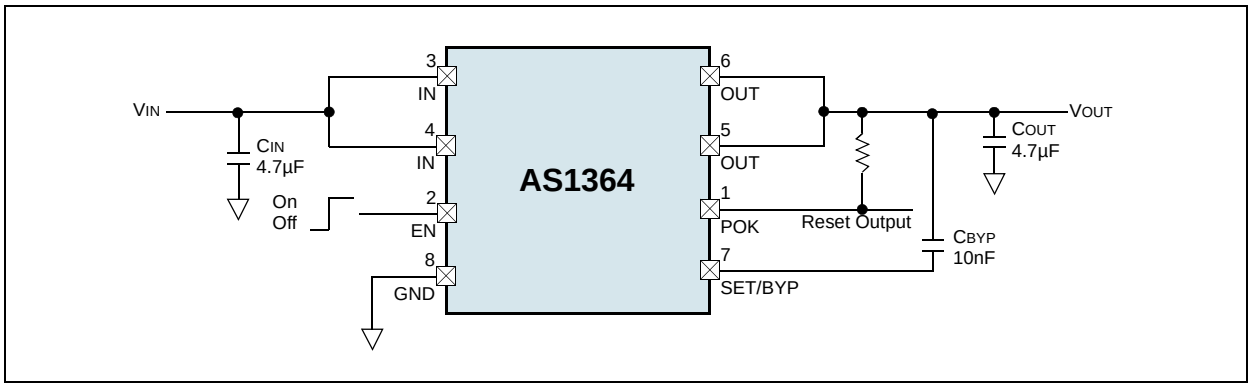
## 2 Key Features

- Guaranteed Output Current: 1A
- Low Dropout: 140mV @ 1A
- Output Voltage Accuracy: Up to ±0.75%
- 2.0 to 5.5V Input Voltage
- Fixed VOUT: 1.2 to 5.0V
- Adjustable VOUT: 1.2 to 5.3V
- Low Ground Current: 35µA
- Low Shutdown Current: 10nA
- Low Output Noise: 45µVRMS (from 10Hz to 1MHz)
- Thermal Overload Protection
- Output Current Limit
- 8-pin TDFN 3x3mm Package

## 3 Applications

The device is ideal for laptops, PDAs, portable audio devices, mobile phones, cordless phones, and any other battery-operated portable device.

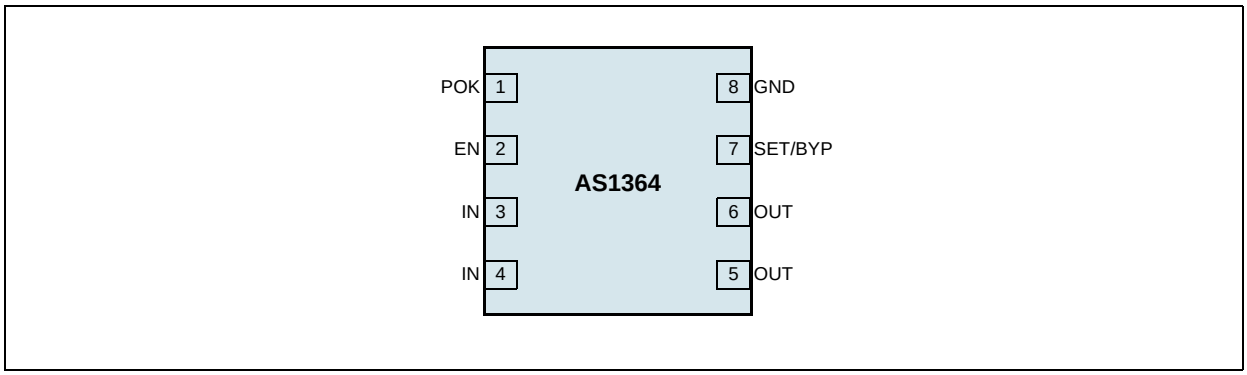
*Figure 1. Typical Application Diagram*



# 4 Pinout

## Pin Assignments

*Figure 2. Pin Assignments (Top View)*




## Pin Descriptions

*Table 2. Pin Descriptions*

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | POK | **Note: Open-Drain POK Output**. POK remains low while $V_{OUT}$ is below the POK threshold. Connect a 100kΩ pull-up resistor from this pin to OUT to obtain an output voltage (see Figure 1 on page 1). |
| 2 | EN | **Active-Low Shutdown Input**. A logic low disables the output and reduces the supply current to 0.1µA. In shutdown, the POK output is low and OUT high impedance.<br>$V_{DD}$: Normal operation.<br>GND: Shutdown. |
| 3, 4 | IN | **2.0V to 5.5V Supply Voltage.** Bypass with a 4.7µF input capacitor to GND (see Capacitor Selection and Regulator Stability on page 12). These inputs are internally connected, but they also must be externally connected for proper operation. |
| 5, 6 | OUT | **Regulator Output**. Bypass with a 4.7µF low-ESR output capacitor to GND. Connect the OUT pins together externally. |
| 7 | SET/BYP | **Voltage-Setting Input**. Connect to GND to select the factory-preset output voltage. Connect this pin to an external resistor-divider for adjustable-output operation (see Figure 1 on page 1). (AS1364-AD only)<br>**Bypass Pin**. Connect a 10nF capacitor from this pin to OUT to improve PSRR and noise performance. (AS1364-AD does not offer this feature) |
| 8 | GND | **Ground** |

# 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 3. Absolute Maximum Ratings*

| Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|
| IN, EN, POK to GND | -0.3 | +7 | V | |
| OUT, SET/BYP to GND | -0.3 | $V_{IN}$ + 0.3 | V | |
| Output Short-Circuit Duration | | Infinite | | |
| Thermal Resistance $\Theta_{JA}$ | | 36.3 | ºC/W | on PCB |
| ESD | 2 | | kV | *HBM MIL-Std. 883E 3015.7* methods |
| Latch-Up | -100 | +100 | mA | *JEDEC 78* |
| Operating Temperature Range | -40 | +85 | ºC | |
| Storage Temperature Range | -65 | +150 | ºC | |
| Junction Temperature | | +150 | ºC | |
| Package Body Temperature | | +260 | ºC | The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn). |

# 6 Electrical Characteristics

*$V_{IN}$ = $V_{OUT(NOM)}$ + 500mV or $V_{IN}$ = +2.0V (whichever is greater),$C_{IN}$ = $C_{OUT}$ = 4.7µF, EN = IN, $T_{AMB}$ = -40 to +85ºC (unless otherwise specified). Typical values are at $T_{AMB}$ = +25ºC.*

*Table 4. Electrical Characteristics*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | | 2.0 | | 5.5 | V |
| $V_{POR}$ | Power On Reset | Falling, 100mV hysteresis | 1.79 | 1.87 | 1.95 | V |
| | Output Voltage Accuracy (Preset Mode) | $I_{OUT}$ = 250mA, $T_{AMB}$ = +25ºC | -0.75 | | +0.75 | % |
| | | $I_{OUT}$ = 250mA | -1.5 | | +1.5 | |
| | | $I_{OUT}$ = 1mA to 1A, $V_{IN}$ > ($V_{OUT}$ + 0.5V)[1] | -2 | | +2 | |
| $V_{OUT}$ | Adjustable Output Voltage Range | | 1.2 | | 5.3 | V |
| $V_{SET/BYP}$ | SET/BYP Voltage Threshold (Adjustable Mode) | $V_{IN}$ = 2.5V, $I_{OUT}$ = 250mA, $V_{OUT}$ set to 2.0V | 1.17 | 1.20 | 1.23 | V |
| $I_{OUT}$ | Guaranteed Output Current (RMS) | | 1 | | | A |
| $I_{LIMIT}$ | Short-Circuit Current Limit | $V_{OUT}$ = 0 | 1.1 | 1.5 | 2.3 | A |
| | In-Regulation Current Limit | $V_{OUT}$ > 96% of nominal value, $V_{IN}$ ≥ 2.0V | | 1.5 | | A |
| | SET/BYP Threshold | | 50 | 100 | 150 | mV |
| $I_{SET}$ | SET/BYP Input Bias Current | $V_{SET/BYP}$ = 1.20V | -100 | | +100 | nA |
| $I_Q$ | Ground-Pin Current | $I_{OUT}$ = 100µA | | 35 | 150 | µA |
| | | $I_{OUT}$ = 1A | | 75 | 200 | |
| $V_{IN}$ - $V_{OUT}$ | Dropout Voltage [2] | $I_{OUT}$ = 250mA, $V_{OUT}$ = 3.3V | | 35 | 85 | mV |
| | | $I_{OUT}$ = 1A, $V_{OUT}$ = 3.3V | | 140 | 320 | |
| $\Delta V_{LNR}$ | Line Regulation | $V_{IN}$ from ($V_{OUT}$ + 100mV) to 5.5V, $I_{LOAD}$ = 5mA | -0.125 | | +0.125 | %/V |
| $\Delta V_{LDR}$ | Load Regulation | $I_{OUT}$ = 1mA to 1A | | | 0.001 | %/mA |
| PSRR | Ripple Rejection | f = 1kHz, $I_{OUT}$ = 10mA, $C_{BYP}$ = 10nF | | 78 | | dB |
| | | f = 1kHz, $I_{OUT}$ = 10mA | | 72 | | |
| | | f = 10kHz, $I_{OUT}$ = 10mA, $C_{BYP}$ = 10nF | | 75 | | |
| | | f = 10kHz, $I_{OUT}$ = 10mA | | 65 | | |
| | | f = 100kHz, $I_{OUT}$ = 10mA, $C_{BYP}$ = 10nF | | 54 | | |
| | | f = 100kHz, $I_{OUT}$ = 10mA | | 46 | | |
| | Output Voltage Noise | 100Hz to 100kHz, $C_{OUT}$ = 3.3µF, $C_{BYP}$ = 10nF; | | 10 | | µVRMS |
| | | 100Hz to 100kHz, $C_{OUT}$ = 3.3µF; | | 50 | | |
| | | 10Hz to 1MHz, $C_{OUT}$ = 3.3µF, $C_{BYP}$ = 10nF; | | 45 | | |
| | | 10Hz to 1MHz, $C_{OUT}$ = 3.3µF; | | 70 | | |

*Table 4. Electrical Characteristics (Continued)*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Shutdown** | | | | | | |
| $I_{OFF}$ | Shutdown Supply Current | EN = GND, $V_{IN}$ = 5.5V, $T_{AMB}$ = 25°C | | 0.01 | 0.5 | µA |
| | | EN = GND, $V_{IN}$ = 5.5V | | 0.1 | 15 | |
| $V_{IH}$ | EN Input Threshold | 2.0V < $V_{IN}$ < 5.5V | 1.6 | | | V |
| $V_{IL}$ | | 2.0V < $V_{IN}$ < 5.5V | | | 0.6 | V |
| $I_{SHDNN}$ | EN Input Bias Current | EN = IN or GND, $T_{AMB}$ = +25ºC | | 1 | | nA |
| | | $T_{AMB}$ = +85ºC | | 5 | | |
| **POK Output** | | | | | | |
| $V_{OL}$ | POK Output Low Voltage | POK sinking 1mA | | 0.05 | 0.25 | V |
| | Operating Voltage Range for Valid POK Signal | POK sinking 100µA | 1.1 | | 5.5 | V |
| | POK Output High leakage Current | POK = 5.5V, $T_{AMB}$ = +25ºC | | 1 | | nA |
| | | $T_{AMB}$ = +85ºC | | 5 | | |
| | POK Threshold | Rising edge (referenced to $V_{OUT(NOM)}$) | 90 | 94 | 98 | % |
| **Thermal Protection** | | | | | | |
| $T_{SHDNN}$ | Thermal Shutdown Temperature | | | 170 | | ºC |
| $\Delta T_{SHDNN}$ | Thermal Shutdown Hysteresis | | | 20 | | ºC |

1. Guaranteed by production test of load regulation and line regulation.
2. Dropout voltage is defined as $V_{IN}$ - $V_{OUT}$, when $V_{OUT}$ is 100mV below the value of $V_{OUT}$ measured for $V_{IN}$ = ($V_{OUT(NOM)}$ + 500mV). Since the minimum input voltage is 2.0V, this specification is only valid when $V_{OUT(NOM)}$ > 2.0V.

# 7 Typical Operating Characteristics

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V, $C_{IN}$ = $C_{OUT}$ = 4.7µF, $T_{AMB}$ = 25°C (unless otherwise specified).

*Figure 3. $V_{DROP}$ vs. $I_{OUT}$;*

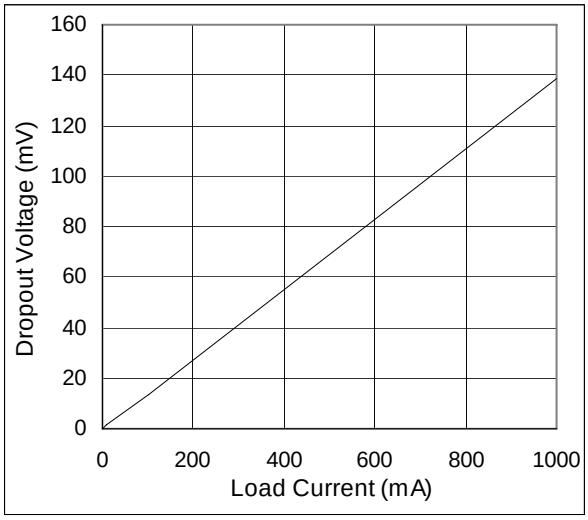



*Figure 4. $V_{OUT}$ vs. $I_{OUT}$; $V_{OUT(NOM)}$ = 3.3V*

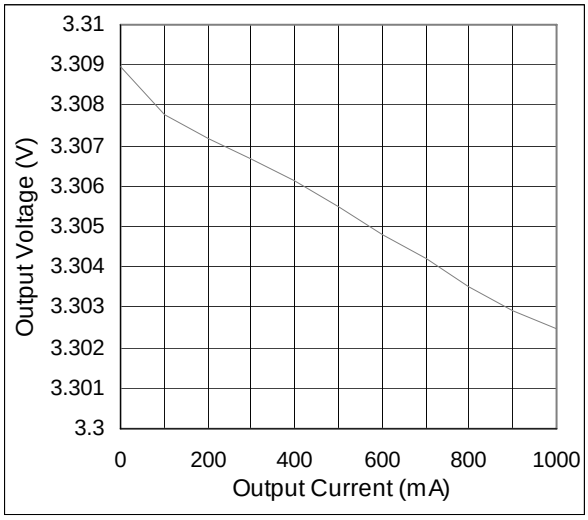



*Figure 5. $V_{OUT}$ vs. Temperature; $V_{OUT(NOM)}$ = 3.3V*

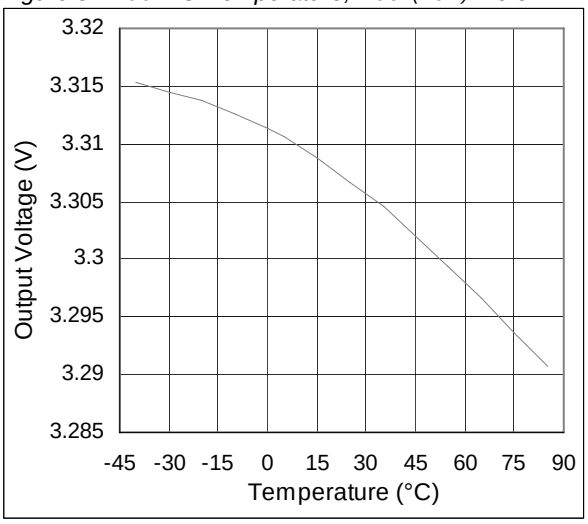



*Figure 6. $V_{OUT}$ vs. $V_{IN}$; $V_{OUT(NOM)}$ = 3.3V*

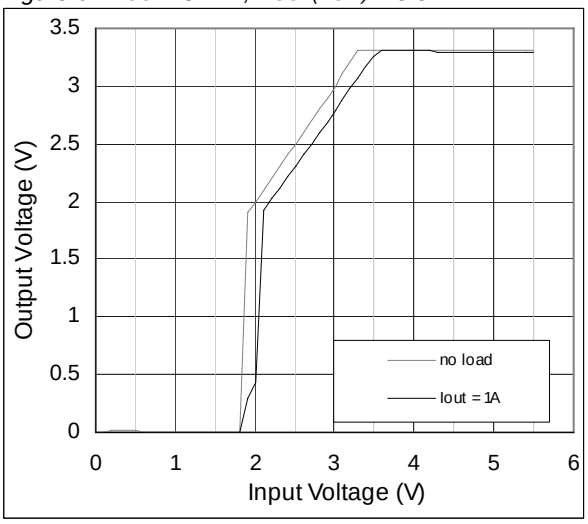



*Figure 7. Quiescent Current vs. $V_{IN}$;*

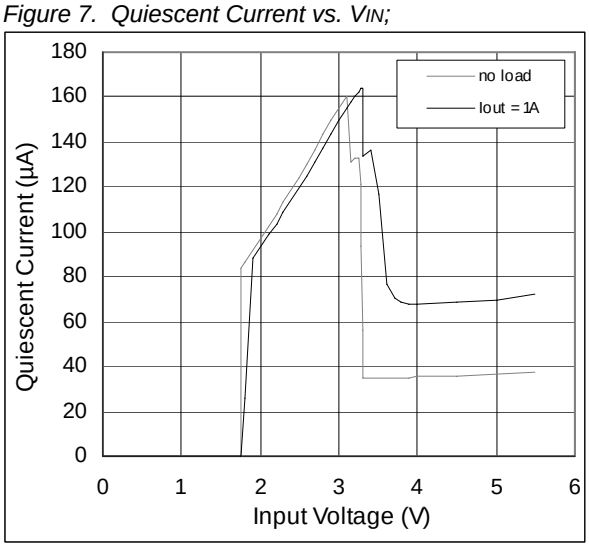



*Figure 8. Quiescent Current vs. $I_{OUT}$;*

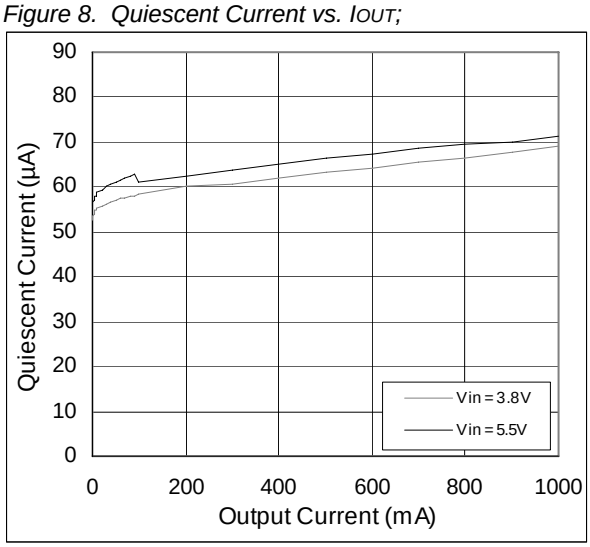


*Figure 9. Quiescent Current vs. Temperature;*

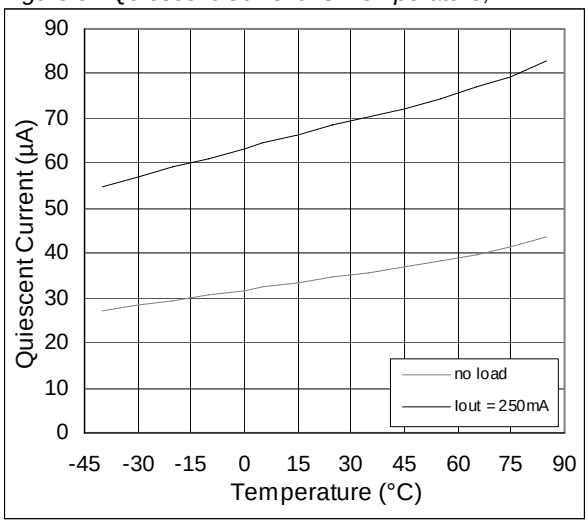



*Figure 10. Spectral Noise vs. Freq.; $I_{OUT}$ = 10mA,*

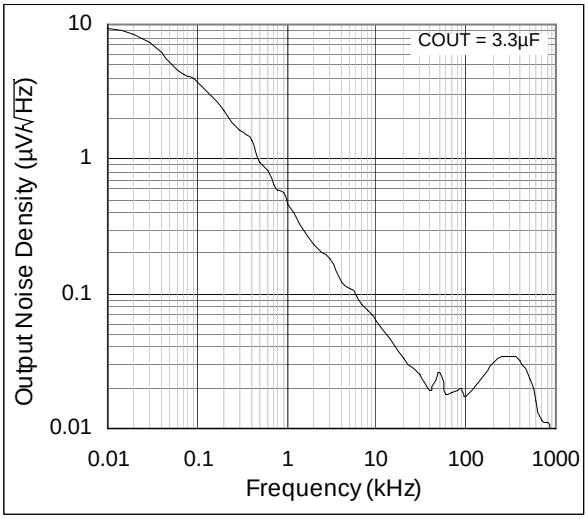



*Figure 11. PSRR vs. Frequency; $I_{OUT}$ = 10mA*

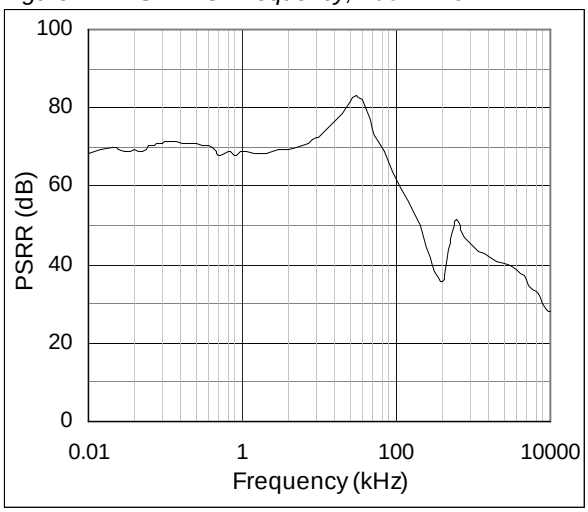


*Figure 12. Line Transient Response; $V_{IN}$ = 3.8V to 4.3V, $I_{OUT}$ = 100mA*

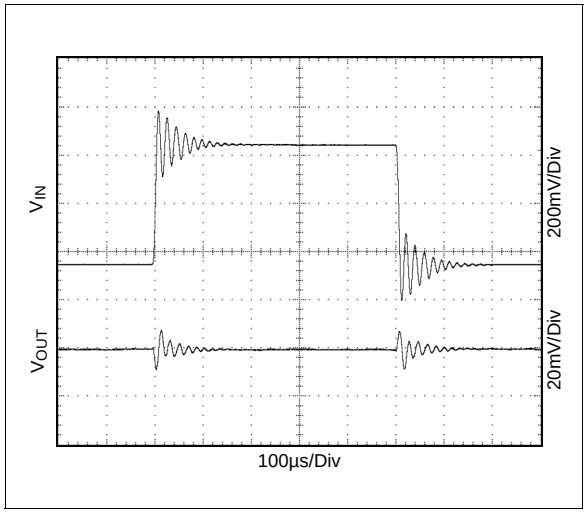



*Figure 13. Load Transient Response; $V_{IN}$ = 3.8V, $I_{OUT}$ = 50mA to 500mA*

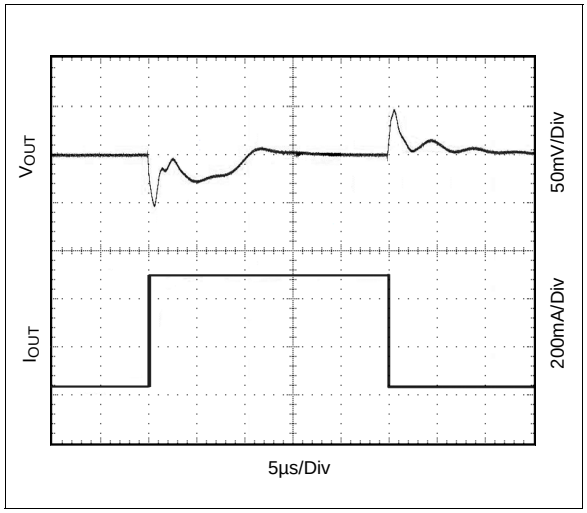



*Figure 14. Startup; $V_{IN}$ = 3.8V, $I_{OUT}$ = 100mA*

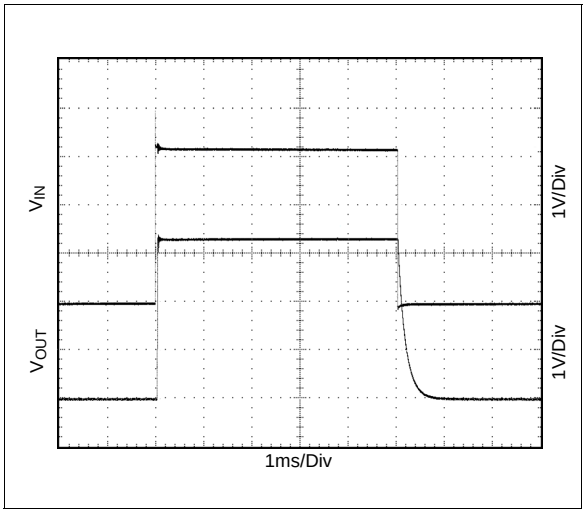
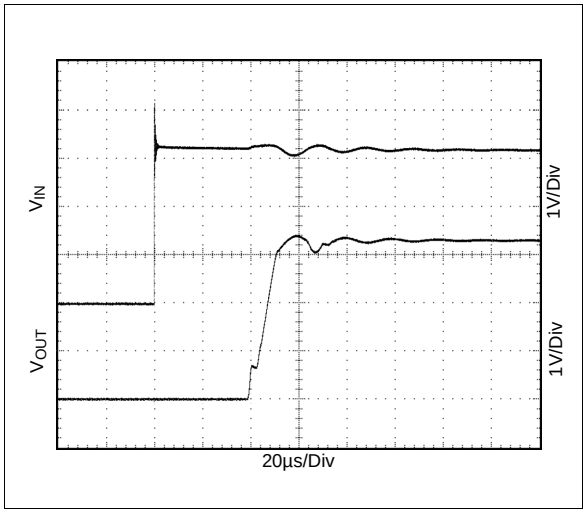


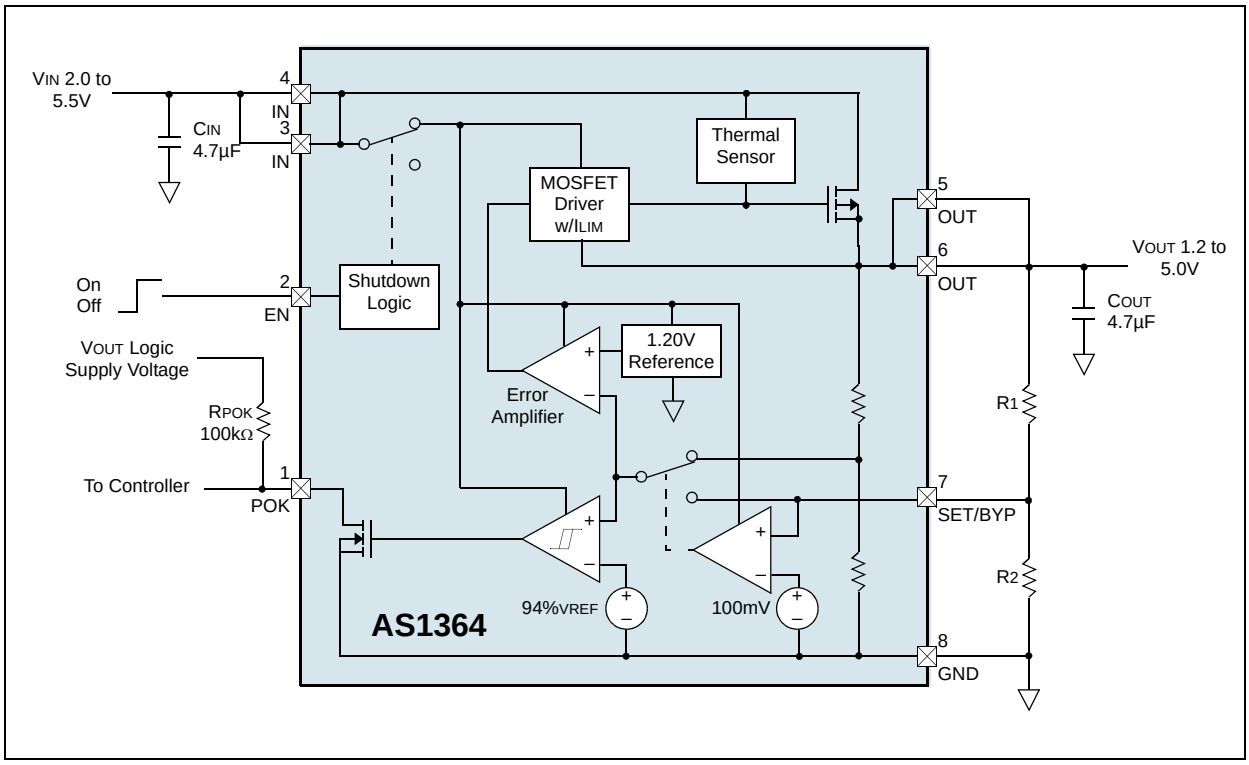

*Figure 15. Startup; $V_{IN}$ = 3.8V, $I_{OUT}$ = 100mA*



# 8 Detailed Description

The AS1364 output voltage is factory-trimmed or is adjustable from +1.2 to +5V, and is guaranteed to supply 1A of output current. The device consists of a +1.20V internal reference, error amplifier, MOSFET driver, P-channel pass transistor, internal feedback voltage-divider and a comparator (see Figure 16).

*Figure 16. Block Diagram*




The +1.20V reference is connected to the inverting input of the error amplifier, which compares this reference with the selected feedback voltage and amplifies the difference.

The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel transistor. If the feedback voltage is lower than the reference, the pass transistor gate is pulled lower, allowing more current to pass increasing the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled up, allowing less current to pass to the output.

The low VOUT comparator senses when the feedback voltage has dropped 6% below its expected level, causing POK to go low.

The output voltage is fed back through either an internal resistor-divider connected to OUT or an external resistor network connected to SET. The comparator examines VSET/BYP and selects the feedback path. If VSET/BYP is below 50mV, the internal feedback path is used and the output is regulated to the factory-preset voltage.

## Output Voltage Selection

At the factory trimmed versions of the AS1364 offering the bypass pin (see Figure 1 on page 1), the output voltage is then set to an internally trimmed voltage (see Ordering Information on page 14).

For the adjustable AS1364-AD, an output voltage between +1.2V and +5V can be set by using two external resistors (see Figure 17). In this mode, VOUT is determined by:

$$V_{OUT} = V_{SETBYP} \times \left(1 + \frac{R_1}{R_2}\right) \quad \textit{(EQ 1)}$$

**Where:**

VSET/BYP = +1.20V.

A simplification of R1 and R2 selection is:

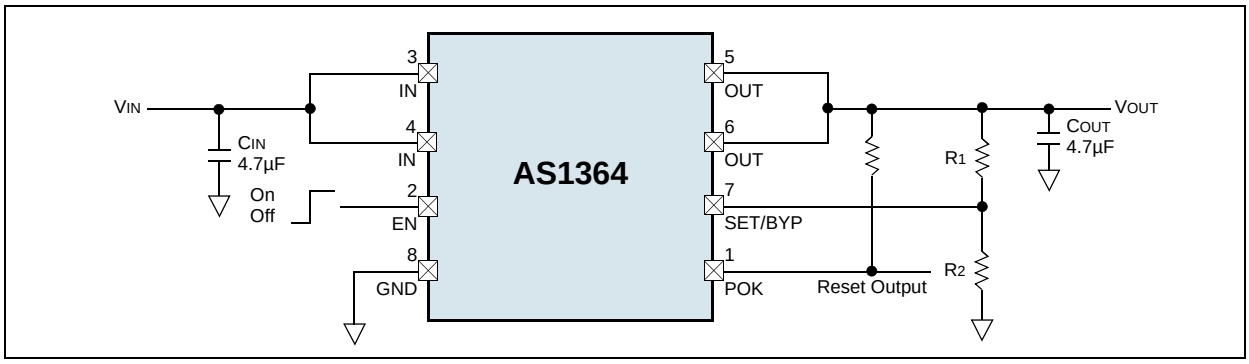
$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{SETBYP}} - 1\right) \quad \textit{(EQ 2)}$$

Since the input bias current at SET is less than 100nA, large resistance values can be used for R1 and R2 to minimize power consumption and therefore increasing efficiency.

**Note:** Up to 125kΩ is acceptable for R2. If the SET pin is connected to GND without a resistor, 3.3V will be set as output voltage.

In preset voltage mode, the impedance from SET to GND should be less than 10kΩ or spurious conditions may cause the voltage at SET to exceed the 50mV threshold.

*Figure 17. Adjustable Output Voltage Typical Application*




## Shutdown

If pin EN is connected to GND the AS1364 is disabled. In shutdown mode all internal circuits are turned off, reducing supply current to 10nA (typ). For normal device operation pin EN must be connected to IN. During shutdown, POK goes low.

## Power-OK

The AS1364 features a power-ok indicator that asserts when the output voltage falls out of regulation. The open-drain POK output goes low when output voltage at OUT falls 6% below its nominal value. A 100kΩ pull-up resistor from POK to a (typically OUT) provides a logic control signal.

POK can be used as a power-on-reset (POR) signal to a microcontroller or can drive an external LED to indicate a power failure condition.

**Note:** POK is low during shutdown.

## Current Limiter

The AS1364 features current limiting circuitry that monitors the pass transistor, limiting short-circuit output current to 1.5A (typ). The circuitry of the AS1364 allows that the output can be shorted to ground for an indefinite period of time without damaging the device.

## Internal P-Channel Pass Transistor

The AS1364 features a 1A P-channel MOSFET pass transistor and consumes only a maximum of 200µA of quiescent current under heavy loads as well as in dropout.

## Thermal Protection

Integrated thermal overload protection limits the total power dissipation in the AS1364. When the junction temperature ($T_J$) exceeds +170ºC typically, the pass transistor is turned off. Normal operation is continued when $T_J$ drops approximately 20ºC.

**Note:** Regardless of the hysteresis, continuous short-circuit condition will result in a pulsed output.

## Operating Region and Power Dissipation

Maximum power dissipation of the AS1364 depends on the thermal resistance of the package and the PCB, the temperature difference between the die junction and ambient air, and the rate of air flow.

The power dissipated in the device is given as:

$$PD = I_{OUT} \times (V_{IN} - V_{OUT}) \quad \textit{(EQ 3)}$$

The maximum power dissipation is calculated:

$$PDMAX = \frac{T_{J(MAX)} - T_{AMB}}{\theta_{JC} + \theta_{CA}} \quad \textit{(EQ 4)}$$

**Where:**
$T_{J(MAX)} - T_{AMB}$ is the temperature difference between the device die junction and the surrounding air.
$\theta_{JC}$ is the thermal resistance of the junction to the case.
$\theta_{CA}$ is the thermal resistance from the case through the PCB, copper traces, and other materials to the surrounding air.

Connect the exposed thermal pad and GND to circuit ground by using a large pad, or multiple vias to the ground plane.

# 9 Application Information

## Capacitor Selection and Regulator Stability

Input and output capacitors are required for stable operation of the AS1364 over the full temperature range and with load currents up to 1A. Connect CIN and COUT as close to the AS1364 as possible to minimize the impact of PC board trace inductance.

### Input Capacitor

For CIN, a 4.7µF capacitor between IN and ground is sufficient. CIN reduces the source impedance of the input supply and may be smaller than 4.7µF if powered from regulated power supplies or low-impedance batteries. Larger input capacitor values and lower ESR provide better noise rejection and line-transient response.

### Output Capacitor

A 4.7µF low-ESR capacitor between OUT and ground is sufficient for COUT. The output capacitor's ESR affects stability and output noise. An output capacitors with an ESR of 0.5Ω or less is recommended to ensure stability and optimum transient response. Reduced output noise and improve load-transient response, stability, and power-supply rejection by using large output capacitors with low ESR.

## Noise, PSRR, and Transient Response

AS1364 output noise is typically 10µVRMS (100Hz to 100kHz) or 45µVRMS (10Hz to 1MHz) during normal operation. This is suitably low for most applications (see Figure 10 on page 7).

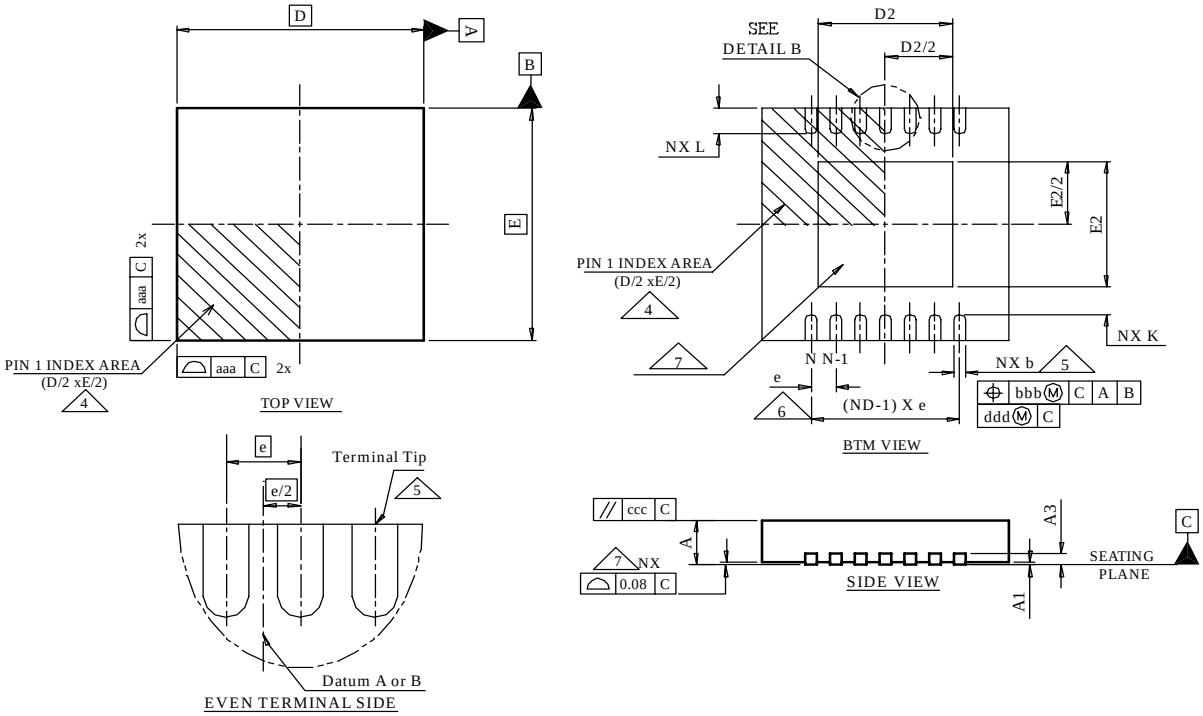
The AS1364 is designed to achieve extremly low dropout voltage and low quiescent current in battery-powered systems while still maintaining excellent noise performance, transient response, and PSRR. See the Figure 11 on page 7 for a plot of power-supply rejection ratio (PSRR) versus frequency.

When operating from very noisy sources, the factory preset variants a recommanded since they offer improved noise performance over the adjustable variants.

# 10 Package Drawings and Markings

The device is available in an 8-pin TDFN 3x3mm package.

*Figure 18. 8-pin TDFN 3x3mm Package*




| Symbol | Min | Typ | Max | Notes |
|---|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 | 1, 2 |
| A1 | 0.00 | 0.02 | 0.05 | 1, 2 |
| A3 | | 0.20 REF | | 1, 2 |
| L1 | | | 0.15 | 1, 2 |
| L2 | | | 0.13 | 1, 2 |
| aaa | | 0.15 | | 1, 2 |
| bbb | | 0.10 | | 1, 2 |
| ccc | | 0.10 | | 1, 2 |
| ddd | | 0.05 | | 1, 2 |
| eee | | 0.08 | | 1, 2 |
| ggg | | 0.10 | | 1, 2 |

| Symbol | Min | Typ | Max | Notes |
|---|---|---|---|---|
| D BSC | | 3.00 | | 1, 2 |
| E BSC | | 3.00 | | 1, 2 |
| D2 | 1.60 | | 2.50 | 1, 2 |
| E2 | 1.35 | | 1.75 | 1, 2 |
| L | 0.30 | 0.40 | 0.50 | 1, 2 |
| θ | 0º | | 14º | 1, 2 |
| K | 0.20 | | | 1, 2 |
| b | 0.25 | 0.30 | 0.35 | 1, 2, 5 |
| e | | 0.65 | | |
| N | | 8 | | 1, 2 |
| ND | | 4 | | 1, 2, 5 |

**Notes:**

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. N is the total number of terminals.
4. Terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the area indicated. The terminal #1 identifier may be either a mold, embedded metal or mark feature.
5. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip.
6. ND refers to the maximum number of terminals on D side.
7. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

# 11 Ordering Information

The device is available as the standard products shown in Table 5.

*Table 5. Ordering Information*

| Model | Marking | Output | SET/BYP | Delivery Form | Package |
|---|---|---|---|---|---|
| AS1364-BTDT-AD | ASRF | adjustable (preset to 3.3V) | SET | Tape and Reel | 8-pin TDFN 3x3mm |
| AS1364-BTDT-12* | ASRN | 1.2V | BYP | Tape and Reel | 8-pin TDFN 3x3mm |
| AS1364-BTDT-15 | ASRG | 1.5V | BYP | Tape and Reel | 8-pin TDFN 3x3mm |
| AS1364-BTDT-18 | ASRH | 1.8V | BYP | Tape and Reel | 8-pin TDFN 3x3mm |
| AS1364-BTDT-30 | ASRJ | 3.0V | BYP | Tape and Reel | 8-pin TDFN 3x3mm |
| AS1364-BTDT-33 | ASRI | 3.3V | BYP | Tape and Reel | 8-pin TDFN 3x3mm |
| AS1364-BTDT-45 | ASRK | 4.5V | BYP | Tape and Reel | 8-pin TDFN 3x3mm |

All devices are RoHS compliant and free of halogene substances.

*Future product.

Non-standard devices are available between 1.4V and 4.6V in 50mV steps and between 4.6V and 5.0V in 100mV steps. For more information and inquiries contact http://www.austriamicrosystems.com/contact-us

## Copyrights



## Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

## Contact Information

**Headquarters**
austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact-us