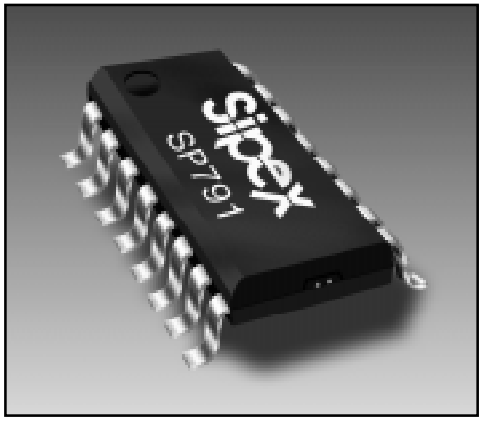
Low Power Microprocessor Supervisory with Battery Switch-Over

- Precision 4.65V Voltage Monitoring
- 200ms Power-OK/Reset Time Delay
- Independent Watchdog Time-Preset or Adjustable
- 75µA Maximum Operating Supply Current
- 1.0µA Maximum Battery Backup Current
- 0.1µA Maximum Battery Standby Current
- Power Switching
  250mA Output in Vcc Mode (0.6Ω)
  25mA Output in Battery Mode (5Ω)
- On-Board Gating of Chip-Enable Signals
  Memory Write-Cycle Completion
  6ns CE Gate Propagation Delay
- Voltage Monitor for Power-Fail or Low Battery
- Backup-Battery Monitor
- RESET Valid to Vcc=1V
- Pin Compatible Upgrade to MAX791



DESCRIPTION

The **SP791** is a microprocessor (µP) supervisory circuit that integrates a myriad of components involved in discrete solutions to monitor power-supply and battery-control functions in µP and digital systems. The **SP791** offers complete µP monitoring and watchdog functions. The **SP791** is ideal for a low-cost battery management solution and is well suited for portable, battery-powered applications with its supply current of 40µA. The 6ns chip-enable propagation delay, the 25mA current output in battery-backup mode, and the 250mA current output in standard operation also makes the **SP791** suitable for larger scale, high-performance equipment.

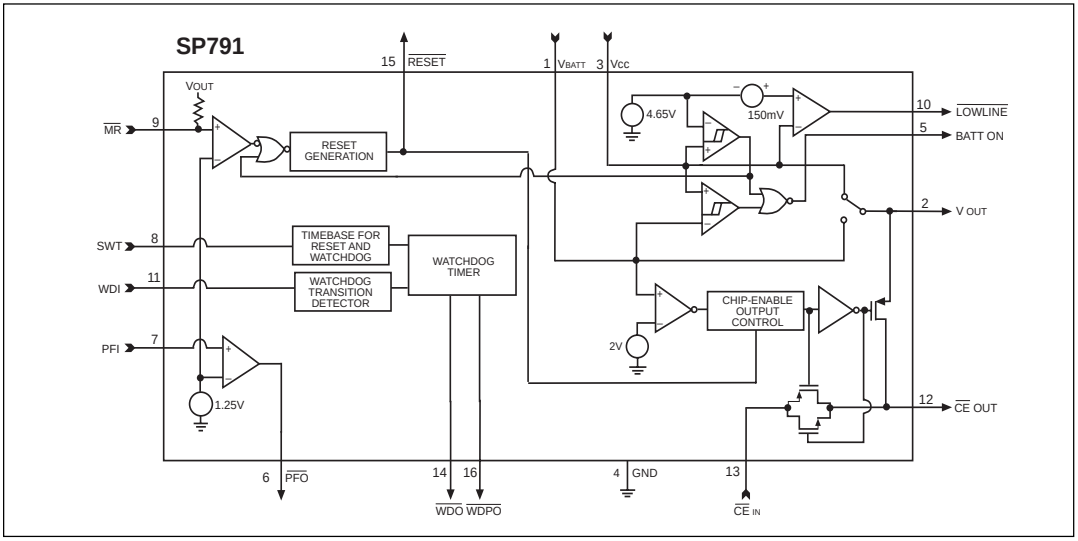


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)
- VCC.....-0.3V to +6V
- VBATT..... .....-0.3V to +6V
- All Other Inputs .....-0.3V to (VOUT + 0.3V)

Input Current
- VCC Peak..... 1.0A
- VCC Continuous 250mA
- VBATT Peak 250mA
- VBATT Continuous.....25mA
- GND, BATT ON 100mA
- All Other Outputs 25mA

Continuous Power Dissipation (TA = + 70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Narrow SO (derate 8.70mW/°C above+70°C) 696mW

ESD Rating.....4KV

Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Temperature Ranges
- SP791C .....0°C to +70°C
- SP791E .....-40°C to +85°C
- Storage Temperature Range.....-65°C to +160°C
- Lead Temperature (soldering,10sec).....+300°C

ELECTRICAL CHARACTERISTICS

(Vcc = 4.75V to 5.5V, V_{BATT} = 2.8V, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted, typicals specified at 25°C)

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Operating Voltage Range V_{CC}, V_{BATT} (Note 1)	0		5.5	V	
V_{OUT} in Normal Operating Mode	V_{CC} - 0.05	V_{CC} - 0.015		V	V_{CC} = 4.5V, I_{OUT} = 25mA
	V_{CC} - 0.3	V_{CC} - 0.15			V_{CC} = 4.5V, I_{OUT} = 250mA
	V_{CC} - 0.2	V_{CC} - 0.09			V_{CC} =3.0V; V_{BATT} = 2.8V, I_{OUT} = 100mA
V_{CC}-to-V_{OUT} On Resistance		0.6	1.2	Ω	V_{CC}=4.5V;
		0.9	2.0		V_{CC}=3.0V;
V_{OUT} in Battery Backup Mode	V_{BATT} - 0.3			V	V_{BATT}=4.5V, I_{OUT}=20mA
	V_{BATT} - 0.25				V_{BATT}=2.8V, I_{OUT}=10mA
	V_{BATT} - 0.15				V_{BATT}=2.0V, I_{OUT}=5mA
V_{BATT}-to-V_{OUT} On Resistance		5	15	Ω	V_{BATT}=4.5V
		7	25		V_{BATT}=2.8V
		10	30		V_{BATT}=2.0V
Supply Current in Normal Operating Mode (Excludes I_{OUT})		40	75	µA	$V_{CC} > V_{BATT} - 1V$
Supply Current in Battery Backup Mode (Excludes I_{OUT}) (Note 2)		0.001	1	µA	$V_{CC} < V_{BATT} - 1.2V$; V_{BATT} = 2.8V
V_{BATT} Standby Current (Note 3)	-0.1		0.02	µA	$V_{BATT} + 0.2V < V_{CC}$
Battery-Switchover Threshold		V_{BATT} +0.03		V	Power up
		V_{BATT} -0.03			Power down
Battery-Switch over Hysteresis		60		mV	Peak to Peak
Low-Battery Detector Threshold		2		V	

ELECTRICAL CHARACTERISTICS (continued)

(Vcc = 4.75V to 5.5V, V_{BATT} = 2.8V, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted, typicals specified at 25°C)

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
BATT ON Output Low Voltage		0.1	0.4	V	I_{SINK} = 3.2mA
		0.7	1.5		I_{SINK} = 25mA
BATT ON Output Short Circuit Current		60		mA	Sink Current
	1	15	100	µA	Source Current
RESET, LOW-LINE AND WATCHDOG TIMER					
$\overline{\text{RESET}}$ Threshold Voltage	4.50	4.65	4.75	V	
$\overline{\text{RESET}}$ Threshold Hysteresis		15		mV	
$\overline{\text{LOWLINE}}$-to-$\overline{\text{RESET}}$ Threshold Voltage		150		mV	
Vcc-to-$\overline{\text{RESET}}$ Delay		100		µs	Power down
Vcc-to-$\overline{\text{LOWLINE}}$ Delay		80		µs	Power down
$\overline{\text{RESET}}$ Active Timeout Period	140	200	280	ms	Power up
Watchdog Timeout Period	1.0	1.6	2.25	sec	SWT connected to V_{OUT}
Minimum Watchdog Timeout Period		10		ms	4.7nF capacitor connected from SWT to GND
Minimum Watchdog Input Pulse Width	100			ns	V_{IL} = 0.8V, V_{IH} = 0.75 X V_{CC}
$\overline{\text{WDPO}}$ Pulse Width		1		ms	
$\overline{\text{WDPO}}$-to-$\overline{\text{WDO}}$ Delay		70		ns	
$\overline{\text{RESET}}$ Output Voltage		0.004	0.3	V	I_{SINK}=50µA,V_{CC}=1.0V,V_{CC} ↘
		0.1	0.4		I_{SINK} = 3.2 mA, V_{CC} = 4.25V
	3.5				I_{SOURCE} = 1.6mA, V_{CC} = 5V
$\overline{\text{RESET}}$ Output Short-Circuit Current		7	20	mA	Output source current
$\overline{\text{LOWLINE}}$ Output Voltage			0.4	V	I_{SINK} = 3.2mA, V_{CC} = 4.25V
	3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
$\overline{\text{LOWLINE}}$ Output Short-Circuit Current		15	100	µA	Output source current
$\overline{\text{WDO}}$ Output Voltage			0.4	V	I_{SINK} = 3.2mA
	3.5				I_{SOURCE} = 500µA, V_{CC} = 5V
$\overline{\text{WDO}}$ Output Short-Circuit Current		3	10	mA	Output source currrent
$\overline{\text{WDPO}}$ Output Voltage			0.4	V	I_{SINK} = 3.2mA
	3.5				I_{SOURCE} = 1mA
$\overline{\text{WDPO}}$ Output Short-Circuit Current		7	20	mA	Output source current

ELECTRICAL CHARACTERISTICS (continued)

(Vcc = 4.75V to 5.5V, V_{BATT} = 2.8V, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted, typicals specified at 25°C)

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
WDI Threshold Voltage	0.75 X V_{CC}			V	V_{IH}
(Note 4)			0.8		V_{IL}
WDI Input Current	-50	-10		µA	WDI = 0V
		20	50		WDI = V_{OUT}
POWER FAIL COMPARATOR					
PFI Input Threshold	1.20	1.25	1.30	V	V_{CC} = 5V
PFI Leakage Current		±0.01	±25	nA	
$\overline{PFO}$ Output Voltage			0.4	V	I_{SINK} = 3.2mA
	3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
$\overline{PFO}$ Short-Circuit Current		60		mA	Output sink current
	1	15	100	µA	Output source current
PFI-to-$\overline{PFO}$ Delay		15		µs	V_{OD} = 15mV
		55			V_{OD} = 15mV
CHIP-ENABLE GATING					
$\overline{CE}$ IN Leakage Current		±0.005	±1	µA	Disabled mode
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Resistance (Note 5)		65	150	Ω	Enabled mode
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)	0.1	0.75	2.0	mA	Disabled mode, $\overline{CE}$ OUT = 0V
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Propagation Delay (Note 6)		6	10	ns	50Ω source impedance driver, C_{LOAD} = 50pF
$\overline{CE}$ OUT Output Voltage High	3.5			V	V_{CC} = 5V, I_{OUT} = 100µA
(Reset Active)	2.7				V_{CC} = 0V, V_{BATT} = 2.8V, I_{OUT} = 1µA
$\overline{RESET}$-to-$\overline{CE}$ OUT Delay		15		µs	Power down
MANUAL RESET INPUT					
$\overline{MR}$ Minimum Pulse Width	25	15		µs	
$\overline{MR}$-to-$\overline{RESET}$ Propagation Delay		7		µs	
$\overline{MR}$ Threshold		1.25		V	V_{CC} = 5V
$\overline{MR}$ Pull-Up Current		23	250	µA	$\overline{MR}$ = 0V

Note 1: Either V_{CC} or V_{BATT} can go to 0V, if the other is greater than 2.0V.

Note 2: The supply current drawn by the SP791 from the battery (excluding I_{OUT}) typically goes to 10µA when (V_{BATT} - 1V) < V_{CC} < V_{BATT}. In most applications, this is a brief period as V_{CC} falls through this region.

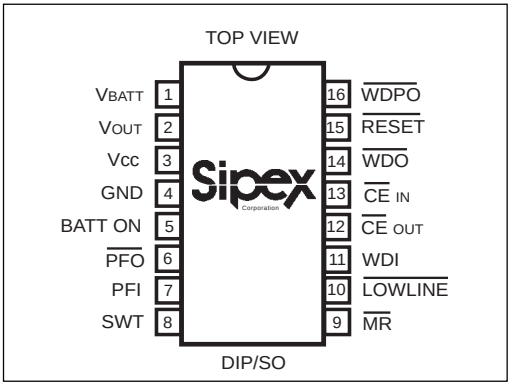
Note 3: "+" = battery-discharging current, "-" = battery-charging current.

Note 4: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

Note 5: The chip-enable resistance is tested with V_{CC} = 4.75V :: $V_{\overline{CE}\ IN} = V_{\overline{CE}\ OUT} = V_{CC}/2$.

Note 6: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}_{OUT}$.

PINOUT



PIN ASSIGNMENTS

Pin 1 — V_{BATT} — Backup-Battery Input. Connect to external battery or capacitor and charging circuit.

Pin 2 —V_{OUT} — Output Supply Voltage. V_{OUT} connects to V_{CC} when V_{CC} is greater than V_{BATT} and V_{CC} is above the reset threshold. When V_{CC} falls below V_{BATT} and V_{CC} is below the reset threshold, V_{OUT} connects to V_{BATT}. Connect a 0.1µF capacitor from V_{OUT} to GND.

Pin 3 — V_{CC} — Input Supply Voltage — +5V input

Pin 4 — GND — Ground reference for all signals

Pin 5 — BATT ON — Battery On Output. Goes high when V_{OUT} switches to V_{BATT}. Goes low when V_{OUT} switches to V_{CC}. Connect the base of a PNP through a current-limiting resistor to BATT ON for V_{OUT} current requirements greater than 250mA.

Pin 6 — $\overline{PFO}$ — Power-Fail Output. This is the output of the power-fail comparator. $\overline{PFO}$ goes low when PFI is less than1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.

Pin 7 — PFI — Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used.

Pin 8 — SWT — Set Watchdog-Timeout Input. Connect this input to V_{OUT} to select the default 1.6 sec watchdog timeout period. Connect a capacitor between this input and GND to select another watchdog-timeout period. Watchdog-timeout period = 2.1 x (capacitor value in nF) ms.

Pin 9 — $\overline{MR}$ — Manual-Reset Input. This input can be tied to an external momentary pushbutton switch, or to a logic gate output. $\overline{RESET}$ remains low as long as $\overline{MR}$ is held low and for 200ms after $\overline{MR}$ returns high.

Pin 10 — $\overline{LOWLINE}$ — $\overline{LOWLINE}$ Output goes low when VCC falls to 150mV above the reset threshold. The output can be used to generate an NMI (nonmaskable interrupt) if the unregulated supply is inaccessible.

Pin 11 — WDI — Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{WDO}$ goes low. $\overline{WDO}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and GND, which sets it to mid-supply when left unconnected.

Pin 12 — $\overline{CE}$ OUT — Chip-Enable Output. $\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and VCC is above the reset threshold. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will stay low for 15us or until $\overline{CE}$ IN goes high, whichever occurs first.

Pin 13 — $\overline{CE}$ IN — Chip-Enable Input. The Input to chip-enable gating circuit. Connect to GND or V_{OUT} if not used.

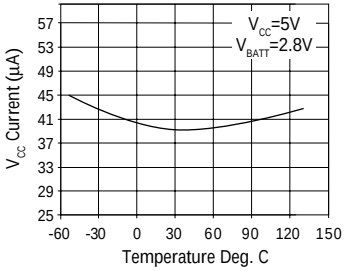
Pin 14 — $\overline{WDO}$ — Watchdog Output. $\overline{WDO}$ goes low if WDI remains either high or low longer than the watchdog timeout period. $\overline{WDO}$ returns high on the next transition at $\overline{WDI}$. $\overline{WDO}$ remains high if WDI is unconnected. $\overline{WDO}$ is also high when $\overline{RESET}$ is asserted.

Pin 15 — $\overline{RESET}$ — $\overline{RESET}$ Output goes low whenever V_{CC} falls below the reset threshold. $\overline{RESET}$ will remain low for 200ms after V_{CC} crosses the reset threshold on power-up.

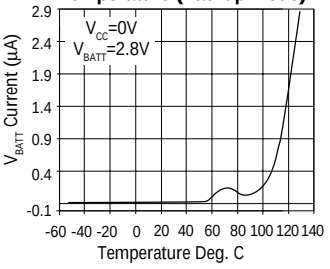
Pin 16 — $\overline{WDPO}$ — Watchdog-Pulse Output. Upon the absence of a transition at WDI, $\overline{WDPO}$ will pulse low for a minimum of 1ms. $\overline{WDPO}$ precedes $\overline{WDO}$ by 70ns.

TYPICAL CHARACTERISTICS (25ºC, unless otherwise noted)

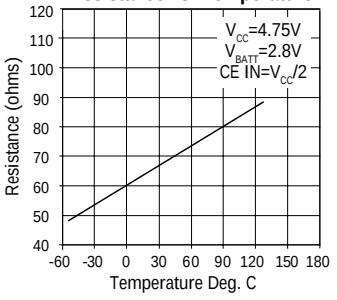
V_{CC} Supply Current vs. Temperature (Normal Mode)



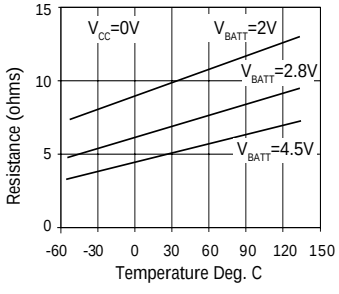
Battery Supply Current vs. Temperature (Backup Mode)



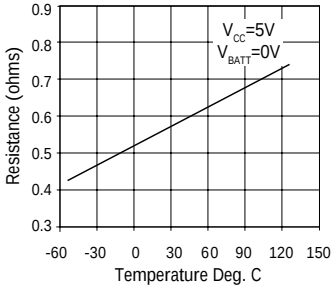
Chip Enable On Resistance vs. Temperature



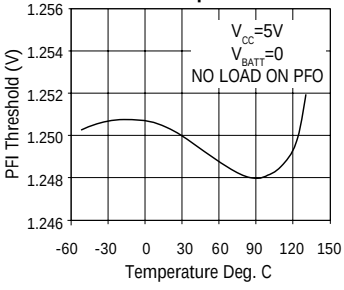
V_{BATT} to V_{OUT} ON Resistance vs. Temperature



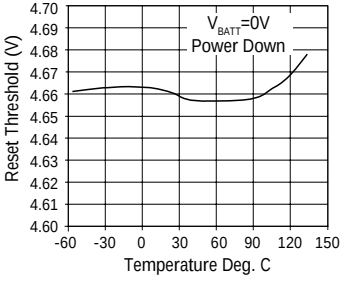
V_{CC} to V_{OUT} On Resistance vs. Temperature



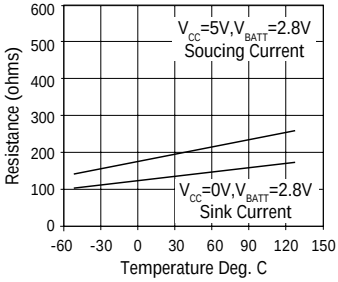
PFI Threshold vs. Temperature



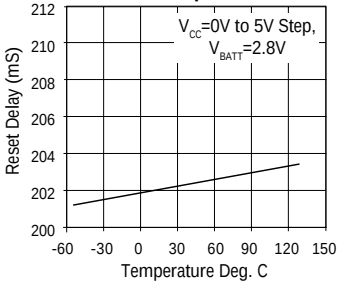
Reset Threshold vs. Temperature



Reset Output Resistance vs. Temperature

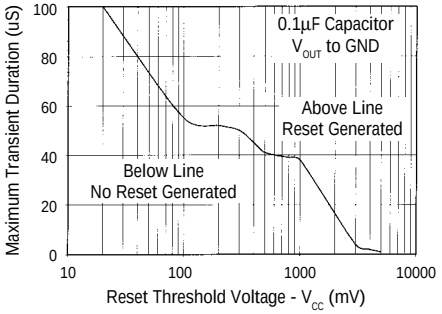


Reset Delay vs. Temperature

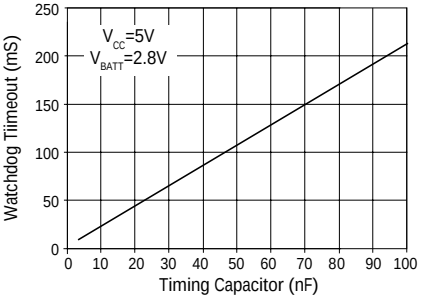


TYPICAL CHARACTERISTICS (25°C, unless otherwise noted)

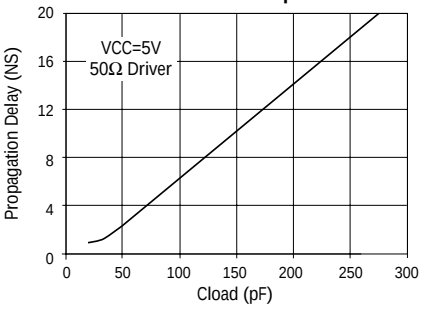
Maximum Reset Comparator Overdrive Without Causing a Reset



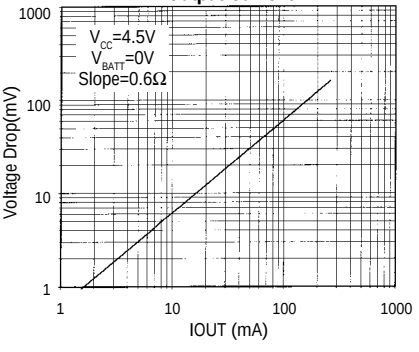
Watchdog Timeout vs. Timing Capacitor



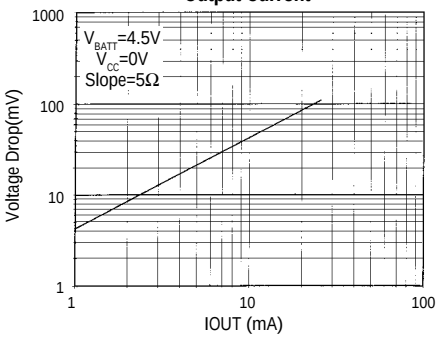
Chip-Enable Propagation Delay vs. CE OUT Load Capacitance



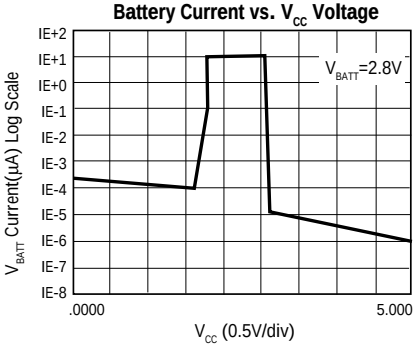
V_{CC} to V_{OUT} vs. Output Current

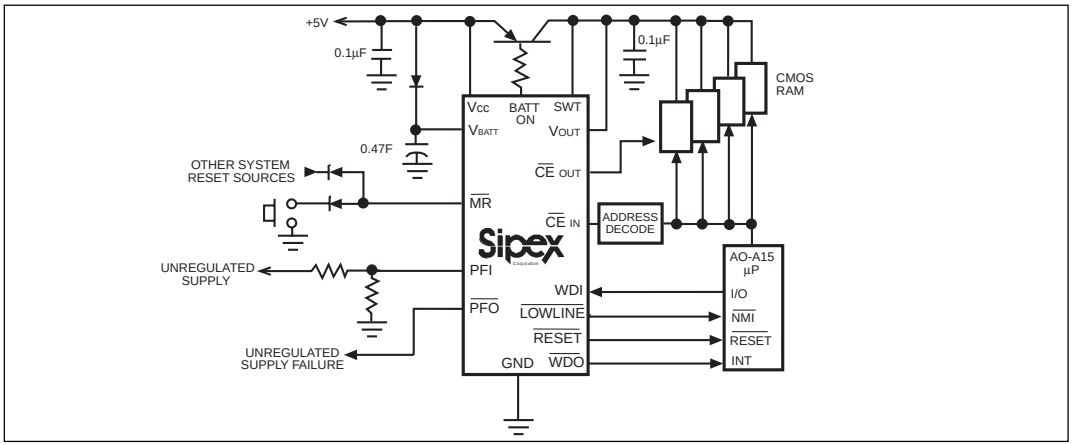


VBATT to VOUT vs. Output Current



Battery Current vs. V_{CC} Voltage





Typical Operating Circuit

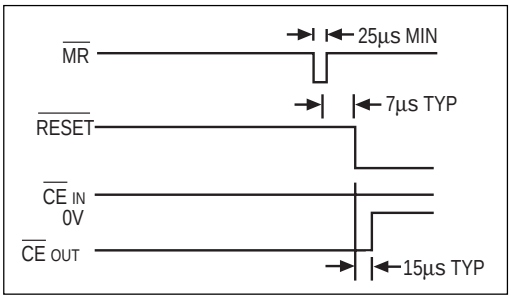


Figure 2. Manual-Reset Timing Diagram

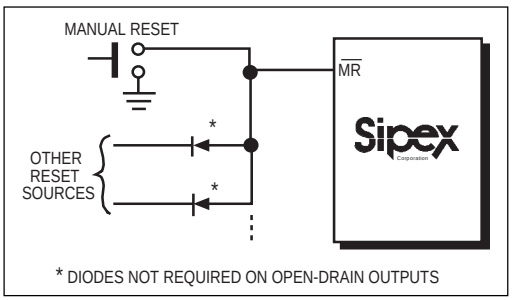


Figure 3. Diode "OR" connections allow multiple reset sources to connect to MR.

FEATURES

The **SP791** is a microprocessor (µP) supervisory circuit that monitors the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The **SP791** is an ideal solution for portable, battery-powered equipment that require power supply monitoring. The **SP791** watchdog functions will continuously oversee the operational status of a system. Implementing the **SP791** will reduce the number of components and overall complexity in a design that requires power supply monitoring circuitry. The operational features and benefits of the **SP791** are described in more detail below.

THEORY OF OPERATION

The **SP791** is a complete µP supervisor IC and provides the following main functions:

1) µP reset ➡ $\overline{\text{RESET}}$ output is asserted during power fluctuations such as power-up, power-down, and brown out conditions, and is guaranteed to be in the correct state for V_{CC} down to 1V.

2) Manual-Reset input ➡ Manually resets RESET output

3) Power Fail Comparator ➡ Provides for power-fail warning and low-battery detection, or monitors another power supply.

4) Watchdog function ➡ Monitors µP activity where the watchdog output goes to a logic LOW state if the watchdog input is not toggled for a period greater than the timeout period.

5) Internal switch ➡ Switches over from V_{CC} to V_{BATT} if the V_{CC} falls below the reset threshold and below V_{BATT}.

MANUAL RESET INPUT

Many microprocessor or microcontroller products include manual-reset capability, allowing the operator or test technician to initiate a reset. The Manual Reset Input ($\overline{\text{MR}}$) can be connected directly to a switch, without an external pull-up resistor. It connects to a 1.25V comparator, and has an internal pull-up to V_{OUT} as shown in *Figure 1*. The propagation delay from asserting $\overline{\text{MR}}$ to $\overline{\text{RESET}}$ being asserted is 7us typical. Pulsing

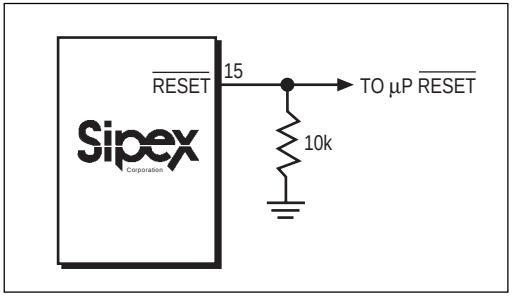


Figure 4. Adding an external pull-down resistor ensures RESET is valid with VCC down to GND.

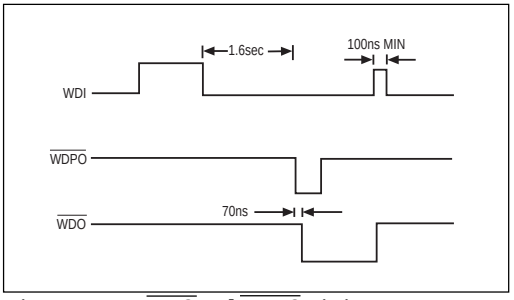


Figure 5. WDI, WDO and WDPO Timing Diagram (VCC mode).

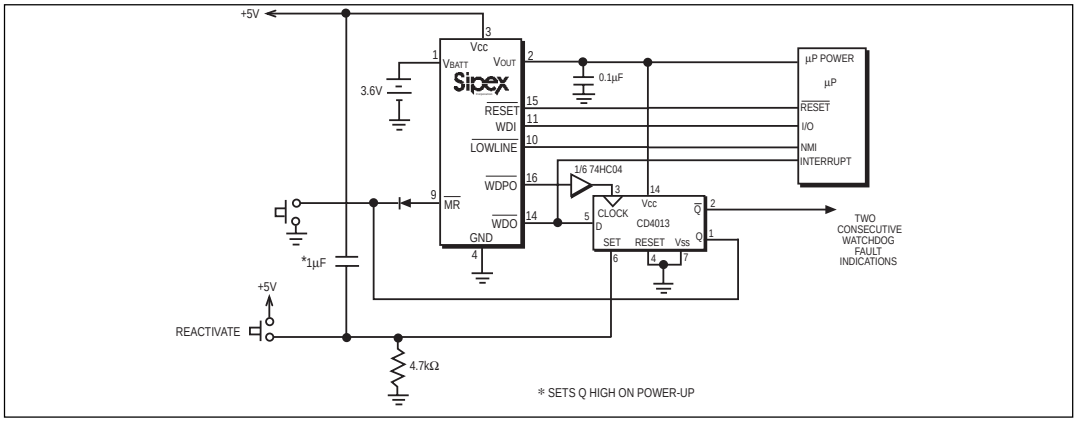


Figure 6. Two consecutive watchdog faults latch the system in reset.

MR low for a minimum of 25µs resets all the internal counters, sets the Watchdog Output (WDO) and Watchdog-Pulse Output (WDPO) high, and sets the Set Watchdog-Timeout (SWT) input to VOUT if it is not already connected to VOUT (for Internal timeouts). It also, disables the Chip-Enable Output (CE OUT) forcing it to a high state. The RESET output remains at a logic low as long as MR is held low, and the reset-timeout period begins after MR returns high, *Figure 2*.

Use this input as either a digital-logic input or a second low-line comparator. Normal TTL/CMOS levels can be wire-OR connected via pull-down diodes, *Figure 3*, and open-drain/collector outputs can be wire-ORed directly.

RESET OUTPUT

The **SP791's** RESET output ensures that the µP powers up in a known state, and prevents code-execution errors during power-down or brown-out conditions.

The RESET output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deasserted, RESET sources 1.6mA at VOUT – 0.5V. When no backup battery is used, RESET output is valid down to VCC = 1V, and an external 10kΩ pull-down resistor on RESET ensures that RESET will be valid with VCC down to GND as shown on *Figure 4*. As VCC goes below 1V, the gate drive to the RESET output switch reduces accordingly, increasing the r_{DS}(ON) and the saturation voltage. The 10kΩ pull-down resistor ensures the parallel combination of switch and external resistor is 10kΩ and the output saturation voltage is below 0.4V, while sinking 40µA. When using a 10kΩ external pull-down resistor, the high state for the RESET output with Vcc = 4.75V is 4.5V typical. For battery voltages greater than or equal to 2V, RESET remains valid for VCC between 0V and 5.5V. RESET will be asserted during the following conditions:

1) VCC < 4.65V (typ)
2) MR < 1.25V (typ)
3) RESET = logic "0" ; for 200 ms (typ) after Vcc rises above 4.65V or after MR has exceeded 1.25V.

The **SP791** battery-switchover comparator does not affect RESET assertion.

WATCHDOG FUNCTION

The watchdog monitors µP activity via the Watchdog Input (WDI). If the µP becomes inactive over a period of time, $\overline{WDO}$ and $\overline{WDPO}$ are asserted.

To use the watchdog functon, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal), $\overline{WDPO}$ and $\overline{WDO}$ are asserted, indicating a software fault or idle condition.

WATCHDOG INPUT

A change of logic state (minimum 100ns duration) at WDI during the watchdog period will reset the watchdog timer. The watchdog default timeout is 1.6sec. To select an alternative timeout period, connect an external capacitor from SWT to GND.

To disable the watchdog function, leave WDI floating. An internal impedance network (100kΩ equivalent at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When Vcc is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal network, thus becoming high impedance.

WATCHDOG OUTPUT

$\overline{WDO}$ remains high if there is activity (transition or pulse) at WDI during the watchdog-timeout period. The watchdog function is disabled and $\overline{WDO}$ is a logic high when VCC is less than the reset threshold, or when WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog-timeout period, $\overline{WDO}$ goes low 70ns after the falling edge of $\overline{WDPO}$ and remains low until the next transition at WDI as shown on *Figure 5*. A flip-flop can force the system into a hardware shutdown if there are two successive watchdog faults, shown on *Figure 6*. $\overline{WDO}$ has a 2 x TTL output characteristic.

WATCHDOG-PULSE OUTPUT

As described in the preceding section, $\overline{WDPO}$ can be used as the clock input to an external D flip-flop. Upon the absence of a watchdog edge or pulse at WDI at the end of a watchdog-timeout period, WDPO will pulse low for 1ms. The falling edge of $\overline{WDPO}$ precedes $\overline{WDO}$ by 70ns. Since $\overline{WDO}$ is high when $\overline{WDPO}$ goes low, the Q output of the flip-flop remains high as $\overline{WDO}$ goes low (*Figure 6*). If the watchdog timer is not reset by a transition at WDI, $\overline{WDO}$ remains low and $\overline{WDPO}$ clocks a logic low to the Q output, causing the **SP791** to latch in reset. If the watchdog timer is reset by a transition at WDI, $\overline{WDO}$ goes high and the flip-flop's Q output remains high. Thus, a system shutdown is only caused by two successive watchdog faults.

The internal pull-up resistors associated with $\overline{WDO}$ and $\overline{WDPO}$ connect to VOUT. Therefore, do not connect these outputs directly to CMOS logic that is powered from VCC since, in the absence of VCC (i.e., battery mode), excessive current will flow from $\overline{WDO}$ or $\overline{WDPO}$ through the protection diode(s) of the CMOS-logic inputs to ground.

SELECTING AN ALTERNATIVE WATCHDOG TIMEOUT PERIOD

SWT input controls the watchdog-timeout period. Connecting SWT to VOUT selects the internal 1.6sec watchdog-timeout period. Select an alternative timeout period by connecting a capacitor between SWT and GND. Do not leave SWT floating, and do not connect it to ground. The following formula determines the watchdog-timeout period:

Watchdog Timeout Period = 2.1 x (capacitor value in nF) ms

This formula is valid for capacitance values between 4.7 nF and 100nF (see the Watchdog Timeout vs. Timing Capacitor graph in the *Typical Operating Characteristics).*

CHIP-ENABLE SIGNAL GATING

The **SP791** provides internal gating of chip-enable (CE) signals to prevent erroneous data from corrupting the CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The **SP791** uses a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT.

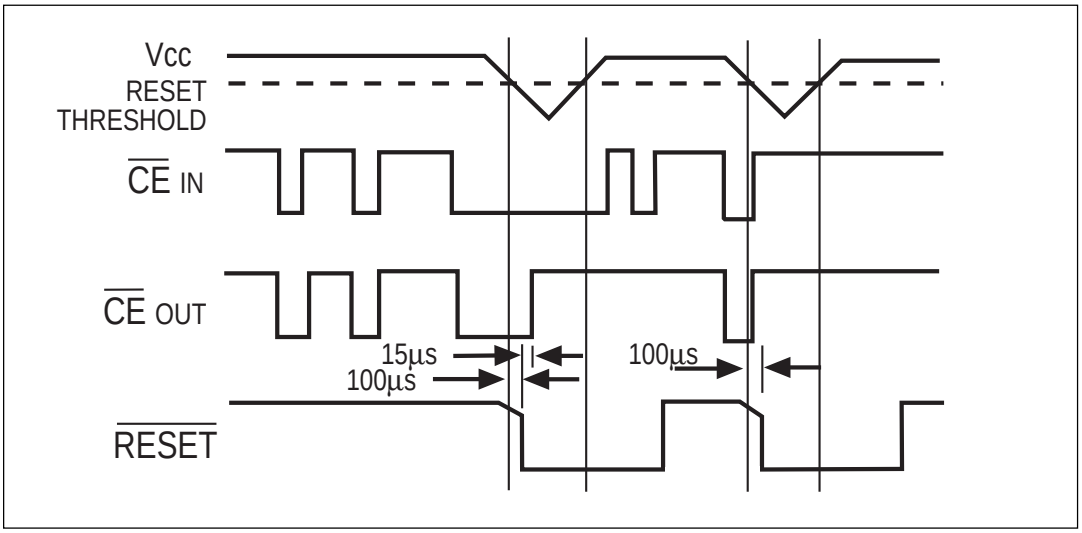


Figure 7. Reset and Chip-Enable Timing

The 10ns maximum $\overline{CE}$ propagation from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the **SP791** to be used with most µPs.

CHIP-ENABLE INPUT

$\overline{CE}$ IN is high impedance (disabled mode) while $\overline{RESET}$ is asserted.

During a power-down sequence where VCC falls below 4.65V, $\overline{CE}$ IN assumes a high impedance state when the voltage at $\overline{CE}$ IN goes high or 15µs after $\overline{RESET}$ is asserted, whichever occurs first, (*Figure 7*).

During a power-up sequence, $\overline{CE}$ IN remains high impedance until $\overline{RESET}$ is deasserted.

In the high-impedance mode, the leakage currents into this input are less than 1µA over temperature. In the low-impedance mode, the impedance of $\overline{CE}$ IN appears as a 65Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the $\overline{CE}$ transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on $\overline{CE}$ OUT (see the Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance graph in the *Typical Operating Characteristics).* The $\overline{CE}$ propagation delay is defined from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver with 50pF load capacitance as in *Figure 8*. For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT and use a low output-impedance driver.

CHIP-ENABLE OUTPUT

In the enabled mode, the impedance of $\overline{CE}$ OUT is equivalent to 65Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 65Ω transmission gate is off and $\overline{CE}$ OUT is actively pulled to VOUT. This source turns off when the transmission gate is enabled.

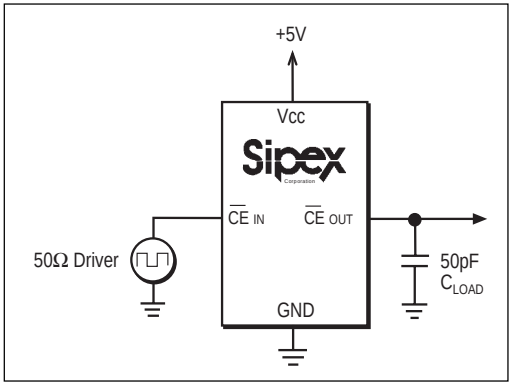


Figure 8. CE Propagation Delay Test Circuit

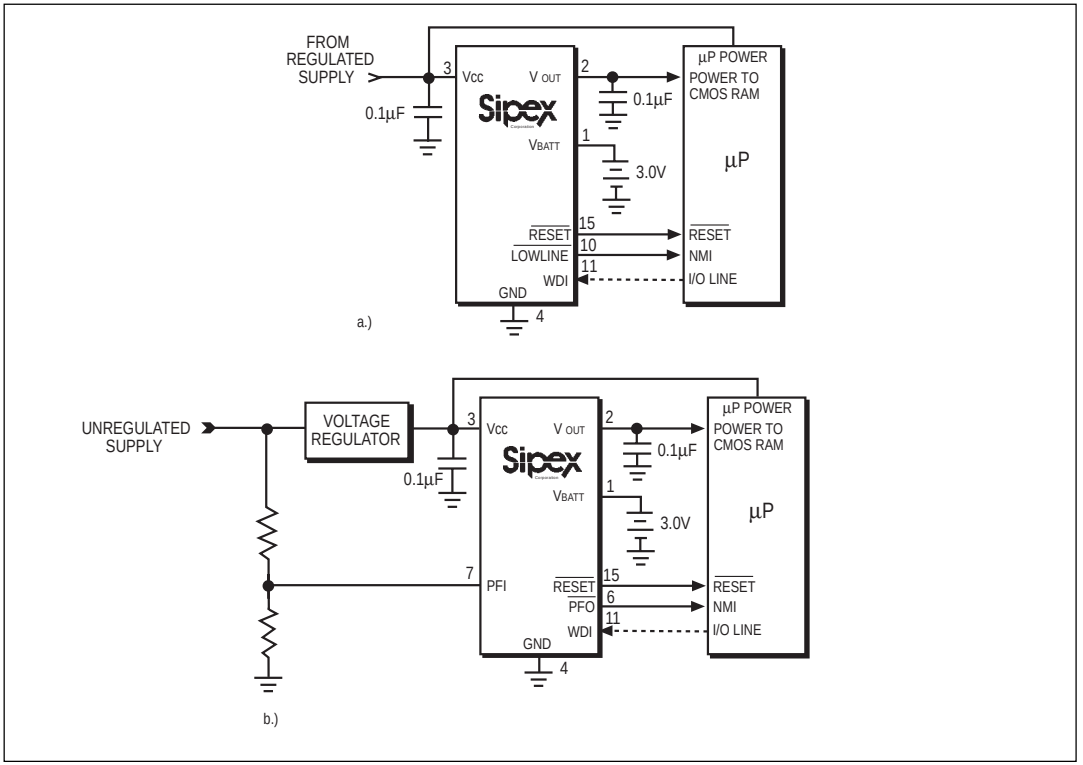


Figure 9. a) If the unregulated supply is inaccessible, LOWLINE generates the NMI for the µP.
b) Use PFO to generate the µP NMI if the unregulated supply is accessible.

LOWLINE OUTPUT

The low-line comparator monitors VCC with a typical threshold voltage 150mV above the reset threshold and has 15mV of hysteresis. $\overline{\text{LOWLINE}}$ typically sinks 3.2mA at 0.1V. For normal operation (Vcc above the $\overline{\text{LOWLINE}}$ threshold), $\overline{\text{LOWLINE}}$ is pulled to VOUT. If access to the unregulated supply is unavailable, use $\overline{\text{LOWLINE}}$ to provide a nonmaskable interrupt (NMI) to the µP as shown in *Figure 9a*.

POWER-FAIL COMPARATOR

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the **SP791**. Common uses include monitoring supplies other than 5V (see the *Typical Operating Circuit* and the *Monitoring a Negative Voltage* section) and early power-fail detection when the unregulated power is easily accessible as shown in *Figure 9b*.

POWER-FAIL INPUT

The Power-Fail Input (PFI) has a guaranteed input leakage of +/-25nA max over temperature. The typical comparator delay is 15µs from VIL to VOL (power failing), and 55µs from VIH to VOH (power being restored). Connect PFI to ground if not used.

POWER-FAIL OUTPUT

The Power-Fail Output ($\overline{\text{PFO}}$) goes low when PFI falls below 1.25V. It sinks 3.2mA with a saturation voltage of 0.1V. With PFI above 1.25V, $\overline{\text{PFO}}$ is actively pulled to VOUT. Connecting PFI through a voltage divider to an unregulated supply allows $\overline{\text{PFO}}$ to generate an NMI as the unregulated power begins to fall (see *Figure 9b*).

INPUT/OUTPUT STATES IN BATTERY-BACKUP MODE

PIN	NAME	STATUS
1	VBATT	Supply current is 1µA maximum When $V_{CC} < V_{BATT}$-1.2V
2	VOUT	VOUT is connected to VBATT through an Internal PMOS switch.
3	VCC	Battery-switchover comparator monitors VCC for active switchover. V_{CC} is disconnected from V_{OUT}
4	GND	GND-0V reference for all signals.
5	BATT ON	Logic high. The open-circuit output is equal to VOUT.
6	$\overline{PFO}$	The power-fail comparator is disabled $\overline{PFO}$ is forced low.
7	PFI	The power-fail comparator is disabled
8	SWT	SWT is Ignored.
9	$\overline{MR}$	$\overline{MR}$ is ignored.
10	$\overline{LOWLINE}$	Logic low.
11	WDI	WDI is ignored, and goes high impedance.
12	$\overline{CE}$ OUT	Logic high. The open-circuit output voltage is equal to VOUT.
13	$\overline{CE}$ IN	High Impedance.
14	$\overline{WDO}$	Logic high. The open-circuit output voltage is equal to VOUT.
15	$\overline{RESET}$	Logic low.
16	$\overline{WDPO}$	Logic high. The open-circuit output voltage is equal to VOUT.

Table 1. Input/Output states in Battery-Backup mode

To enter the Battery-Backup mode, V_{CC} must be less than the Reset threshold and less than V_{BATT}.

BATTERY-BACKUP MODE

The **SP791** requires two conditions to switch to battery-backup mode: 1) VCC must be below the reset threshold; 2) VCC must be below VBATT. *Table 1* lists the status of the inputs and outputs in battery-backup mode.

BATTERY ON OUTPUT

The Battery On Output (BATT ON) indicates the status of the internal VCC/battery-switchover comparator, which controls the internal VCC and VBATT switches. For VCC greater than VBATT (ignoring the small hysteresis effect), BATT ON is a logic low. For VCC less than VBATT, BATT ON is a logic high. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications (see *Typical Operating Circuit).*

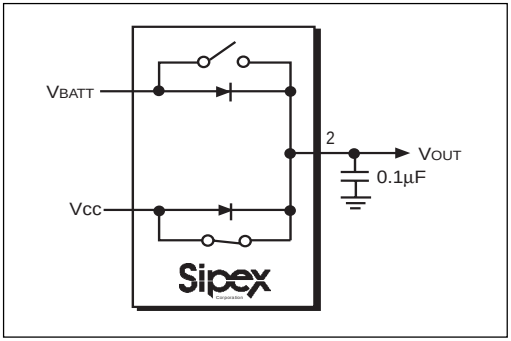


Figure 10. VCC and VBATT-to-VOUT Switch

INPUT SUPPLY VOLTAGE

The Input Supply Voltage (VCC) should be a regulated +5V source. VCC connects to VOUT via a parallel diode and a large PMOS switch (*Figure 10*). The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

BACKUP-BATTERY INPUT

The Backup-Battery Input (VBATT) is similar to VCC, except the PMOS switch and parallel diode are much smaller. Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of this input is less than 1µA over temperature and supply voltage.

OUTPUT SUPPLY VOLTAGE

The Output Supply Voltage (VOUT) supplies all the current to the external system and internal circuitry. All open-circuit outputs will, for example, assume the VOUT voltage in their high states rather than the VCC voltage. At the maximum source current of 250mA, VOUT will typically be 200mV below VCC. VOUT should be decoupled with 0.1µF capacitor.

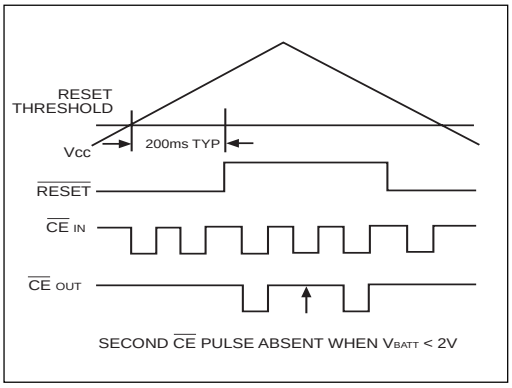


Figure 11. Backup-Battery Monitor Timing Diagram

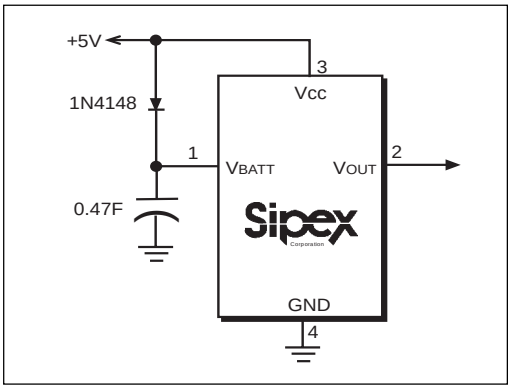


Figure 12. High Capacity Capacitor on VBATT

LOW-BATTERY MONITOR

The **SP791** low-battery voltage function monitors VBATT. Low-battery detection of 2.0V ±0.15V is monitored only during the reset-timeout period (200ms) that occurs either after a normal power-up sequence or after the $\overline{MR}$ reset input has been returned to its high state. If the battery voltage is below 2.0V, the second CE pulse is inhibited after reset timeout. If the battery voltage is above 2.0V, all CE pulses are allowed through the CE gate after the reset timeout period. To use this function, after the 200ms reset delay, write 00 (HEX) to a location using the first CE pulse, and write FF (HEX) to the same location using the second CE pulse following $\overline{RESET}$ going inactive on power-up. The contents of the memory then indicates a good battery (FF) or a low battery (00), *Figure 11*.

TYPICAL APPLICATIONS

The **SP791** is not short-circuit protected. Shorting VOUT to ground, other than power-up transients such as charging a decoupling capacitor, may destroy the device. All open-circuit outputs swing between VOUT and GND rather than VCC and GND. If long leads connect to the chip inputs, ensure that these lines are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

1) Normal operating mode with all circuitry powered up from VCC. Typical supply current from VCC is 40µA, while only leakage currents flow from the battery.

2) Battery-backup mode where VCC is typically within 0.7V below VBATT. All circuitry is powered up from VBATT, and the supply current is typically less than 40µA.

3) Battery-backup mode where VCC is less than VBATT by at least 0.7V. VBATT supply current is less than 1µA.

USING HIGH CAPACITY CAPACITOR WITH THE SP791

VBATT has the same operating voltage range as VCC, and the battery-switchover threshold voltages are typically +30mV centered at VBATT, allowing use of a capacitor and a simple charging circuit as a backup source (see *Figure 12)*.

If VCC is above the reset threshold and VBATT is 0.5V above VCC, current flows to VOUT and VCC from VBATT until the voltage at VBATT is less than 0.5V above VCC.

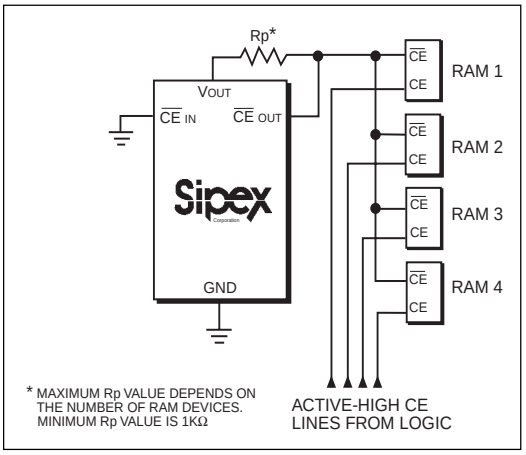


Figure 13. Alternate CE Gating

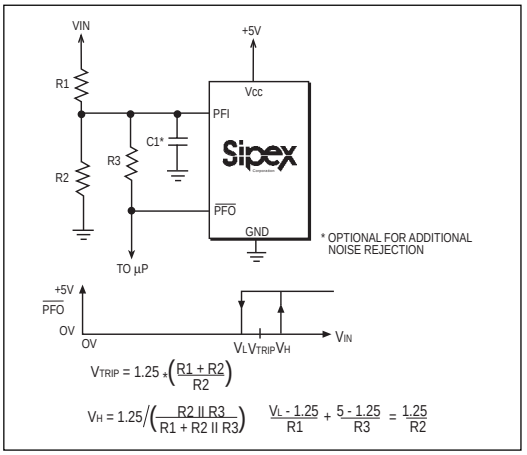


Figure 14. Adding Hysteresis to the Power-Fail Comparator

Leakage current through the capacitor charging diode and the **SP791** internal power diode eventually discharges the capacitor to VCC. Also, if VCC and VBATT start from 0.5V above the reset threshold and power is lost at VCC, the capacitor on VBATT discharges through VCC until VBATT reaches the reset threshold; the **SP791** then switches to battery-backup mode.

USING SEPARATE POWER SUPPLIES FOR VBATT AND VCC

If using separate power supplies for VCC and VBATT, VBATT must be less than 0.3V above VCC when VCC is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at VCC, current flows continuously from VBATT to VCC via the VBATT-to-VOUT diode and the VOUT-to-VCC switch until the circuit is broken.

ALTERNATIVE CHIP-ENABLE GATING

Using memory devices with $\overline{CE}$ and $\overline{CE}$ inputs allows the **SP791** $\overline{CE}$ loop to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull up $\overline{CE}$ OUT to VOUT, and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device as shown in *Figure 13*. The $\overline{CE}$ input of each part then connects directly to the chip-select logic, which does not have to be gated by the **SP791**.

ADDING HYSTERESIS TO THE POWER-FAIL COMPARATOR

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when VIN is near the trip point. *Figure 14* shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 to R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

MONITORING A NEGATIVE VOLTAGE

The power-fail comparator can be used to monitor a negative supply voltage using the circuit shown in *Figure 15*. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the VCC voltage, and resistors R1 and R2.

BACKUP-BATTERY REPLACEMENT

The backup battery may be disconnected while VCC is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

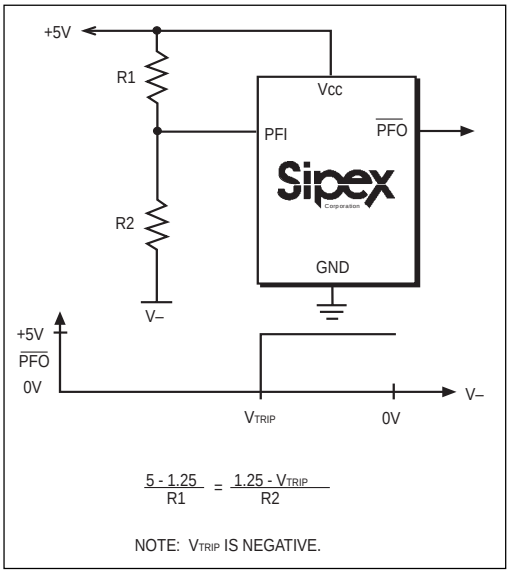


Figure 15. Monitoring a Negative Voltage

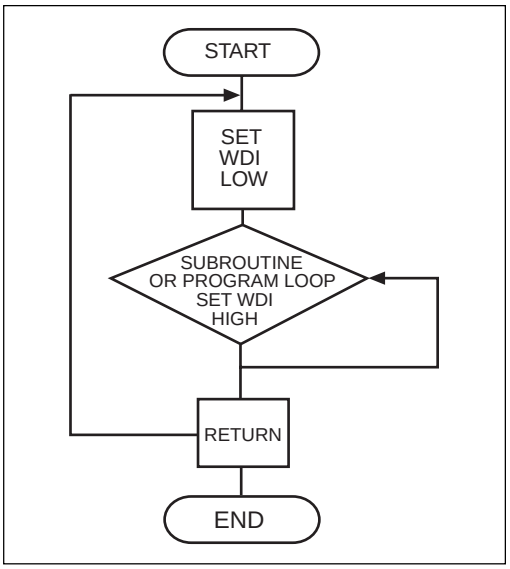


Figure 16. Watchdog Flow Diagram

NEGATIVE-GOING V_{CC} TRANSIENTS

The **SP791** is relatively immune to short-duration negative-going VCC transients resulting from power up, power down, and brownout conditions. It is usually undesirable to reset the µP when VCC experiences only small glitches.

Typically, a VCC transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the VCC pin provides additional transient immunity.

CONNECTING A TIMING CAPACITOR TO THE SWT PIN

To prevent timing errors minimize external current leakage sources at this pin, and locate the capacitor as close to SWT as possible. The sum of PC board leakage + SWT capacitor leakage must be small compared to ±100 nA.

WATCHDOG SOFTWARE CONSIDERATIONS

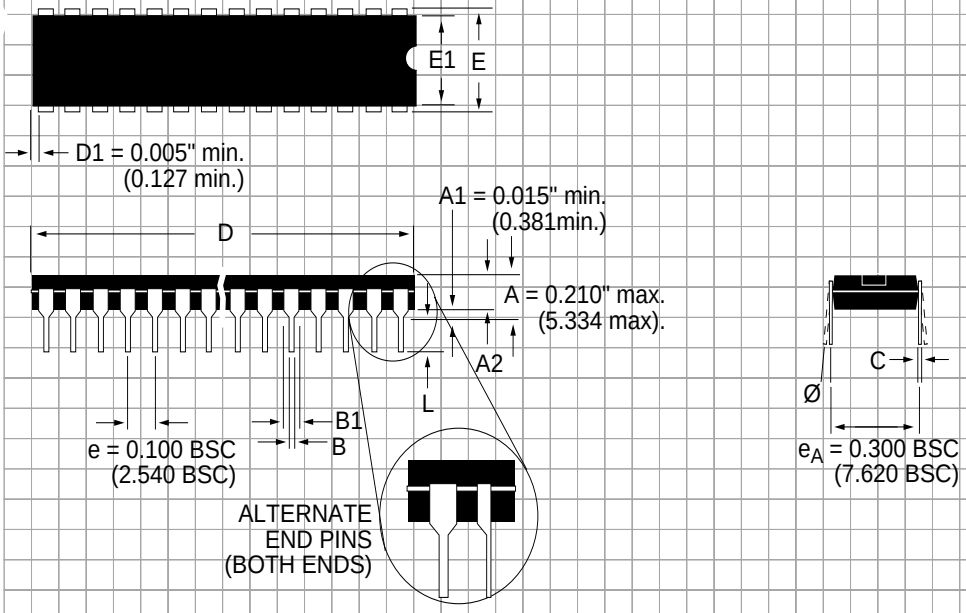
A way to help the watchdog timer keep a closer watch on software execution involves setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out.

Figure 16 shows an example flow diagram where the I/O driving the watchdog input is set low at the beginning of the program, set high at the beginning of every subroutine or loop, then set low again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set high and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

MAXIMUM VCC FALL TIME

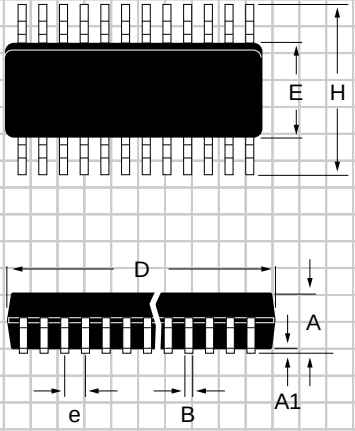
The VCC fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/µs. A standard rule of thumb for filter capacitance on most regulators is on the order of 100µF per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial VCC fall rate is just the inverse of 1A/100µF = 0.01V/µs. The VCC fall rate decreases with time as VCC falls exponentially, which more than satisfies the maximum fall-time requirement.

PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN	18–PIN	20–PIN	22–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN	14–PIN	16–PIN			
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)			
A1	0.004/0.010 (0.102/0.249	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)			
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)			
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)			
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)			
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)			
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)			
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)			
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)			
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)			

ORDERING INFORMATION

Model	Temperature Range	Package
SP791CP	0˚C to +70˚C	16-pin, Plastic DIP
SP791CN	0˚C to +70˚C	16-pin, Narrow SOIC
SP791EP	-40˚C to +85˚C	16–pin, Plastic Dip
SP791EN	-40˚C to +85˚C	16–pin, Narrow SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

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