## Precision, Low Noise FGA™ Voltage References

The ISL21009 FGA™ voltage references are extremely low power, high precision, and low noise voltage references fabricated on Intersil's proprietary Floating Gate Analog technology. The ISL21009 features very low noise ($4\mu V_{P-P}$ for 0.1Hz to 10Hz), low operating current (180µA, Max), and 3ppm/°C of temperature drift. In addition, the ISL21009 family features guaranteed initial accuracy as low as ±0.5mV

This combination of high initial accuracy, low drift, and low output noise performance of the ISL21009 enables versatile high performance control and data acquisition applications with low power consumption.

## Available Options

| PART NUMBER | $V_{OUT}$ OPTION (V) | INITIAL ACCURACY (mV) | TEMPCO. (ppm/°C) |
|---|---|---|---|
| ISL21009BFB812Z *Coming Soon* | 1.250 | ±0.5 | 3 |
| ISL21009CFB812Z *Coming Soon* | 1.250 | ±1.0 | 5 |
| ISL21009DFB812Z *Coming Soon* | 1.250 | ±2.0 | 10 |
| ISL21009BFB825Z | 2.500 | ±0.5 | 3 |
| ISL21009CFB825Z | 2.500 | ±1.0 | 5 |
| ISL21009DFB825Z | 2.500 | ±2.0 | 10 |
| ISL21009BFB850Z | 5.000 | ±0.5 | 3 |
| ISL21009CFB850Z | 5.000 | ±1.0 | 5 |
| ISL21009DFB850Z | 5.000 | ±2.0 | 10 |

## Features

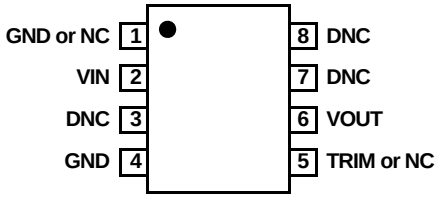
- Output Voltages . . . . . 1.25V, 2.500V, 5.000V
- Initial Accuracy . . . . . .±0.5mV, ±1.0mV, ±2.0mV
- Input Voltage Range. . . . . Up to 16.5V
- Output Voltage Noise . . . . . $4uV_{P-P}$ (0.1Hz to 10Hz)
- Supply Current . . . . . .180µA (Max)
- Temperature Coefficient . . . 3ppm/°C, 5ppm/°C, 10ppm/°C
- Output Current Capability. . . . . .±7.0mA
- Operating Temperature Range. . . . . .-40°C to +125°C
- Package . . . . . 8 Ld SOIC
- Pb-Free Plus Anneal Available (RoHS Compliant)

## Applications

- High Resolution A/Ds and D/As
- Digital Meters
- Bar Code Scanners
- Basestations
- Battery Management/Monitoring
- Industrial/Instrumentation Equipment

## Pinout

**ISL21009**
**(8 LD SOIC)**
TOP VIEW




## Pin Descriptions

| PIN NUMBER | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | GND or NC | Can be either Ground or No Connect |
| 4 | GND | Ground Connection |
| 2 | VIN | Power Supply Input Connection |
| 6 | VOUT | Voltage Reference Output Connection |
| 5 | TRIM | Allows user trim typically ±2.5%. Leave Unconnected when unused. |
| 3,7,8 | DNC | Do Not Connect; Internal Connection – Must Be Left Floating |

## Ordering Information

| PART NUMBER (Note) | PART MARKING | $V_{OUT}$ OPTION (V) | GRADE | QUANTITY PER REEL/TUBE | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|---|---|---|
| ISL21009BFB825Z | 21009BF Z25 | 2.500 | ±0.5mV, 3ppm/°C | 100 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009BFB825Z-TK | 21009BF Z25 | 2.500 | ±0.5mV, 3ppm/°C | 1000 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009CFB825Z | 21009CF Z25 | 2.500 | ±1.0mV, 5ppm/°C | 100 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009CFB825Z-TK | 21009CF Z25 | 2.500 | ±1.0mV, 5ppm/°C | 1000 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009DFB825Z | 21009DF Z25 | 2.500 | ±2.0mV, 10ppm/°C | 100 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009DFB825Z-TK | 21009DF Z25 | 2.500 | ±2.0mV, 10ppm/°C | 1000 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009BFB850Z | 21009BF Z50 | 5.000 | ±0.5mV, 3ppm/°C | 100 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009BFB850Z-TK | 21009BF Z50 | 5.000 | ±0.5mV, 3ppm/°C | 1000 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009CFB850Z | 21009CF Z50 | 5.000 | ±1.0mV, 5ppm/°C | 100 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009CFB850Z-TK | 21009CF Z50 | 5.000 | ±1.0mV, 5ppm/°C | 1000 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009DFB850Z | 21009DF Z50 | 5.000 | ±2.0mV, 10ppm/°C | 100 | -40 to +125 | 8 Ld SOIC | M8.15 |
| ISL21009DFB850Z-TK | 21009DF Z50 | 5.000 | ±2.0mV, 10ppm/°C | 1000 | -40 to +125 | 8 Ld SOIC | M8.15 |

NOTES:

A) Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

B) Add “-T” suffix for tape and reel

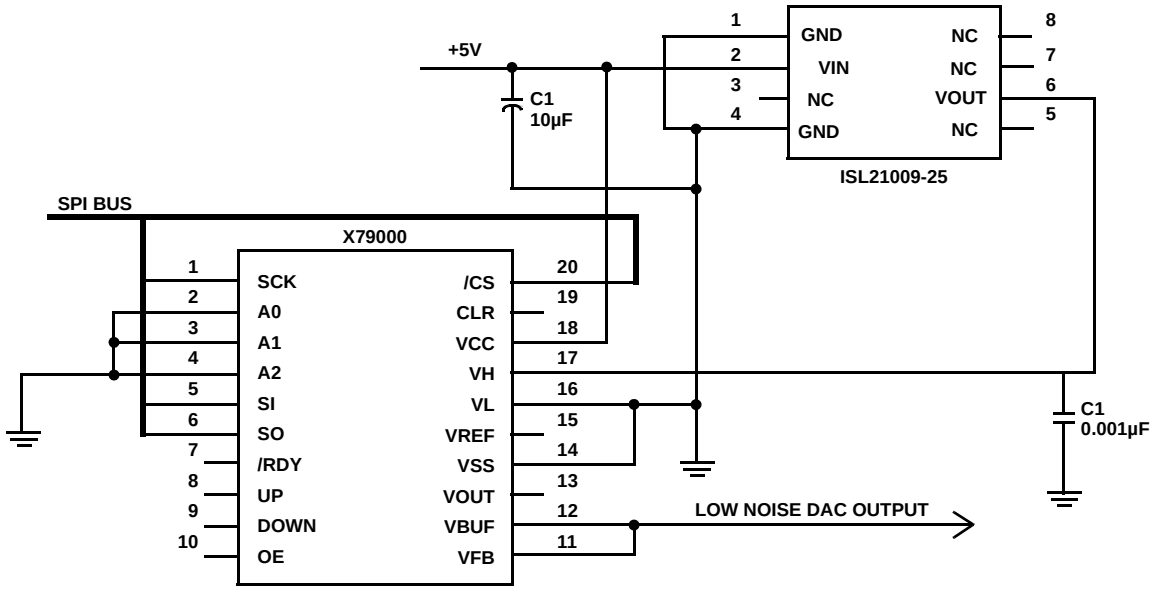



**FIGURE 1. TYPICAL APPLICATION PRECISION 12-BIT SUBRANGING DAC**

## Absolute Voltage Ratings

Storage Temperature Range . . . . . .-65°C to +150°C
Max Voltage $V_{IN}$ to Gnd . . . . . .-0.5V to +18V
Max Voltage $V_{OUT}$ to Gnd (10s). . . . . -0.5V to $V_{OUT}$ +1V
Voltage on “DNC” pins . . . . No connections permitted to these pins.
Lead Temperature, soldering (10s) . . . . . .+260°C
ESD Ratings
(HBM) . . . . . .6kV
(CBM) . . . . . .2kV

## Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +125°C

## Thermal Information

Continuous Power Dissipation ($T_A$ = +70°C)

8 Ld SOIC derate 5.88mW/°C above +70°C. . . . . 471mW
Pb-free reflow profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Common Electrical Specifications (ISL21009-25, -50)

$T_A$ = -40°C to +125°C, unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OA}$ | $V_{OUT}$ Accuracy @ $T_A$ = +25°C | ISL21009B | -0.5 | | +0.5 | mV |
| | | ISL21009C | -1.0 | | +1.0 | mV |
| | | ISL21009D | -2.0 | | +2.0 | mV |
| TC $V_{OUT}$ | Output Voltage Temperature Coefficient (Note 1) | ISL21009B | | | 3 | ppm/°C |
| | | ISL21009C | | | 5 | ppm/°C |
| | | ISL21009D | | | 10 | ppm/°C |
| $\Delta V_{OUT}/\Delta t$ | Long Term Stability (Note 4) | $T_A$ = +25°C | | 50 | | ppm/$\sqrt{1kHrs}$ |
| | Trim Range | | ±2.0 | ±2.5 | | % |
| $I_{SC}$ | Short Circuit Current (Note 3) | $T_A$ = +25°C, $V_{OUT}$ tied to Gnd | | 10 | | mA |
| $t_R$ | Turn on Settling Time | $V_{OUT}$ = ±0.1% | | 100 | | µs |
| | Ripple Rejection | f = 10kHz | | 60 | | dB |
| $e_N$ | Output Voltage Noise | 0.1Hz ≤ f ≤ 10Hz | | 4 | | $\mu V_{P-P}$ |
| $V_N$ | Broadband Voltage Noise | 10Hz ≤ f ≤ 1kHz | | 2.2 | | $\mu V_{RMS}$ |
| | Noise Density | f = 1kHz | | 60 | | nV/$\sqrt{Hz}$ |

## Electrical Specifications (ISL21009-25, $V_{OUT}$ = 2.50V)

$V_{IN}$ = 5.0V, $T_A$ = -40°C to +125°C, unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage | | | 2.500 | | V |
| $V_{IN}$ | Input Voltage Range | | 3.5 | | 16.5 | V |
| $I_{IN}$ | Supply Current | | | 95 | 180 | µA |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line Regulation | 3.5V ≤ $V_{IN}$ ≤ 5.5V | | 50 | 150 | µV/V |
| | | 5.5V ≤ $V_{IN}$ ≤ 16.5V | | 10 | 50 | µV/V |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load Regulation | Sourcing: 0mA ≤ $I_{OUT}$ ≤ 7mA | | 10 | 50 | µV/mA |
| | | Sinking: -7mA ≤ $I_{OUT}$ ≤ 0mA | | 20 | 100 | µV/mA |
| $\Delta V_{OUT}/\Delta T_A$ | Thermal Hysteresis (Note 2) | $\Delta T_A$ = +125°C | | 100 | | ppm |

## Electrical Specifications (ISL21009-50, $V_{OUT}$ = 5.0V)

$V_{IN}$ = 10.0V, $T_A$ = -40°C to +125°C, unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage | | | 5.000 | | V |
| $V_{IN}$ | Input Voltage Range | | 5.5 | | 16.5 | V |
| $I_{IN}$ | Supply Current | | | 95 | 180 | µA |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line Regulation | 5.5V ≤ $V_{IN}$ ≤ 16.5V | | 20 | 90 | µV/V |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load Regulation | Sourcing: 0mA ≤ $I_{OUT}$ ≤ 7mA | | 10 | 60 | µV/mA |
| | | Sinking: -7mA ≤ $I_{OUT}$ ≤ 0mA | | 20 | 100 | µV/mA |
| $\Delta V_{OUT}/\Delta T_A$ | Thermal Hysteresis (Note 2) | $\Delta T_A$ = +125°C | | 50 | | ppm |

NOTES:

1. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in $V_{OUT}$ is divided by the temperature range; in this case, -40°C to +125°C = +165°C.
2. Thermal Hysteresis is the change of $V_{OUT}$ measured @ $T_A$ = +25°C after temperature cycling over a specified range, $\Delta T_A$. $V_{OUT}$ is read initially at $T_A$ = +25°C for the device under test. The device is temperature cycled and a second $V_{OUT}$ measurement is taken at +25°C. The difference between the initial $V_{OUT}$ reading and the second $V_{OUT}$ reading is then expressed in ppm. For $\Delta T_A$ = +165°C, the device under test is cycled from +25°C to +125°C to -40°C to +25°C.
3. Guaranteed by device characterization and/or correlation to other device tests.
4. FGA voltage reference long term drift is a logarithmic characteristic. Changes that occur after the first few hundred hours of operation are significantly smaller with time, asymptotically approaching zero beyond 1,000 hours. Because of this decreasing characteristics, long term drift is specified in ppm/$\sqrt{1kHrs}$.

## *Typical Performance Curves (ISL21009-25) ($R_{EXT}$ = 100kΩ)*

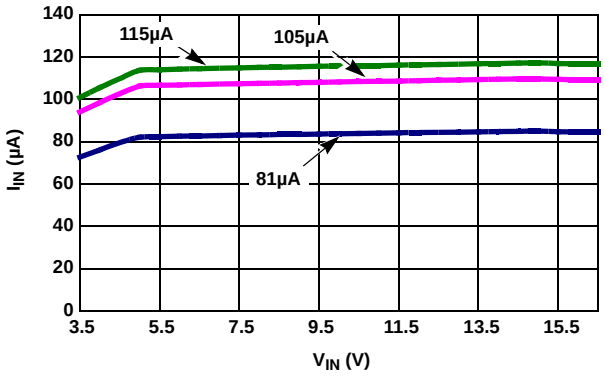



FIGURE 2. $I_{IN}$ vs $V_{IN}$ 3 UNITS

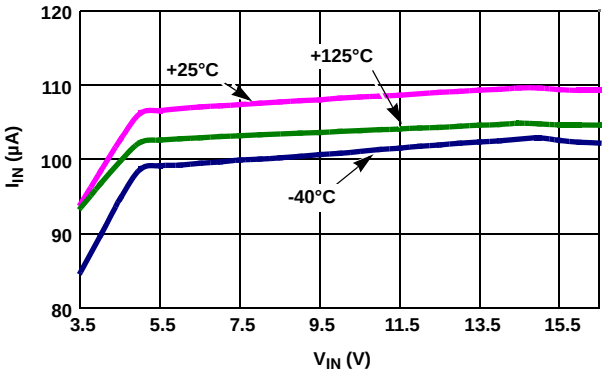



FIGURE 3. $I_{IN}$ vs $V_{IN}$, 3 TEMPERATURES

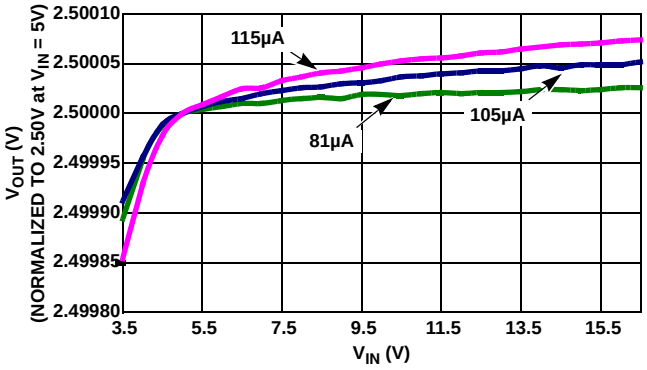



FIGURE 4. LINE REGULATION

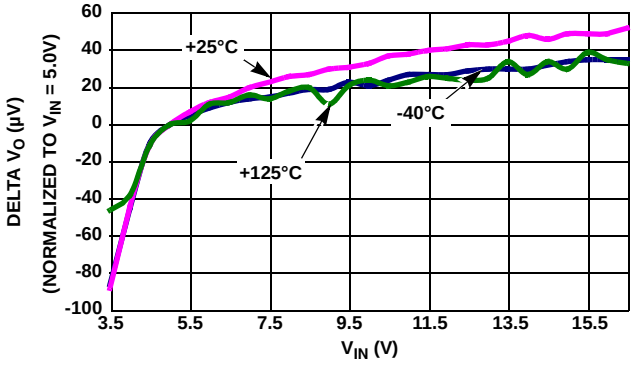



FIGURE 5. LINE REGULATION OVER TEMPERATURE

## Typical Performance Curves (ISL21009-25) ($R_{EXT}$ = 100kΩ) (Continued)

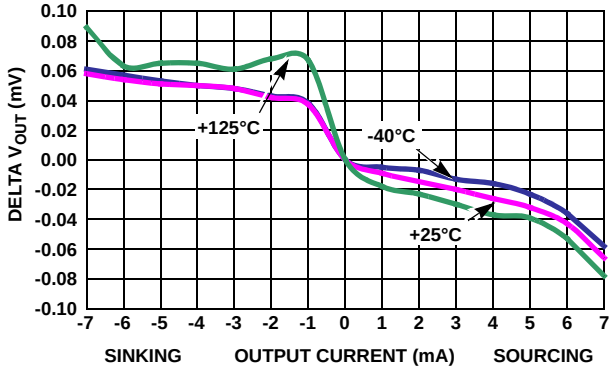



FIGURE 6. LOAD REGULATION

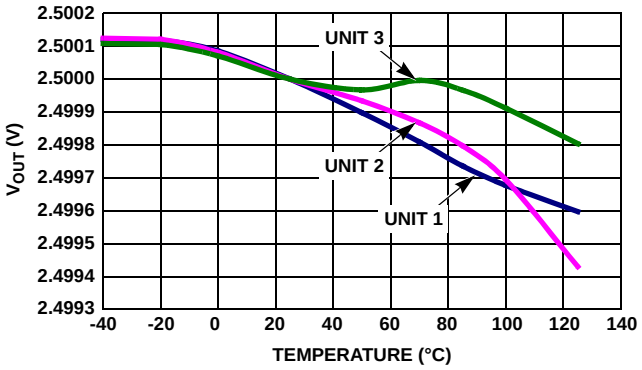



FIGURE 7. $V_{OUT}$ vs TEMPERATURE

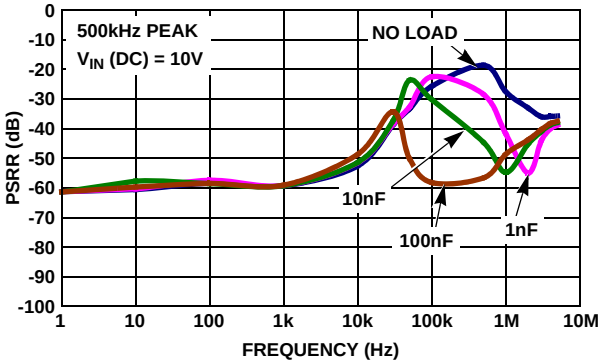



FIGURE 8. PSRR AT DIFFERENT CAPACITIVE LOADS

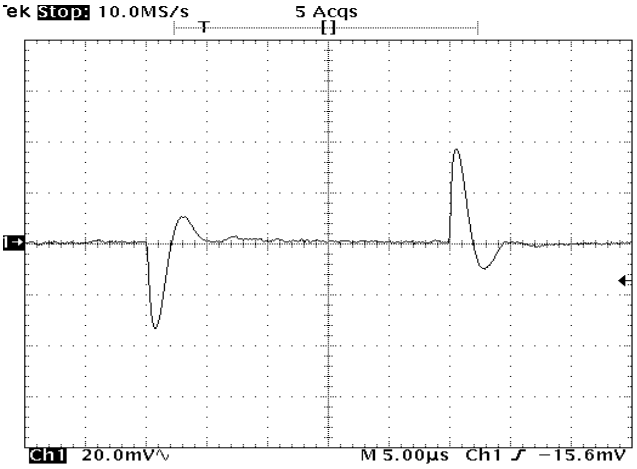



FIGURE 9. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

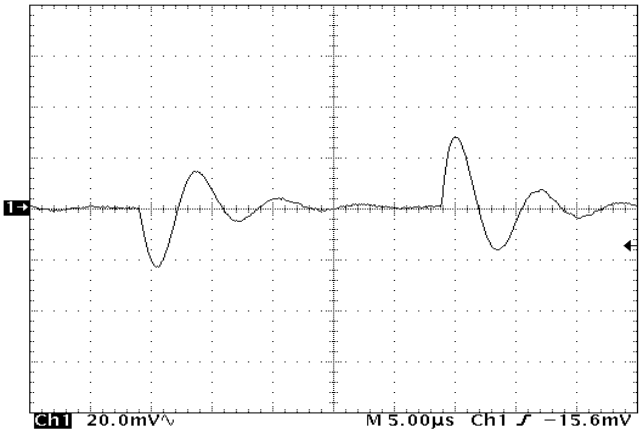



FIGURE 10. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

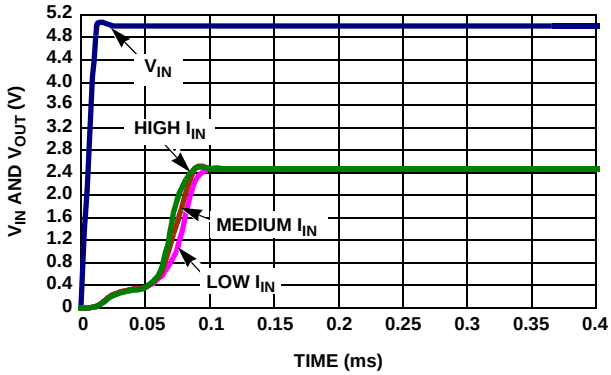



FIGURE 11. TURN ON TIME

## Typical Performance Curves (ISL21009-25) ($R_{EXT}$ = 100kΩ) (Continued)

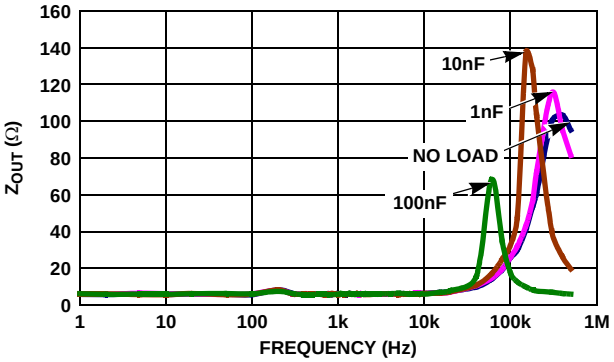



FIGURE 12. $Z_{OUT}$ vs FREQUENCY

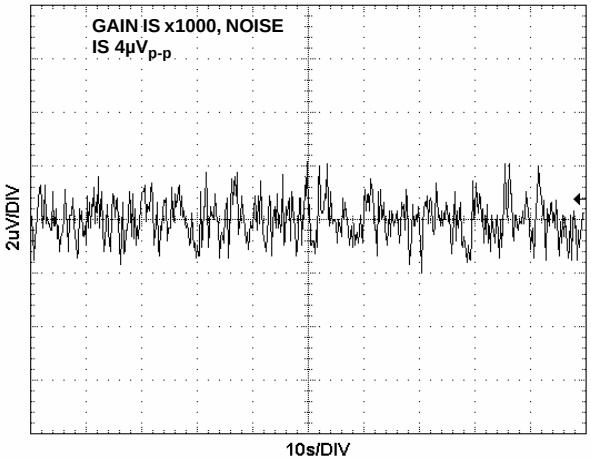



FIGURE 13. $V_{OUT}$ NOISE, 0.1Hz to 10Hz

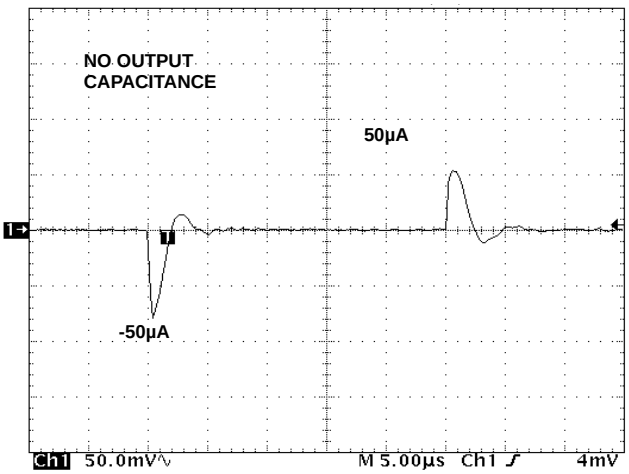



FIGURE 14. LOAD TRANSIENT RESPONSE

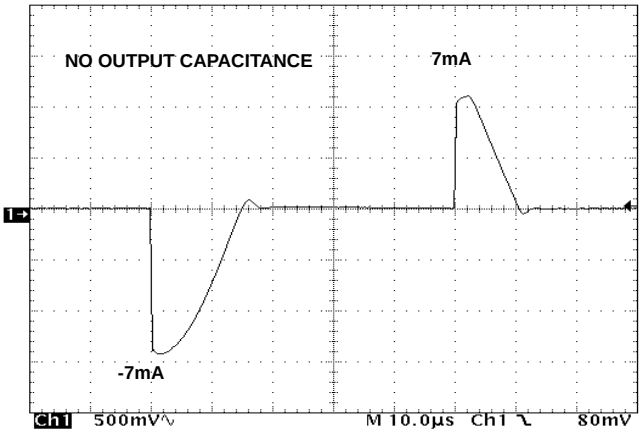



FIGURE 15. LOAD TRANSIENT RESPONSE

## Typical Performance Curves (ISL21009-50) ($R_{EXT}$ = 100kΩ)

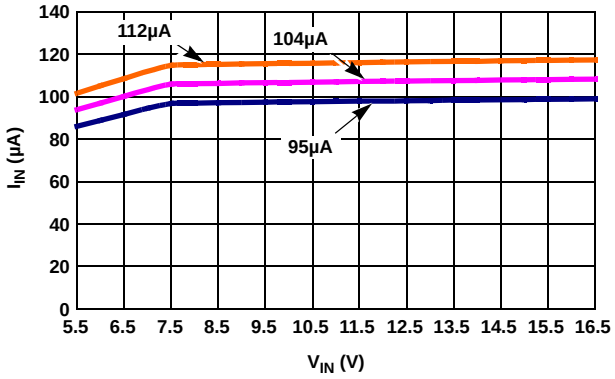



FIGURE 16. $I_{IN}$ vs $V_{IN}$ 3 UNITS

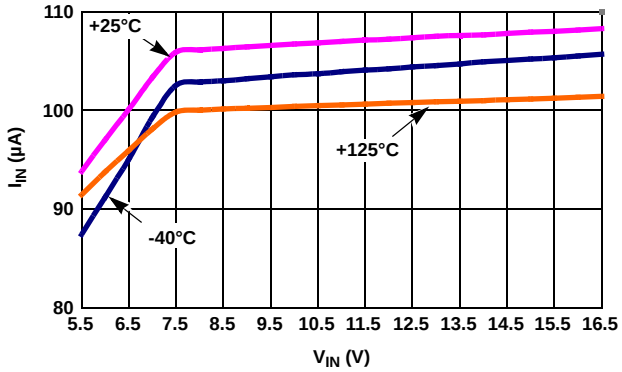



FIGURE 17. $I_{IN}$ vs $V_{IN}$, 3 TEMPERATURES

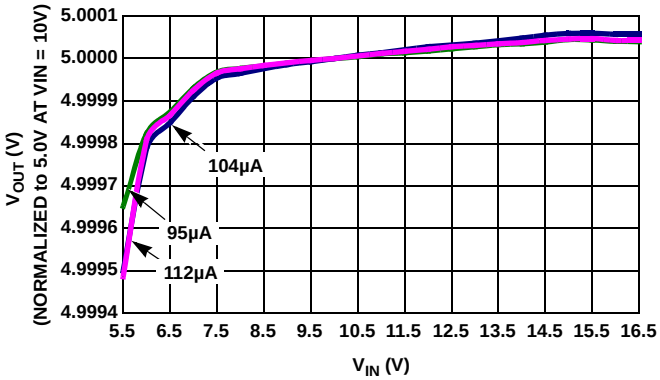



FIGURE 18. LINE REGULATION

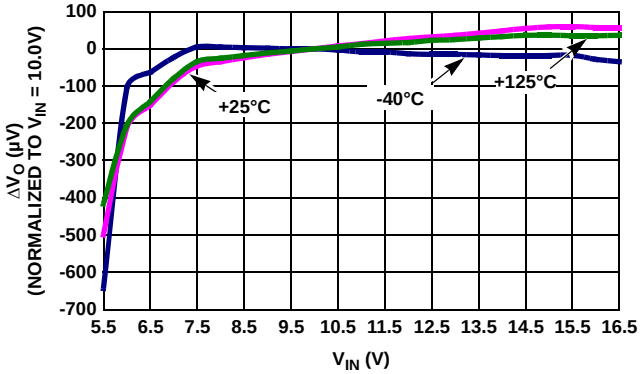



FIGURE 19. LINE REGULATION OVER TEMPERATURE

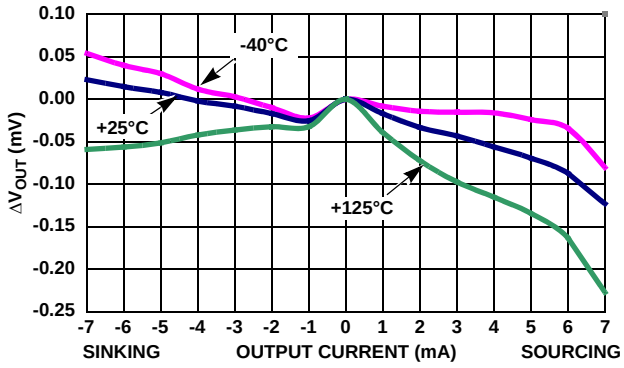



FIGURE 20. LOAD REGULATION

## Typical Performance Curves (ISL21009-50) ($R_{EXT}$ = 100kΩ) (Continued)

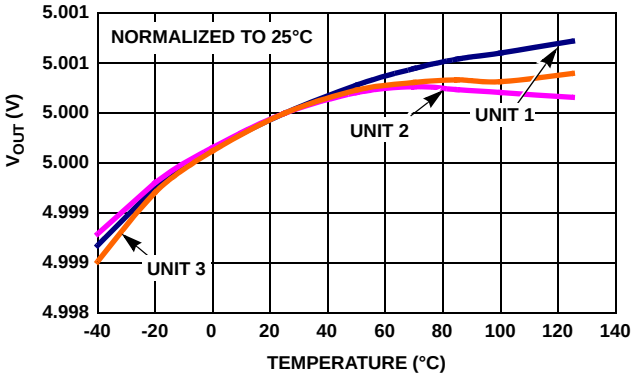



FIGURE 21. $V_{OUT}$ vs TEMPERATURE

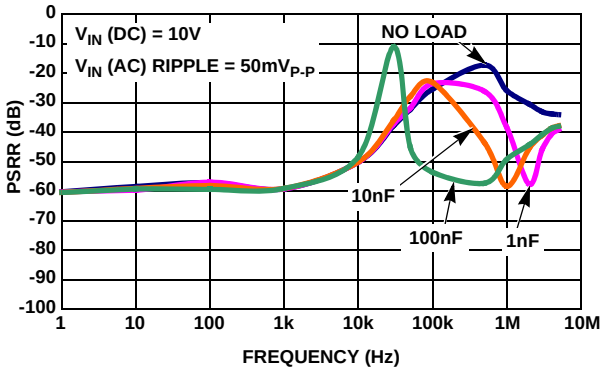



FIGURE 22. PSRR AT DIFFERENT CAPACITIVE LOADS

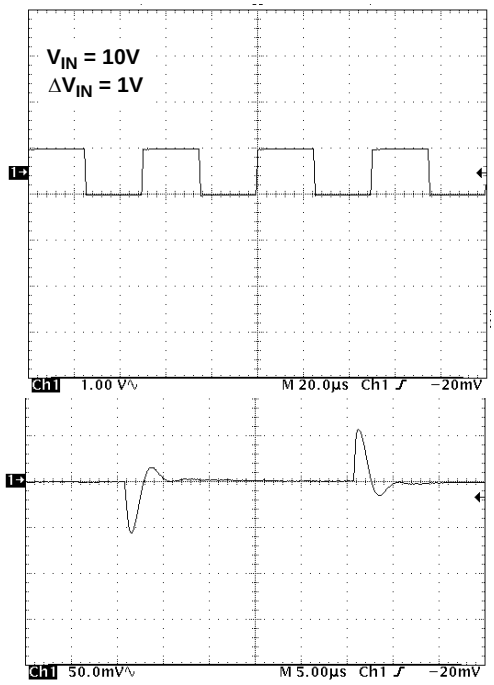



FIGURE 23. LINE TRANSIENT RESPONSE, NO CAPACITIVE LOAD

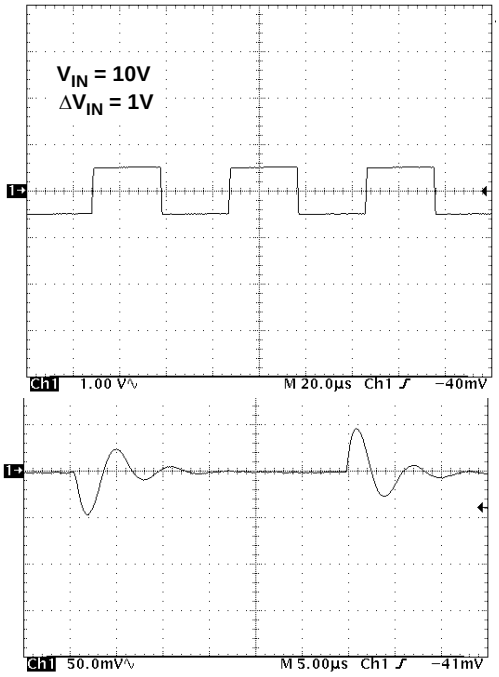



FIGURE 24. LINE TRANSIENT RESPONSE, 0.001µF LOAD CAPACITANCE

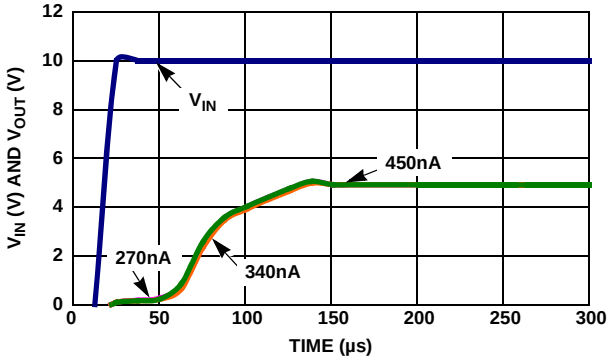



FIGURE 25. TURN ON TIME

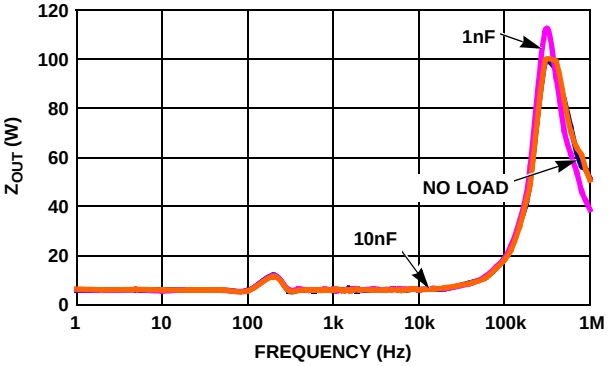



FIGURE 26. $Z_{OUT}$ vs FREQUENCY

## Typical Performance Curves (ISL21009-50) ($R_{EXT}$ = 100kΩ) (Continued)

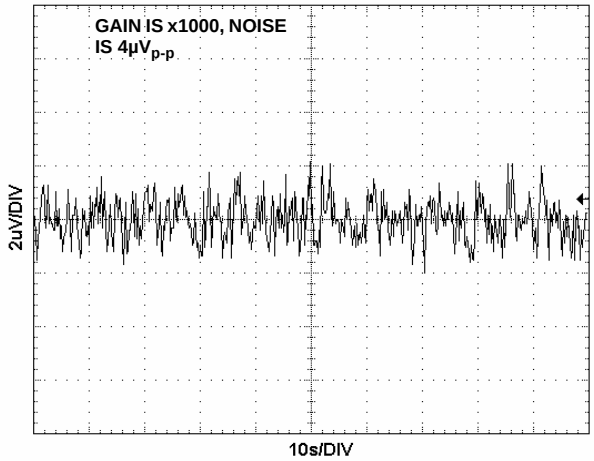



FIGURE 27. $V_{OUT}$ NOISE, 0.1Hz to 10Hz

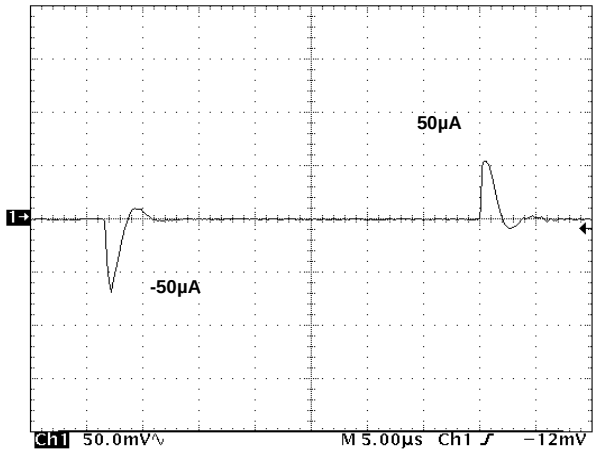



FIGURE 28. LOAD TRANSIENT RESPONSE

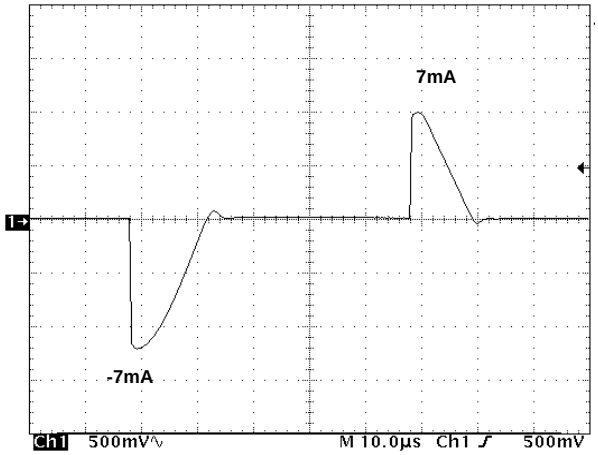



FIGURE 29. LOAD TRANSIENT RESPONSE

## Applications Information

### FGA Technology

The ISL21009 voltage reference uses floating gate technology to create references with very low drift and supply current. Essentially the charge stored on a floating gate cell is set precisely in manufacturing. The reference voltage output itself is a buffered version of the floating gate voltage. The resulting reference device has excellent characteristics which are unique in the industry: very low temperature drift, high initial accuracy, and almost zero supply current. Also, the reference voltage itself is not limited by voltage bandgaps or zener settings, so a wide range of reference voltages can be programmed (standard voltage settings are provided, but customer-specific voltages are available).

The process used for these reference devices is a floating gate CMOS process, and the amplifier circuitry uses CMOS transistors for amplifier and output transistor circuitry. While providing excellent accuracy, there are limitations in output noise level and load regulation due to the MOS device characteristics. These limitations are addressed with circuit techniques discussed in other sections.

### Micropower Operation

The ISL21009 consumes extremely low supply current due to the proprietary FGA technology. Low noise performance is achieved using optimized biasing techniques. Supply current is typically 95µA and noise is 4µ$V_{P-P}$ benefitting precision, low noise portable applications such as handheld meters and instruments.

Data Converters in particular can utilized the ISL21009 as an external voltage reference. Low power DAC and ADC circuits will realize maximum resolution with lowest noise.

### Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a plastic SOIC package which will subject the die to mild stresses when the PC board is heated and cooled and slightly changes shape. Placing the device in areas subject to slight twisting can cause degradation of the accuracy of the reference voltage due to these die stresses. It is normally best to place the device near the edge of a board, or the shortest side, as the axis of bending is most limited at that location. Mounting the device in a cutout also minimizes flex. Obviously mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

### Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically $4\mu V_{P-P}$. The noise measurement is made with a bandpass filter made of a 1 pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Noise in the 10kHz to 1MHz bandwidth is approximately $40\mu V_{P-P}$ with no capacitance on the output. This noise measurement is made with a 2 decade bandpass filter made of a 1 pole high-pass filter with a corner frequency at 1/10 of the center frequency and 1-pole low-pass filter with a corner frequency at 10 times the center frequency. Load capacitance up to 1000pF can be added but will result in only marginal improvements in output noise and transient response. The output stage of the ISL21009 is not designed to drive heavily capactive loads, so for load capacitances above 0.001µF the noise reduction network shown in Figure 30 is recommended. This network reduces noise significantly over the full bandwidth. Noise is reduced to less than $20\mu V_{P-P}$ from 1Hz to 1MHz using this network with a 0.01µF capacitor and a 2kΩ resistor in series with a 10µF capacitor. Also, transient response is improved with higher value output capacitor. The 0.01µF value can be increased for better load transient response with little sacrifice in output stability.

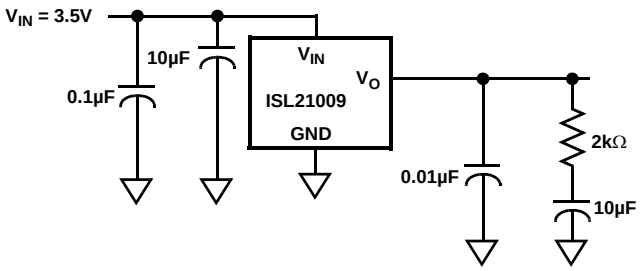



**FIGURE 30. HANDLING HIGH LOAD CAPACITANCE**

### Turn-On Time

The ISL21009 devices have low supply current and thus the time to bias up internal circuitry to final values will be longer than with higher power references. Normal turn-on time is typically 100µs. This is shown in Figure 11. Circuit design must take this into account when looking at power up delays or sequencing.

### Temperature Coefficient

The limits stated for temperature coefficient (tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, ($V_{HIGH} - V_{LOW}$), and divide by the temperature extremes of measurement ($T_{HIGH} - T_{LOW}$). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by $10^6$ to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

### Output Voltage Adjustment

The output voltage can be adjusted up or down by 2.5% by placing a potentiometer from Vout to ground, and connecting the wiper to the TRIM pin. The TRIM input is high impedance, so no series resistance is needed. The resistor in the potentiometer should be a low tempco (<50ppm/°C) and the resulting voltage divider should have very low tempco <5ppm/°C. A digital potentiometer such as the ISL95810 provides a low tempco resistance and excellent resistor and tempco matching for trim applications.

## Typical Application Circuits

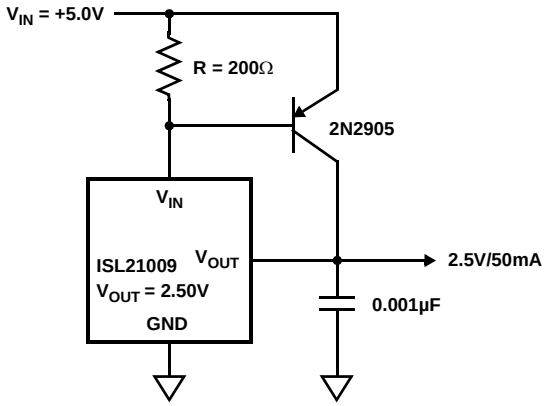



FIGURE 31. PRECISION 2.5V 50mA REFERENCE

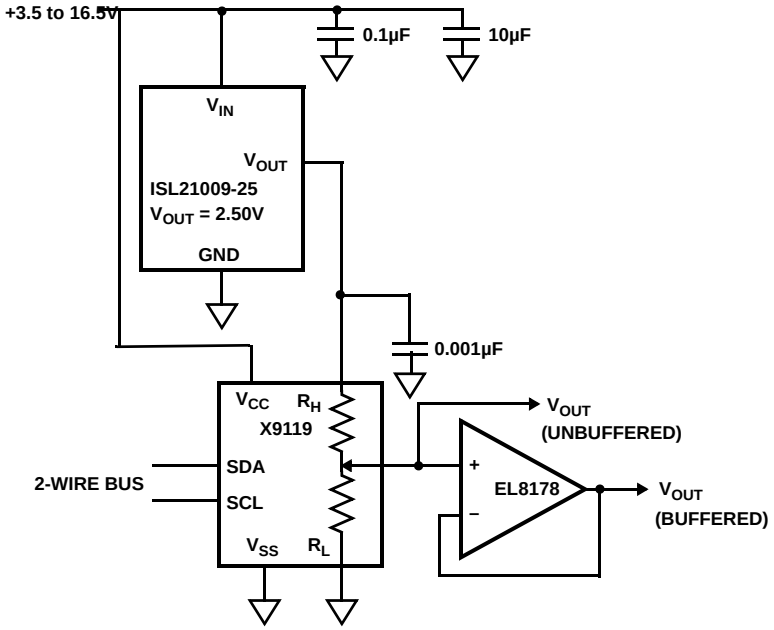



FIGURE 32. 2.5V FULL SCALE LOW-DRIFT, LOW NOISE, 10-BIT ADJUSTABLE VOLTAGE SOURCE

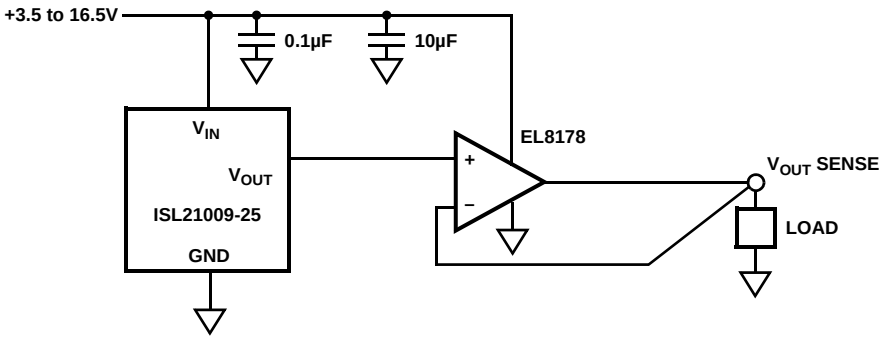



FIGURE 33. KELVIN SENSED LOAD

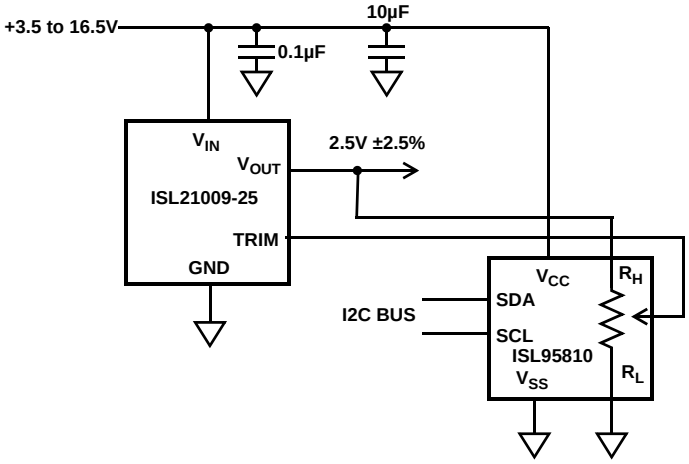
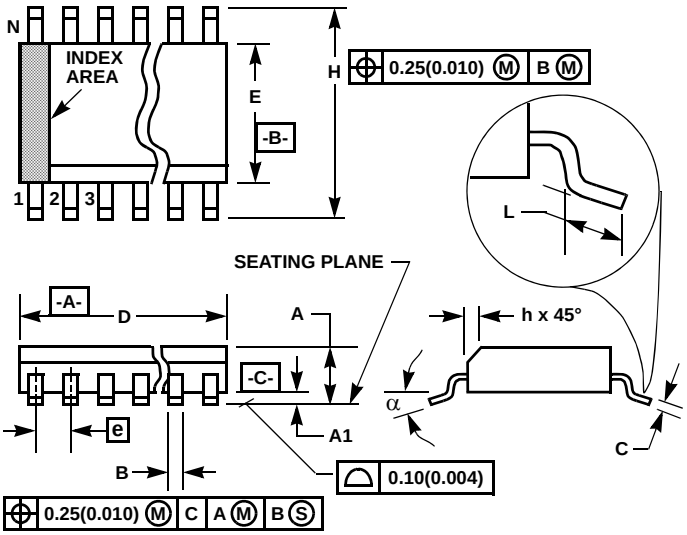



FIGURE 34. OUTPUT ADJUSTMENT USING THE TRIM PIN

## Small Outline Plastic Packages (SOIC)




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M8.15 (JEDEC MS-012-AA ISSUE C)**
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| a | 0° | 8° | 0° | 8° | - |

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