

# DATA SHEET

**74LV139**

**Dual 2-to-4 line decoder/demultiplexer**

Product specification  
Supersedes data of 1997 Feb 12  
IC24 Data Handbook

1998 Apr 28

# Dual 2-to-4 line decoder/demultiplexer

# 74LV139

## FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7\text{ V}$  and  $V_{CC} = 3.6\text{ V}$
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- $I_{CC}$  category: MSI

## APPLICATIONS

- Memory decoding or data-routing
- Code conversion

## DESCRIPTION

The 74LV139 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT139.

The 74LV139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs ( $nA_0$  and  $nA_1$ ) and providing four mutually exclusive active LOW outputs ( $n\bar{Y}_0$  to  $n\bar{Y}_3$ ). Each decoder has an active LOW enable input ( $n\bar{E}$ ).

When  $n\bar{E}$  is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay $nA_n$ to $n\bar{Y}_n$ , $n\bar{E}$ to $n\bar{Y}_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	11 10	ns
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per multiplexer	$V_{CC} = 3.3\text{ V}$ $V_I = \text{GND to } V_{CC}^1$	42	pF

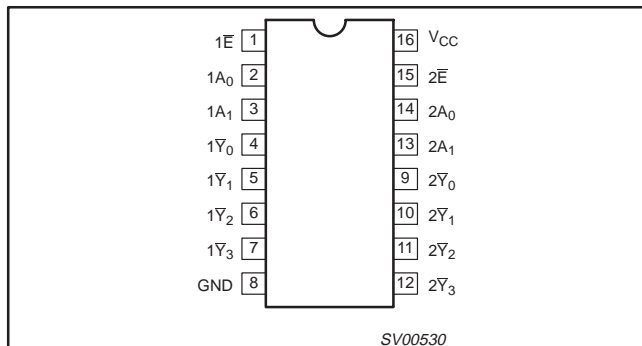
### NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	-40°C to +125°C	74LV139 N	74LV139 N	SOT38-4
16-Pin Plastic SO	-40°C to +125°C	74LV139 D	74LV139 D	SOT109-1
16-Pin Plastic SSOP Type II	-40°C to +125°C	74LV139 DB	74LV139 DB	SOT338-1
16-Pin Plastic TSSOP Type I	-40°C to +125°C	74LV139 PW	74LV139PW DH	SOT403-1

## PIN CONFIGURATION



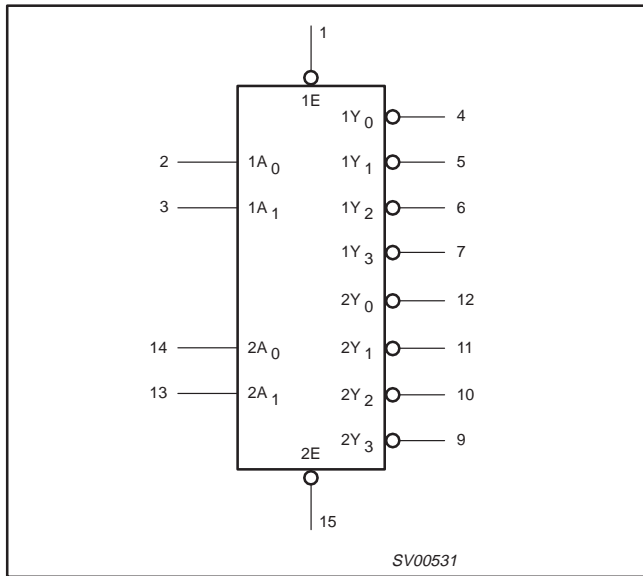
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	1E, 2E	Enable inputs (active LOW)
2, 3	1A <sub>0</sub> , 1A <sub>1</sub>	Address inputs
4, 5, 6, 7	1Y <sub>0</sub> to 1Y <sub>3</sub>	Outputs (active LOW)
8	GND	Ground (0 V)
12, 11, 10, 9	2Y <sub>0</sub> to 2Y <sub>3</sub>	Outputs (active LOW)
14, 13	2A <sub>0</sub> , 2A <sub>1</sub>	Address inputs
16	V <sub>CC</sub>	Positive supply voltage

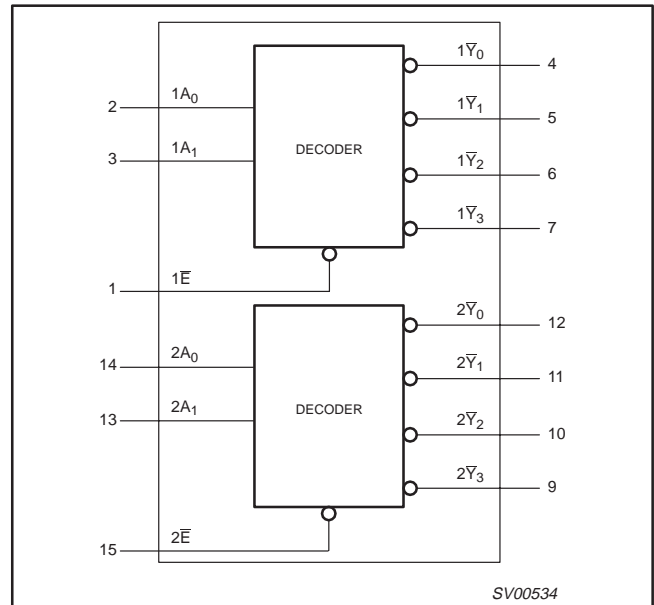
# Dual 2-to-4 line decoder/demultiplexer

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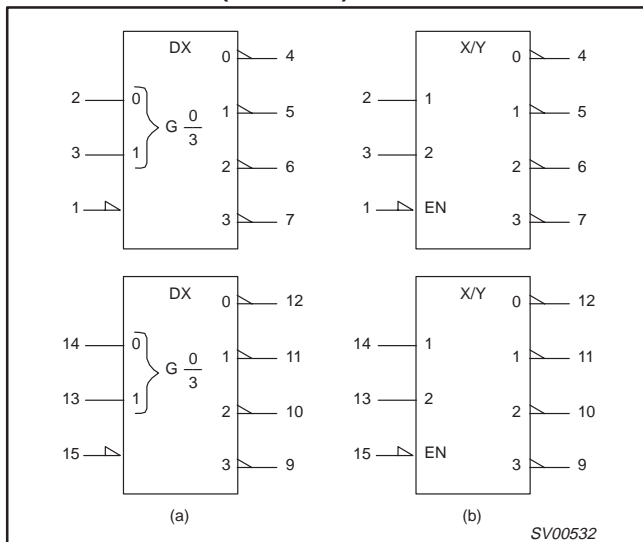
## LOGIC DIAGRAM



## FUNCTIONAL DIAGRAM



## LOGIC SYMBOL (IEEE/IEC)



## FUNCTION TABLE

INPUTS			OUTPUTS			
nE	nA <sub>0</sub>	nA <sub>1</sub>	nY <sub>0</sub>	nY <sub>1</sub>	nY <sub>2</sub>	nY <sub>3</sub>
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

### NOTES:

- H = HIGH voltage level
- L = LOW voltage level
- X = don't care

## Dual 2-to-4 line decoder/demultiplexer

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note 1	1.0	3.3	5.5	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

## NOTE:

1. The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 5.5V$ .

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with – standard outputs		50	mA
$T_{stg}$	Storage temperature range		–65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Dual 2-to-4 line decoder/demultiplexer

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2 V	0.9			0.9		V
		V <sub>CC</sub> = 2.0 V	1.4			1.4		
		V <sub>CC</sub> = 2.7 to 3.6 V	2.0			2.0		
		V <sub>CC</sub> = 4.5 to 5.5 V	0.7 * V <sub>CC</sub>			0.7 * V <sub>CC</sub>		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2 V			0.3		0.3	V
		V <sub>CC</sub> = 2.0 V			0.6		0.6	
		V <sub>CC</sub> = 2.7 to 3.6 V			0.8		0.8	
		V <sub>CC</sub> = 4.5 to 5.5			0.3 * V <sub>CC</sub>		0.3 * V <sub>CC</sub>	
V <sub>OH</sub>	HIGH level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA		1.2				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	1.8	2.0		1.8		
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	2.5	2.7		2.5		
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	2.8	3.0		2.8		
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	4.3	4.5		4.3		
V <sub>OH</sub>	HIGH level output voltage; STANDARD outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 6mA	2.40	2.82		2.20		V
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 12mA	3.60	4.20		3.50		
V <sub>OL</sub>	LOW level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
V <sub>OL</sub>	LOW level output voltage; STANDARD outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.25	0.40		0.50	V
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.35	0.55		0.65	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND			1.0		1.0	µA
I <sub>CC</sub>	Quiescent supply current; MSI	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			20.0		160	µA
ΔI <sub>CC</sub>	Additional quiescent supply current per input	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V			500		850	µA

**NOTE:**1. All typical values are measured at T<sub>amb</sub> = 25°C.

# Dual 2-to-4 line decoder/demultiplexer

# 74LV139

## AC CHARACTERISTICS

GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 1\text{K}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay $nA_n$ to $\bar{Y}_n$	Figures 1, 2	$V_{CC}(V)$						ns
			1.2		70				
			2.0		24	31		39	
			2.7		18	23		29	
			3.0 to 3.6		13 <sup>2</sup>	18		23	
4.5 to 5.5			15		19				
$t_{PHL}/t_{PLH}$	Propagation delay $n\bar{E}$ to $\bar{Y}_n$	Figures 1, 2	$V_{CC}(V)$						ns
			1.2		60				
			2.0		20	27		34	
			2.7		15	20		25	
			3.0 to 3.6		11 <sup>2</sup>	16		20	
4.5 to 5.5			13		16				

### NOTES:

1. Unless otherwise stated, all typical values are measured at  $T_{amb} = 25^\circ\text{C}$
2. Typical values are measured at  $V_{CC} = 3.3\text{V}$ .

## AC WAVEFORMS

$V_M = 1.5\text{V}$  at  $V_{CC} \geq 2.7\text{V}$  and  $\leq 3.6\text{V}$ ;

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{V}$  and  $\geq 4.5\text{V}$ .

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

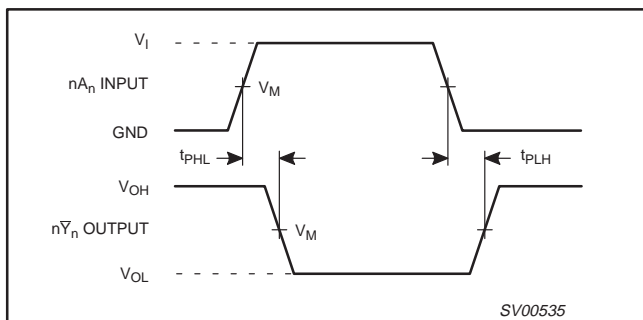


Figure 1. Address input ( $nA_n$ ) to output ( $n\bar{Y}_n$ ) propagation delays.

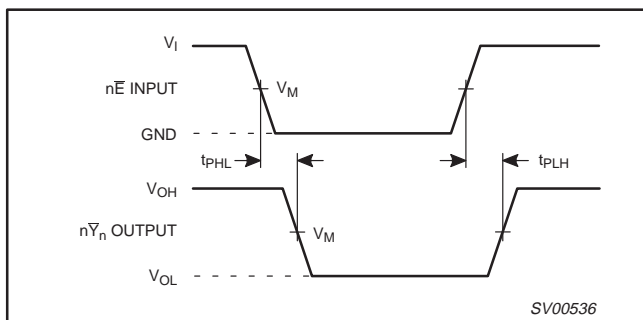


Figure 2. Enable input ( $n\bar{E}$ ) to output ( $n\bar{Y}_n$ ) propagation delays.

## TEST CIRCUIT

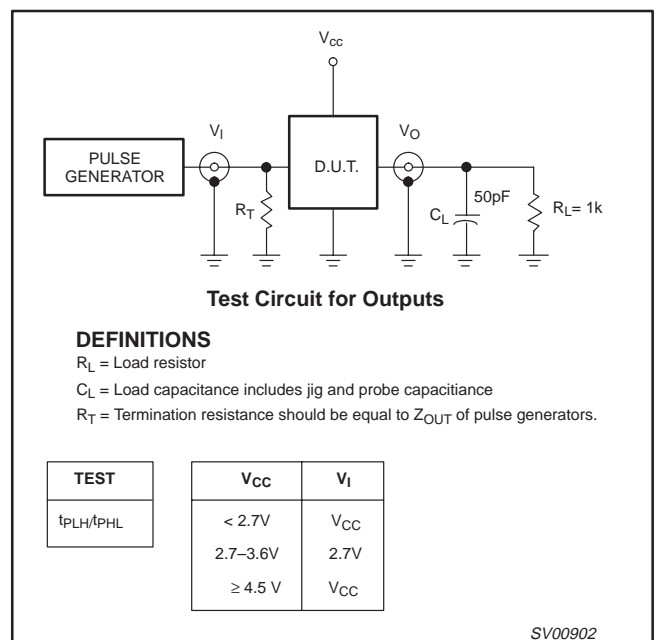


Figure 3. Load circuitry for switching times.

# Dual 2-to-4 line decoder/demultiplexer

## 74LV139

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

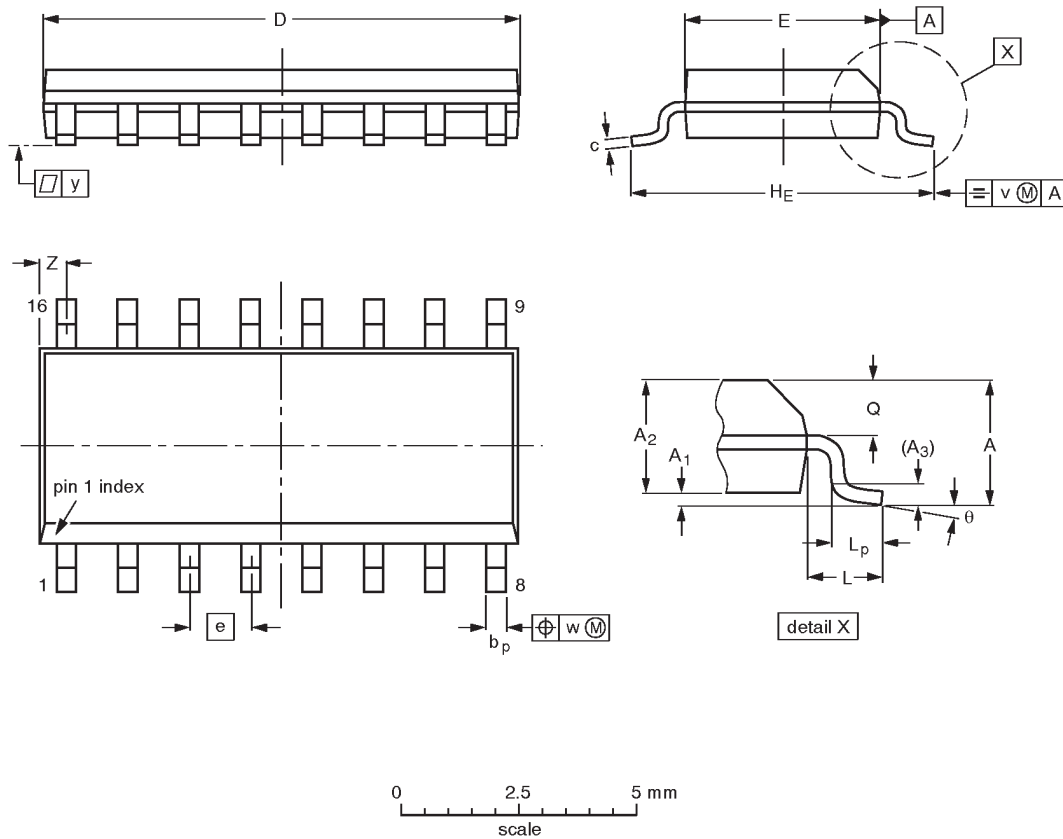
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

# Dual 2-to-4 line decoder/demultiplexer

# 74LV139

**SO16: plastic small outline package; 16 leads; body width 3.9 mm**

**SOT109-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

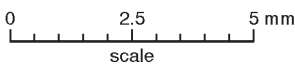
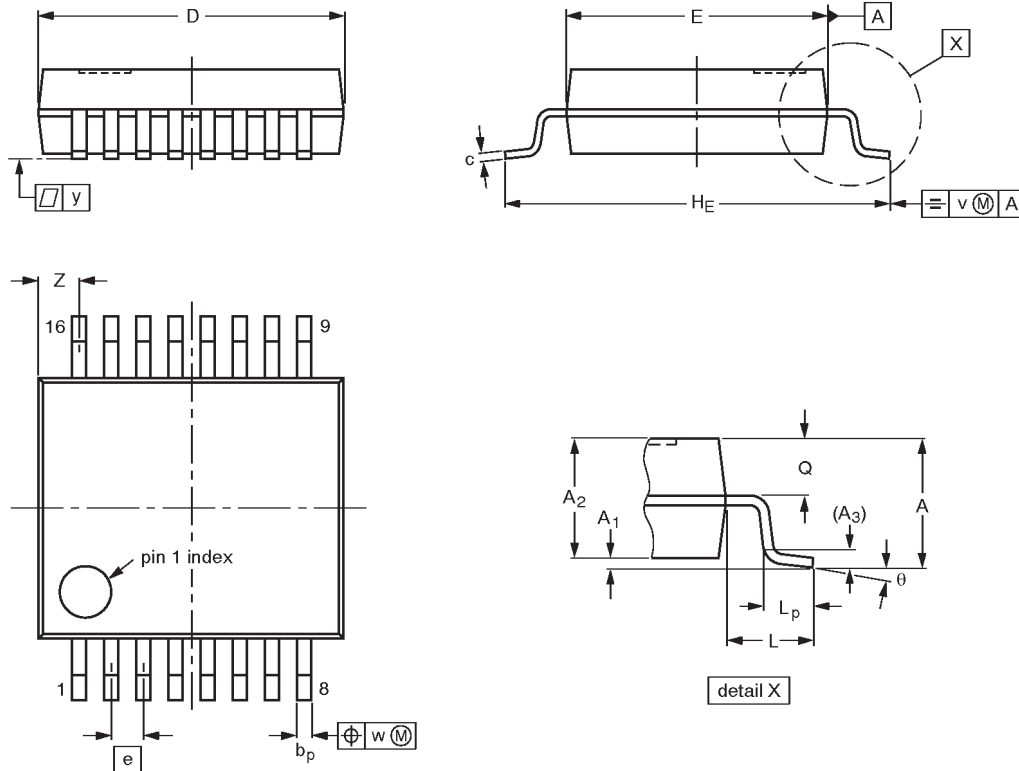


# Dual 2-to-4 line decoder/demultiplexer

# 74LV139

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm**

**SOT338-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

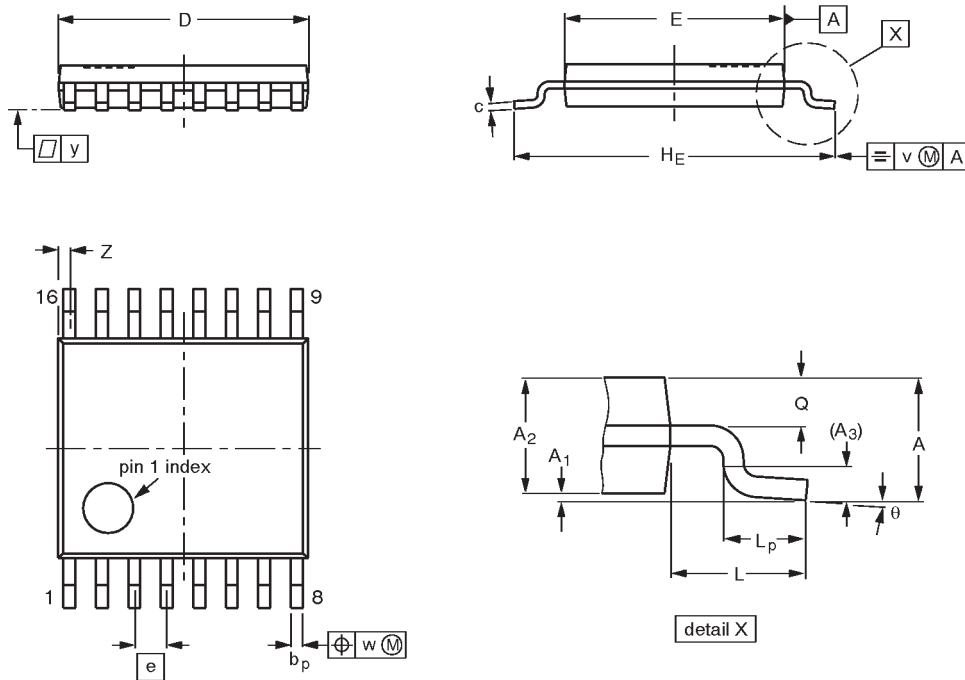
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14- 95-02-04

# Dual 2-to-4 line decoder/demultiplexer

# 74LV139

**TSSOP16:** plastic thin shrink small outline package; 16 leads; body width 4.4 mm

**SOT403-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

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Dual 2-to-4 line decoder/demultiplexer

74LV139

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**NOTES**

## Dual 2-to-4 line decoder/demultiplexer

74LV139

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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