June 22, 2010

Industrial HMI: Driving Displays Basics and Roadmap

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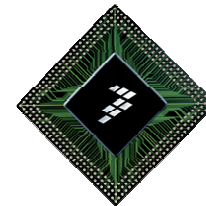
John Weil

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Agenda

► Trends and Trade-Offs

► Hardware Interfacing

► Content Generation

► Freescale Solutions

► Conclusion

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▶ General Observations

- iPhone and iPad have ushered in a new era of UI expectation
- Public welcomes and expects digital content everywhere
- Cost, low-power and longer battery life are key enablers

▶ Trade-Off – Creation vs. Delivery Cost

- Reducing content creation cost
    - Leverage development community skill set
    - Leverage common tool sets
    - Leverage existing content
- Reducing content delivery cost
    - Implies increasing content creation and management costs
    - Efficiencies can be gained with specialized tool sets
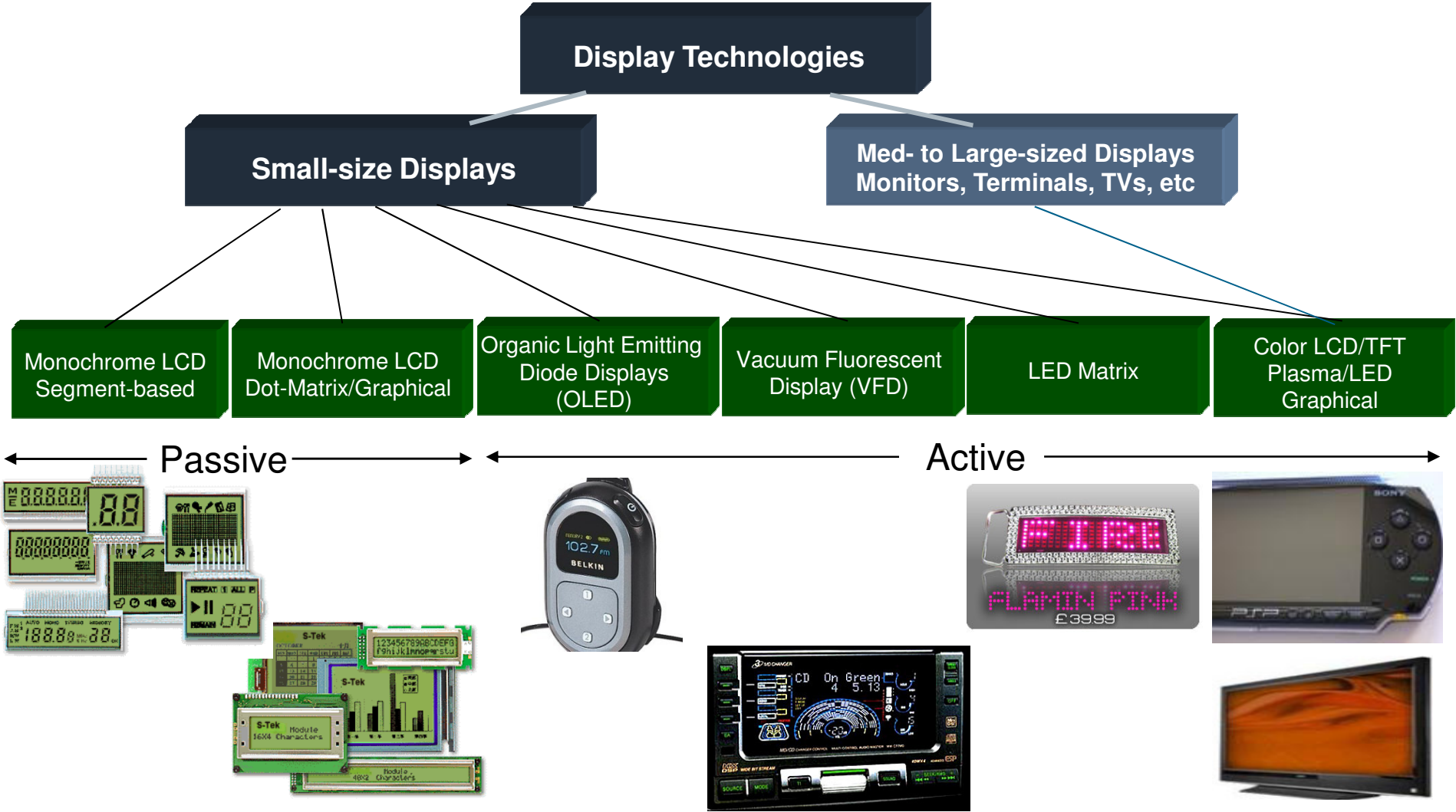   - UI expectations works against cost reductions

▶ Change on the Horizon?

- There is a push for more efficient embedded solutions, e.g. MID/tablet/netbook
- Embedded UIs are becoming more complex but still have high cost pressure
- Controlling delivery costs enables more public deployment and ROI

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Display Solutions Tiers

► Segmented Display (288 Segments & Below)

- Low-end integrated MCU solutions
- 288 segments is the cost cross-over point to pixel based displays

► Smart Pixel Display (VGA & Below)

- Low/mid-range general MCU/MPU solutions
- Smart displays have an integrated frame buffer and MCU to refresh display
- Memory mapped communication is used to update pixel changes
- Serial/Parallel bus communication accommodates generic MPU/MCU solutions
- Amount of pixel update is limited by communication bandwidth

► Dumb Pixel Display (VGA & Above)

- Low/mid/high-end integrated display controller MCU/MPU solutions
- Dumb displays have no buffer and are refreshed by the MCU/MPU
- Display interface contains all data to update entire display at a refresh rate
- Clocked interface happens over RGB, LVDS, HDMI and Display Port
- Mid-range integrates multi-plane blend, graphics and video acceleration
- High-end solutions interface to high-end graphics processors

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Display Spectrum

Display Technologies

Small-size Displays

Med- to Large-sized Displays Monitors, Terminals, TVs, etc

| Monochrome LCD Segment-based | Monochrome LCD Dot-Matrix/Graphical | Organic Light Emitting Diode Displays (OLED) | Vacuum Fluorescent Display (VFD) | LED Matrix | Color LCD/TFT Plasma/LED Graphical |

Passive — Active

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Display Spectrum

Monochrome LCD Segment-based	Monochrome LCD Dot-Matrix/Graphical	Color LCD Graphical	Vacuum Fluorescent Display (VFD)	Organic Light Emitting Diode Displays (OLED) – SM and P	LED Matrix
Strengths: ►Inexpensive ►Easily customizable ►Multiple suppliers of glass and controllers ►Power consumption is relatively low for comparable sizes	►Standard and customizable displays ►Graphics vs fixed characters ►Price approaching seg/char-based	►Color graphical display ►Range up to full graphics (VGA)	►Very bright, color display ►High contrast ►Very wide viewing angle ►Functionality in harsh environments (very cold climates)	►Brightness and color approaching VFD ►No backlight req'd ►Seg/char and graphical displays available ►Manufacturing options (i.e. flexible display for PLEDs) and process ►Lower power consumption	Very bright display with multiple color options Could be used for larger displays
Weaknesses: ►Monochrome ►Fixed displays ►Requires very high segment count for graphics ►Viewing angle	►Graphics can be limited due to controller code and/or dot count ►Code req'd is more complex than seg/char-based displays ►Viewing angle	►Power consumption ►Cost ►Controller reqs ►Backlight needed ►Limited number of suppliers with affordable displays ►Viewing angle	►Power consumption ►Fixed displays ►Manufacturing process	►Life span ►Patented technology by Kodak (SM) ►Patented tech by CDT (polymer) ►Water resistance (lack thereof)	Power consumption Viability for smaller displays
Opportunities: "will always be around"	Demand is increasing for graphical display	►Demand increasing for graphical displays	►Still used in Industrial applications in outdoor/cold climates	►If longer life can be realized, offers many benefits over LCD	
Threats: ►Other displays coming down to seg/char-based display prices offer key advantages	Consumer demand for color displays		►Being taken over by OLED in many applications		

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Common Display Resolutions

Hardware Interfacing

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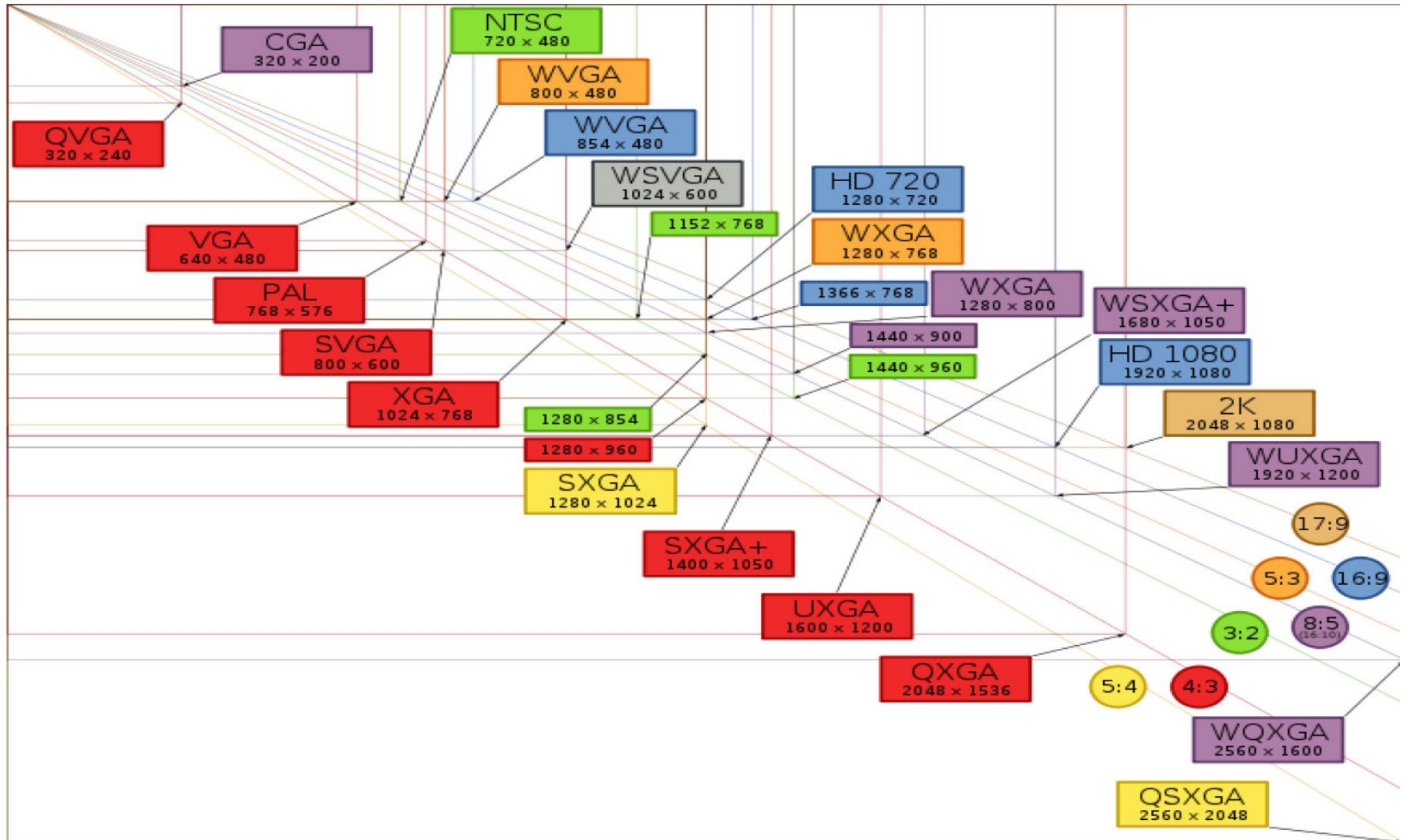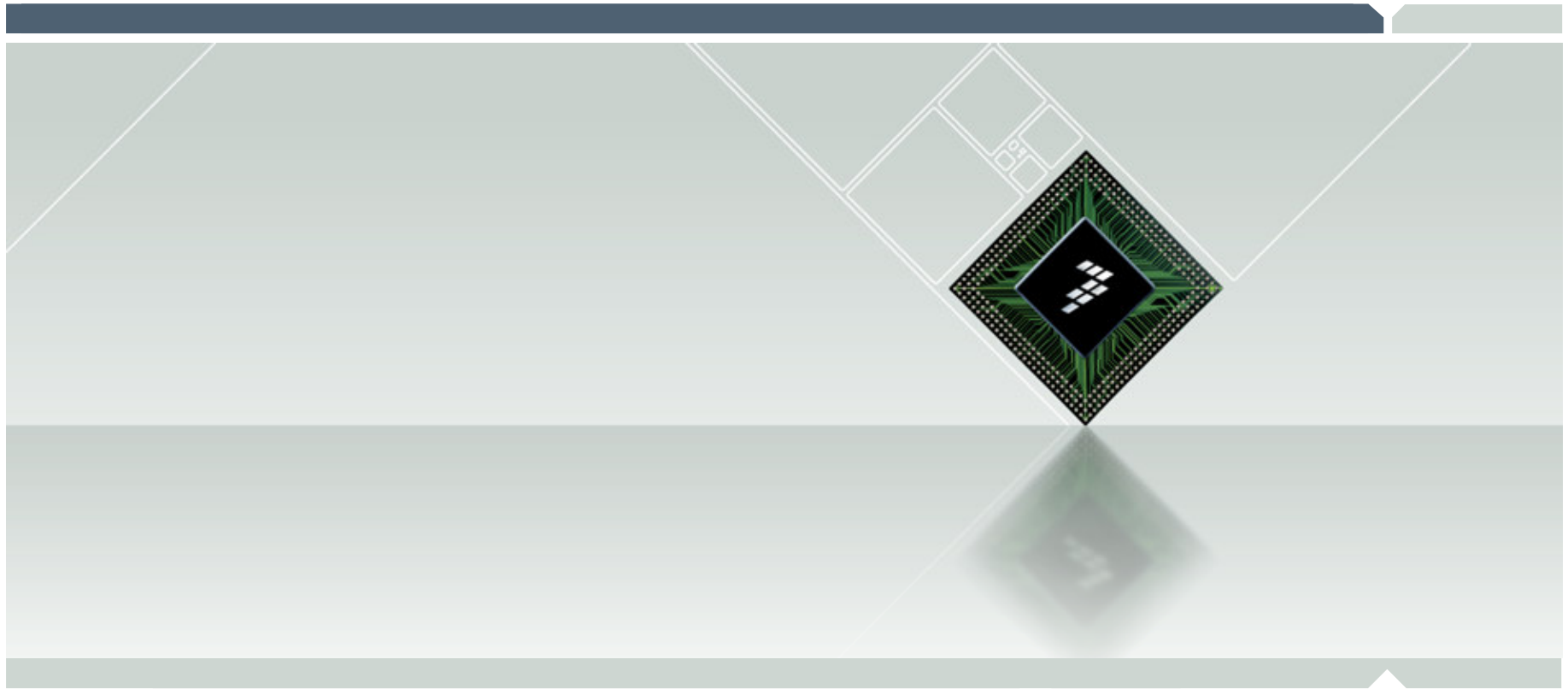
Segment LCD Interface Options

Integrated LCD driver

-LCD peripheral generates the FP and BP signals necessary to drive the display

40 FP (seg)

4 BP (com)

GPIO

LED
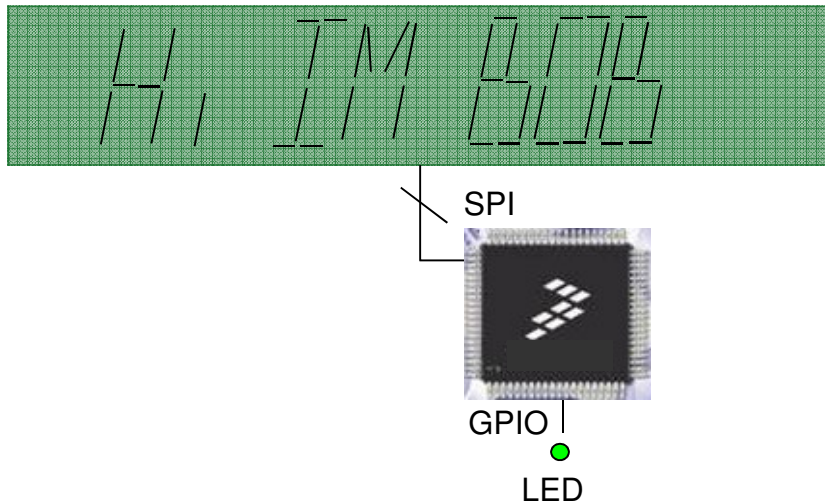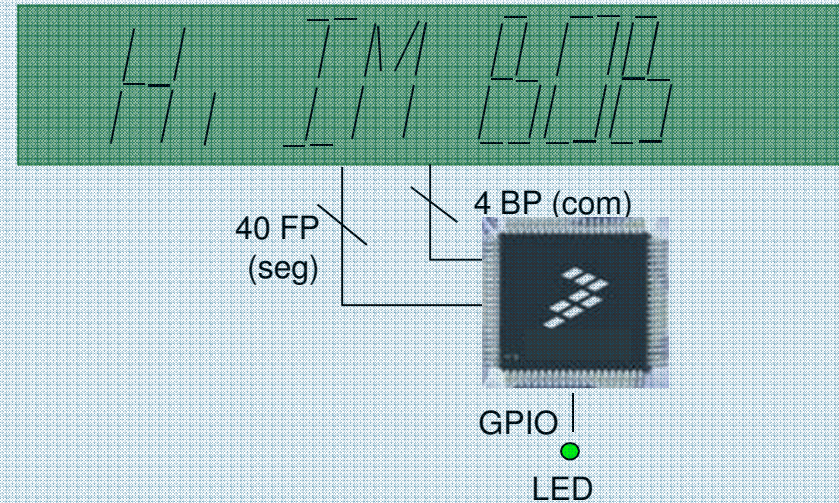
LCD Glass module with SPI interface

 - MCU generates the communication protocol necessary to interface to a smart LCD display

SPI

GPIO

LED

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LCD Interface Options

Smart Displays

| MPU Unified Memory | MCU/MPU | SPI / Mem Mapped Parallel | LCD Frame Buffer |

Dumb Displays

| MPU Unified Memory | MCU/MPU | RGB | VGA HDMI DP | LCD |

| MPU Unified Memory | MCU/MPU | RGB | LVDS | Long Run Cable | LVDS | LCD |

| MPU Unified Memory | MCU/MPU | ITU 656 | CVBS | Long Run Cable | CVBS | LCD |

| MPU Memory | MPU | PCI | External GPU | LCD |
| DRAM |

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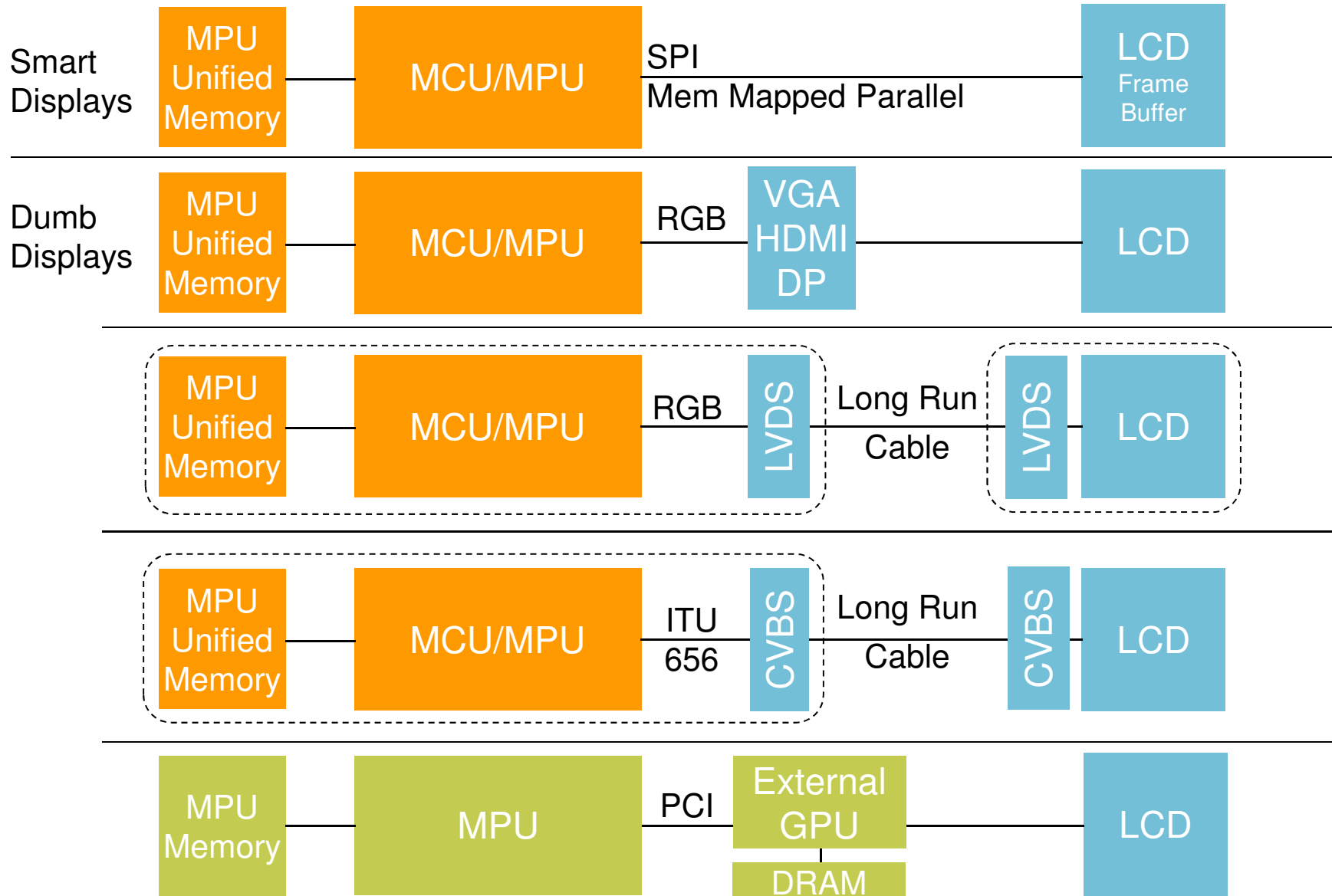
Memory Mapped vs. RGB Interface Trade-Off

24-bit	Efficiency	QVGA	VGA	WQVGA	SVGA	XGA	720p	WXGA	1080p
Horizontal		320	640	800	800	1024	1280	1366	1920
Vertical		240	480	480	600	768	720	768	1080
Pixels (MPix)		0.08	0.31	0.38	0.48	0.79	0.92	1.05	2.07
Buffer (MB)		0.23	0.92	1.15	1.44	2.36	2.76	3.15	6.22
Bus Width		40 MHz		(1-bit interface = SPI)					
1-bit	90%	19.53	4.88	3.91	3.13	1.91	1.63	1.43	0.72
8-bit	70%	121.53	30.38	24.31	19.44	11.87	10.13	8.90	4.50
16-bit	70%	243.06	60.76	48.61	38.89	23.74	20.25	17.79	9.00
RGB Width		66 MHz							
8-bit	100%	173.61	43.40	34.72	27.78	16.95	14.47	12.71	6.43
24-bit	100%	520.83	130.21	104.17	83.33	50.86	43.40	38.13	19.29

* Example frequencies and interface efficiencies are not necessarily reflective of all market solutions

► Interface efficiency is a measure of addressing overhead on an interface
► At a given bit width an RGB is more efficient in number of lines, however memory mapped is shared
► Memory mapped will have a higher frame rate for partial screen updates in proportion to the subset
► Motion graphics needs an update rate of at least 30fps to appear smooth
► RGB interface needs a refresh rate of at least 60fps (based on CRTs, LCDs can take less)
► RGB interfaces clock at higher than frequency due to front/back porch and line blanking intervals

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RGB Interface Frequency Overhead

Interface Rate

Vertical Blanking
Front Porch (Y_front)

Horizontal Blanking Front Porch (X_front)

Higher effective pixel rate
over refreshed resolution rate
due to horizontal blanking

Horizontal Blanking Back Porch (X_back)

Pixel Processing Rate

Vertical Blanking
Back Porch (Y_back)
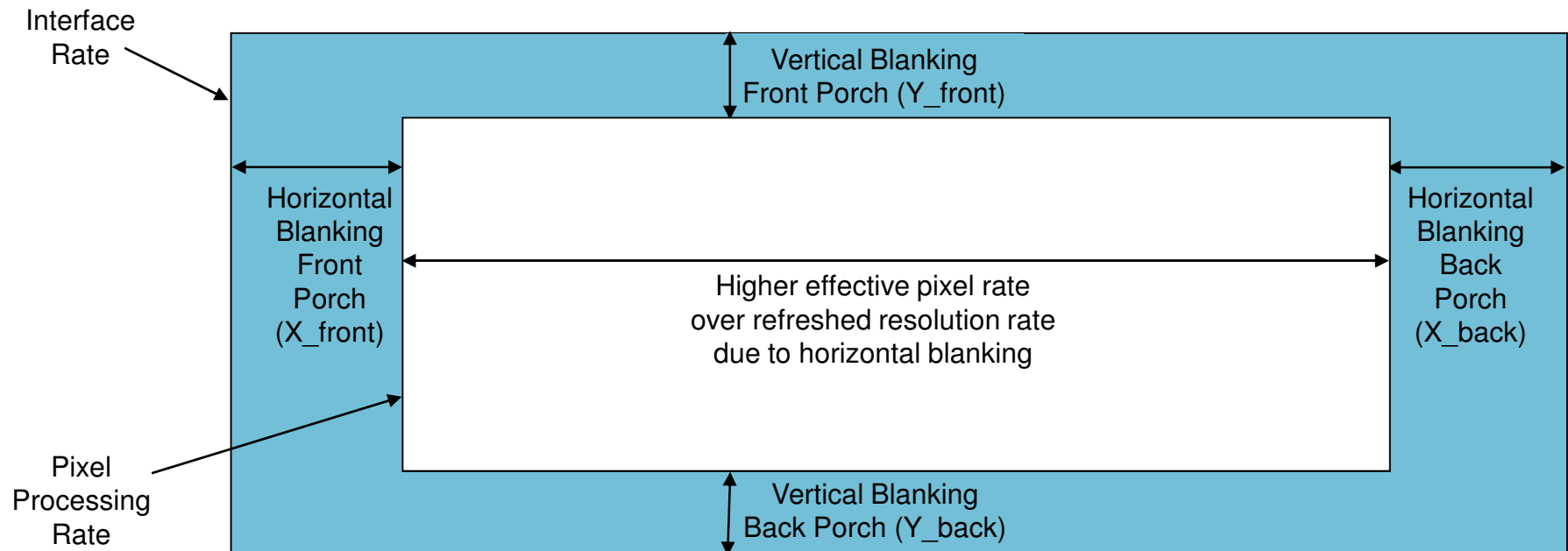
- ▶ **LCD technology follows CRT interface standards**
  - Front/Back porch horizontal and veridical blanking are an artifact of CRT signaling
  - LCD specs maintain 60fps refresh, crystals can be refreshed slower
- ▶ **Pixel rate not to same as interface rate**
  - Blanking intervals results in inflated horizontal/vertical interface pixel rates
  - Pixel processing can runs slower than interface, but need to buffer pixels (buffer up pixel during blue regions):
    - Pixel_processing_rate = X * Y * refresh_rate
    - Buffer_size >= X * ((PIX_CLK_freq – Pixel_processing_rate) / PIX_CLK_freq), cover higher interface pixel rate
    - Buffer_size <= Pixel_processing_rate * ((X_front + X_back) / PIX_CLK_freq), max buffering on horizontal blanking

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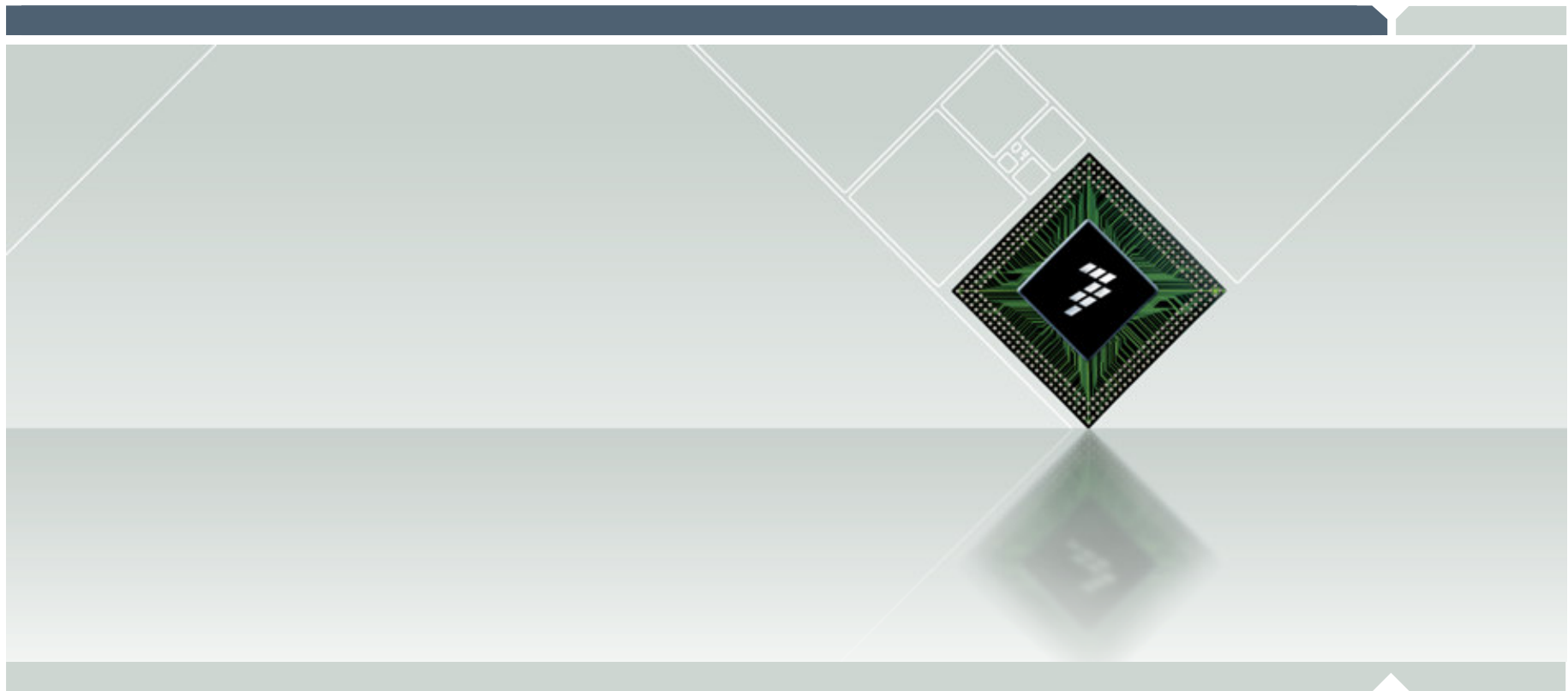
Digital Content

Common Standards

Important Video Codec Formats

Video codecs provide the mechanism to reduce storage and bandwidth requirements to deliver changing display content. Codecs are judged on the basis of compression, quality and total cost to deploy.

► MPEG2
  • DVD playback

► H.263
  • Video conference, internet content

► H.264 / MPEG4 AVC
  • DivX, QuickTime, Flash FLV, IPTV, YouTube

► Sorenson, On2 VP
  • Flash FLV, YouTube

► WMV, VC-1
  • PC, internet content

► Real Video, RMVB

► Theora
  • Open source, royalty free

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Khronos – Driving Open Standards

The Khronos Group is an industry consortium creating open standards for the authoring and acceleration of parallel computing, graphics and dynamic media on a wide variety of platforms and devices.

► Website: www.khronos.org

► The consortium has a wide and involved membership

► Good industry push towards their open royalty free standards

► "Foundation-Level" API standards close to the hardware

► Heavy focus on portable platforms aside from OpenGL

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Ecosystem of APIs
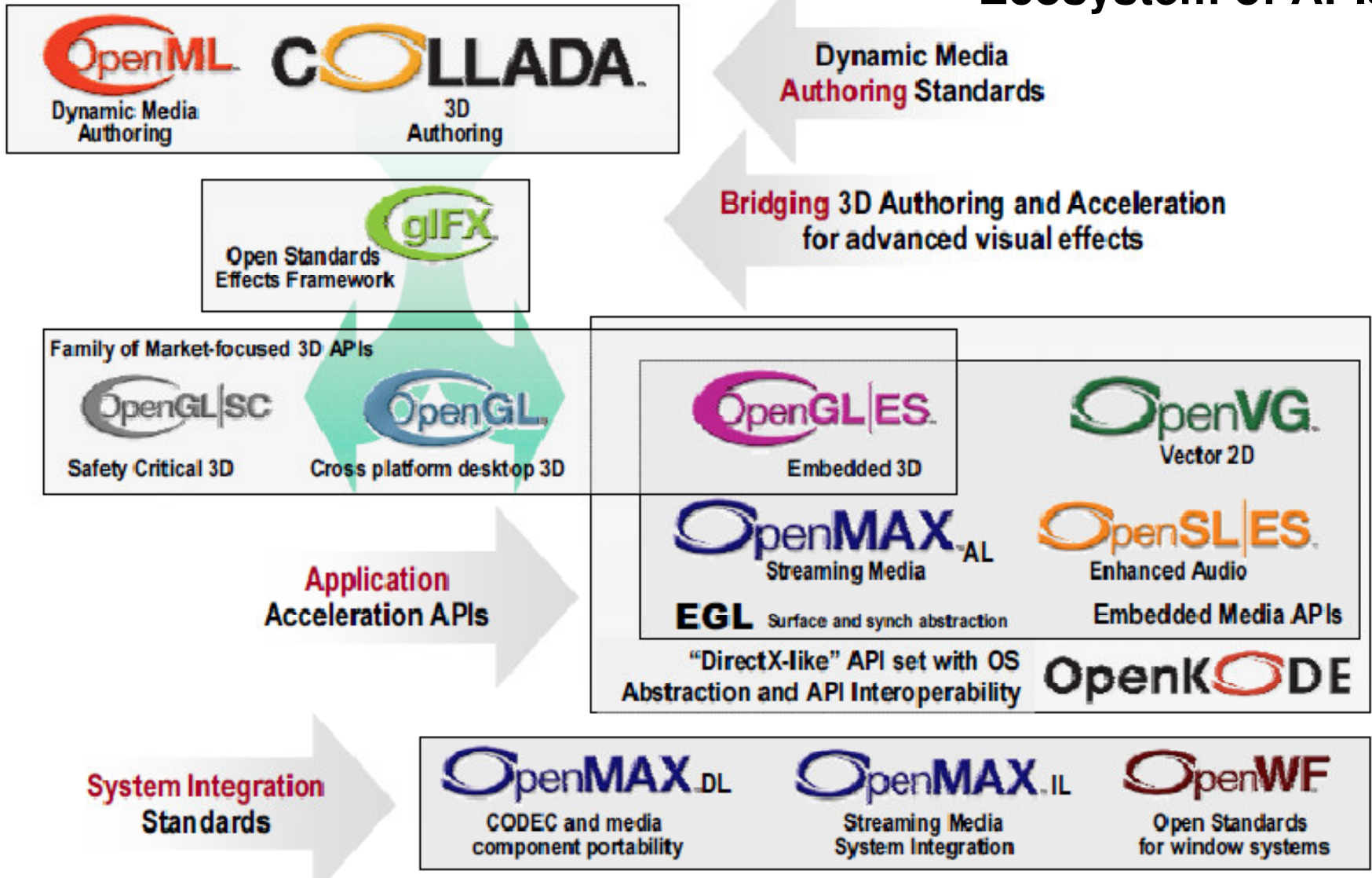
Adobe® Flash®

Adobe Flash is the most established content delivery mechanism given its wide deployment and developer community. Adobe made its first attempt to open this "defacto" standard with Adobe FlashLite 3.1 and has recently released the follow-on Adobe Flash10 standard. Both imply licenses and runtime fees and working within the bounds of an approved Adobe system house or license agreement.

► Desktop Adobe Flash
  - Adobe Flash 9 introduced ActionScript3
  - Adobe Flash 10 introduced 3D manipulation

► Embedded Flash
  - Adobe FlashLite 3.1 (based on Flash 8)
  - QNX Aviage built on FlashLite 3.1.7
  - Gnash open source flash player
  - Swfdec open source library

► FLV - Video Container
  - Supports Sorenson, On2 and H.264 codecs

► Converters
  - Content is covered off-line to support a more efficient runtime display engine.

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JAVA™ – Hardware Independence

Java offers a hardware independent platform for delivering graphics on an embedded system.

► Java 2D API

► AWT (Abstract Windowing Toolkit) API

► Swing build widgets on top of Java 2D API

► M3G – Mobile 3D Graphics API

► JOGL – JAVA Open Graphics Library (OpenGL binding)

Apache Harmony project created a JVM with an Apache License to allow closed code work as oppose to the open GPL License.

There are many open source JVM solutions emphasizing reduced memory footprint, performance and safety critical certified aspects. These can be build from GPL or Apache code base.

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Android™ OS – Open Smartphone Platform

Android OS offers a hardware independent platform enabling an apps development community, while offering vertical customization.

► Dalvik VM is derived from the Apache Harmony code base

► Graphics: Canvas (drawing + paint) -> bitmap

► AppWidgets allows sharing Widgets between apps

► EGL Interface

► OpenGL ES API Interface

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Android OS Architecture
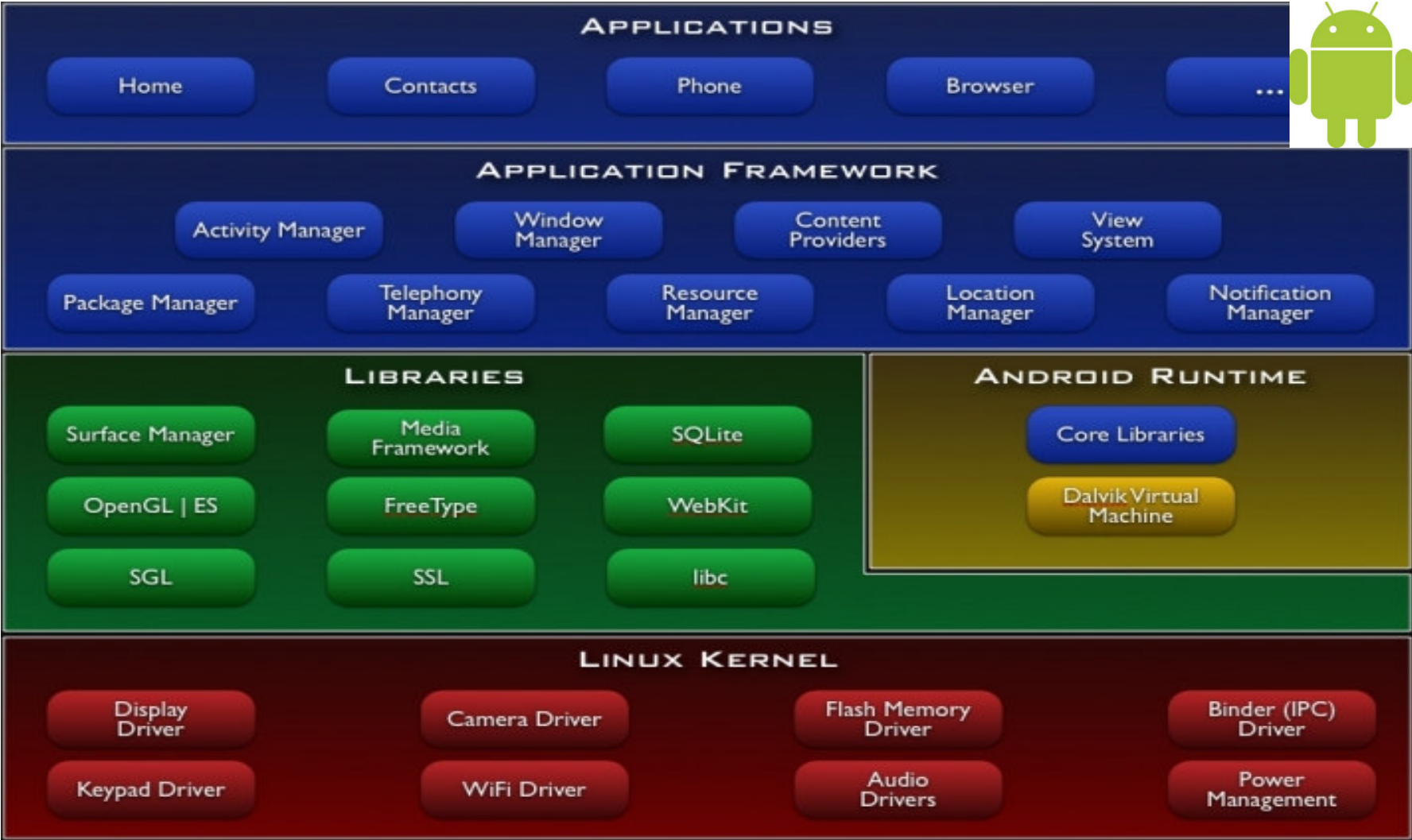
Window Managers & GUI

► Linux® Frameworks/Players

- • MPlayer
- • VLC
- • GStreamer

► Frame Buffer

- • DirectFB – lightweight

► Windowing Library

- • X-Server: X11, Tiny-X , Nano-X, … (heavy to lightweight)

► Desktops

- • GNOME, KDE, …

► GUI development tools

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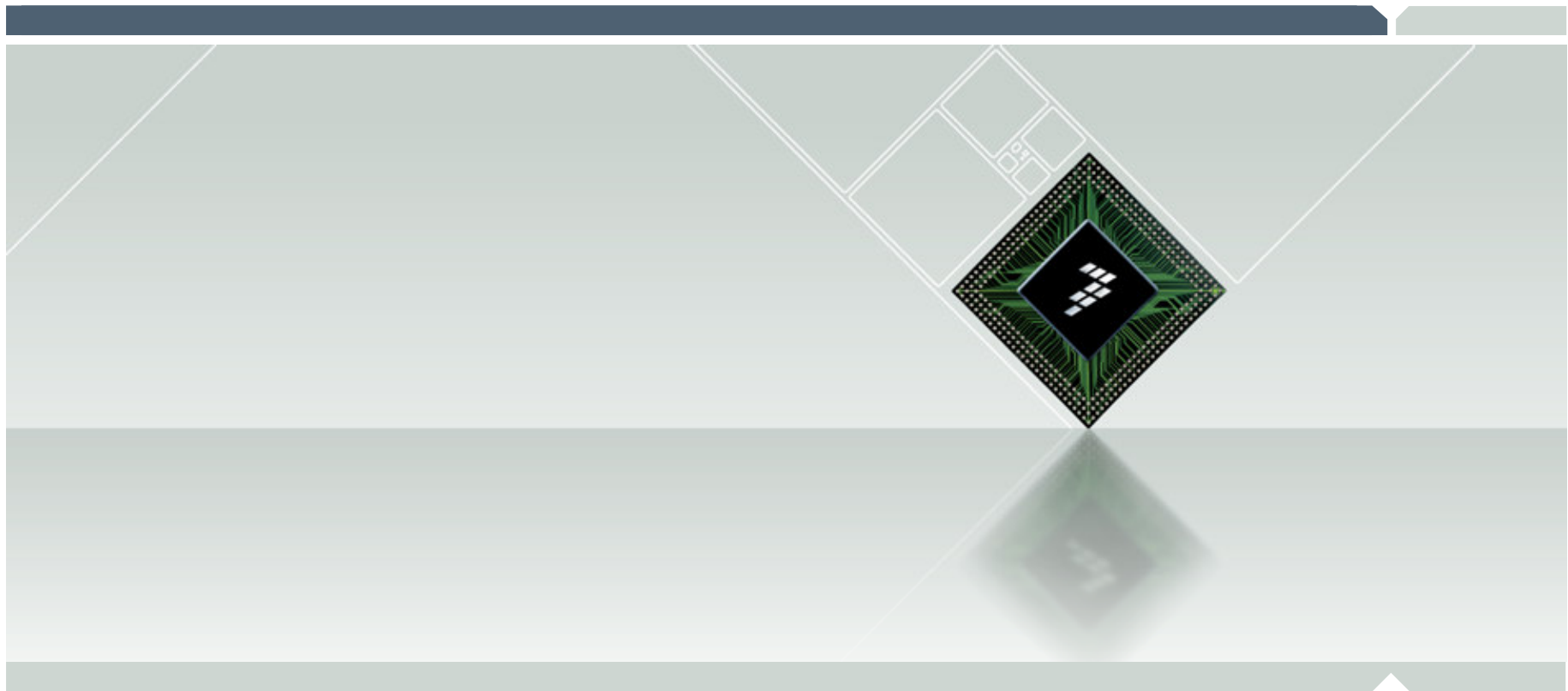
Digital Content

Custom GUI Development

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Freescale Embedded GUI (eGUI)

► GUI library enabling rapid development of cost-effective graphical interfaces

► Pre-configured objects (button, check box, radio button, gauge, icon, label, menu, slider, picture and graph) complete with CodeWarrior demo projects

► Touch screen support

► Window manager for objects

► Interface support for SPI, memory mapped parallel bus and frame buffer to RGB

► Utilities including font, image and PC graphics converters

► Complimentary source code with any Freescale device

► Support for Freescale MQX and Linux
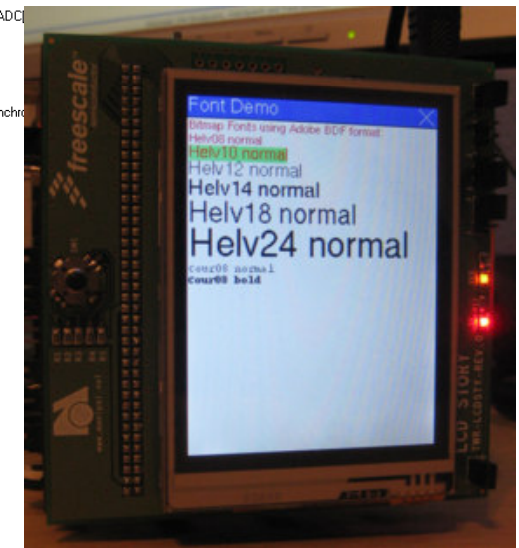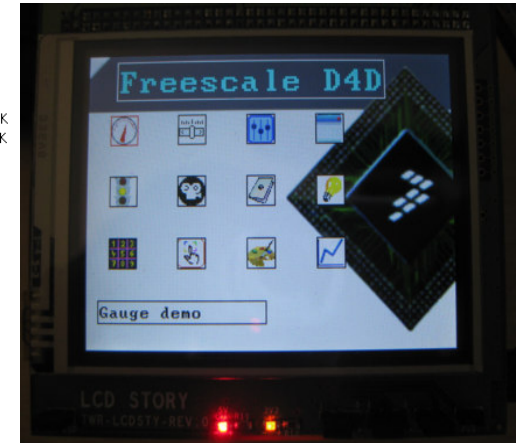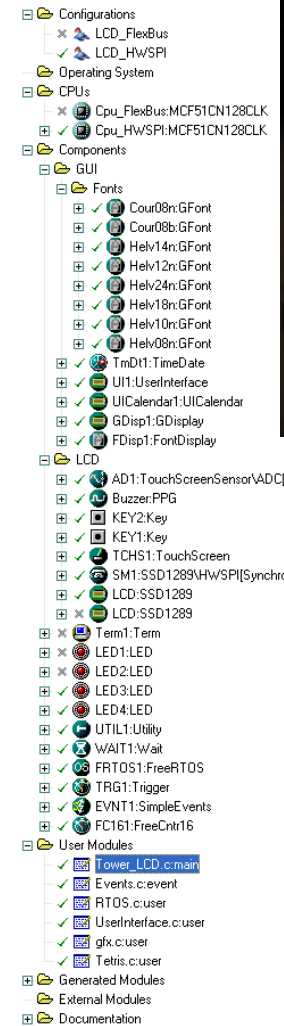
► User application – layer of user application code

► Application programmable interface - interface layer between user application and FGUI

► eGUI high level - layer that manage all screens and objects (redraws, input keys, touch screen events etc.)

► LCD low level – manage communication with LCD and provides some basic function (Draw line, bitmap, circle etc.)

SW	User application
SW API	User interface - API (D4D API)
SW D4D	LCD High level driver
	LCD Low level driver
HW	MCU/MPU
	LCD module

24

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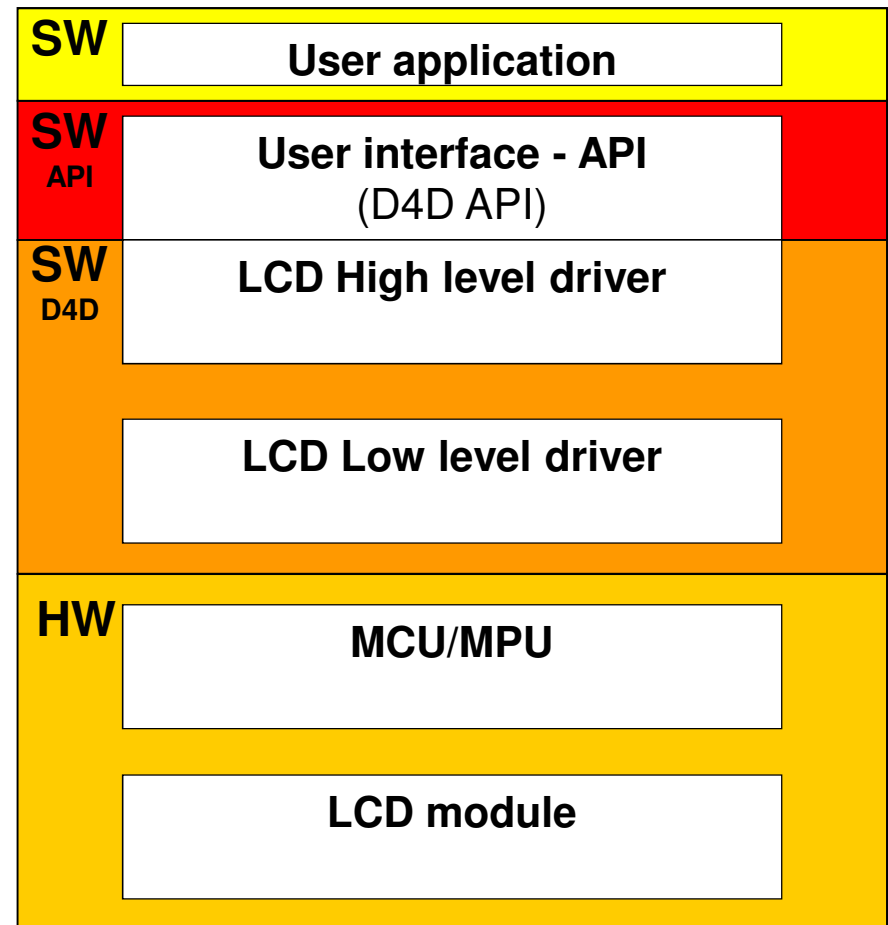
PEG Value Proposition

C/PEG™

- ► Designed for:
  - Small LCDs
  - Low color-depth
- ► Very small footprint
- ► Single window display
- ► Multi-language capable
- ► Written in ANSI C

PEG +™

- ► Overlapping windows
- ► Alpha-blended images
- ► Decorated windows
- ► Run-time image decoders
- ► Run-time language resources
- ► Written in C++

PEG Pro™

- ► Screen transitions
- ► Multiple alpha-blended windows
- ► True anti-aliased line & font drawing
- ► Dynamic themes
- ► Written in C++

The smallest footprint and most efficient code base available

90 KB	175 KB	250 KB

PEG (Portable Embedded GUI) is a suite of products for rapid GUI development for embedded systems.

PEG offers an effective method to scale GUIs from high-end MPU down to low-end MCU product families.

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FMSoft provides a mature GUI support system has been shown run smoothly on real-time embedded systems

► The new MiniGUI 3.0 includes many more features such as double buffering of main window, Look and Feel Renderer, Irregular Windows, etc.

► For a video demo of MiniGUI click here

► For more information visit: http://www.minigui.com

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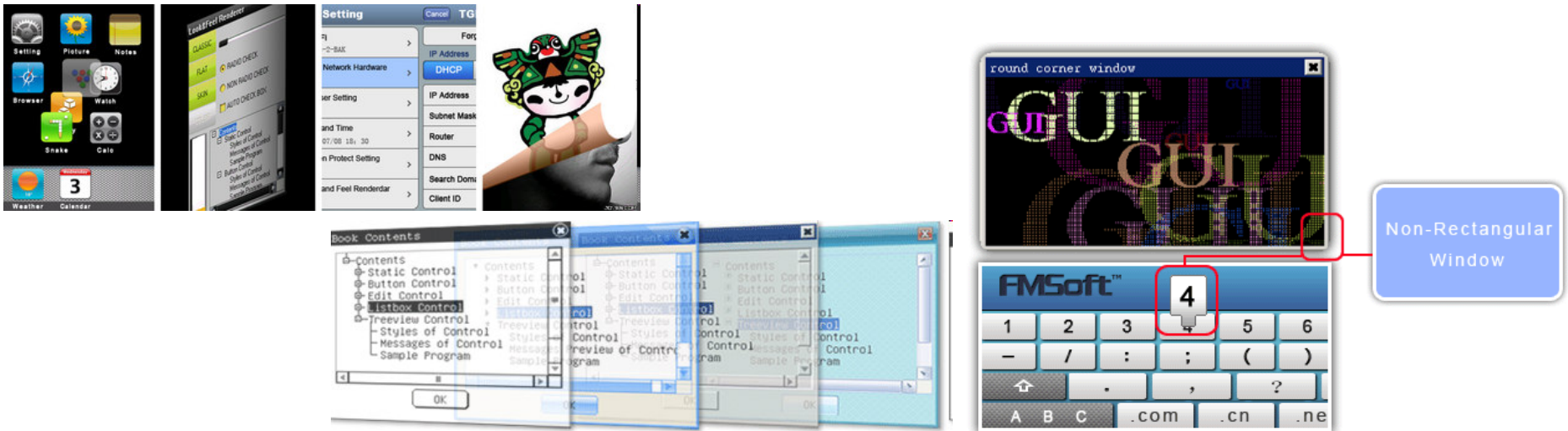
Segger GUI Library

www.segger.com

► MCF5227x & MCF532x devices are supported with
- emWin (GUI
- embOS (RTOS)
- emFile (USB
- emUSB

► emWin: An efficient, processor- and LCD controller-independent graphical user interface (GUI) for any application that operates with a graphical LCD
- Any display, any CPU, any application
- Easy switch from b/w to grey scale or color
- Small footprint
- Extremely flexible for small graphics applications to high end graphics
- Simulation environment included
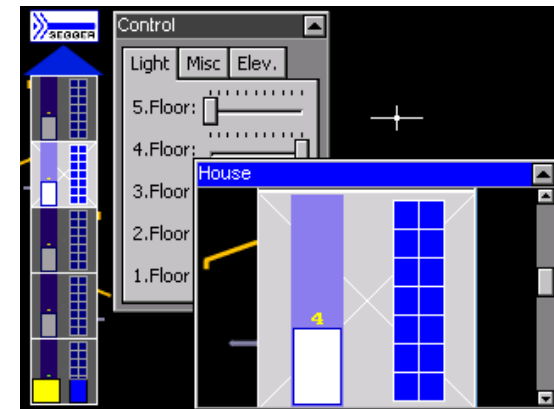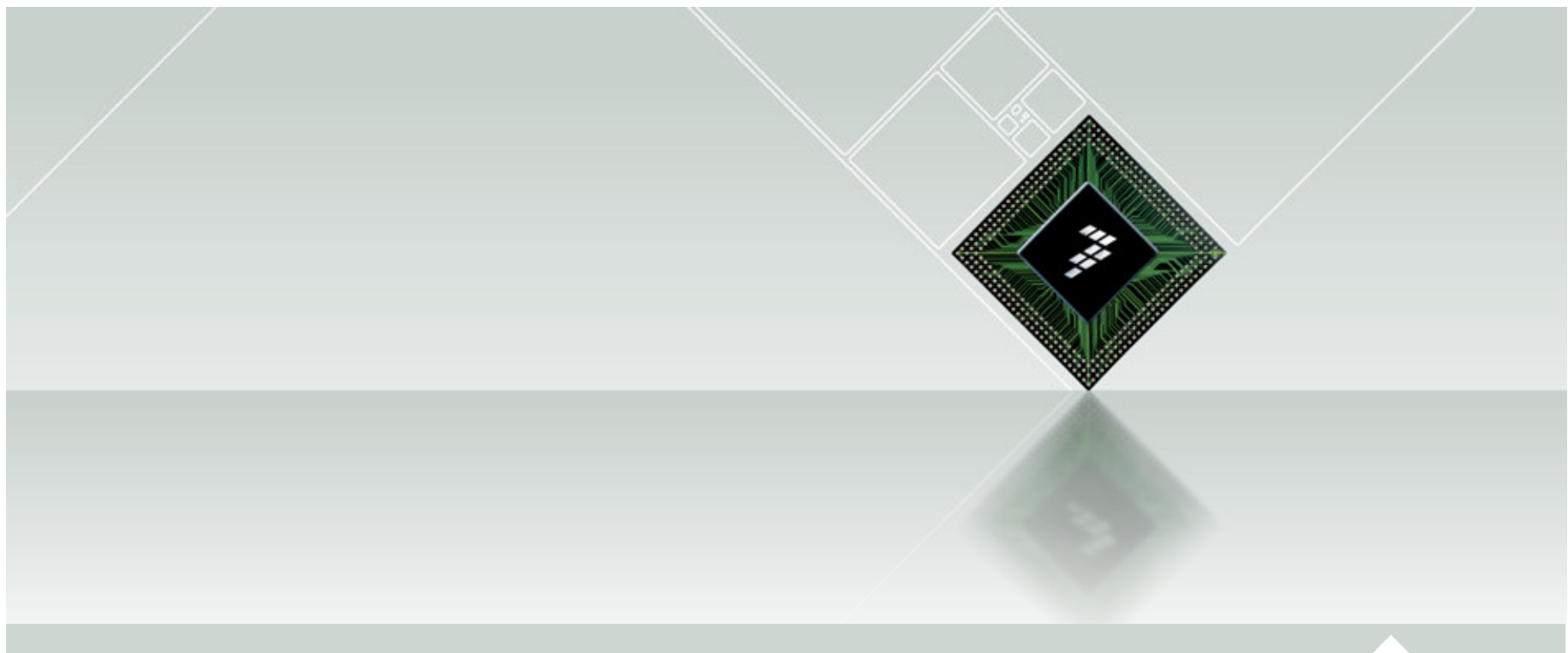
Freescale Display Enabled Products

Overview

Freescale Display Enabled Products

Freescale Processor	Seg/BP Resolution	Arch	Max MIPS	HW Accel	Display Buffer	Display Out	LCD Cntrl	Video In/Out	Other
MC9RS08LE4	112 / 8	RS08	20MHz	-	eFlash	3/5V	-	-	low-cost
MC9S08LL8	160 / 8	S08	20MHz	-	eFlash	3/5V	-	-	ultra-lp/rcp
MC9RS08LA8	168 / 8	RS08	20MHz	-	eFlash	3/5V	-	-	low-cost
MC9S08LL16	192 / 8	S08	20MHz	-	eFlash	3/5V	-	-	ultra-lp/rcp
MC9S08LL/LH36/64	288 / 8	S08	40MHz	-	eFlash	3/5V	-	-	ultra-lp/rcp
MC9S08LG32	296 / 8	S08	40MHz	-	eFlash	3/5V	-	-	ultra-lp/rcp
MCF51EM128/256	288 / 8	CFv1	47	-	eFlash	3/5V	-	-	ultra-lp/rcp
MCF5227x	SVGA	CFv2	160	-	DDR1	RGB19	LCDC	-	rtouch
MCF532x/7x	SVGA	CFv3	240	-	DDR1	RGB18	LCDC	-	-
MPC560xS	WQVGA	PAe200z0	85	-	eFlash	RGB24	DCU	In	gauge
MPC5125	WXGA/720p	PAe300c4	800	-	DDR2	RGB24	DIU	-	-
MPC5121e/5123	WXGA/720p	PAe300c4	800	OGL/AXE	DDR2	RGB24	DIU	In	-
MPC8610	SXGA	PAe600	3060	AltiVec	DDR2/3	RGB24	DIU	-	-
P1022/1013	SXGA	PAe500v2	5000	-	DDR2/3	RGB24	DIU	-	-
i.MX233	SVGA	A926EJ-S	500	PXP/DCP	LPDDR1	RGB18	LCDIF	Out	rtouch/vDAC
i.MX25x	SVGA	A926EJ-S	440	-	DDR2	RGB24	LCDC	In/Out	rtouch
i.MX27	SVGA	A926EJ-S	440	VC	LPDDR1	RGB24	LCDC	In	-
i.MX31	SVGA	A1136JF-S	585	OGL/VC	LPDDR1	RGB24	IPU	In/Out	-
i.MX35x	WSGA	A1136JF-S	585	OVG	DDR2	RGB24	IPU	In/Out	-
i.MX51	WXGA/720p	ACortex-A8	1600	OGL/OVG/VC	DDR2	RGB24	IPU	In/Out	-

OGL   OpenGL hardware accelerator (also provides OpenVG and video codec support)
OVG   Dedicated OpenVG hardware accelerator
VC   Dedicated video codec hardware accelerator
PXP   Pixel pipeline processing block handling blending, CSC and scaling
DCP   Data co-processor that supports CSC
AXE   Audio/DSP core

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► DIU

- 3-plane + cursor blend with N-plane writeback iterative blending
- Each plane has flexible linked list of Area Of Interest (AOI) source buffer
- Flexible αRGB and 8-bit palletized pixel formats

► DCU (DIU derivative)

- 4-plane blend selected from 16-layers (fixed priority) with bkgnd/cursor blit
- Direct ITU656 input which can be a slave to or master display clock
- Compressed data formats supported with tile and luminous modes

► IPU

- 2-plane blend (video with graphics)

► LCDC (IPU derivative)

- 2-plane blend (graphics with background)

► LCDIF/PXP

- Single plane
- PXP accelerator does mem-mem blending and processing

► Segment Drivers

- Integrated front and backplane segment drivers supporting 3V and 5V

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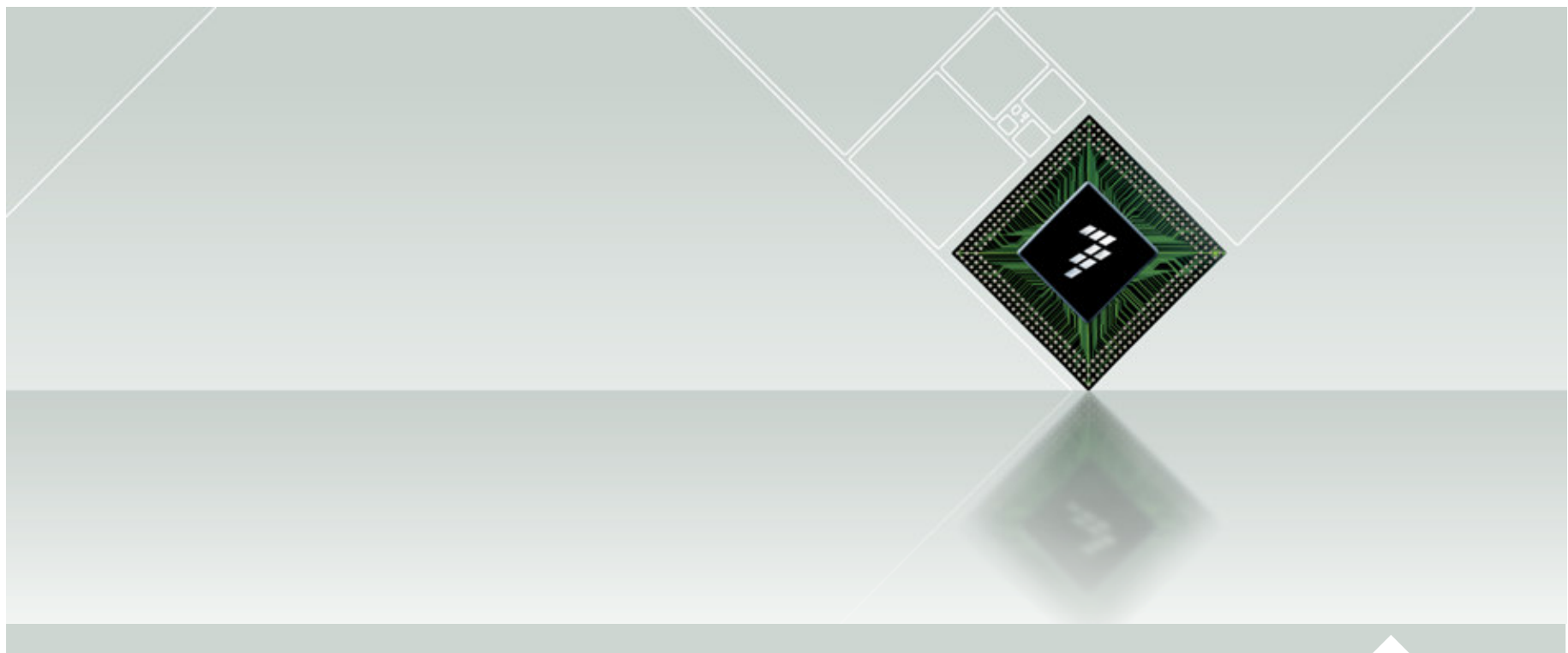
Freescale Display Enabled Products

8-Bit S08 & 32-Bit ColdFire MCU Segment Drivers

8bit Architecture Overview; Part Freescale's Controller Continuum

ColdFire® V4

ColdFire V3

ColdFire V2

ColdFire V1

32-bit

Flexis™ Series
The Controller Continuum
"Connection Point"

S08 core

RS08 core

8-bit
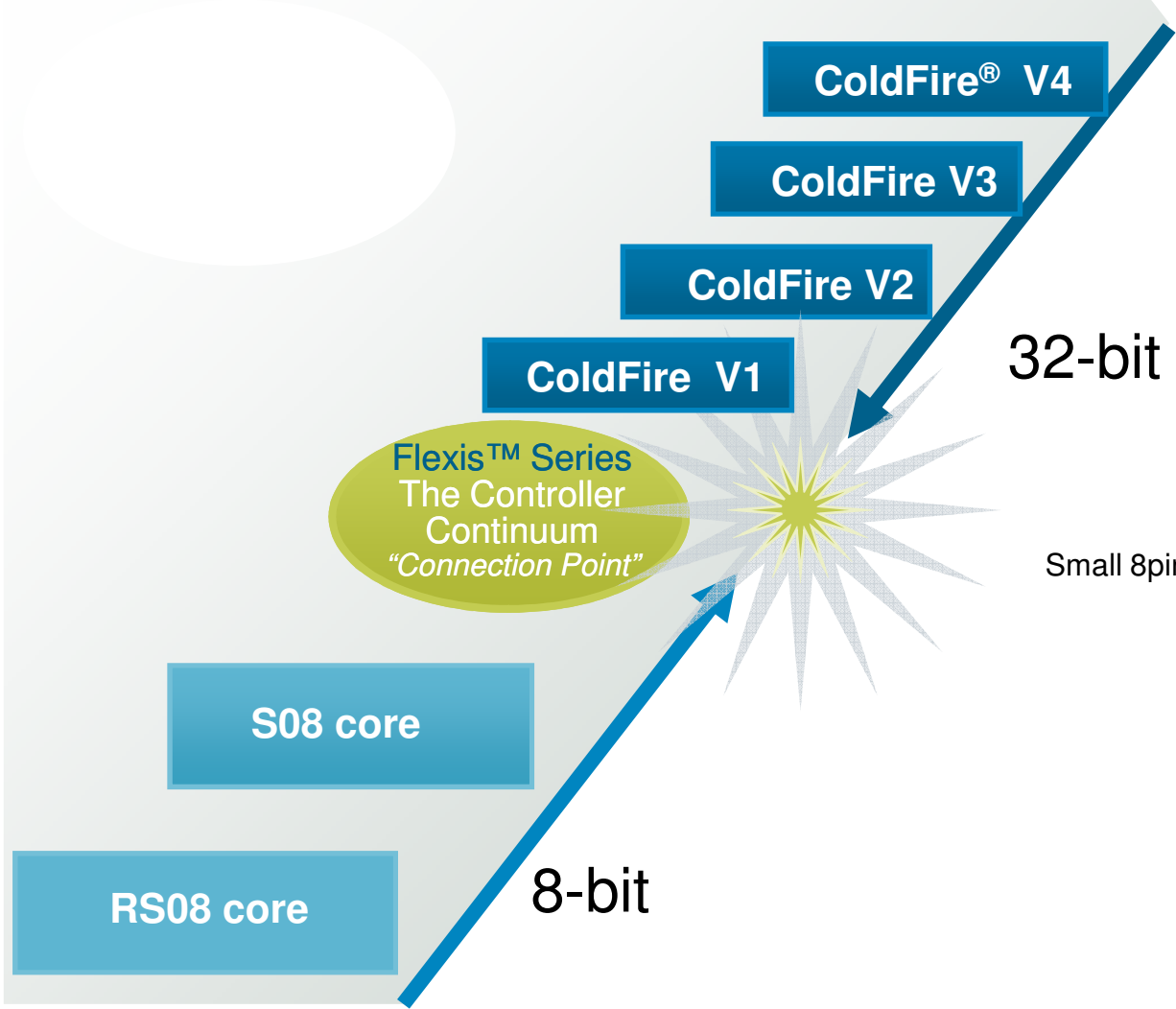
S08 Based Families
Broad range of Solutions
From 2KB to 128KB Memory Sizes
Small 8pin packages up to highly function 80pin options
Starting from $0.60 - $4.00
Compatible with 32bit, part of Flexis Series

RS08 Based Products
Entry Level Line
Ultra-Low-Cost, starting sub $0.50
Small Packages; 6pin – 20pin
Small Memory Sizes; 1KB – 8KB

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LCD controller

►LCD waveforms functional in LPRun, LPWait, wait, stop2 and stop3 low-power modes

►64 LCD (LCD[63:0]) pins with selectable frontplane/backplane configuration

►Programmable LCD frame frequency with software configurable frame interrupt

►Programmable blink modes and frequency

►Integrated charge pump requires only four external capacitors for generating LCD bias voltages configurable to drive 3-V or 5-V LCD panels

►Internal regulated voltage source with a 4-bit trim register to apply contrast control

►Internal ADC channels are connected to VLL1 and VLCD to monitor their magnitudes. This feature allows software to adjust the contrast.

►Backplane reassignment to assist in vertical scrolling on dot-matrix displays

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Key Differentiating Features

►Fewer pins required to drive LCD segments

- 32 pins required for 192 segments in 8x24 mode
- 28 pins required for 160 segments in 8x20 mode
- 17 pins required for 104 segments in 8x13 mode

►Low power blinking mode

- Internal software selectable regulated power supply that keeps constant voltage across LCD glass to avoid degradation
- LL16 offers 4 bits resolution trim to adjust contrast control (Only for S08 and V1 cores)

►Front and back plane re-assignment

- FP and BP can be software selectable to be either FP or BP, making board layout an easier task and very flexible for changes

►Internal charge pump provides all voltages required to power up LCD glass

- Internal software selectable regulated power supply that keeps constant voltage across LCD glass to avoid degradation
- LL16 offers 4 bits resolution trim to adjust contrast control (Only for S08 and V1 cores)

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Using Blink Mode

Benefits of using blink mode

1- Blinking to a blank screen turns all segments off, leading to lower standby current for the time that the screen is blank

78°C		78°C	

Stop Mode ──────────────────────►

2 - Using the Alternate blink mode allows the application to remain in Stop mode for longer periods of time.
Example: Using alternate display to show time across 2 Seconds

WITHOUT ALT BLINK

7:01:54   7:01:55

Stop Mode ──────►■ ──────►■

LCD Glass   LCD Glass

WITH ALT BLINK

7:01:54   7:01:55

Stop Mode ──────────────────►■

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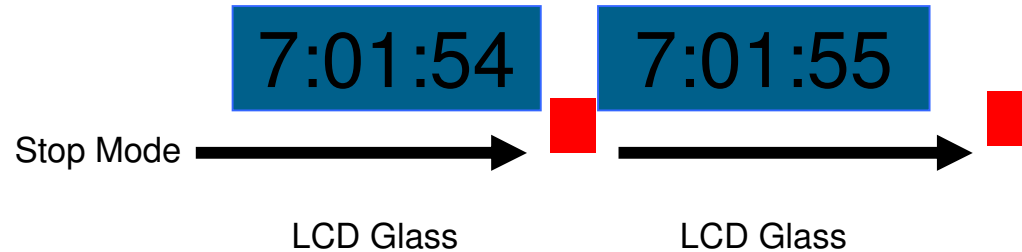
LCD Frame Rate – Frame rate is the rate at which the LCD segments will be refreshed. Frame rates that are too fast will produce ghosting, frame rates that are too slow will have poor contrast.

Table 11-13. LCD Module Frame Frequency Calculations[1]

Duty Cycle	1/1	1/2	1/3	1/4	1/5	1/6	1/7	1/8
Y	16	8	5	4	3	3	2	2
LCLK[2:0]								
0	64	64	68.3	64	68.3	56.9	73.1	64
1	51.2	51.2	54.6	51.2	54.6	45.5	58.5	51.2
2	42.7	42.7	45.5	42.7	45.5	37.9	48.8	42.7
3	36.6	36.6	39	36.6	39	32.5	41.8	36.6
4	32	32	34.1	32	34.1	28.4	36.6	32
5	28.4	28.4	30.3	28.4	30.3	25.3	32.5	28.4
6	25.6	25.6	27.3	25.6	27.3	22.8	29.3	25.6
7	23.3	23.3	24.8	23.3	24.8	20.7	26.6	23.3

[1] LCD clock input ~ 32.768 kHz
Shaded table entries are out of specification and invalid.

LCD Peripheral allows for configurable frame rate.

Using the LCLK bits the frame rate can be optimized for the custom glass.

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Factors that will affect LCD standby current

LCD Glass Capacitance -   LCD glass capacitance is determined by the area of the segments on the glass. The larger the segment area, the larger the Capacitance will be.

500pF glass

8000pF glass
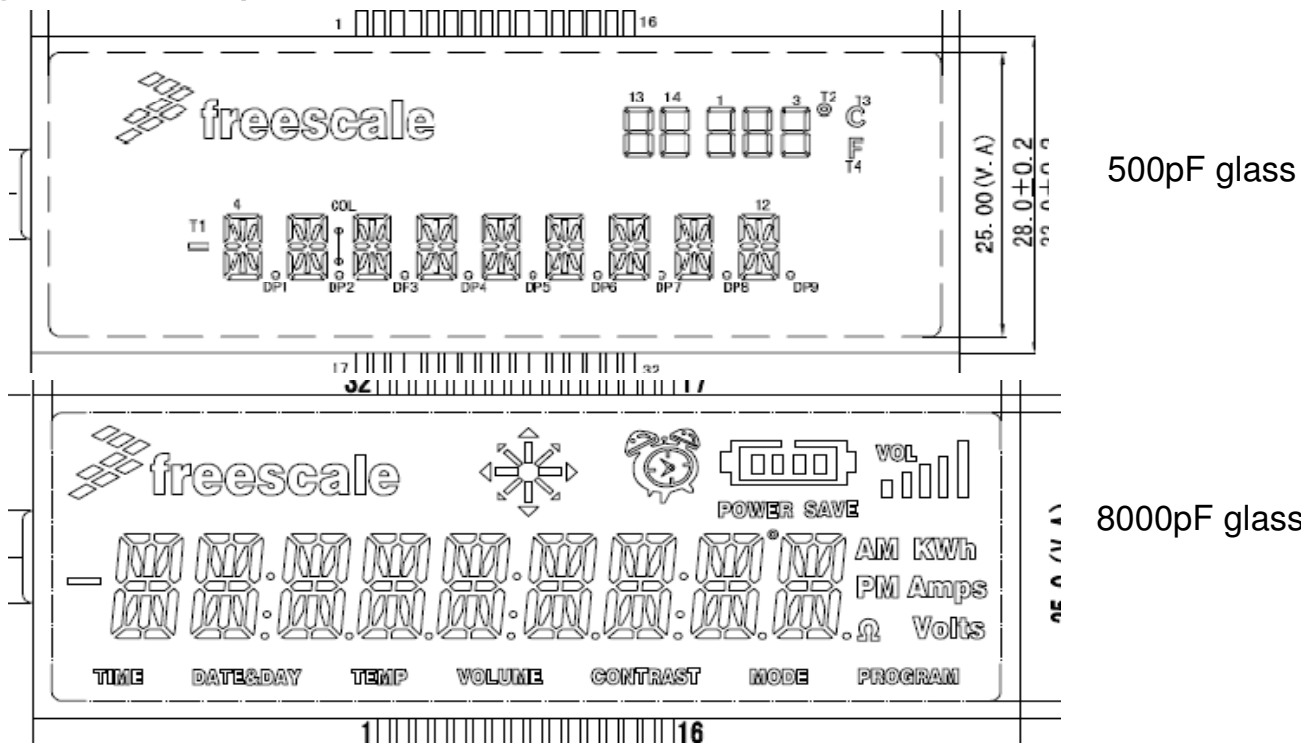
Factors that will affect LCD standby current

Segments configuration – Worst case configuration will be every other segment on. This will cause a rail to rail square wave on the Segment pins. Best case configuration will be all segments off.
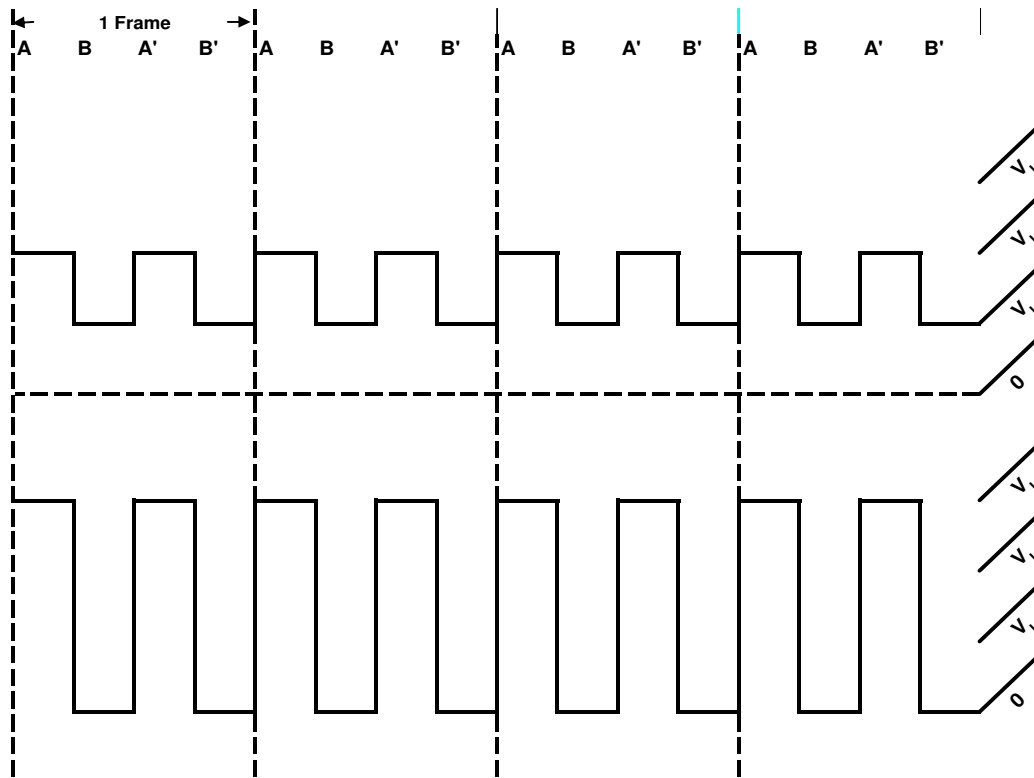
For all segments off the LCD Front plane wave forms switch between VLL1 and VLL2

For every other segment on the LCD front plane waveforms switch between 0 and VLL3

Even more factors that will affect LCD standby current

Number of segments supported – More segments will lead to higher power consumption.
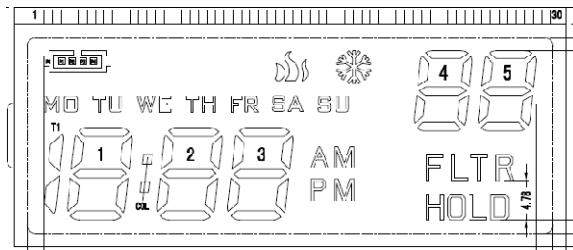
Temperature - Due to leakage at high temperatures, there is a sharp increase after 70C.

Glass Voltage – When supporting 5V glass, the power consumption will increase due to the increased demands to the LCD charge pump.

Product Comparison: LL16 vs. TI MSP430

Configuration	Segments Configuration	MSP430FG4618/F2013 IDD	LL16 IDD	PERCENT Improvement %
No Contrast control, Low power Mode, Crystal Oscillator enabled, 32Hz frame rate, 4x22	ALL ON	6uA	1.8uA	70
No Contrast control, Low power Mode, Crystal Oscillator enabled, 32Hz frame rate, 4x22	ALL OFF	5uA	1.2uA	76
No Contrast control, Low power Mode, Crystal Oscillator enabled, 32Hz frame rate, 4x22	EVERY OTHER SEG	5.4uA	1.8uA	67
With Contrast control (3.08V), Low power Mode, Crystal Oscillator enabled, 32Hz frame rate, 4x22	ALL ON	9.8uA	3.3uA	66
With Contrast control (3.08V), Low power Mode, Crystal Oscillator enabled, 32Hz frame rate, 4x22	ALL OFF	7.4uA	2.0uA	73
With Contrast control (3.08V), Low power Mode, Crystal Oscillator enabled, 32Hz frame rate, 4x22	EVERY OTHER SEG	7.9uA	3.3uA	58

Significant improvement

Which is your choice?

LL16 beats MSP430 on the power consumption with over 70% improvement.
* Base on the same testing environment.

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LCD MCU Series Roadmap

ColdFire®

S08/RS08

MCF532x
Graphic LCD
MPU

MCF52274/7
Graphic LCD
MPU

S08LC60
Segment LCD
MCU

S08LC36
Segment LCD
MCU

S08LG32
5V Segment
MCU

S08LL16
Ultra-low power
Segment LCD
MCU

S08LL8
Ultra-low power
Segment LCD
MCU

RS08LA8
Segment LCD
MCU

RS08LE4
Segment LCD
MCU

S08LL64
Ultra-low-power
Segment LCD
MCU

S08LL36
Ultra-low-power
Segment LCD
MCU

ColdFire
Graphic LCD
MCU

S08
Segment LCD
MCU

Current

Future

Roadmap designates planned devices.

41

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Explore new segment LCD solutions

S08LC60/36	3V up to 160segments with charge pump, up to 64K Flash
S08LL16/8	ULP, Up to 192 Segment LCD, Flexible LCD solution, 1.8-3.3V, with charge pump
RS08LA8	2.7-5V LCD, up to 168 segment LCD with change pump
RS08LE4	2.7-5.5V LCD, up to 112 segment in small (28SOIC) footprint.
S08LG32/16 – NEW!!	2.7-5.5V LCD, up to 288 segments with charge pump, up to 32K Flash

►**LCD Family Features:**
- From 72 up to 288 segment LCD support; Drive more segments with less pins
- FP or BP reassignment
- Blink in Stop capability
- Internal Charge Pump (RS08LA, S08LL, S08LG)
- 3V ULP and 5V solutions

►**LCD Resources**
- Application Notes, Reference Designs, Demos, www.freescale.com/lcd

►**LCD Developments**
- Expansion of LL family to larger packages with more memory, higher accuracy ADCs

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Block diagram:

| BDM | VREG | GPIO | 2-ch. Timer/PWM | 16-bit Timer | 2 x 8-bit Timer |

Core Clock
- 32 kHz/ 1–16 MHz osc → Internal Clock

Robust Flash
- 64/128K Flash | Swap | 64/128K Flash

- Alarms
- Atomic Counter
- 32B RAM

Independent RTC
- 32 kHz osc
- Tamper Detect
- Calendaring
- Clock Compensation

— Vmcu

Power Switch

— Vbat

SAR ADC
- 4 x 16-bit SAR ADC | Sequencer (PDB)

SCI
- 2 x Comparator 0–1.2V ref | 2 x SCI

16/8K RAM	16-bit CRC	1.2V ref	AMR SPI
I²C	KB I	2 x SPI	AMR SCI
V1 ColdFire® MCU inc MAC	LCD (1–8) x (43–36)

► **ColdFire V1 32-bit Core with Multiply Accumulate unit**
- Efficiently supports complex power calculations
- Inherently supports large memory systems
- Provides enough throughput for application and connectivity

► **Independent Real Time Clock (RTC)**
- Operates from an independent power supply, even during power outages when other MCU systems are not powered
- Consumes very little power, less than 2µA

► **Robust Firmware Update**
- Meter continues to operate from one Flash block, while other is updated and verified with new firmware
- Flash block swap reliably completes firmware update

► **Tamper Detection**
- Detects and records tamper attempt even during power off
- Detects and records attempts to disconnect backup battery

► **Four 16-bit high speed SAR ADCs**
- Support simultaneous sampling of four analog inputs
- Include phase shift compensation needed with Current Transformers

► **LCD Controller**
- Supports a wide range of displays, up to 288 segments
- Up to eight backplanes reduces number of pins and system cost

Part #	Flash	SRAM	SPIs	Package	10K Sugg Resale Price
MCF51EM256CLL	2x 128KB	16KB	3	100 LQFP	$4.22
MCF51EM256CKL	2x 128KB	16KB	2	80 LQFP	$3.97
MCF51EM128CLL	2x 64KB	8KB	3	100 LQFP	$3.86
MCF51EM128CKL	2x 64KB	8KB	2	80 LQFP	$3.60

MC product available by end of Q1, 2010

Samples available now as PCF

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MC9RS08LE4

LCD Driver	9RS08LE4	Packages

LCD Driver

Based on 8 backplanes
8x14 = 112 segments

Based on 4 backplanes
4x18 = 72 segments

9RS08LE4

RS08 **Core**	LVI	ICS
4K **Flash**	KBI	RTI
256 **RAM**	COP	SCI
RS08BDM	LCD Driver 8x14 or 4x18	8-10 bits ADC
		2x2-ch 16-bit Timer

Packages

28 SOIC

▶ **Voltage Range**
- 2.7V to 5.5V

▶ **Core**
- RS08

▶ **1-20MHz Capability**

▶ **Features**
- 8-ch keyboard interrupt
- Up to 26 GPIOs
- LVI (low voltage inhibit)
- RTI

▶ **Internal Clock Source (ICS)**
- FLL
- On-chip oscillator
- External crystal support
- 2% accuracy over full operating range
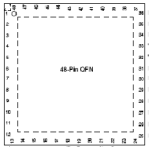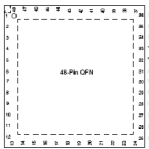
▶ **Development Tools**
- On-chip BDM

▶ **Memory**
- 4K flash
- 256 bytes RAM

▶ **$0.90 MSRP at 10K units**

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MC9RS08LA8

LCD Driver	9RS08LA8			Packages
Based on 8 backplanes 8x21 = 168 segments Based on 4 backplanes 4x25 = 100 segments	RS08 **Core** 8K **Flash** 256 **RAM** **RS08BDM**	LVI KBI COP **SPI** LCD Driver 8x21	ICS SCI MTIM Comparator 6-10 bits ADC 1x2-ch 16-bit Timer	48 QFN 48 LQFP

► **Voltage Range**
 • 2.7V to 5.5V

► **Core**
 • 10 MHz CPU speed

► **Features**
 • 8-ch keyboard interrupt
 • Up to 34 GPIOs
 • 16 LCD pins mux with GPIO
 • LVI (low voltage inhibit)
 • RTI
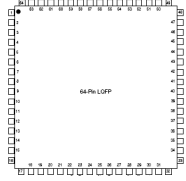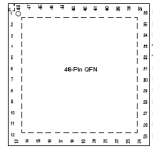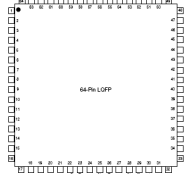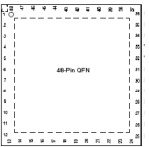
► **Internal Clock Source (ICS)**
 • FLL
 • On-chip oscillator
 • External crystal support
 • 2% accuracy over full operating range

► **Development Tools**
 • On-chip ICE and RS08BDM

► **$0.99 MSRP at 10K units**

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MC9S08LL16/8

LCD Driver	9S08LL16/8	Packages

LCD Driver

LL16:

Based on 8 backplanes
8x24 = 192 segments
Based on 4 backplanes
4x28 = 112 segments

LL8:

Based on 8 backplanes
8x16 = 128 segments

Based on 4 backplanes
4x20 = 80 segments

9S08LL16/8

- S08 Core
- LL16: 16K LL8: 8K
- 2K **RAM**
- **ICE + 08BDM**
- LVD
- KBI
- COP
- SPI
- Comparator
- LCD Driver
- IIC
- SCI
- ICS
- TOD
- 8-12 bits ADC
- LL16: 2x2-ch 16-bit Timer LL8: 1x2-ch 16-bit Timer

Packages

LL16 — 48 & 64 LQFP — 48 QFN
LL8 — 48 LQFP — 48 QFN

64-Pin LQFP 64-Pin LQFP 48-Pin QFN 48-Pin QFN

► **Voltage Range**
- 1.8V to 3.6V

► **Core**
- 20 MHz CPU speed

► **Features**
- 8-ch keyboard interrupt
- Up to 38 GPIOs
- Up to 18 LCD pins mux with GPIO
- LVD (low voltage detect)
- Time-of-day module

► **Internal Clock Source (ICS)**
- FLL
- On-chip oscillator
- External crystal support
- 2% accuracy over full operating range

► **Development Tools**
- On-chip ICE and 08BDM

► **Start from $1.50* MSRP at 10K units**

*Varies by package

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► ## LCD Driver

- Up to 288 segment LCD drive(8x mode)
- BP/FP reassignment
- Blink operation in low-power modes
- Drive 3V and 5V LCD glass

► ## Features

- 2xSCIs, IIC, SPI, KBI, TOD, ACMP
- 2x2ch 16bit TPM
- 10ch 12bit ADC
- VREF1.2 (1.2v – 40PPM/°C)
- EEPROM emulation
- 80LQFP/64LQFP package
- Up to 39 GPIO

► ## Memory

- Dual bank 32K flash
- 4K RAM

► ## Internal Clock Source (ICS)

- FLL
- On chip oscillator
- External crystal support(32Khz, 1-16Mhz)
- 2% accuracy over full operating range

► ## Development Tools

- On chip BDM

► ## Design Considerations:

- Ultra-Low Power
- S08 core
- 1.8V – 3.6V

► ## Availability:

- LL64 Beta samples: July 2009
- LL64 Qualification: September 2009 (MC)

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5V MC9S08LG Family Overview

► Family overview

- Targets low end cluster and general purpose LCD applications for autos, motorcycles, scooters, marine, etc.

- Integrated LCD, supporting both x8 and x4 mode up to 8 x 37 or 4 x 41 segments

- Dual bank flash for EEPROM emulation

- Multiple time bases for motor control

- Internal Clock Source
  - 2% accuracy across temp

- Strong EMC performance in tough environment

- -40°C to 105°C and 2.7–5.5V operation available

► Availability

- Alpha samples March 2009

- MC Qual April 2009

Block diagram:

1xSPI		WDG COP
1xI²C	2 x 16 KB Dual Flash	16ch 12bit ADC
2xSCI	2 KB RAM	6-ch. + 2-ch., 16-bit Timer 1-ch., 8-bit MTIM
RTC	ICE / BDM ICS	37x8 / 41X4 LCD
GPIO	S08 CPU 20 MHz Bus	80 LQFP 64 LQFP 48 LQFP
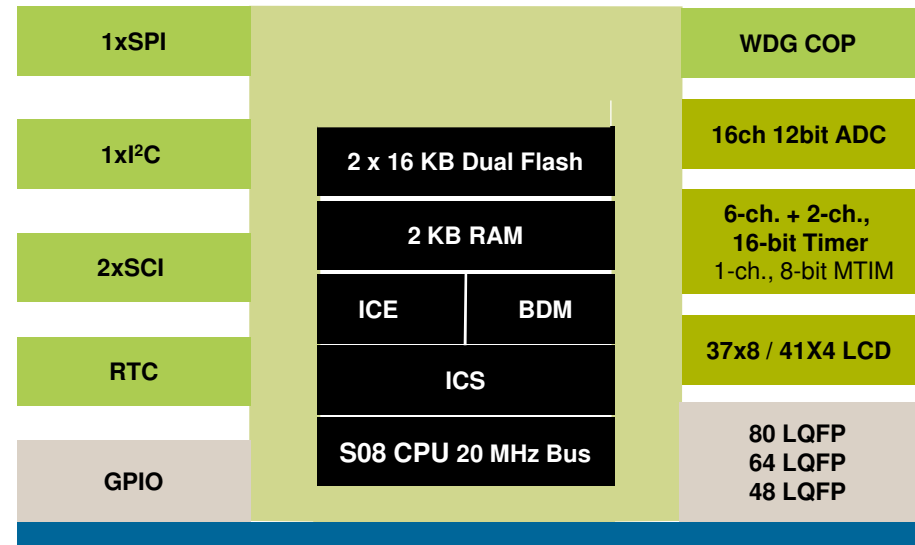
Note: block diagram represents the LG32

Family Differences

Device	Package	Flash	LCD	ADC	GPIO
LG32	80-LQFP	Dual 16+16K	8x37, 4x41	16-ch., 12-bit	69
	64-LQFP	Dual 16+16K	8x29. 4x33	12-ch., 12-bit	53
	48-LQFP	Dual 16+16K	8x21, 4x25	9-ch., 12-bit	53
LG16	64-LQFP	Dual 16+2K	8x29. 4x33	12-ch., 12-bit	39
	48-LQFP	Dual 16+2K	8x21, 4x25	9-ch., 12-bit	39

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Block diagram components:
- S08 Core w/MMU
- Dual 32K Flash Arrays = 64K
- 4K RAM
- BDM
- LVD
- KBI
- COP
- SPI
- LCD Driver 8x36=288
- TOD
- ACMP
- 2xSCI
- ICS
- IIC
- 10ch-16 bit ADC 2 dedicated differentials
- 2x2-ch 16bit TPM
- Vref
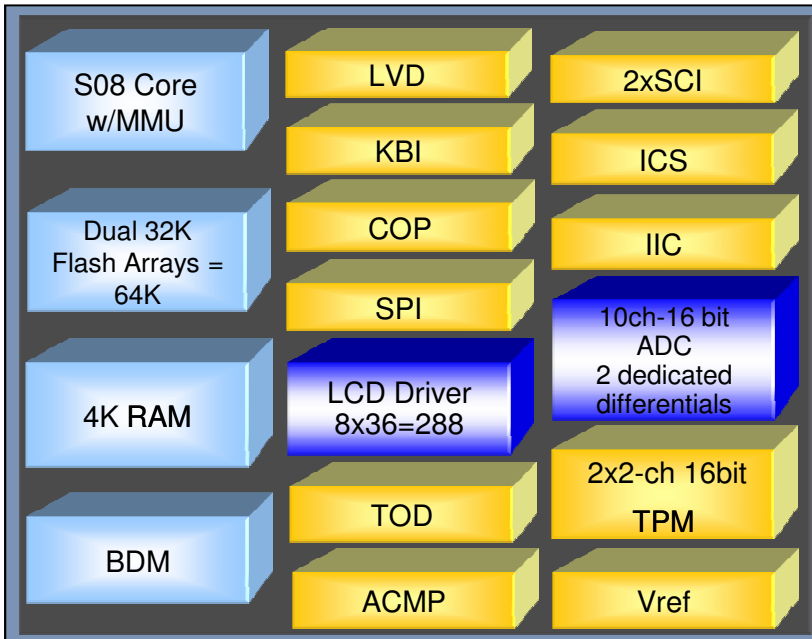
▶ Design Considerations:

- Ultra-Low Power
- S08 core
- 1.8V – 3.6V

▶ Availability:

- LH64 Beta samples: October 2009
- LH64 Qualification: January 2010 (MC)

▶ LCD Driver

- Up to 288 segment LCD drive(8x mode)
- BP/FP reassignment
- Blink operation in low-power modes
- Drive 3V and 5V LCD glass

▶ Features

- 2xSCIs, IIC, SPI, KBI, TOD, ACMP
- 2x2ch 16bit TPM
- 10ch 16bit ADC, 2 dedicated differentials
- VREF1.2 (1.2v – 40PPM/°C)
- EEPROM emulation
- 80LQFP/64LQFP package
- Up to 39 GPIO

▶ Memory

- Dual bank 32K flash
- 4K RAM

▶ Internal Clock Source (ICS)

- FLL
- On chip oscillator
- External crystal support(32Khz, 1-16Mhz)
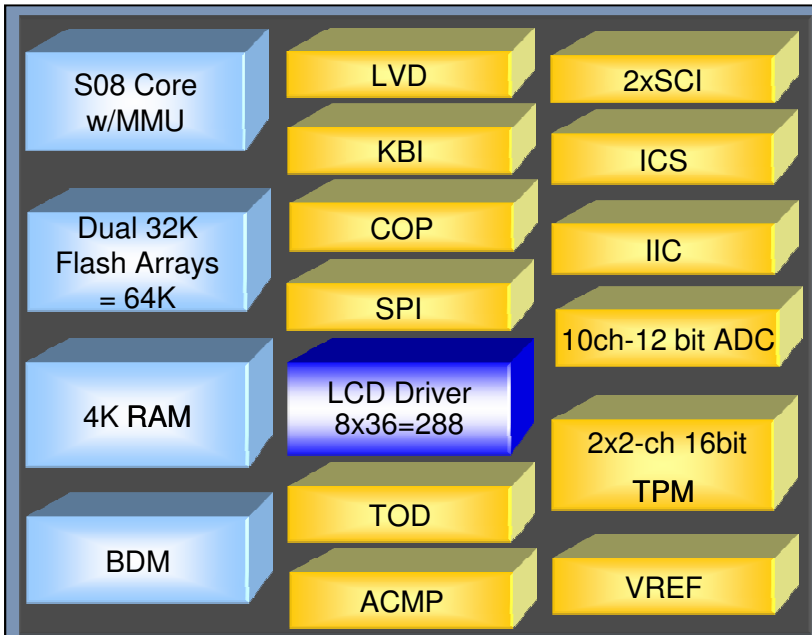- 2% accuracy over full operating range

▶ Development Tools

- On chip BDM

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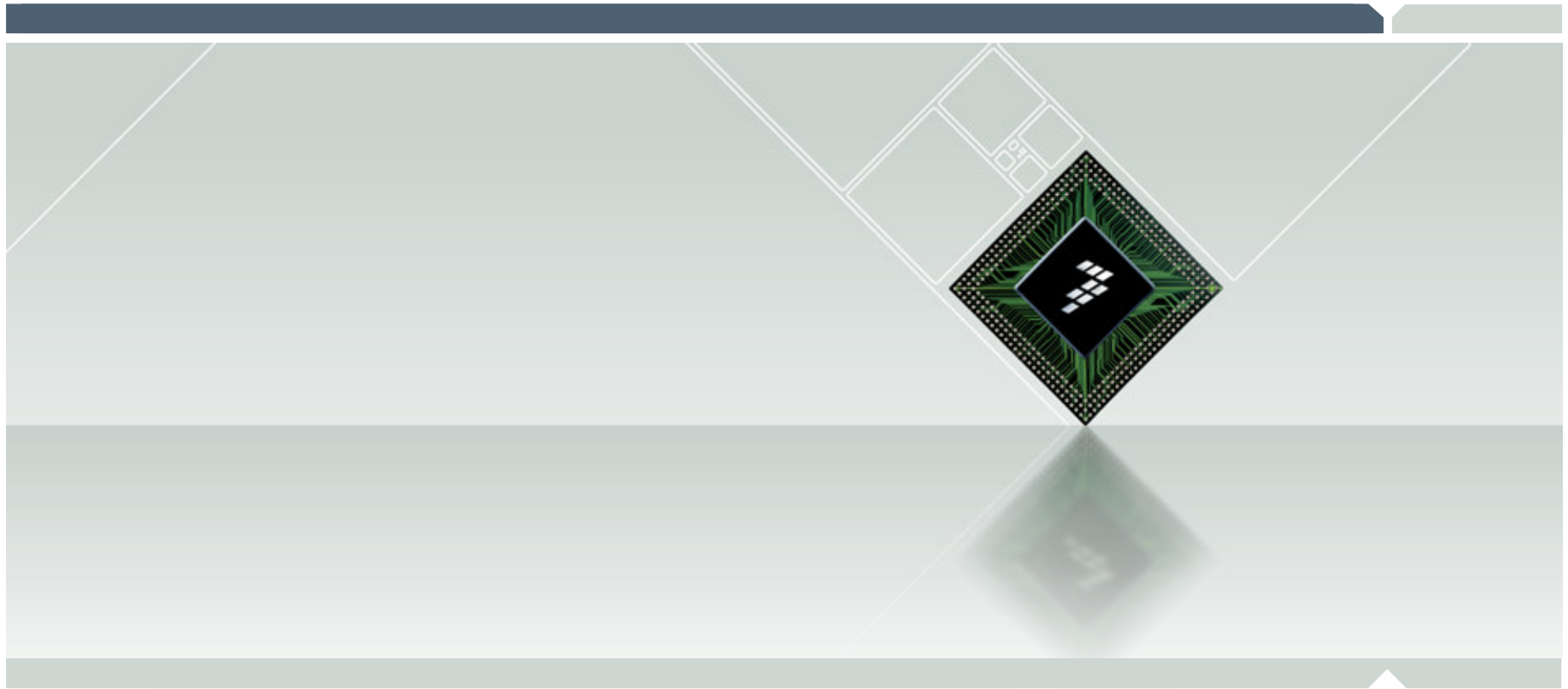
Freescale Display Enabled Products

ColdFire MPU Products

MCF5227x

68K/*ColdFire®* V2 Core

- ▶ Up to 158 Dhrystone 2.1 MIPS @ 160 MHz (Hip7A)
- ▶ Enhanced Multiply Accumulate and Hardware Divide
- ▶ 16K bytes Configurable I/D Cache
- ▶ 128K bytes SRAM
- ▶ Integrated LCD Controller
  - ▶ CSTN and TFT w/ Up to 800x 600(SVGA) resolution
- ▶ 8x12-bit ADC w/ Touch-screen Controller
  - ▶ **Real touch screen controller**
- ▶ USB 2.0 full-speed On-the-go Controller
- ▶ CAN 2.0B Controller (FlexCAN)
- ▶ 3 UARTs
- ▶ DMA Serial Peripheral Interface (DSPI)
- ▶ I^{2}C bus interface
- ▶ Synchronous Serial Interface (SSI)
- ▶ 4 ch. 32-bit timers with DMA support
- ▶ Real Time Clock
- ▶ 16 ch. DMA controller
- ▶ 16-bit DDR / 32-bit SDR SDRAM controller
- ▶ Up to 55 General-Purpose I/O
- ▶ System Integration (PLL, SW Watchdog)
- ▶ 1.5V Core, 1.8V/2.5V/3.3V Bus I/O
- ▶ Temperature Range: -40°C to +85°C
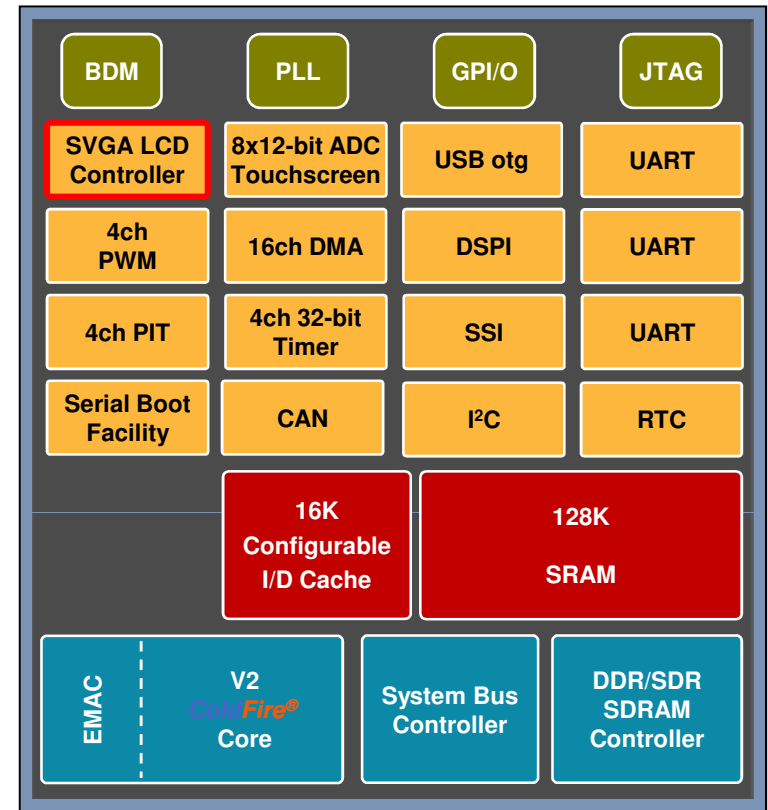
- • M52277EVB Full Evaluation Platform
- • Available packages: **176QFP** and **196BGA**
- • Lowered pricing starting at $5.99 10K SRP

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68K/*ColdFire* V3 Core

▶ Up to 200 Dhrystone 2.1 MIPS @ 240 MHz
▶ Enhanced MAC Module and HW Divide
▶ 16K bytes Unified Cache
▶ 32K bytes SRAM
▶ Integrated LCD Controller
  • STN and TFT
  • Up to 800x 600(SVGA) resolution
▶ USB 2.0 host controller
▶ USB 2.0 Host/Device/On-the-go Controller
  • High Speed ULPI support
▶ Optional 10/100 Ethernet MAC (external PHY)
▶ Optional Hardware Accelerated Encryption
  • Random Number Generator
  • DES, 3DES, AES, Block Cipher Engine
  • MD5, SHA-1, HMAC, Hash Accelerator
▶ Optional CAN 2.0B Controller
▶ Synchronous Serial Interface (SSI)
▶ 3 UARTs
▶ Queued Serial Peripheral Interface (QSPI)
▶ I²C bus interface
▶ 4 ch. 32-bit timers with DMA support
▶ 4 ch. 16-bit PWM timer
▶ 16 ch. DMA controller
▶ 16-bit DDR / 32-bit SDR SDRAM controller
▶ Up to 94 General-Purpose I/O
▶ System Integration (PLL, SW Watchdog)
▶ 1.5V Core, 1.8V/2.5V/3.3V Bus I/O
▶ Temperature Range: -40°C to +85°C
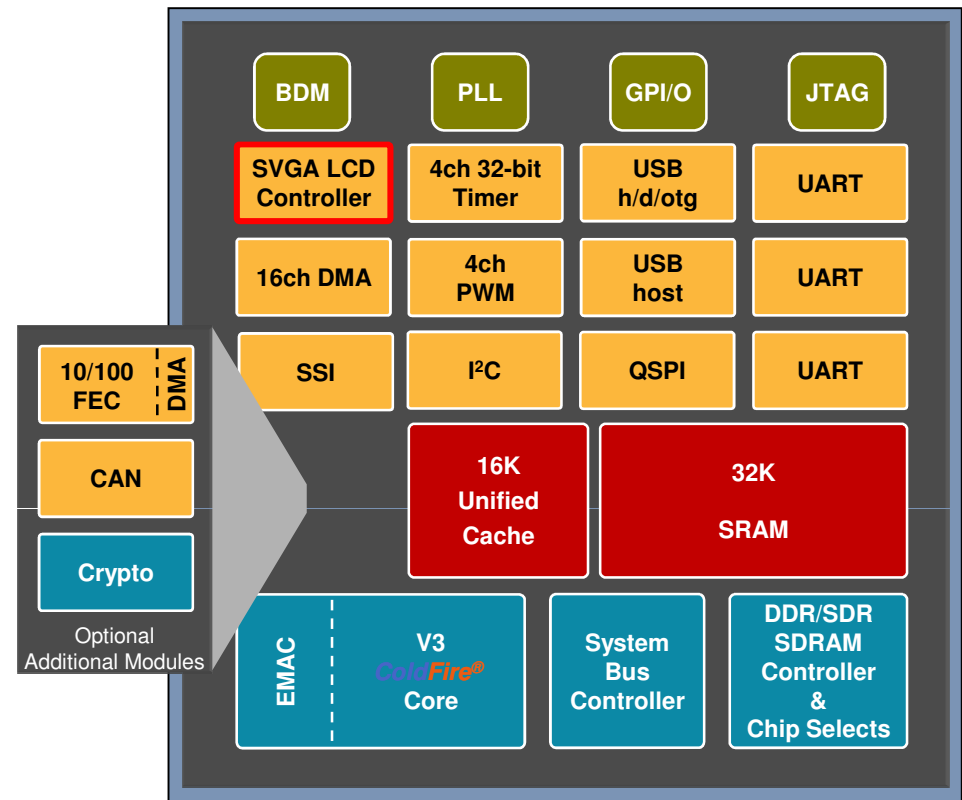
• M5329EVB Evaluation Platform
• M53281KIT VoIP Solution
• Available packages: **196BGA** and **256BGA**
• Pricing starting at $6.49 10K SRP
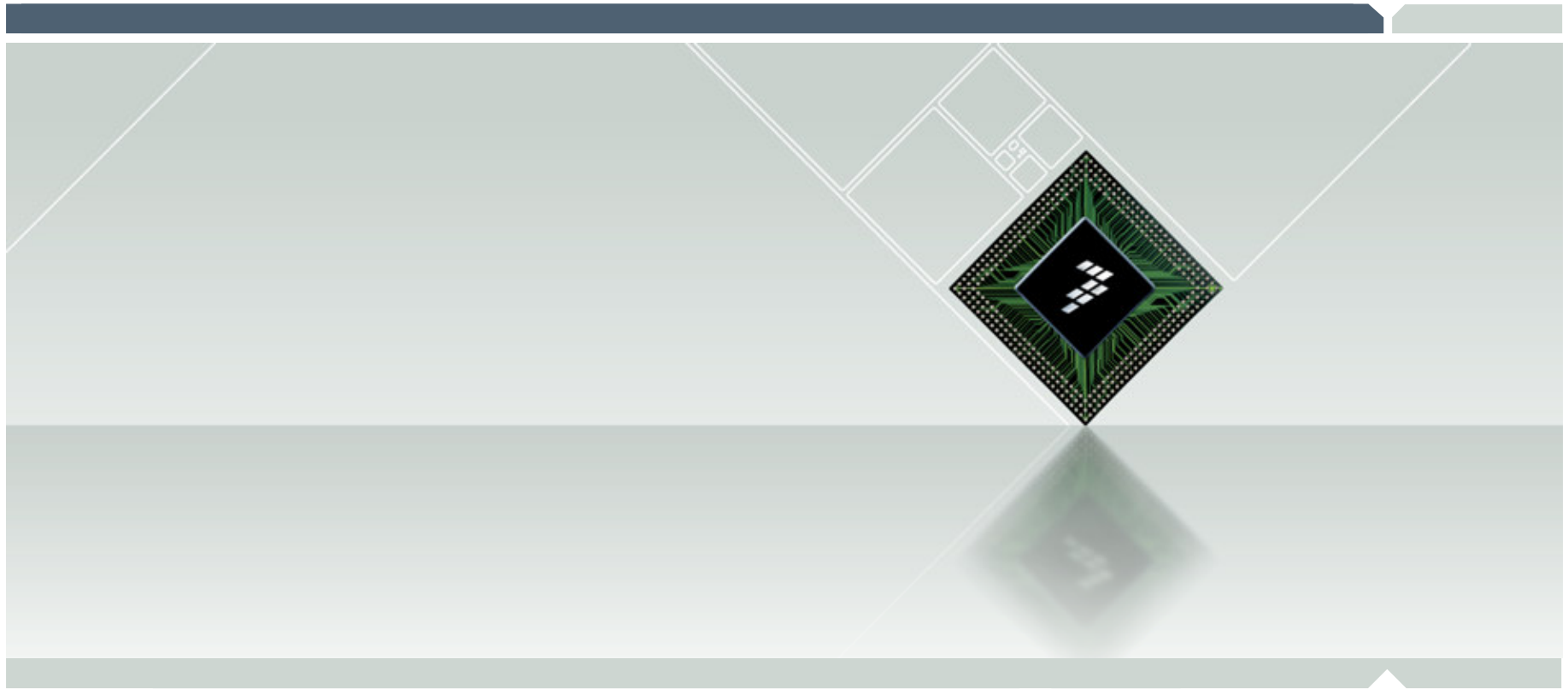
Freescale Display Enabled Products

Power Architecture MCU Products (MPC560xS)

- ► **16 Layers**
- ► **4 planes**
- ► **Frame buffer limited by memory size (all memories, RAM, ROM INT, EXT)**
- ► **Target size WVGA (Limited by memory bandwidth and pixel clock speed)**
- ► **Support 16, 24, 32 bit color depth.**
- ► **Support 1, 2, 4, 8bpp indirect color mode**
- ► **Support TFT type LCD with 16, 18, 24bit wide digital RGB interface**
- ► **Alpha blend (per pixel and per layer in 4 planes)**
- ► **Chroma key (range per RGB component in 4 planes)**
- ► **Combined alpha blend and chroma key modes**
- ► **Font mode blending (transparency mode/alpha map)**
- ► **Highlight area mode. (luminance offset)**
- ► **Tile mode**
- ► **Digital video input**
- ► **Safety mode support**
- ► **Hardware cursor**

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DCU (MPC56xxS Main Display Port)

Memory mapped register area

- Layer CD
- DCU registers
- CLUT
- Tile memory
- Gamma correction table
- Hardware cursor

DMA → Foreground plane FIFO → Format converter → 24bpp / 24bpp → Blend/Chr key → 24bpp → Gamma correction → 24bpp → Display drive → 24bpp → RSDS or Dig RGB

DMA → Foreground Plane FIFO

DMA → Foreground plane FIFO → Format converter → 24bpp / 24bpp

DMA → Background Plane FIFO

TCON (Rainbow) → 12bit

System CLK 64MHz

PDI → Ext. Video Sync → CLK manager
PDI → Ext. Video CLK

Signature calculator X 1 → CRC result output

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▶ Layer priority is fixed.

▶ Layers arbitrate for 4 planes on per pixel basis.

▶ The active layer that has the highest priority loads in the foreground plane 1, the next loads in foreground plane 2 etc….

▶ If no layer qualifies for the BG plane the BG color is loaded in the BG plane

MPC5606S – Single chip cluster example

LEDs

TFT DISPLAY

DCU on MPC5606S enables direct drive of Quarter VGA and WQVGA.

PDI allows cheap video input (no buffer) eg to display reversing camera image on dashboard TFT.

20,3°
St. Michael st.
100 m
0'000'324 km
P R N **D** L

MPC5606S

- 2x CAN
- GP I/O
- 2x LIN
- PWMs
- QuadSPI
- 6 Stepper Motor Drivers with patented stall detection
- 48kb RAM
- EEPROM
- 160kb RAM
- 1MB FLASH
- **DCU**
- 40x4 LCD seg driver
- **PDI**

sound

VIDEO INPUT

Serial Flash

123456.7
TRIP

SEE "MPC5606S" DEMO ON **You Tube**

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DCU Tool Workflow

Graphic Designer Uses →

Tools
Illustrator
Photoshop
Paint
Gimp
Blender

Outputs →

Images
Fonts
Skins
Vector Files
3D Models

Images
Fonts
Skins
Vector Files
3D Models

Are used →

UI Designer Uses →

Tools
Adobe Flash
GIMP
Excel
Image processing
Batch processing
[Others tools]

Outputs →

Specification
(excel files)
(requirements document)

+

Images
Fonts
Vector Files

Specification
(excel files)
(requirements document)

+

Images
Fonts
Vector Files

Are used →

Developer Uses →

Tools Libraries
Spectrum Libraries
Image Encoder
Font Encoder

Outputs →

Spectrum Application Code

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Freescale Display Enabled Products

Power Architecture MPU Products (mobileGT, MPC8610 and QorIQ)

Flexible DIU Blending

▶ 3-plane blend
  - All planes fetched and blended at refresh rate and sent to display

▶ N-plane blend
  - Plane 1 is fetched at refresh rates and sent to display
  - Iterative blends of planes 2 and 3 used to construct future plane 1 to be displayed

Video and/or graphic planes

Video | 2D/3D Graphics | Plane 1 | Plane 2 | Plane 3 | Display Interface Unit

3-Plane Blend or Plane 1

plane 2/3 blend (option)

Unified DRAM Memory System

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DIU Area Descriptors

▶ Area descriptors (AD) defines areas of interest (AOI) on a plane
▶ Each AOI has its own independent definition specified by the AD
▶ Planes can have unlimited AOIs as long as they do no share a horizontal scan line
▶ DIU accesses ADs in vertical order using a linked list of pointers to the next AD
▶ Only pixels within AOIs are fetched by the DIU using the format specified in the AD
▶ AD linked lists can be manipulated to change plane content and move an AOI between planes

Source Frame Buffer

▶ 32-Byte AD Specifies:
• Pixel format (extremely flexible)
• Chroma key RGB max/min values
• Global alpha override
• Endian byte swapping
• Source buffer address & dimension
• Source crop offset & dimension
• AOI display position
• Image flipping (horizontal or vertical)
• Next AD pointer

DIU Area Descriptors

- ► Area descriptors (AD) defines areas of interest (AOI) on a plane
- ► Each AOI has its own independent definition specified by the AD
- ► Planes can have unlimited AOIs as long as they do no share a horizontal scan line
- ► DIU accesses ADs in vertical order using a linked list of pointers to the next AD
- ► Only pixels within AOIs are fetched by the DIU using the format specified in the AD
- ► AD linked lists can be manipulated to change plane content and move an AOI between planes

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8/16/24/32-Bit Pixel Input
(can vary per AOI within planes)

Endian ✕ Swapping

LSB 0~8 bits MSB	LSB 0~8 bits MSB	LSB 0~8 bits MSB	LSB 0~8 bits MSB
Alpha	Red	Green	Blue

Component Swapping ✕ Palette LUT

LSB 8 bits MSB	LSB 8 bits MSB	LSB 8 bits MSB	LSB 8 bits MSB
Alpha	Red	Green	Blue

Blending ↓ Gamma Correction

LSB 8 bits MSB	LSB 8 bits MSB	LSB 8 bits MSB
Red	Green	Blue

24-Bit Pixel Output

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Freescale Power Architecture MPU/MCU Family

Display enabled devices
Embedded flash e200 MCUs

MPC8610
e600 AltiVec SIMD
1.33GHz

PowerQUICC III
MPC85xx - e500
1GHz

QorIQ P4 – e500
4 ~ 32 cores
533MHz ~ 1.5GHz

QorIQ P2 – e500
1~2 cores
800MHz ~ 1.2GHz

QorIQ P1 – e500
1~2 cores
533MHz ~ 800MHz

QorIQ P5 – e500
Multi-core

QorIQ P3 – e500
Multi-core

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PowerQUICC II Pro
MPC83xx – e300
400 ~ 667MHz

Power ISA 1.10 Compatibility

Power ISA 2.x Migration

mobileGT
MPC5121e – e300
800DMIPS, 400MHz

mobileGT
MPC5123 – e300
800DMIPS, 400MHz

mobileGT
MPC5125 – e300
800DMIPS, 400MHz

mobileGT
MPC5200B – e300
760DMIPS, 400MHz

PowerQUICC II Pro
MPC830x – e300
266 ~ 400MHz

PowerQUICC
XPC823E
100DMIPS, 75MHz

MPC551x <=1.5M
120DMIPS, 80MHz

MPC563xM <=1.5M
150DMIPS, 80MHz

MPC560xS <=1M
85DMIPS, 64MHz

MPC560xP/B <=512K
85DMIPS, 64MHz

MPC567xx <=4M
715DMIPS, 264MHz

- High degree of binary compatibility
- Migratable OS solutions (Linux, MQX, WR…)
- Best-in-class density / performance (VLE)

	Power Architecture		
		Power ISA (2.x) – Merged Architecture	
	Desktop (PowerPC Architecture 1.10)	Category: Embedded (formerly Book E/EIS)	Category: Server (formerly PowerPC Architecture 2.02)
ISA	UISA (with extensions)		
VEA	Book II	Book II (with extensions)	
OEA	Book III: (Desktop)	Book III-E: (Embed)	Book III-S: (Server)
	G2/e300 e600	e200 e500 e700	G5 IBM 970 P5

Now

Future

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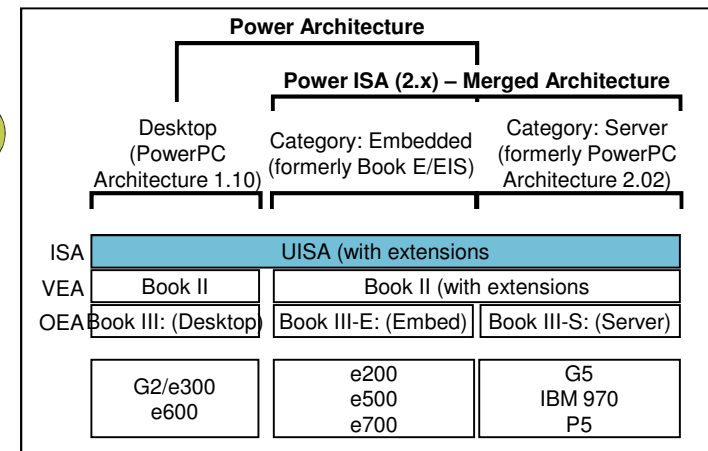
MPC52xx/512x Family

	XPC823e	MPC5200B	MPC5121e	MPC5123	MPC5125
CPU Core	PPC	PPC e300c0, DP-FPU	PPC e300c4, DP-FPU	PPC e300c4, DP-FPU	PPC e300c4, DP-FPU
CPU Freq (DMIPS)	66MHz (90DMIPS)	400MHz (760DMIPS)	400MHz (800DMIPS)	400MHz (800DMIPS)	400MHz (800DMIPS)
Cache (I/D)	16K / 8K	16K / 16K	32K / 32K	32K / 32K	32K / 32K
Graphics Core	-	-	*100MHz PowerVR-MBX*	-	-
Audio/DSP Core	*66MHz CPM*	-	*200MHz AXE*	*200MHz AXE*	-
DRAM Controller	-	16/32-bit SDR/DDR1	16/32-bit DDR1/2, LPDDR	16/32-bit DDR1/2, LPDDR	16/32-bit DDR1/2, LPDDR, 32-bit SDR
DRAM Clk Freq (BW)	-	133MHz (300MB/s)	200MHz (1100MB/s)	200MHz (1100MB/s)	200MHz (1100MB/s)
NAND Flash controller	-	-	8/16-bit, 4-bit ECC bootable	8/16-bit, 4-bit ECC bootable	*8/16-bit, 32-bit ECC 4-page robust bootable*
Display Controller	yes	-	WXGA/720p 24-bit	WXGA/720p 24-bit	WXGA/720p 24-bit
Video Input	ITU-656	-	ITU-656	ITU-656	-
PCI	-	PCI-2.2, 32-bit, 66MHz	*PCI-2.3, 32-bit, 66MHz*	*PCI-2.3, 32-bit, 66MHz*	-
USB	USB 1.1 FS	USB 1.1 FS	2x USB2.0 HS OTG 1x PHY HS OTG	2x USB2.0 HS OTG 1x PHY HS OTG	2x USP 2.0 HS OTG
Ethernet	-	1x 10/100BaseT	1x 10/100BaseT	1x 10/100BaseT	*2x 10/100BaseT*
CAN	-	2	4	4	4
UART	2	6	12	12	10
I2C	1	2	3	3	2
SPI	1	7	12	12	10
GPIO		32	32	32	64
SD / SDIO	PCMCIA	-	1	1	2
PATA/SATA	-	1x PATA	1x PATA / 1x SATA	1x PATA / 1x SATA	-
Chip ID / OTP	-	-	256-bits / 256-bits	256-bits / 256-bits	256-bits / 256-bits
Package	256 PBGA 23x23mm, 1.27mm	292 PBGA 27x27mm, 1.27mm	516 PBGA 27x27mm, 1mm	516 PBGA 27x27mm, 1mm	324 PBGA 23x23mm, 1mm
Power (Standby)	<1W (10uA)	<2W (50mW)	<1.5W (25uW)	<1.5W (25uW)	<1W (25uW)
Junction Temp	-40C to 95C	-40C to 115C	-40C to 125C	-40C to 125C	-40C to 125C
Silicon Status	Production	Production	Production	Production	Production
Price @ 10Ku Ind	~ $30	$20.95	$23.24	$22.08	*$10.95*

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MPC5125

Robust high-performance Power Architecture™ display solution at a low-cost/power-efficient point with full OS and middleware support.

▶ **Dual 10/100BT Ethernet for bridging solutions**

▶ **Display interface supporting WXGA / 720p, 24-bit color**

▶ **Rich set of connectivity**
- 10x Flexible PSC (SPI, UART, AC'97, I²S, Multi-Ch TDM)
- 4x CAN2.0 A/B , data rates in excess of 1Mbs
- 2x High Speed USB 2.0 Host/Device/On-The-Go
- 2x SDHC (MMC, SD, SDIO expansion)

▶ **Cost-effective / low-power memory systems support**
- Bootable NAND flash interface
  - ECC corrects up to 32 errors (beyond MLC support)
  - Pipelined multi-access/correction/DMA operation
  - Robust booting with x4 redundant boot image scheme
- DRAM interface (high-bandwidth, low-latency)
  - 32/16-bit DDR2 and 32-bit SDR support (low-cost)
  - 32/16-bit MobileDDR support (low-power)

▶ **Low-Power**
- Total system power is typically <1W @400MHz
- Hibernation power down mode <25uW

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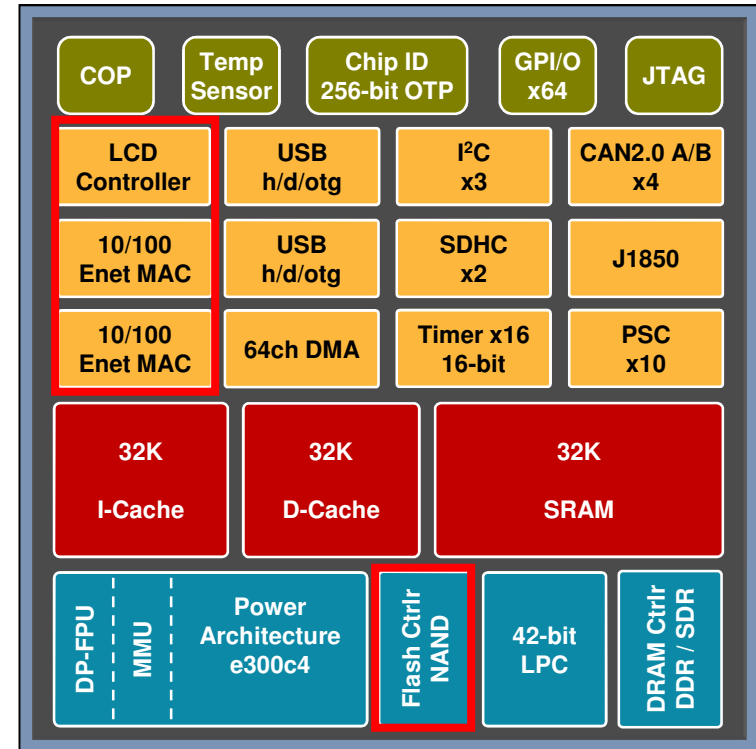
- 800 DMIPS @ 400 MHz
- Packages: 324 PBGA, 23x23mm, 1mm pitch
- In production (industrial/consumer)
- Documentation available on request
- ADS5125 development board $1999
- **TWR-MPC5125 dev system $119 / KIT $169**
- **Price: $10.95 @ 10Ku**

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Robust high-performance Power Architecture™ display solution at a low-cost/power-efficient point with full OS and middleware support.

MPC5121e / MPC5123

▶**Display / processing support**
- Display interface supporting WXGA / 720p, 24-bit color
- Audio / Intelligent DMA acceleration, DSP-C programmable
- OpenGL / OpenVG graphics acceleration (MPC5121e)
- ITU-656 video input

▶**Rich set of connectivity**
- 12x Flexible PSC (SPI, UART, AC'97, I^{2}S, Multi-Ch TDM)
- 4x CAN2.0 A/B, supports data rates in excess of 1Mbs
- 2x High Speed USB 2.0 with 1x PHY Host/Device/On-The-Go
- 1x SDHC (MMC, SD, SDIO expansion)
- 66MHz PCI-2.3 expansion

▶**Cost-effective / low-power memory system support**
- Bootable NAND flash interface
  - ECC corrects up to 4 errors (MLC support)
  - Pipelined access/correction operating at NAND speeds
  - Bootable interface
- DRAM interface (high-bandwidth, low-latency)
  - 32/16-bit DDR2 support (low-cost)
  - 32/16-bit MobileDDR support (low-power)

▶**Low-Power**
- Total system power is typically <1.5W @400MHz
- Hibernation power-down mode <25uW

BUILT ON
Power™
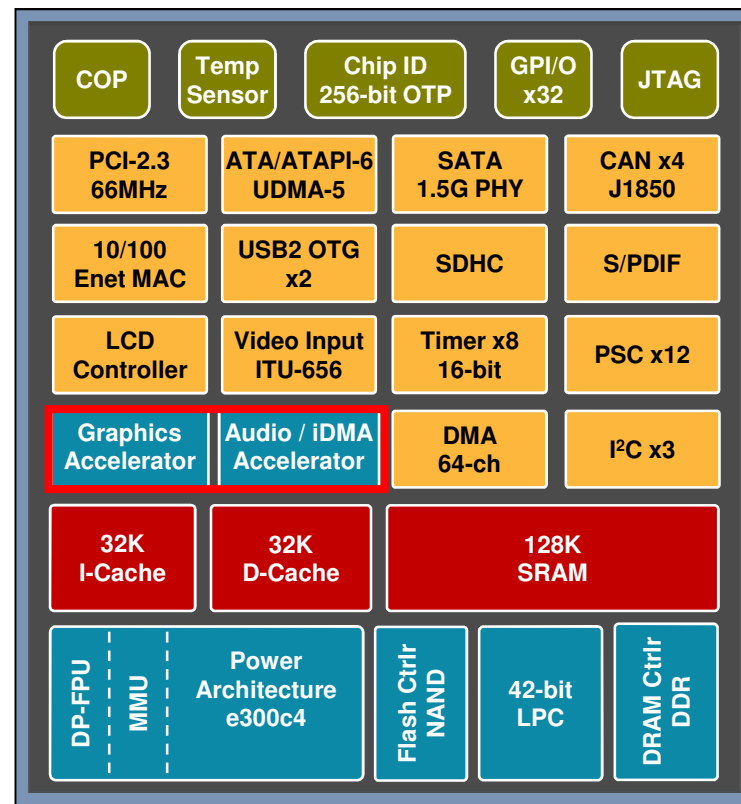
- 800 DMIPS @ 400 MHz
- Packages: 516 PBGA, 27x27mm, 1mm pitch
- In production (industrial/consumer)
- Documentation available on Freescale website
- ADS512101 development board $1999
- **TWR-MPC5121 dev system $139 / KIT $189**
- Price: $23.24(5121e) / $22.08(5123) @ 10Ku

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PowerVR™ MBX Tile Based Deferred Rendering

Immediate Mode Rendering

| Pixel Processing | → | Texturing | → | Hidden Pixel Removal | → | Blending |

Off-chip memory: Texture memory | Z-buffer memory | Frame Buffer memory

Tile Based Deferred Rendering

| Tiling | Hidden Pixel Removal | → | Texturing | → | Blending |

Tile Buffer

Off-chip memory: Tile Data | Texturing
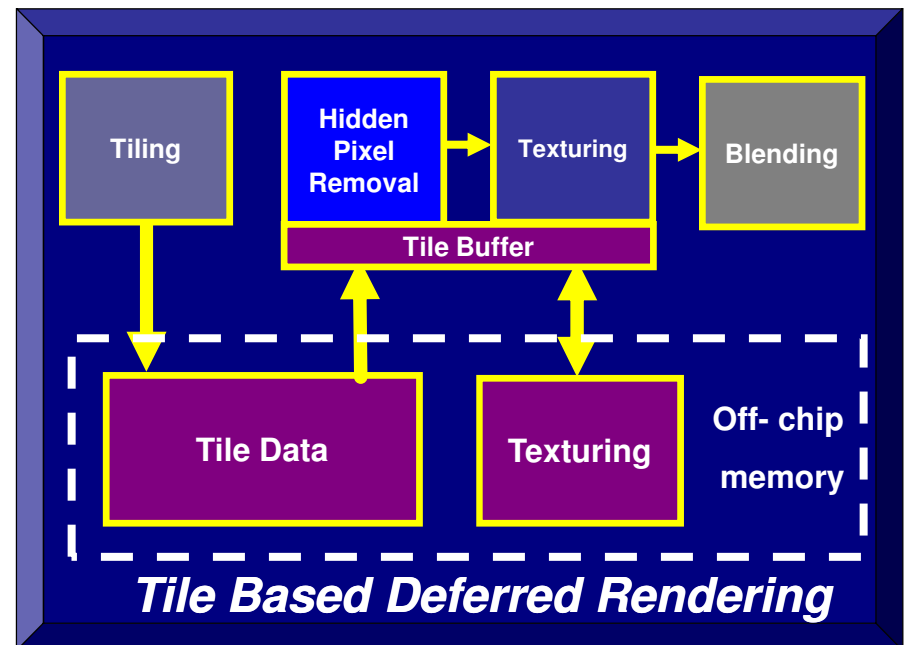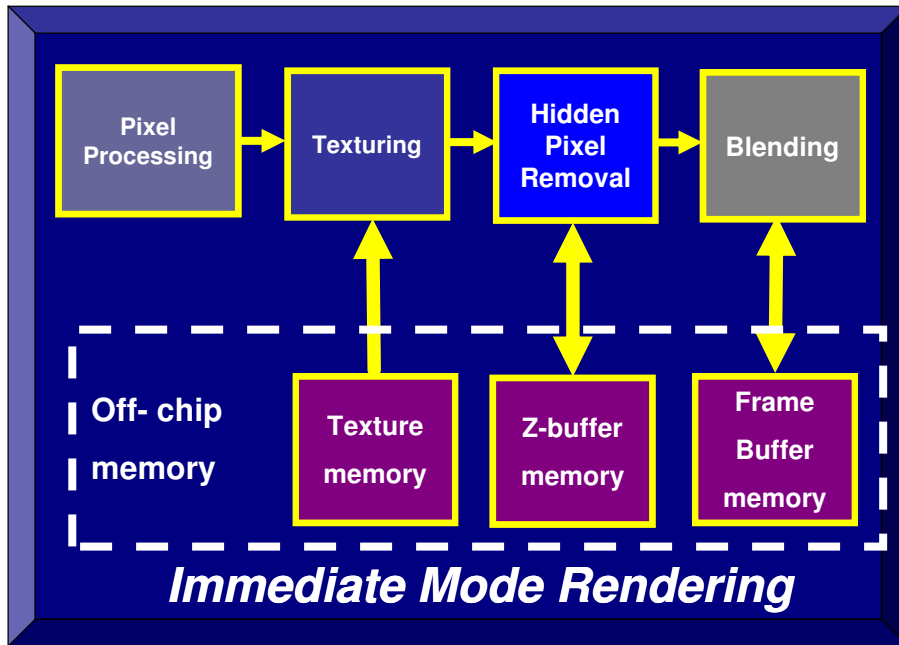
▶ Developed for unified memory embedded systems
- Unnecessary pixel processing is removed early in the rendering process
- Memory intensive pixel processing is confined to a small on chip tile memory

▶ Benefit
- Greatly reduces power and memory bandwidth
- Enables more efficient scalability to higher frame resolutions

Screen Tiling

69

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General Applications:

Robotic Vision, Point-of-sale terminals, Printers,
Military/Aerospace, Single-Board Computers

e600 CPU:

667 MHz – 1.33 GHz e600 CPU

AltiVec vector processor for image processing

256 KB on-chip L2 Cache

Interfaces:

DDR/DDR2 controller, 64 or 32-bit, 400-533 MHz

LCD Controller, 24 bit/pixel, 60 Hz refresh

· SXGA 1280x1024, XGA 1024x768, QVGA 320x240,
WVGA 854x480, SVGA 800x600, VGA 640x480

PCI-Express x 2 ports (x1/x2/x4/x8 and x1/x2/x4)

PCI 2.2, 32-bit, 33/66 MHz

I2C x 2, GPIO x 32 (16 dedicated, 16 multiplexed)

UART x 4ch, 115 kb/s

IrDA x 2ch FIR/SIR, 4 Mb/s

DMA 2 x 4ch, Watch dog timer

SPI

Machine Check external interrupt pin

Local bus, 32-bit, up to 133 MHz

Power, Package, Technology, Schedule:

15W max at 1066 MHz, 105C, 0.95V ➔ fanless

11.5W max at 667 MHz, 105C, 0.95V ➔ fanless

783 PBGA CMOS90SOI NodeC ➔ 6-layer board

Rev 1.0 Samples 2Q07, Production 1Q08

e600 Core — 256K L2 Cache — AltiVec™ Engine

MCP interrupt — MPX Bus

Local Bus 32bit | PIC (Timer x4) | MPX Coherency Module | Queue | 64/32b DDR/DDR2 SDRAM Controller

2 x DMA 4 ch each

2x I2C WDT 32x GPIO | SPI UART 4ch IrDA 2ch | LCD Controller (DIU) | X | X

PCI Exp x1/2/4/8 | PCI Exp x1/2/4 | PCI 32bit 33/66MHz

Execution

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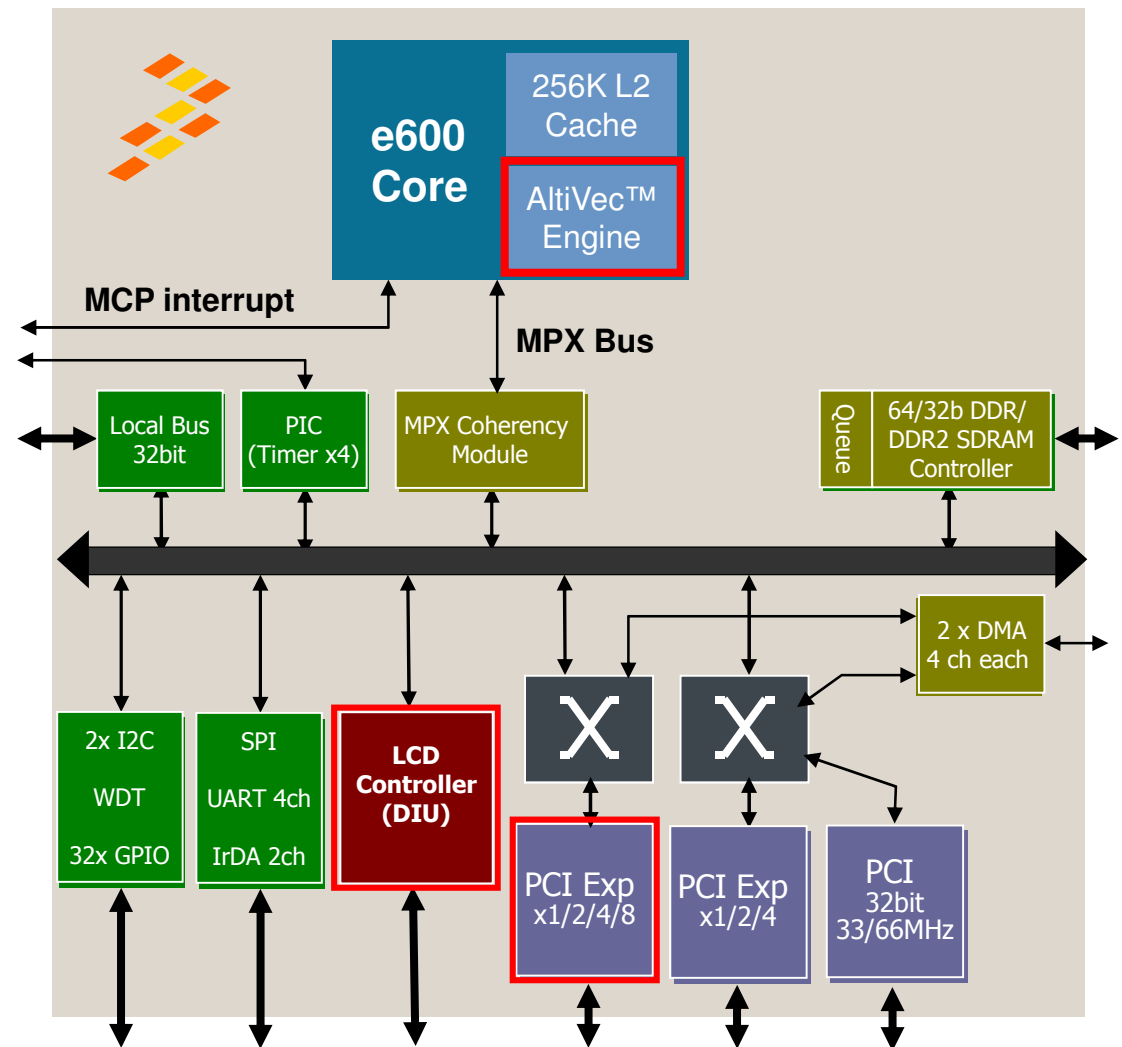
QorIQ™ P1022/13 Processor
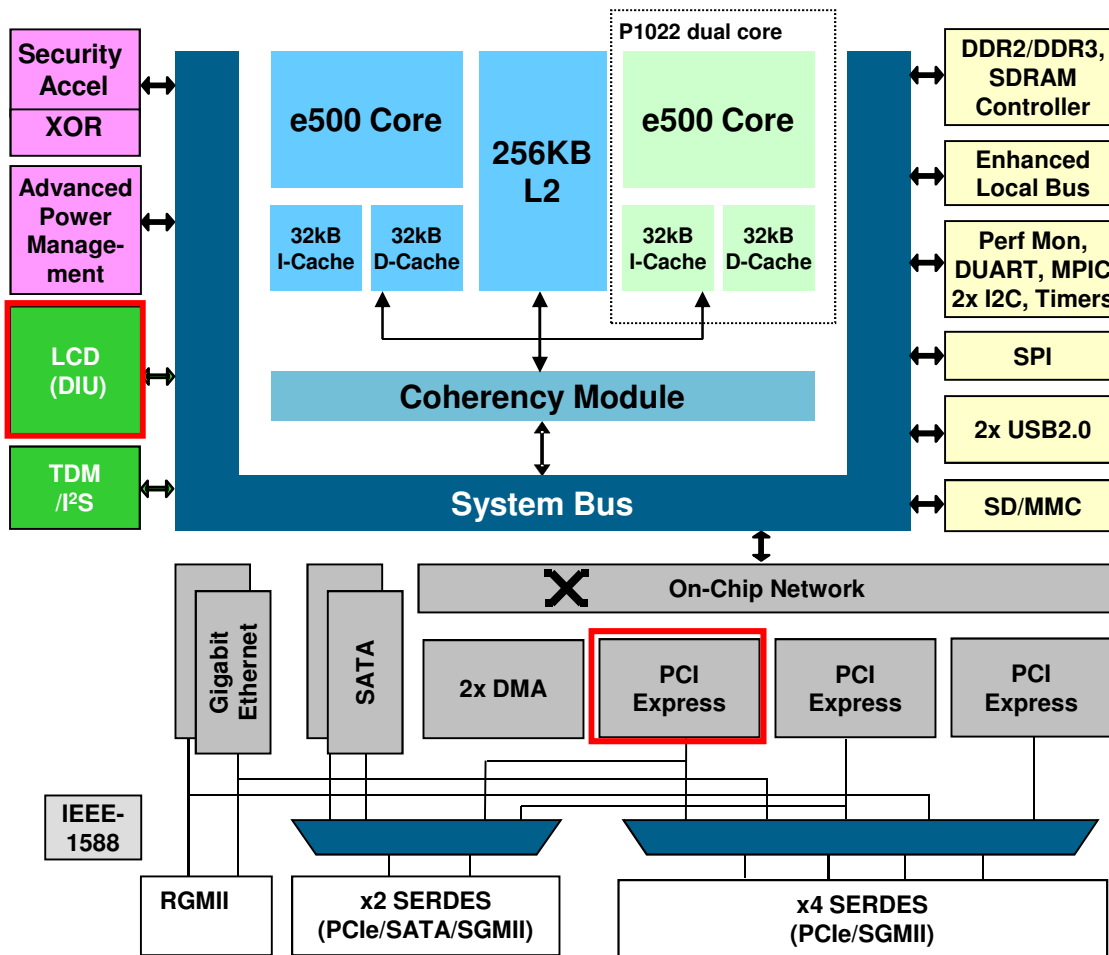
▶ **Scalable Processing Performance**
- Single/Dual e500v2r5
- Up to 1.067GHz operation
- High Speed DDR2 and DDR3 (667MHz)
- HW math and secure networking acceleration

▶ **Low System Cost**
- Integrated system peripherals
  - Dual USB 2.0   SD/MMC
  - Dual SATA   Dual Gigabit Ethernet
  - LCD   Audio /VoIP TDM
- Low cost 6 layer PCB layout

▶ **High Speed Serial Interconnect**
- 3 PCI Express Controller (6 lanes)
- High Speed SPI
- SGMII

▶ **Green Energy Operation**
- Fanless dynamic <2.75W core power
  (dual core 1GHz + logic, typ., est.)
- Packetlossless deepsleep for EnergyStar™ support
  - <200mW deepsleep @35C (typ., est.)
  - Programmable wake-on-packet ;
  - Wake-on-timer/GPIO/USB/IRQ

▶ **Process & Package**
- 45nm, 1.0V+/-50mV
- 689 pin TePBGAII
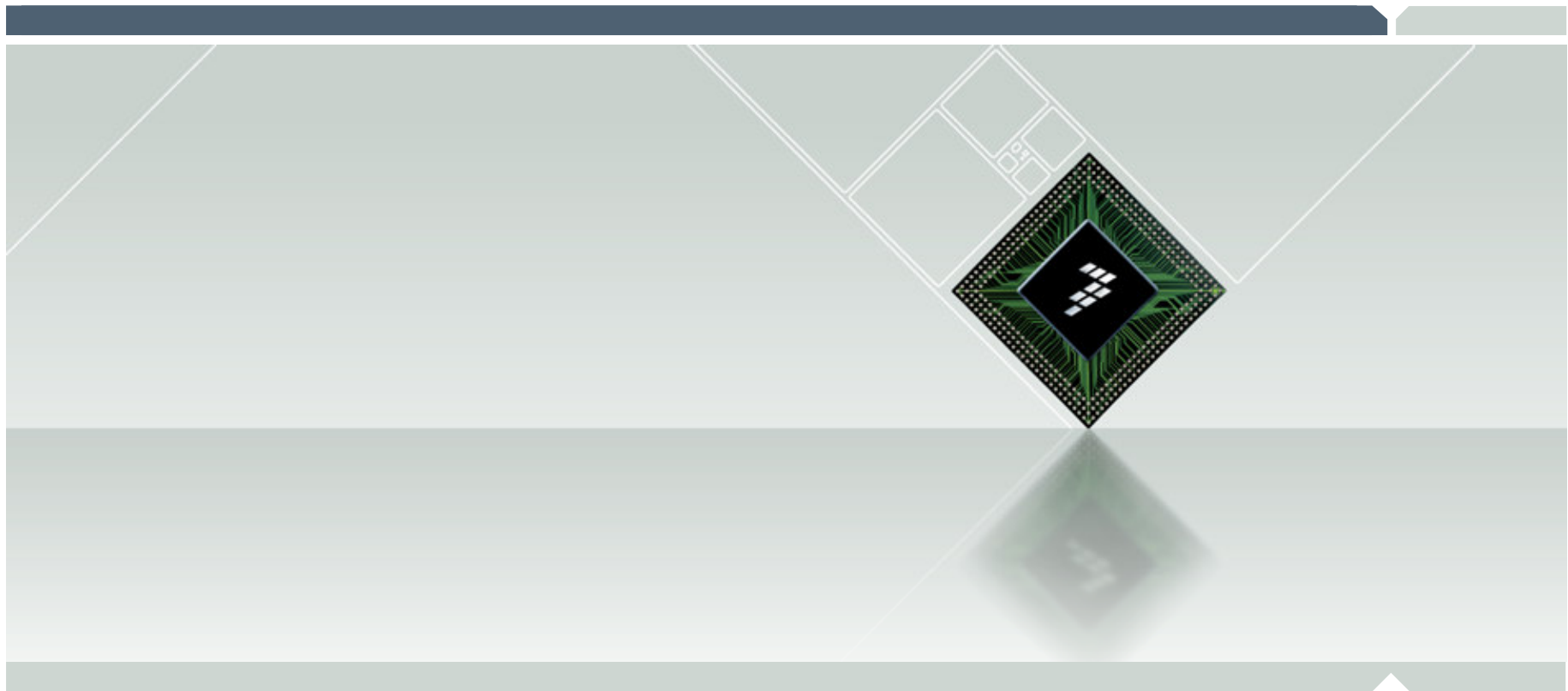
Freescale Display Enabled Products

ARM® MPU i.MX Products

Freescale Applications Processor Value Proposition

► Performance (MHz & Memory Efficiency)

► Low Power (Audio < 18 mW system, HD720 Video < 250 mW)

► State of the art Audio, Video, Graphics and Codecs

► Consistent and scalable architecture

► Complete OS/SW platform

► Mixed signal integration
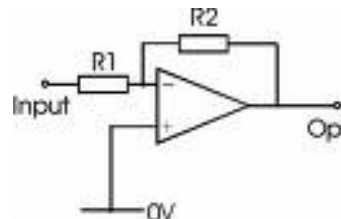
i.MX Industrial & General Embedded Roadmap

Cortex A8

ARM11

ARM9

Associated PMIC: MC13892

i.MX515
- Open VG
- OpenGL ES 2.0
- Security

i.MX5x

i.MX5x

i.MX5x

i.MX5x

i.MX357
- Open VG 1.1

i.MX513
- 720p Video Decode
- D1 Video Encode

i.MX353
- ARM1136, 532 MHz
- Ethernet, DDR2
- USB Phy x 2, CAN x 2

i.MX512
- Cortex A8, 800MHz
- Ethernet, DDR2, USB Phy

Associated PMIC: MC13783

i.MX31
- OpenGL ES 1.1 3D

i.MX31L
- ARM1136, 400 MHz
- USB (High Speed)

i.MX258
- Security

Associated PMIC: MC34704B

i.MX27
- D1 Video Encode
- D1 Video Decode

i.MX257
- Touchscreen
- CAN x 2

i.MX27L
- ARM926, 400MHz
- Ethernet

i.MX253
- ARM926, 400MHz
- Ethernet, DDR2
- USB Phy x 2

i.MX233
- ARM926, 450MHz
- Touchscreen
- Integrated PM, Audio

i.MX2x

i.MX2x

i.MX2x

2009   **2010**   **2011**

74

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i.MX35 Applications Processor

▶ Specifications

CPU: ARM1136JF-S, 400/532 MHz
   Process: CMOS90LP
Core Voltage 1.22-1.47V@400MHz, -40/85C, TBD@532 MHz
Package: 400 ball 0.8mm BGA

▶ i.MX35 Value Proposition

Same high performance CPU complex as i.MX31

Enhancements from the i.MX31

- IPU - Image Processing Unit supporting 24-bit WVGA
- OpenVG vector graphics processor (i.MX356)
- Enhanced Audio Peripherals – Multi-channel audio, S/PDIF, sample rate conversion
- Flexible Memory Support
  - SDRAM 16/32 bit, 133 MHz
  - DDR2 16/32 bit, 266MHz
  - SLC/MLC NAND
- Connectivity enhancements
  - CAN (x2) and MLB (MOST)
  - USB PHY integration
  - 10/100 Ethernet

Block Diagram — i.MX356

System Control
- JTAG, ETM
- Bootstrap
- System Reset
- PLL & Power Mgmt

Multimedia & Human Interface
- 8x8 Keypad
- ASRC
- OpenVG 1.1 2.5D Accel.
- Image Processing Unit Inversion and Rotation
- Pre & Post Processing
- Camera I/F
- Blending
- Display Ctrl

CPU Complex
- ARM1136 CPU
- Smart Speed Switch (MAX)
- 16KB i-cache
- 16KB d-cache
- 128KB L2-cache
- 32KB Boot ROM 2KB Secure RAM
- 128KB SRAM
- Vector Floating Point Unit

Special Functions
- Security HW

External Memory
- SDRAM mSDRAM mDDR DDR2 NOR SLC NAND MLC NAND

Standard System I/O
- sDMA
- 3 x Timers
- PWM
- WD Timer
- RTC
- GPIO

Connectivity
- 2 x CSPI
- 2 x SSI/I²S
- ESAI
- 3 x I²C
- 3 x UART
- USB HS Host FS-PHY or ULPI
- USB HS OTG w/ HS-PHY
- S/PDIF I/O
- 2 x FlexCAN
- MLB
- Ethernet
- 1-Wire
- 2 x SDIO/MMC
- SDIO/ Memory Stick
- PATA
- CE-ATA

Legend: ■ Inherited from i.MX31   ■ New or enhanced from i.MX31

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i.MX35 Enabling an Efficient and Rich UI

▶ **Low platform cost impact from graphics**

- Graphics hardware should not significantly add to platform cost beyond the added value

▶ **Simple driver layer**

- Small memory footprint
- Low CPU impact
- Easy integration

▶ **Low power consumption**

▶ **Easily approachable development path**

▶ **Ability to utilize legacy content**

▶ **Easy-to-integrate UI software layer**

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i.MX51 Family Applications Processor

Specifications:

- **CPU:** Cortex A8, up to 800MHz
- **Process:** 65nm, LP/GP
- **Core Voltage:** 0.8-1.15V
- **Package:** 19x19 0.8mm
- **Temp Range:** -20 to 70C* (consumer)
  -40 to 85C* (industrial)
  -40 to 85C* (Auto)

* See Datasheet for case/junction temperatures

Key i.MX515 Features and Advantages

- High performance CPU: Cortex A8
- Low power multimedia
- Delivers rich graphics and UI in HW
  - OpenGL ES 2.0 3D accelerator (AMD Z430)
  - OpenVG 1.1 graphics accelerator (AMD Z160)
  - Neon Vector floating point co-processor
  - Display up to WXGA
- Drives high resolution video in HW
  - Multi-format D1 video encode
  - Multi-format HD720 video decode
- Mixed signal integration - HD720 TV out and high speed USB with embedded PHY

Available Parts

- i.MX512, i.MX513, i.MX514, i.MX515, i.MX516

Availability:

- **Market:** Consumer, Industrial & Auto
- **Sample:** Now
- **Production:** Now (C, April 10 A) May 10 (I)

i.MX51

System Control
- Secure JTAG
- Power Mgmt
- PLL x 3
- Clock Reset

Timers
- Timer x3
- PWM x2
- Watch Dog

Memory
- ROM 32KB
- RAM 128KB

Security
- Sahara v4
- TrustZone®
- RTIC
- SCC v2
- SRTC

CPU Platform
- ARM Cortex™-A8
- 32KB i-cache
- 32KB d-cache
- 256KB L2-cache
- Neon
- ETM
- Vector Floating Point Unit

Multimedia
- OpenGL ES 2.0
- OpenVG1.1
- HW Video Codecs
- HD720 TV-Out

Imaging Processing Unit
- Display Controller
- Resizing & Blending
- Inversion / Rotation
- Image Enhancement
- Camera

Connectivity
- Fast IrDA
- HS MMC/SDIO x4
- CSPI HS x2 / LS x1
- UART x3
- I²C x3
- SSI/I²S x3
- 1-Wire
- ATA-6
- USB OTG HS+PHY
- USB HS Host x3
- SPDIF Tx
- GPIO
- Keypad
- Ethernet
- Ext Memory I/F mDDR 200 MHz DDR2 200 MHz

eFUSES   **Smart DMA**

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i.MX51 Graphics

▶ **Native OpenGL ES 2.0** 3D based on ATI/AMD Unified Shader Architecture

- **Same architecture** and **same content tools** as in **Xbox 360** and AMD's PC graphics chips

- Licensed by several industry leaders, providing for a strong foundation for a content creation ecosystem

- Binning architecture provides for low memory/power requirements

- 27 M triangles / sec

- 166 M pixels / sec raw performance (1 pixel / clock)
  - 500 M pixels / sec (effective w/ 3x overdraw)

▶ **A native OpenVG 1.1** 2D hardware implementation

- Driving high-quality UIs and Flash based internet browsing with extremely low power consumption

- Free 16x antialiasing for very high-quality fonts and graphics

- Capable of delivering a full 3D user interface experience beyond anything on the market today with a fraction of the power consumption compared to any other solution

- 166 M pixels / sec raw performance (1 pixel / clock)

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i.MX51 Applications Processor

System Control	Cortex A8 ARM-based CPU	Connectivity
Timers	SIMD/Neon	
	Vector Floating Point Unit	
Memory	**Video Processing Unit**	
Security	Image Processing Unit	
	2D Graphics	3D Graphics
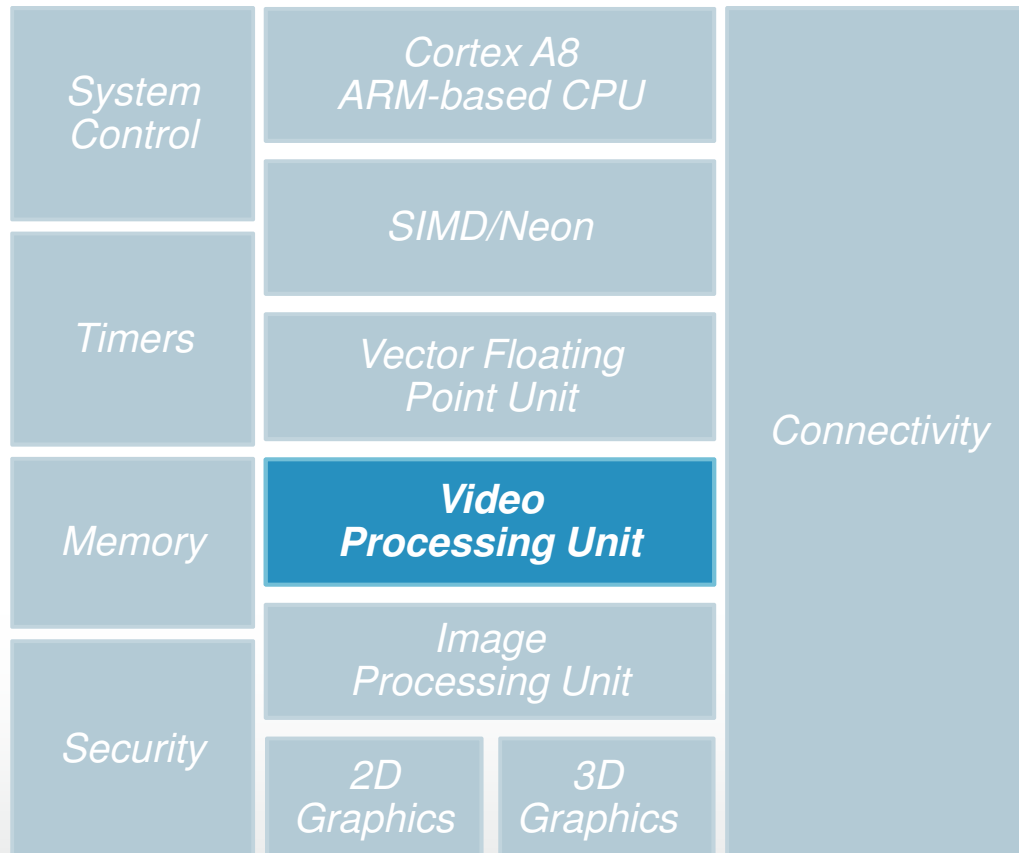
Video Processing Unit

- ▶ Multi-standard video playback/record
- ▶ Video telephony
- ▶ Video transcoding
- ▶ You Tube, Skype, Hulu

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i.MX233 Applications Processor

▶ **Key Features and Advantages**

- 454MHz ARM926EJ-S core
- Based on Sigmatel IP platform
- PMU with high efficiency on-chip DC/DC with 4.2V output, supports Li-Ion batteries
- LCD Controller with Touchscreen
- 1.5W Mono speaker amplifier
- Stereo headphone DAC w/ 99dB SNR & Stereo ADC w/ 85 dB SNR with integrated amplifiers
- NAND support – SLC/MLC and managed
- Hardware BCH (up to 20-bit correction) and RS ECC8 for current and future MLC NAND support
- DDR1 Support with integrated 2.5V regulator
- High speed USB with embedded PHY

▶ **Package and Temperature**

- 169fpBGA 11x11mm .8mm
- 128LQFP 14x14mm
- -10 to +70C (Consumer)
- -40C to +85C (Industrial)

	128 LQFP	169 BGA
UART	2	3
12-bit ADC	2	6
PWM	3	5

Standard Connectivity
- I²C
- SPI x 2
- UART
- 12-bit ADC
- HS USB Phy
- GPIO

Audio
- I²S x 2
- S/PDIF Tx
- 1.5W Mono Speaker Amp
- Stereo ADC/DAC with Amp

Multimedia
- 10-bit Video DAC
- PAL/NTSC Analog TV Encoder

Power Management
- DC/DC – 4.2V
- LD0 x 4
- Battery Charger

i.MX233 ARM926EJ-S 454MHz

16K I Cache **16K D Cache**

Security
- DRM Unique ID
- OTP AES Key
- 128-bit AES
- SHA-1 Hashing

Standard System
- Timer x 4
- PWM x 5
- Watch Dog
- DMA

System Debug
- ETM
- SJTAG

Ext Memory I/F
- NAND
- BCH 20-bit
- ECC8
- DDR1
- mDDR

Internal Memory
- 32KB SRAM
- 64KB ROM

Ext Storage
- MMC⁺/SD x 2

User I/F
- LCD Controller
- Touchscreen
- Scaling
- Alpha Blending
- Rotation
- Color Space Conversion

■ Not available in QFP package

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80
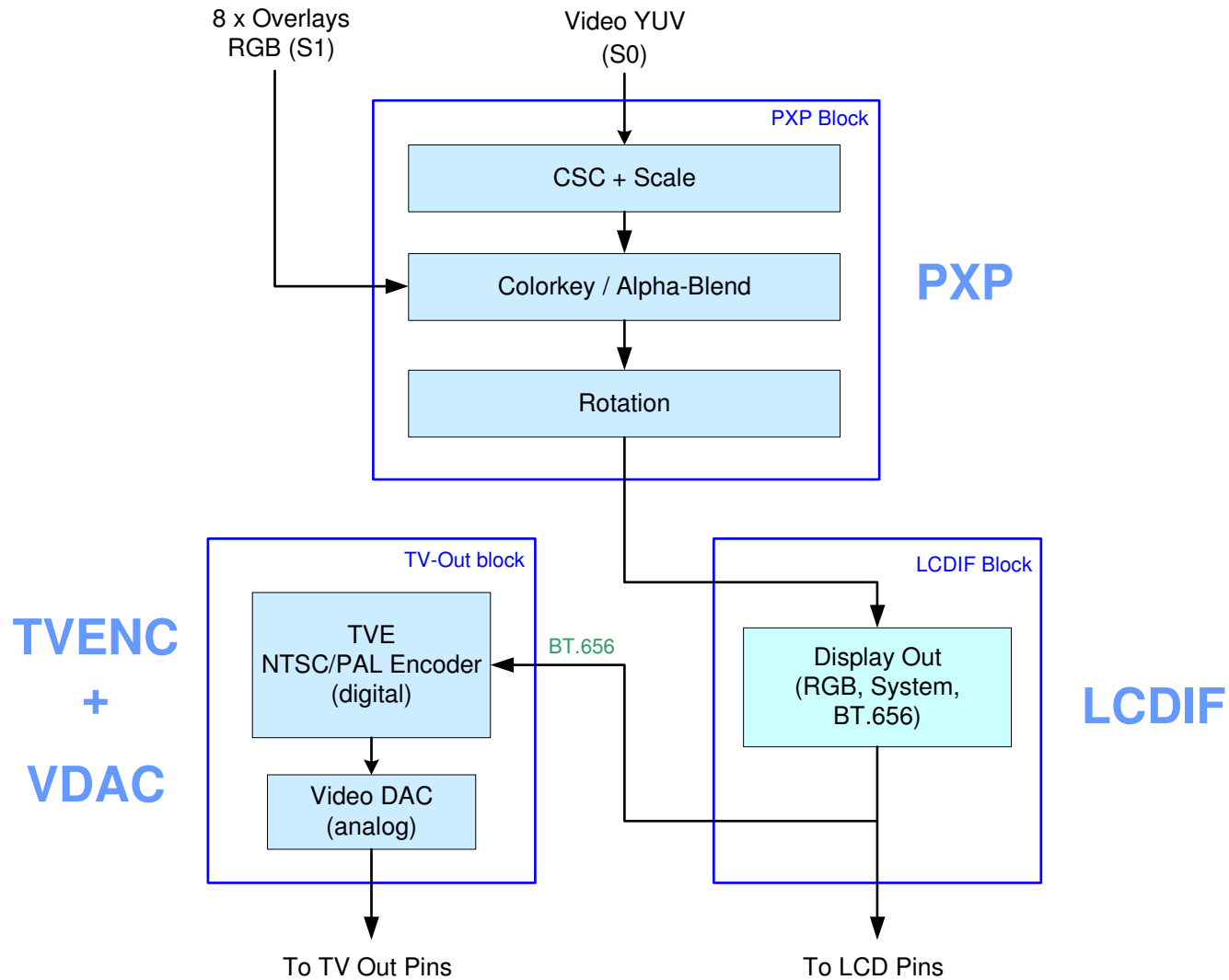
▶ PiXel Pipeline

- Bi-linear YUV/YCbCr scaling and color space conversion, rotation
- Multiple graphic overlays (BITBLT) with concurrent alpha blending and color keying
- Processes 8x8 blocks, and linked commands

4 source image pixel:
p00, p10, p01, p11

Ry

(1-Ry)

1 destination image pixel:
P, bilinear filter

Overlay → S1

RGB

Y
U
V → Scaler → CSC → S0

S1 → alpha blending/ color key → S3 → rotation

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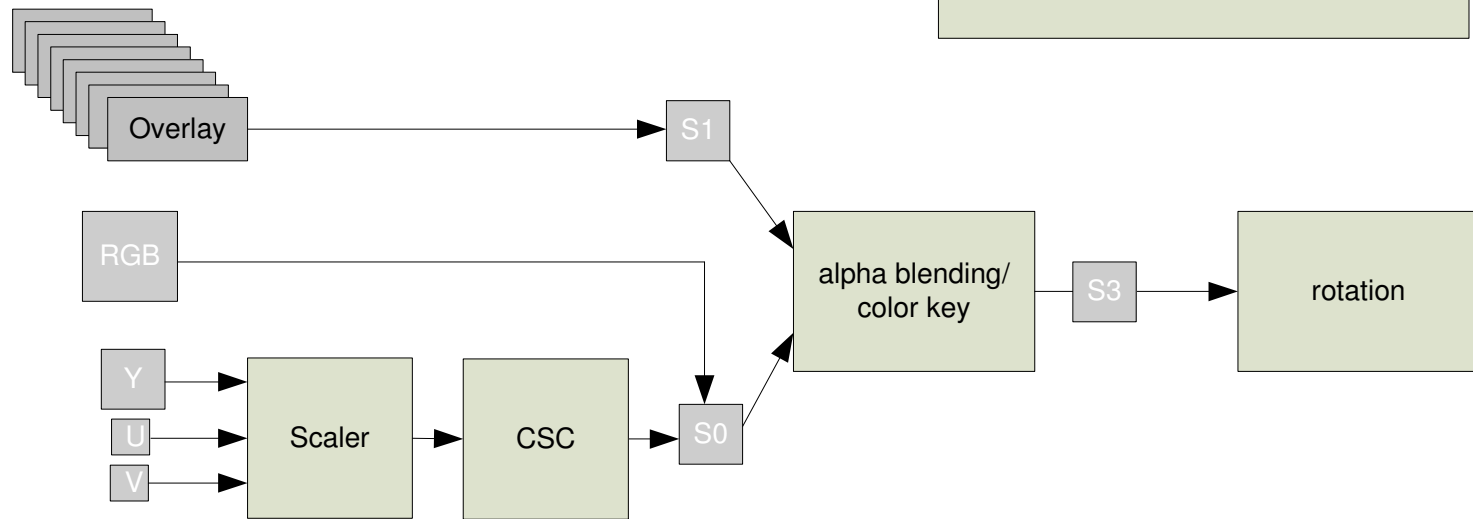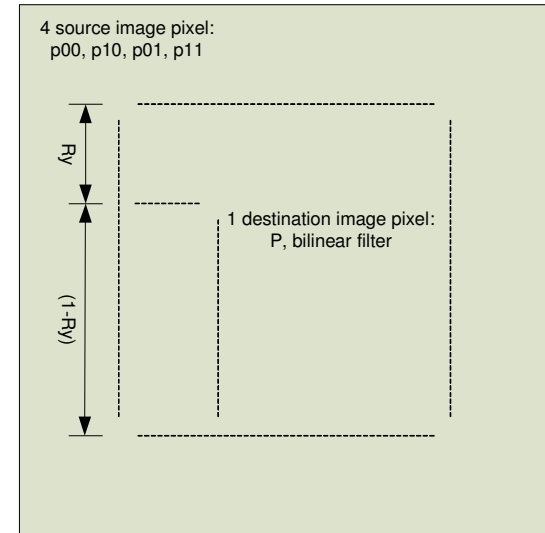
▶ Display Controller (LCDIF)

- Up to 24-bit DOTCLK, system-mode, VSYNC with programmable timings.

- On-the-fly RGB->YCbCr 4:2:2 for ITU-R/BT.656 DV interface (with interlacing)

- Rich support for RGB formats including pixel packing and swizzling.

- 128-pixel FIFO provides robustness for up to VGA resolution at 60Hz.

- AXI Master for efficiency

- Direct internal connection to TVE

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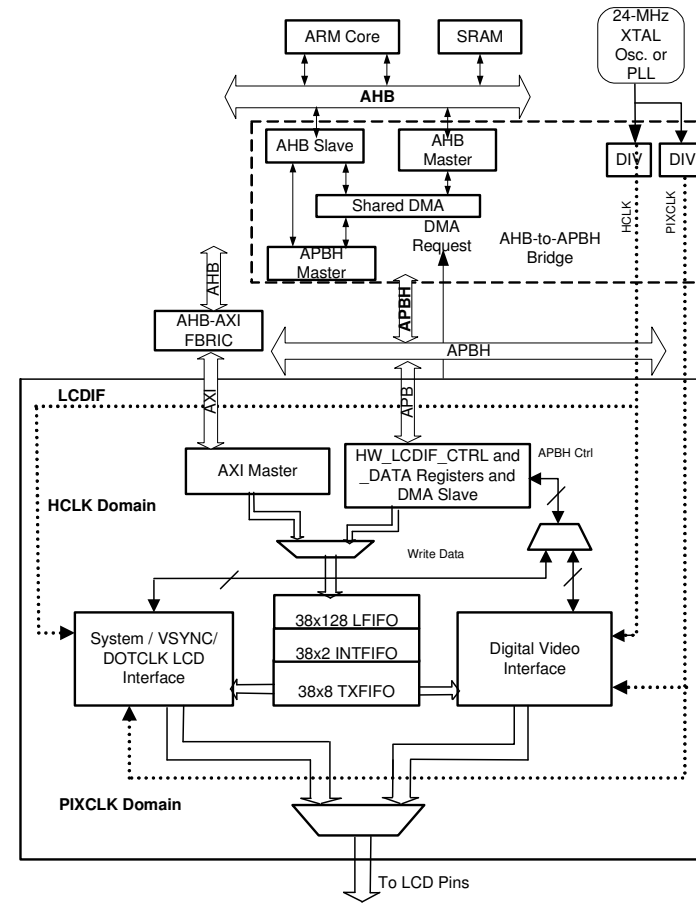
► **Key Features and Advantages**
- 400MHz ARM926EJ-S™
- 16KB L1 I-Cache, 16KB L1 D-Cache
- 128KB on-chip SRAM for low power LCD refresh
- External memory interface supports DDR2, mDDR, or SDRAM up to 133MHz, 16-bit data bus
- Supports off-chip NAND or NOR Flash
- 10/100 Ethernet MAC with RMII support
- USB 2.0 OTG 480Mbps with high-speed PHY
- USB 2.0 Host 480Mbps with full-speed PHY or ULPI
- Two CAN interfaces
- Two Smartcard interfaces
- SDIO interface for external Wi-Fi module
- VGA (640x480) LCD controller
- Resistive touchscreen controller
- CMOS sensor interface
- P-ATA for external CD connection or HDD
- CE-ATA and SD/MMC+ for external storage
- Enhanced serial audio interface
- 3 general purpose 12-bit ADC channels
- UART's, CSPI's, I2C, I2S
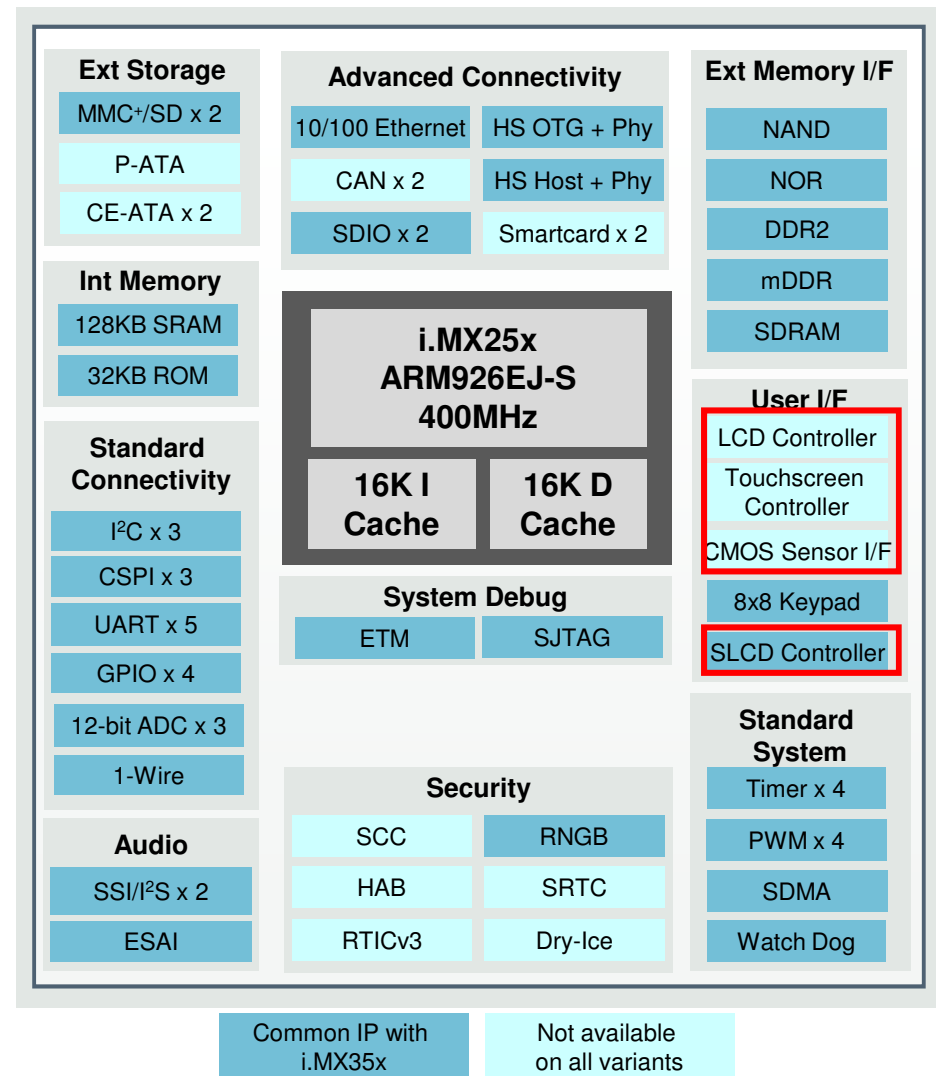- Enhanced security features, including tamper detection for voltage, frequency and temperature
- High-Assurance Boot (HAB)
- 3.3V I/O reduces external component count

► **Available Parts**
- i.MX251, i.MX255, i.MX253, i.MX257, i.MX258

► **Package and Temperature**
- 0.8mm, 400-pin MAPBGA
- -20C to +70C, -40C to +85C temperature options
- AEC-Q100 Grade3 Qualification

Ext Storage
- MMC+/SD x 2
- P-ATA
- CE-ATA x 2

Int Memory
- 128KB SRAM
- 32KB ROM

Standard Connectivity
- I²C x 3
- CSPI x 3
- UART x 5
- GPIO x 4
- 12-bit ADC x 3
- 1-Wire

Audio
- SSI/I²S x 2
- ESAI

Advanced Connectivity
- 10/100 Ethernet
- CAN x 2
- SDIO x 2
- HS OTG + Phy
- HS Host + Phy
- Smartcard x 2

i.MX25x ARM926EJ-S 400MHz
- 16K I Cache
- 16K D Cache

System Debug
- ETM
- SJTAG

Security
- SCC
- HAB
- RTICv3
- RNGB
- SRTC
- Dry-Ice

Ext Memory I/F
- NAND
- NOR
- DDR2
- mDDR
- SDRAM

User I/F
- LCD Controller
- Touchscreen Controller
- CMOS Sensor I/F
- 8x8 Keypad
- SLCD Controller

Standard System
- Timer x 4
- PWM x 4
- SDMA
- Watch Dog

Common IP with i.MX35x

Not available on all variants

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i.MX27(L) Applications Processor

►Specifications:

- CPU: ARM926EJ-S, 400MHz
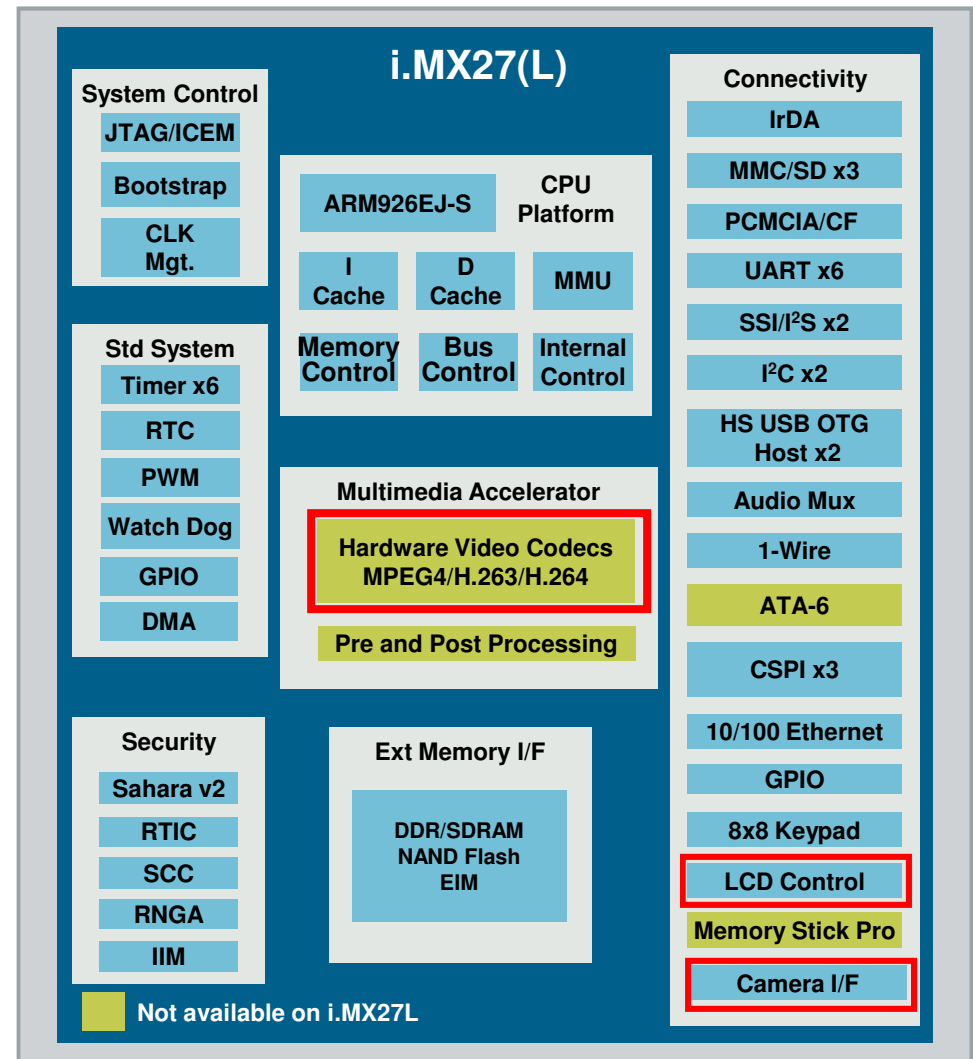- Process: 90nm
- Core Voltage: 1.2-1.5V

IP cameras

►Key i.MX27 Features and Advantages

- 16 KB L1 I-Cache and D-Cache
- 16-channel DMA
- Multi-standard video codecs at D1 resolution (i.MX27 only)
  - Video pre- and post-processing, scaling
- Security
  - Crypto Accelerator
  - Security controller with encrypted RAM storage
  - Electronically blown fuse box
  - High-assurance boot
- Real-time OS/SW integrity checker
- Dynamic Process temperature Compensation (DPTC)
- Connectivity
  - Ethernet 802.3 MAC
  - USB 2.0 OTG 480Mbps
  - USB 2.0 Host 12Mbps, USB 2.0 Host 480Mbps
  - PCMCIA/CF, Audio MUX
  - MMC, SD, IrDA, 8x8 keypad, CMOS sensor interface
  - ATA-6, Memory Stick (i.MX27 only)

►Availability:

- Package types
  - 404-ball, 17x17, MAPBGA, 0.65mm pitch
  - 473-ball, 19 x 19, MAPBGA, 0.8mm pitch,
    - Extended temp -40 to 85C & qual'd for greater than 10 years operating life at 100% duty cycle

i.MX27(L)

System Control
- JTAG/ICEM
- Bootstrap
- CLK Mgt.

CPU Platform
- ARM926EJ-S
- I Cache
- D Cache
- MMU
- Memory Control
- Bus Control
- Internal Control

Std System
- Timer x6
- RTC
- PWM
- Watch Dog
- GPIO
- DMA

Multimedia Accelerator
- Hardware Video Codecs MPEG4/H.263/H.264
- Pre and Post Processing

Security
- Sahara v2
- RTIC
- SCC
- RNGA
- IIM

Ext Memory I/F
- DDR/SDRAM NAND Flash EIM

Connectivity
- IrDA
- MMC/SD x3
- PCMCIA/CF
- UART x6
- SSI/I²S x2
- I²C x2
- HS USB OTG Host x2
- Audio Mux
- 1-Wire
- ATA-6
- CSPI x3
- 10/100 Ethernet
- GPIO
- 8x8 Keypad
- LCD Control
- Memory Stick Pro
- Camera I/F

Not available on i.MX27L

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i.MX31 Applications Processor
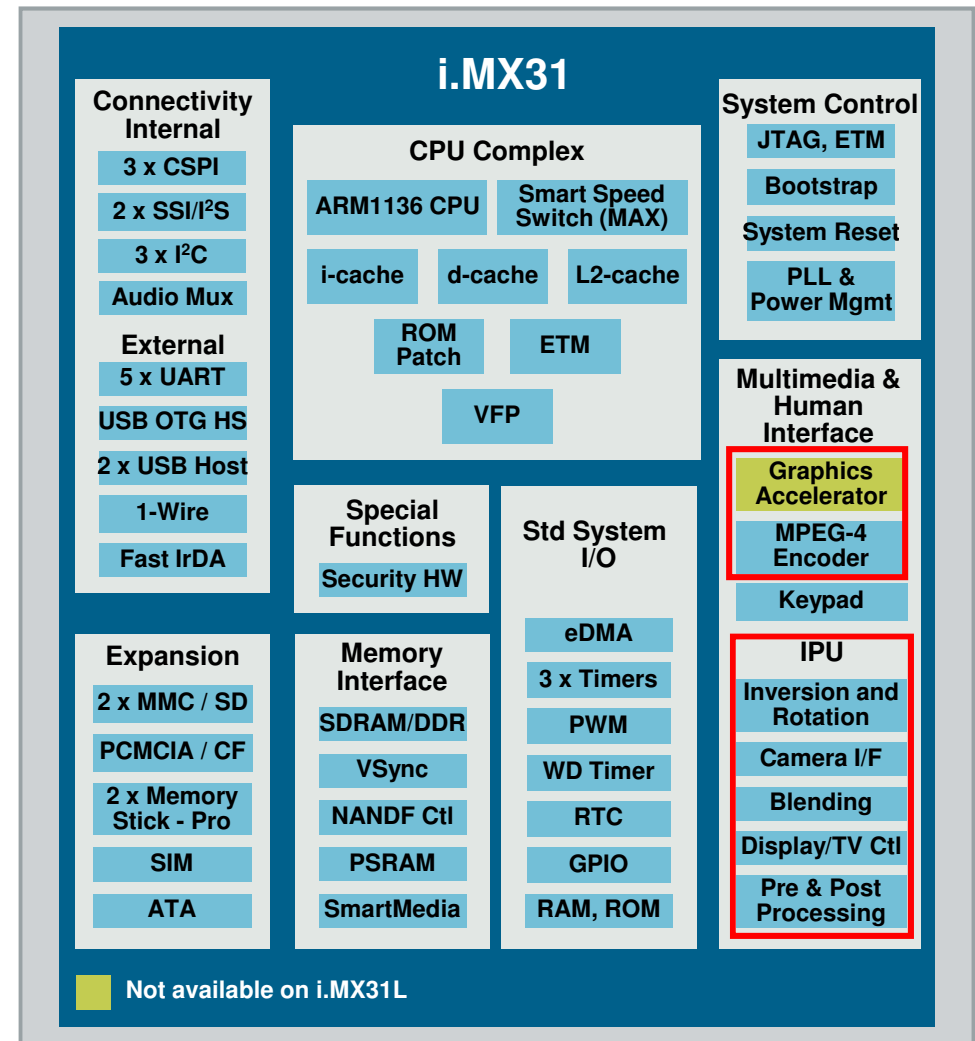
▶ **Specifications:**
- CPU: ARM1136, 532MHz, **400 MHz Auto**
- Process: 90nm
- Core Voltage: 1.2-1.6V

▶ **Key i.MX31 Features and Advantages:**
- ARM1136 with 128 KB L2 Cache
- Integrated 3D graphics processor
  - Eliminates 2 chip solution
- Integrated HW Image Processing Unit (IPU)
  - CMOS/CCD Interface
  - Resize, CSC, Deblock, Dering, Blending
- Vector Floating Point Co-Processor (VFP)
- Smart DMA RISC-based DMA controller
- Connectivity
  - WLAN, BT, GPS via external chipset
  - HS USB, ATA-6, MMC/SDIO, MS-Pro, Compact Flash
  - 266MHz Mobile DDR, NAND/NOR, Mobile SDRAM, SRAM
- Scale - shipped multi-million units
- Breadth – design wins in PMP, PND, Cellular, IP Telephony, POS terminals

▶ **Availability:**
- Shipping Now
- Package types
  - 14x14 MAPBGA 0.5mm pitch
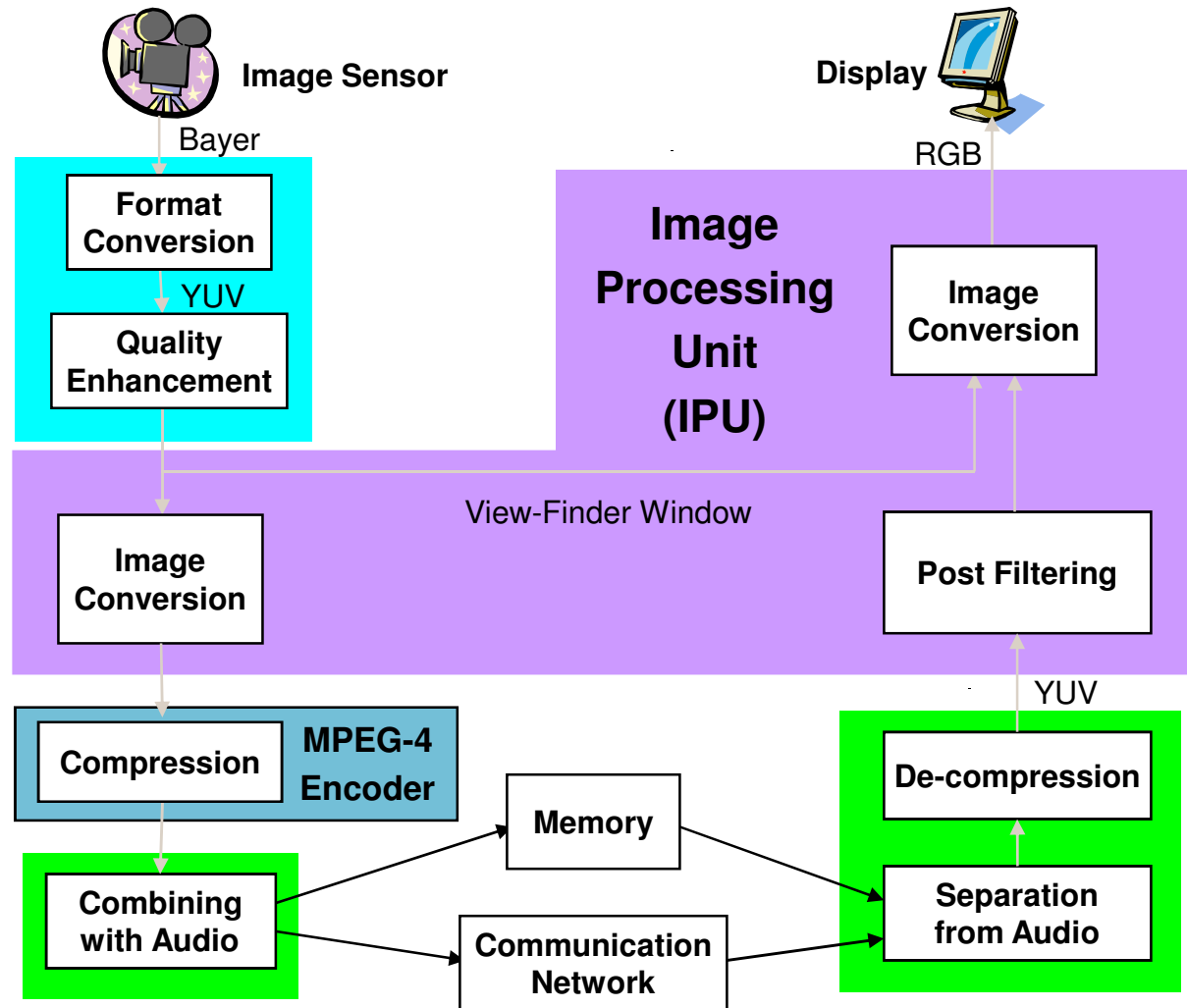 - 19x19 MAPBGA 0.8mm pitch
- 2007 10K re-sale pricing $16.69 - $24.86

i.MX31 (block diagram)

Connectivity

Internal
- 3 x CSPI
- 2 x SSI/I²S
- 3 x I²C
- Audio Mux

External
- 5 x UART
- USB OTG HS
- 2 x USB Host
- 1-Wire
- Fast IrDA

CPU Complex
- ARM1136 CPU
- Smart Speed Switch (MAX)
- i-cache
- d-cache
- L2-cache
- ROM Patch
- ETM
- VFP

Special Functions
- Security HW

Std System I/O
- eDMA
- 3 x Timers
- PWM
- WD Timer
- RTC
- GPIO
- RAM, ROM

System Control
- JTAG, ETM
- Bootstrap
- System Reset
- PLL & Power Mgmt

Multimedia & Human Interface
- Graphics Accelerator
- MPEG-4 Encoder
- Keypad

IPU
- Inversion and Rotation
- Camera I/F
- Blending
- Display/TV Ctl
- Pre & Post Processing

Expansion
- 2 x MMC / SD
- PCMCIA / CF
- 2 x Memory Stick - Pro
- SIM
- ATA

Memory Interface
- SDRAM/DDR
- VSync
- NANDF Ctl
- PSRAM
- SmartMedia

■ Not available on i.MX31L

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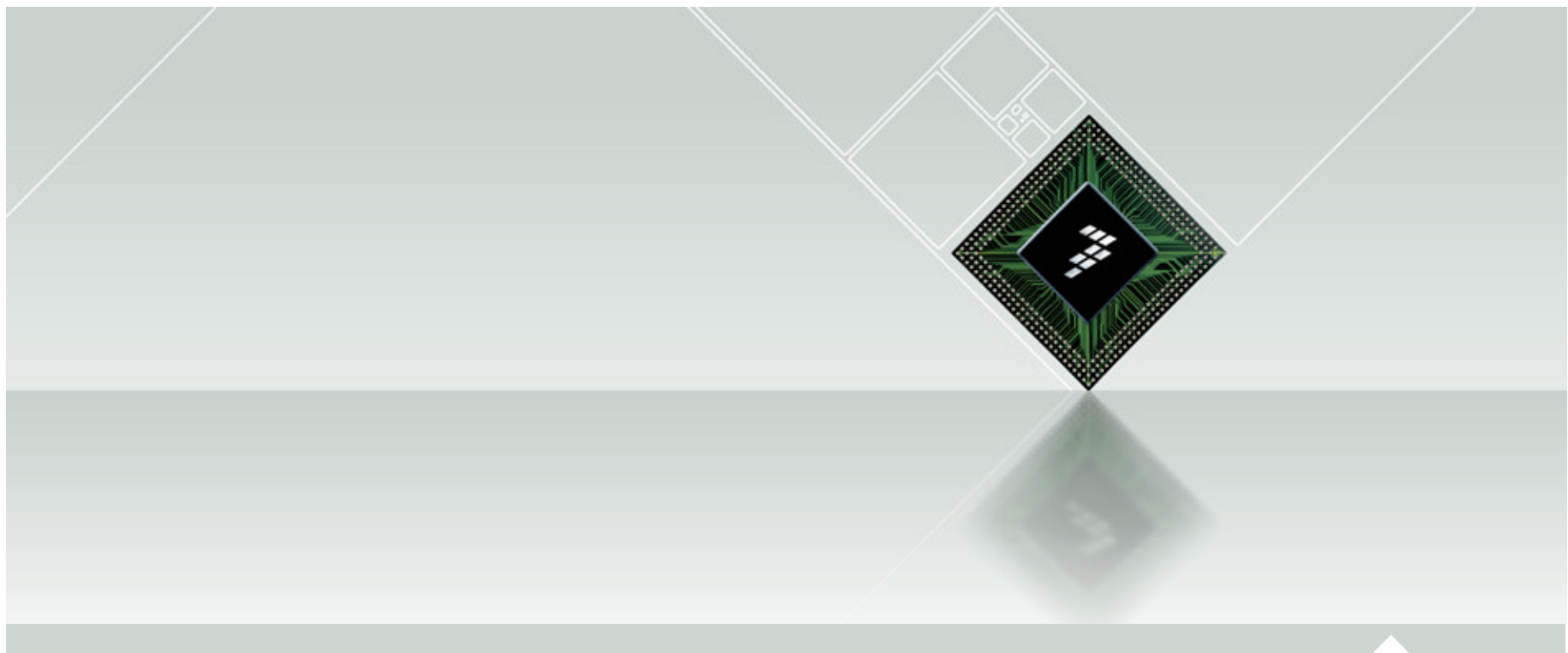semiconductor

Video Processing Implementation

Performed by:

- **Camera (Image Signal Processing) (or ARM11 SW)**
- **Image Processing Unit in i.MX31**
- **MPEG4 Encoder in i.MX31**
- **ARM11 SW**

Image Conversion:

► Resizing (resolution adjustment)
► Rotation & Inversion
► Pixel format conversion (color space, packing…)
► Combining with a graphics overlay

Image Sensor

Bayer

Format Conversion

YUV

Quality Enhancement

Image Conversion

Compression   **MPEG-4 Encoder**

Memory

Combining with Audio

Communication Network

Display

RGB

Image Processing Unit (IPU)

Image Conversion

View-Finder Window

Post Filtering

YUV

De-compression

Separation from Audio

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Freescale Display Enabled Products

8-Bit S08 & 32-Bit ColdFire MCU Segment Drivers

► Extensive roadmap

- Segment drivers
    - RS08 - low-cost MCUs
    - S08 - ultra low-power MCUs
    - ColdFire - low-power pin-compatible 32-bit MCUs
- LCD drivers
    - ColdFire - low-cost MPUs
    - Power Architecture - low-cost to extreme high-performance MCU/MPUs
    - i.MX – low-cost to high-performance integrated multimedia MPUs

► Learn More

- Automotive: AUT-F0656, AUT-F0668, AUT-F0674, AUT-F0675
- Consumer: CON-F0581
- Enabling Tech: ENT-F0573, ENT-F0757, ENT-F0758
- Industrial: IND-F0554, IND-F0602

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Glossary

► Active Matrix –

► Analog Resistive Touch Panel - This touch panel is comprised of two transparent resistive layers, separated by small spacers. Touching the screen causes the two layers to come in contact and form a switch closure. By measuring the voltage gradient in the horizontal and vertical axis, position can be determined.

► COB – Chip on Board. The LCD driver is epoxied onto the PCB and wire bonds are installed for connections to the IC. The chip plus bonding wires are covered with black epoxy as a seal.

► COG – Chip on Glass. method of bonding driver integrated circuits (ICs) directly to the edges of active matrix liquid crystal displays (LCDs) for smaller packages, higher quality, and improved ruggedness.   The driver IC is mounted upside down (flip chip) eliminating bond wires and interconnects. Reliability is improved due to reduction in interconnects.

► COF – Chip on Flex. The LCD driver is incorporated into a flex connector, which is attached by a heat seal method to the contact edge of the LCD glass.

► CSTN - Color Super Twisted Nematic. A passive matrix display technology used to produce low cost color displays without resorting to TFT manufacturing technology. Color STN Technology is actually STN technology that uses a white backlight and color filters to produce the hues required for a color display. Each visual pixel of a CSTN display is actually 3 separate pixels using a colored filter of Red. Green, and Blue. Each of those colors is controlled individually by the graphic controller chip. So actually a 320 by 240 pixel CSTN display contains 960 by 240 individually colored pixels.

► Dot Matrix /Graphic Display- A display made up of an array of pixel elements in a matrix. Also called "graphic display". Can be used to display graphics, pictures and text.

► Driver - Voltage IC mounted on the display, which provides the voltage to each row and column (do not confuse with the controller IC).

► Controller: An IC, usually mounted in the graphics board, which takes the microprocessor output and tells the display which pixels to light up to produce the image requested.

► Direct Drive: Direct electrical contact from the microprocessor or controller to each pixel on a display. Used in simple glass displays with a few segments and icons, like a thermostat or digital meter. Also known as Static Drive.

► EL Backlight - A type of backlight using electroluminescent material. The thinnest available backlight. Electroluminescent can also be a type of display. Provides uniform light distribution over the active area. Requires an inverter to provide 90VAC at 400Hz. Low power consumption.

► Emissive - A direct-view display, such as cathode ray tube (CRT), field emission display (FED), plasma, electroluminescent (EL), and organic light emitting diode (OLED), where the light generation, switching, and coloring are all done at once by the display. These displays do not need a separate backlight to provide light for the image.

► FSTN - Film Super Twist Nematic display. STN display with a film layer to improve contrast and viewing angle. This film also changes the display "on" color from blue to black.

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Glossary

- ► LCD - Active matrix liquid crystal display (LCD). A display technology that uses a switch at each pixel to create high resolution and fast response times. One type of LCD in which the switch used is a thin film transistor (TFT), is known as a TFT-LCD. Displays based on this technology range from as small as 1" diagonal up to 40" diagonal.

- ► LCD Module - A thin film transistor-passive or active matrix liquid crystal display (TFT-LCD) that contains all components, including backlight and driver integrated circuits (ICs), and is ready to be integrated into an end product such as a TV, monitor, notebook PC, or other device. This term is often used interchangeably with LCD panel.

- ► LCD Panel - A thin film transistor-passive or active matrix liquid crystal display (TFT-LCD) that includes the array, color filter, and liquid crystal. May also include a backlight and driver integrated circuits (ICs), but sometimes is used to refer to just the glass-liquid crystal composite. Often used interchangeably with LCD module.

- ► LED Backlights - LEDs are becoming the most popular type of backlight because they do not require an inverter, and they have a longer lifetime than EL or CCFL. Character modules and small graphic modules use yellow-green LEDs because they are lowest in cost and have the longest life. Monochrome FSTN and color modules require white LEDs, which are becoming lower in cost and longer in lifetime.

- ► Mother Glass – similar to silicon wafers, LCD factories are designed with equipment sets for specific mother glass size

- ► MTBF - Mean Time Between Failures. This is the lifetime of the component or the system. System lifetime can be calculated from the lifetime of the individual components and the number of interconnects. Lifetime is usually expressed in hours. For LCDs, the lifetime is determined by the backlight. EL panels are the lowest, yellow-green LEDs are the highest.

- ► Multiplex - Method of sharing rows or columns of pixels on a display to reduce the number of connections to the driver or controller. As the display resolution increases, the multiplex rate must increase to allow all of the individual pixels to be addressed.

- ► OLED - Organic light emitting diode (OLED), an emissive flat panel display that uses organic compounds to emit light. OLEDs can be passive or active matrix. Passive matrix devices are easier to make, but not capable of full color or high resolution. Currently, active matrix devices use a poly-crystalline silicon thin film transistor (TFT) array, similar to low temperature poly-crystalline silicon (LTPS) active matrix liquid crystal displays (LCDs). There has been limited production to date because of short product lifetimes and differential aging rates of the OLED materials. This is also known as Organic EL.

- ► NTSC - National Television Standard Committee. International television standard which uses 525 lines per frame at 60Hz field rate.

- ► PAL - Phase Alternation Line. International television standard which uses 625 lines per frame at 50Hz field rate.

- ► Passive Matrix LCDs - These are the predecessors to active matrix liquid crystal displays (LCDs); these displays do not incorporate a thin film transistor (TFT) or switch at each pixel. As a result, they tend to have lower resolution, slower refresh rates, and poorer viewing angles than active matrix LCDs.

- ► Pixel - An individual dot on the display. Short for "picture element," a pixel is the basic unit of information on a display. It can be made up of different colored sub-pixels.

- ► Polarizer - This is a material that selectively transmits light with a given polarization. Polarizers are critical in the operation of most active matrix liquid crystal displays (LCDs), as the liquid crystal manipulates polarized light. A twisted-nematic (TN) LCD typically has polarizers on both sides of the LCD cell.

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Glossary

▶ Reflective - A display without a backlight. Reflective displays rely on ambient light to provide the image. Excellent for outdoors or bright light conditions. Most digital watches and calculators use reflective LCDs, although some color versions have been developed for mobile phones and PDAs. See also Emissive, Transmissive, and Projection. Emerging reflective technologies include Electrophoretic (made by E Ink and others), electrochromic (made by NTERA and others), and microelectromechanical systems (MEMS)-based (made by Iridigm and others).

▶ Refresh Rate - The time interval required for the electronics to fully address a display. This rate determines the capability of the display to show video images.

▶ Resolution - The number of pixels available for information display. More pixels (higher resolution) enables finer details to be displayed and generally results in a better image quality.

▶ Segment - A single active area in the segmented displays (as opposed to the background area).

▶ STN - Super Twisted Nematic. A type of high-performance passive matrix display used to improve optical properties at high multiplex rates. Method is to increase the twist angle in the LCD construction from the 90 degrees used in TN to a much higher twist (270 degrees or more). Hence the nickname "super twist". Used exclusively in character modules and graphic modules, including Color STN.

▶ TAB Tape Automated Bonding - The LCD driver / controller is encapsulated in a bubble on a flex circuit. The flex is attached directly to the glass or a PCB.

▶ TFT - Thin-film transistor (TFT). Electronic technology upon which active matrix liquid crystal displays (LCDs) are based. Each pixel is driven by a separate IC gate to speed the response time and improve the optics. The foundation of the TFT is a semiconductor layer (typically based on silicon) which can switch current flow on or off by the application of an electric field. The IC gates are deposited directly onto the LCD glass substrate in a combination of wafer fabrication and glass assembly.

▶ TN - Twisted Nematic. The original construction method for LCDs using 90 degree twist angles. Used in 7 segment and direct drive display applications. Very low cost manufacturing.

▶ Touch Panel Controller - The hardware element that translates the information between the touch panel and the host system.

▶ Touchscreen - A transparent glass or hard plastic sheet that mounts over the display viewing area and allows users to make a choice and input via touching the screen.

▶ Transflective - A display that combines reflective and transmissive qualities. In dark ambient light environments, the backlight can be used to provide light for the display. In bright ambient light environments, the backlight can be switched off and the display used in reflective mode to save battery life. Most often used in PDAs and mobile phones. Good in sunlight and outdoor applications. Contrast ratio and brightness are decreased compared to transmissive type.

▶ Transmissive - A display that uses a backlight shining through the LCD to produce the image. Good in regular or dim lighting. Not for use in sunshine. Ambient light interferes with the backlight, and "washes out" the display image. The light is created by a CCFL or light emitting diode (LED) backlight, the switching is provided by the thin film transistor (TFT) array, and the color is provided by the color filter.

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Glossary

► TSTN - Triple Super Twist Nematic. Sharp name for film compensated super twist display which uses a retardation film to correct the color shift in STN displays, and so produces a black and white image.

► Viewing Angle - The angle at which the viewer must be in comparison to the screen, in order to see the image on a display. For example, a 0° horizontal viewing angle is directly in front of the display and a 90° horizontal viewing angle is directly to the side. Emissive displays show the same brightness and color regardless of viewing angle, however, rear projection displays and transmissive displays can show some differences in color, brightness, and gray scale, with the most difference being noticed at the steepest viewing angles.

► VFD - Vacuum Fluorescent Display.

► Zebra Strip - Conductive rubber strip, also called Elastomer, used to connect the contacts on the glass display to the printed circuit board of a LCD character module. Also use in low resolution graphic modules. Electrical contact is made by compression with the bezel frame.

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REFLECTIVE LCD

A reflector is bonded to the
rear polarizer. This mirror-like polarizer
reflects the incoming ambient light.
Used in thermostats and calculators.
Best performance in direct sunlight.

TRANSFLECTIVE LCD

A porous reflector is bonded to the
rear polarizer. This polarizer reflects the ambient
light as well as allowing light to pass through the
rear of the polarizer.   Good performance indoors
& outdoors.

TRANSMISSIVE LCD

This viewing mode has neither a reflective or
transflective rear polarizer. A backlight is
required to view this module.   Not suitable for
outdoor operation.
Usually operates in negative mode.
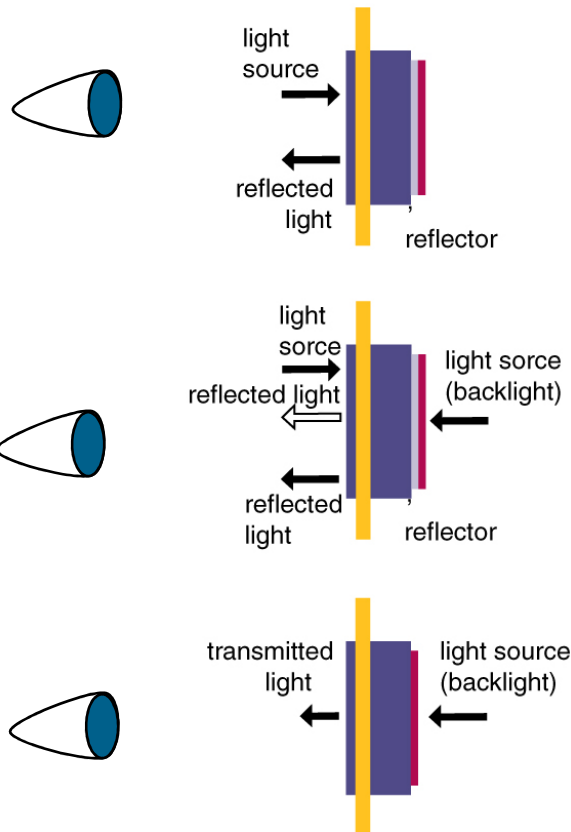
Active elements when energized appear dark in color against a light background non-energized (Transflective Positive)

Active elements when energized appear light in color against a dark background non energized (Transmissive Negative)
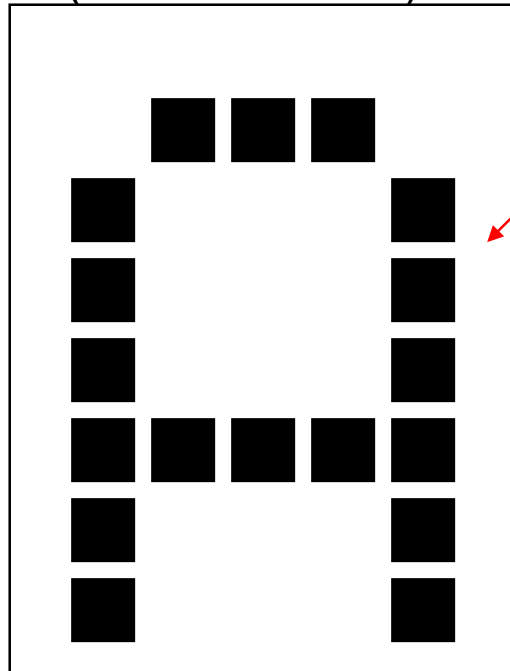
(Most Common) Small To Mid Graphic Displays (Outdoor)

(Least Common) Mid to Large Graphic Displays (Indoor)
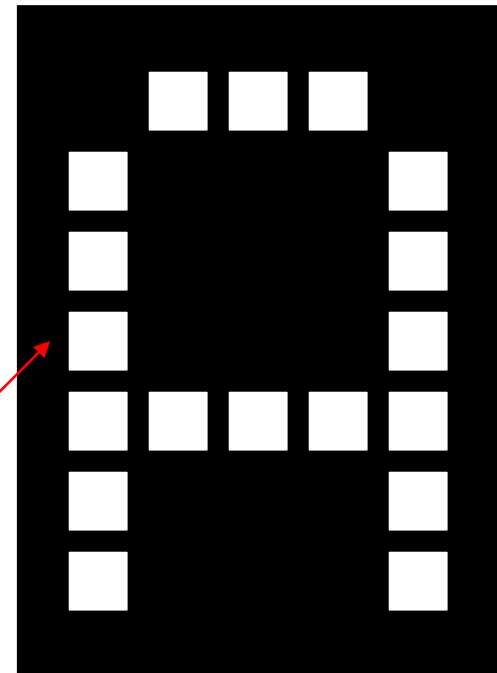
The viewing area is in the off state. This Is achieved by having both the front and rear polarizers in the same axis. In this mode light passes through the energized area. (A backlight Is required)

POSITIVE Type "+"
Reflective & Transflective

## NEGATIVE Type "-"
Transmissive

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Viewing Modes

Viewing Mode	Display Description	Application Comments	Direct Sunlight	Office Light	Subdued Light	Very Low Light
Reflective Positive Image	Dark segments on light background	Not backlit. Provides best head-on contrast and environmental stability	Excellent	Very Good	Average	Poor
Transflective Positive Image	Dark segments on grey background	Can be viewed by reflected ambient light or with backlighting	Excellent (No Backlight)	Good (No Backlight)	Good (Backlit)	Very Good (Backlit)
Transflective Negative Image	Light grey segments on dark background	Needs high ambient light or backlighting. Frequently used with color and multicolor transflector	Good (No Backlight)	Fair (No Backlight)	Good (Backlit)	Very Good (Backlit)
Transmissive Negative Image	Backlit segments on dark background	Cannot be read by reflection	Poor (Backlit)	Good (Backlit)	Very Good (No Backlight)	Excellent (Backlit)
Transmissive Positive Image	Dark segments on backlit background	Designed for very low light conditions, yet able to be read in bright ambient lights.	Good (No Backlight)	Good (Backlit)	Very Good (Backlit)	Excellent (Backlit)

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Fluid Types

▶ TN = Twisted Nematic: Used in segment displays and icon displays with low multiplex rates.

▶ STN = Super Twist Nematic: Character modules, first generation graphic modules. Improved optics over TN.

▶ FSTN = Film Super Twist Nematic: Uses film layer over STN to double viewing angles and increase contrast 3X in monochrome graphic modules.

▶ CSTN = Color Super Twist Nematic: Passive color. Uses filters to produce color. Low cost color solution.

▶ TFT = Thin Film Technology = Active Matrix. Marriage of semiconductor and LCD technology to add individual drivers for each pixel right on the glass. Dramatic increase in contrast, viewing angles, and response time.

▶ OLED =   ??

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The orientation of the LCD display is often stated with reference to a clock face. If the LCD is best viewed from above the horizontal, it is referred to as a "12:00" or top view.
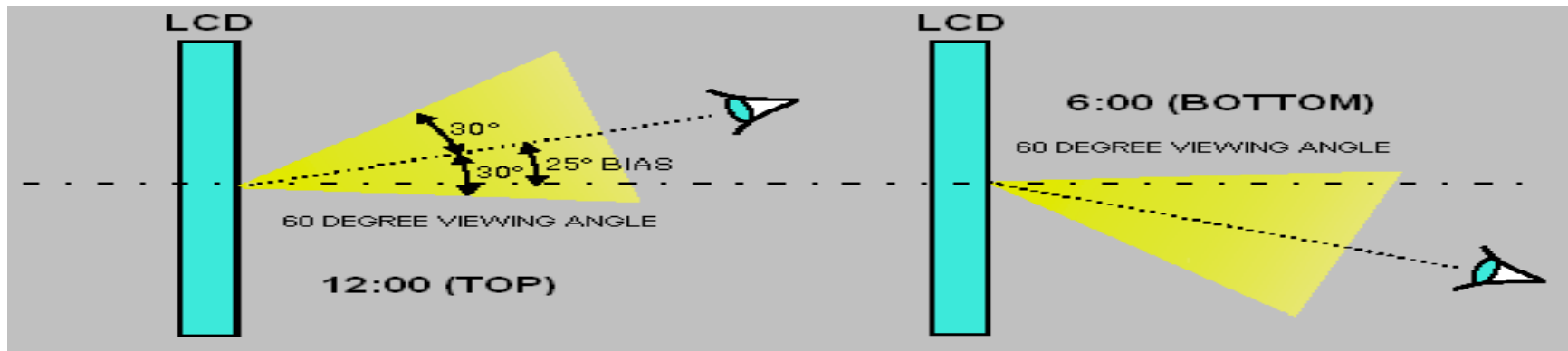
If the LCD is best viewed from below the horizontal, it is referred to as a "6:00" view.

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