MCP6271/2/3/4/5

170 µA, 2 MHz Rail-to-Rail Op Amp

Features

- Gain Bandwidth Product: 2 MHz (typ.)
- Supply Current: I_Q = 170 µA (typ.)
- Supply Voltage: 2.0V to 5.5V
- Rail-to-Rail Input/Output
- Extended Temperature Range: -40°C to +125°C
- Available in Single, Dual and Quad Packages
- Single with Chip Select ($\overline{CS}$) (**MCP6273**)
- Dual with Chip Select ($\overline{CS}$) (**MCP6275**)

Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Available Tools

- SPICE Macro Model (at www.microchip.com)
- FilterLab® Software (at www.microchip.com)

Description

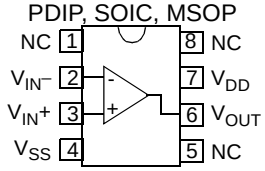
The Microchip Technology Inc. MCP6271/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 2 MHz Gain Bandwidth Product (GBWP) and a 65° phase margin. This family also operates from a single supply voltage as low as 2.0V, while drawing 170 µA (typ.) quiescent current. Additionally, the MCP6271/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of operational amplifiers is designed with Microchip's advanced CMOS process.

The MCP6275 has a Chip Select input ($\overline{CS}$) for dual op amps in an 8-pin package and is manufactured by cascading two op amps (the output of op amp A connected to the non-inverting input of op amp B). The $\overline{CS}$ input puts the device in Low-power mode.

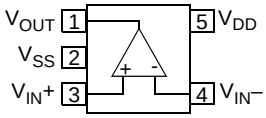
The MCP6271/2/3/4/5 family operates over the Extended Temperature Range of -40°C to +125°C, with a power supply range of 2.0V to 5.5V.

Package Types

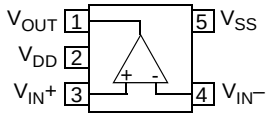
MCP6271
PDIP, SOIC, MSOP



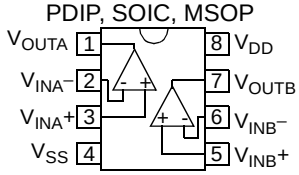
MCP6271
SOT-23-5



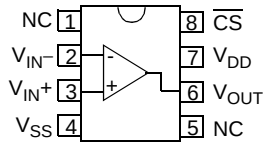
MCP6271R
SOT-23-5



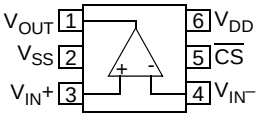
MCP6272
PDIP, SOIC, MSOP



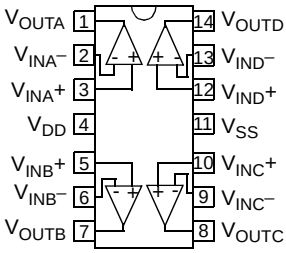
MCP6273
PDIP, SOIC, MSOP



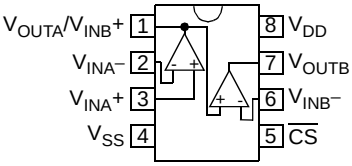
MCP6273
SOT-23-6



MCP6274
PDIP, SOIC, TSSOP



MCP6275
PDIP, SOIC, MSOP



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AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	2.0	—	MHz	
Phase Margin at Unity-Gain	PM	—	65	—	°	
Slew Rate	SR	—	0.9	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	3.5	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	20	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	3	—	fA/√Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.0V to +5.5V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

MCP6273/MCP6275 CHIP SELECT ($\overline{CS}$) SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	$0.2V_{DD}$	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	0.01	—	µA	$\overline{CS} = V_{SS}$
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	$0.8V_{DD}$	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	2	µA	$\overline{CS} = V_{DD}$
GND Current per Amplifier	I_{SS}	—	-0.7	—	µA	$\overline{CS} = V_{DD}$
Amplifier Output Leakage	—	—	0.01	—	µA	$\overline{CS} = V_{DD}$
Dynamic Specifications (Note 1)						
$\overline{CS}$ Low to Valid Amplifier Output, Turn-on Time	t_{ON}	—	4	10	µs	$\overline{CS}$ Low ≤ 0.2 V_{DD}, G = +1 V/V, $V_{IN} = V_{DD}/2$, V_{OUT} = 0.9 $V_{DD}/2$, V_{DD} = 5.0V
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	0.01	—	µs	$\overline{CS}$ High ≥ 0.8 V_{DD}, G = +1 V/V, $V_{IN} = V_{DD}/2$, V_{OUT} = 0.1 $V_{DD}/2$
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5V

Note 1: The input condition (V_{IN}) specified applies to both op amp A and B of the MCP6275. The dynamic specification is tested at the output of op amp B (V_{OUTB}).

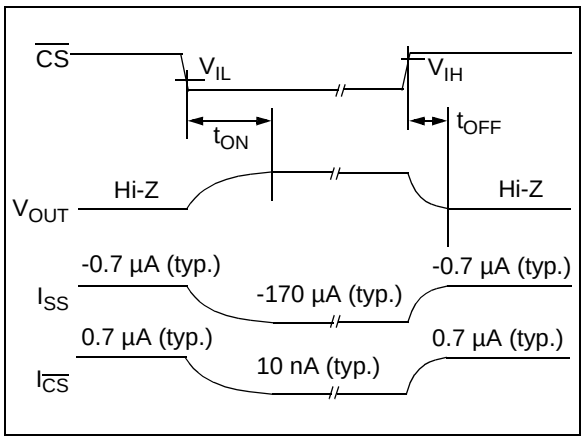

FIGURE 1-1: *Timing Diagram for the Chip Select ($\overline{CS}$) pin on the MCP6273 and MCP6275.*

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

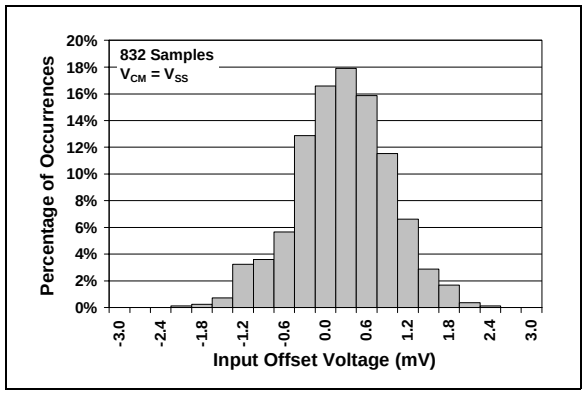

FIGURE 2-1: *Input Offset Voltage.*

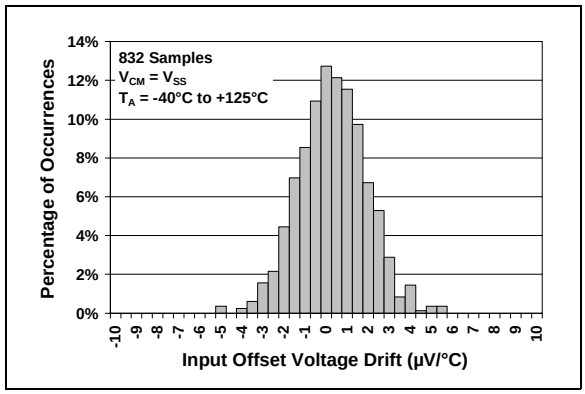

FIGURE 2-4: *Input Offset Voltage Drift.*

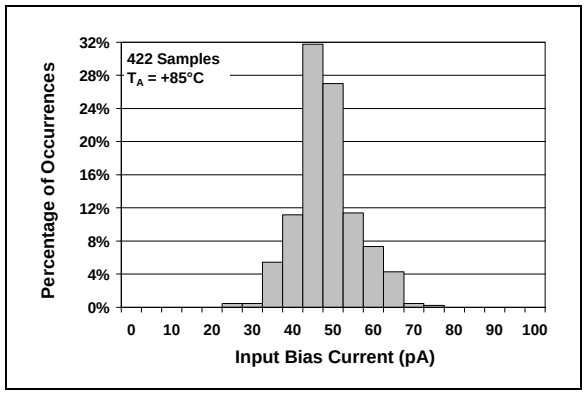

FIGURE 2-2: *Input Bias Current at T_A = +85°C.*

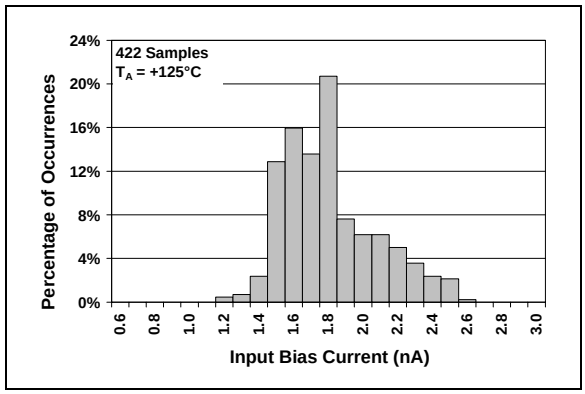

FIGURE 2-5: *Input Bias Current at T_A = +125°C.*

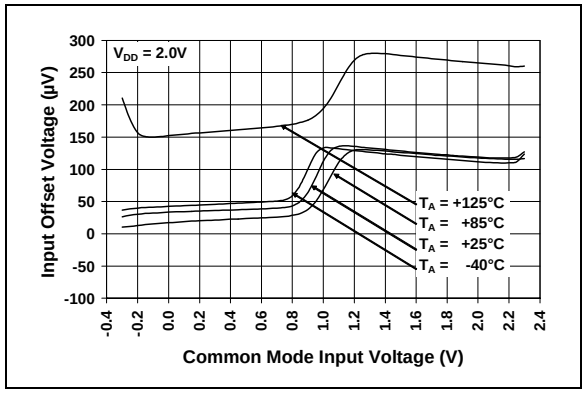

FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 2.0V.*

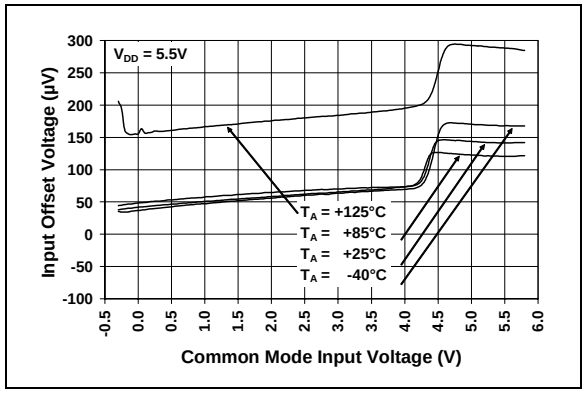

FIGURE 2-6: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

TYPICAL PERFORMANCE CURVES (Continued)

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

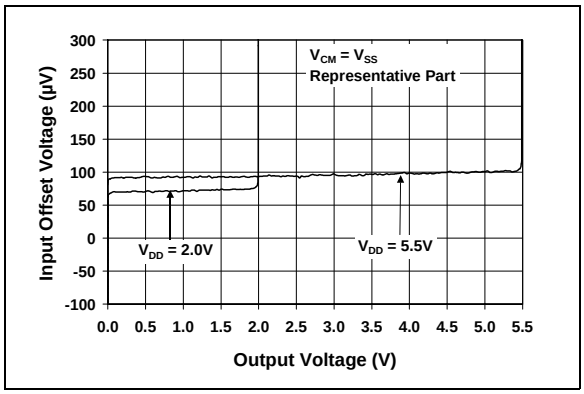

FIGURE 2-7: *Input Offset Voltage vs. Output Voltage.*

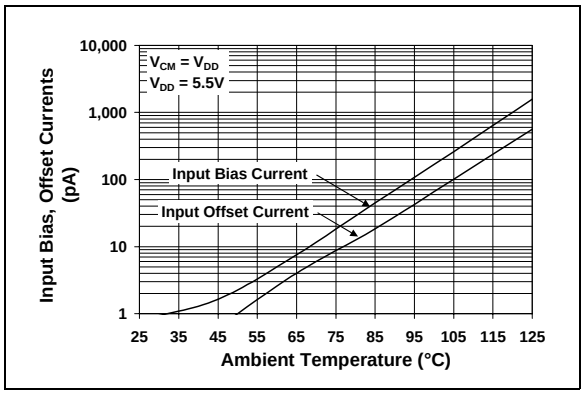

FIGURE 2-10: *Input Bias, Input Offset Currents vs. Ambient Temperature.*

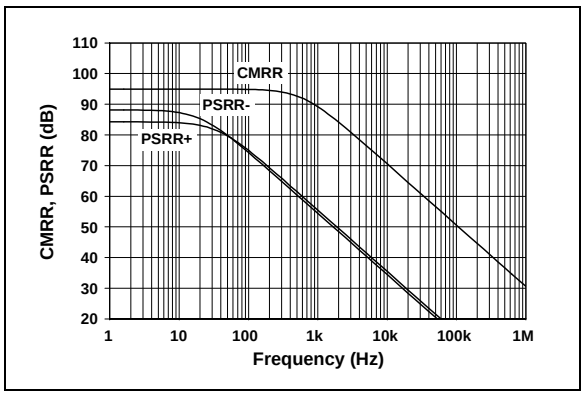

FIGURE 2-8: *CMRR, PSRR vs. Frequency.*

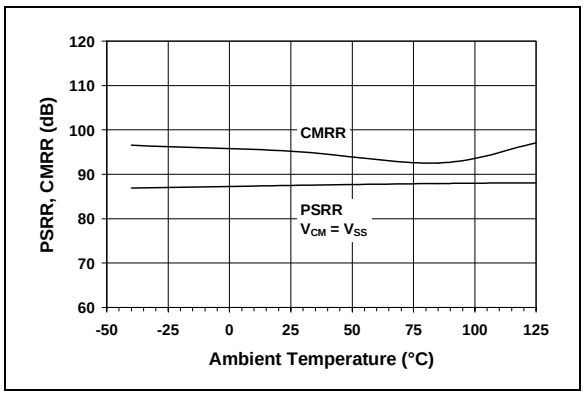

FIGURE 2-11: *CMRR, PSRR vs. Ambient Temperature.*

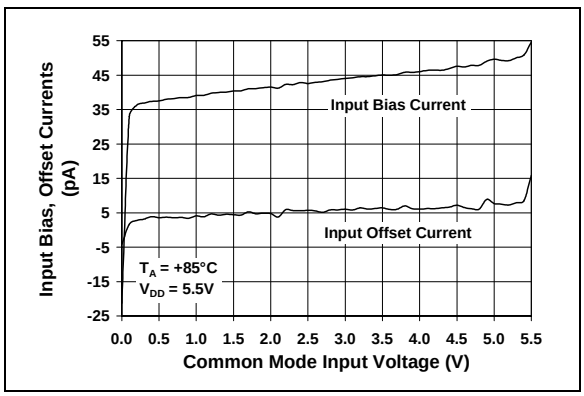

FIGURE 2-9: *Input Bias, Offset Currents vs. Common Mode Input Voltage at T_A = +85°C.*

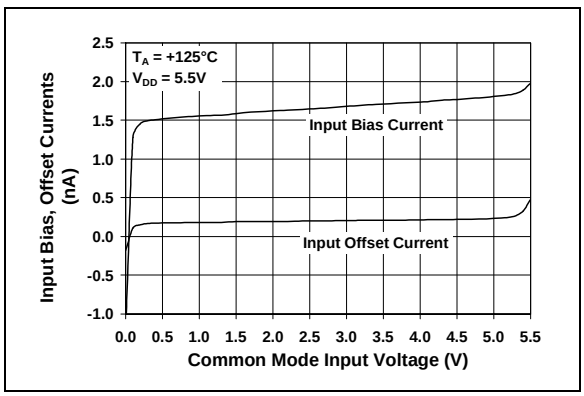

FIGURE 2-12: *Input Bias, Offset Currents vs. Common Mode Input Voltage at T_A = +125°C.*

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TYPICAL PERFORMANCE CURVES (Continued)

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

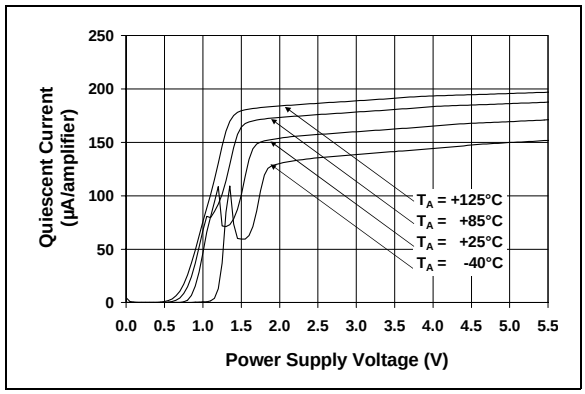

FIGURE 2-13: *Quiescent Current vs. Power Supply Voltage.*

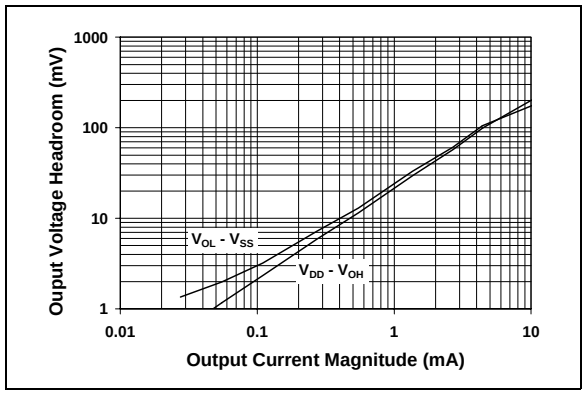

FIGURE 2-16: *Output Voltage Headroom vs. Output Current Magnitude.*

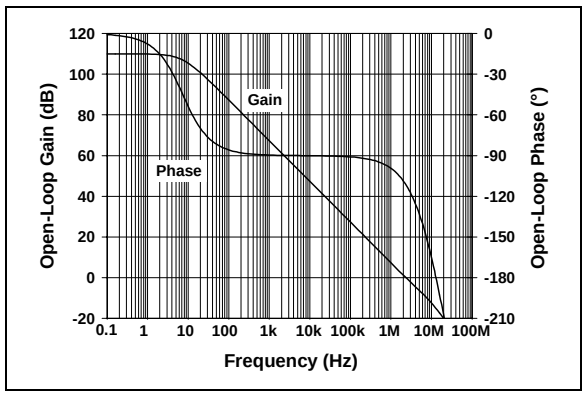

FIGURE 2-14: *Open-Loop Gain, Phase vs. Frequency.*

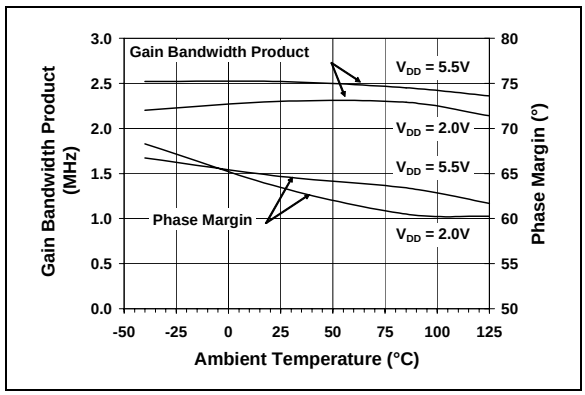

FIGURE 2-17: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

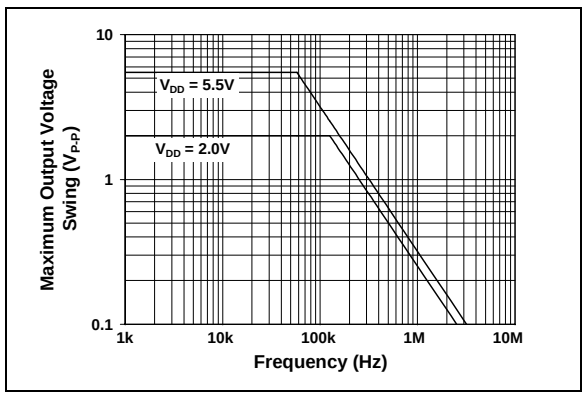

FIGURE 2-15: *Maximum Output Voltage Swing vs. Frequency.*

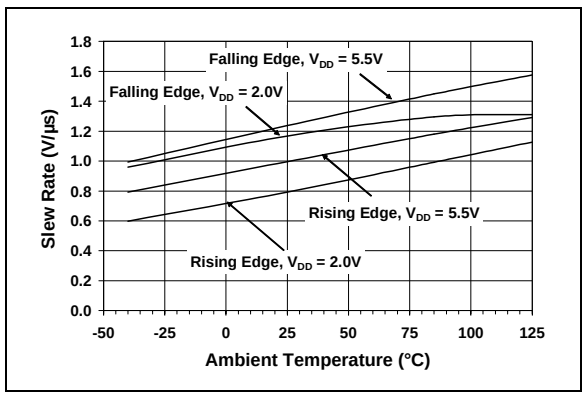

FIGURE 2-18: *Slew Rate vs. Ambient Temperature.*

TYPICAL PERFORMANCE CURVES (Continued)

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

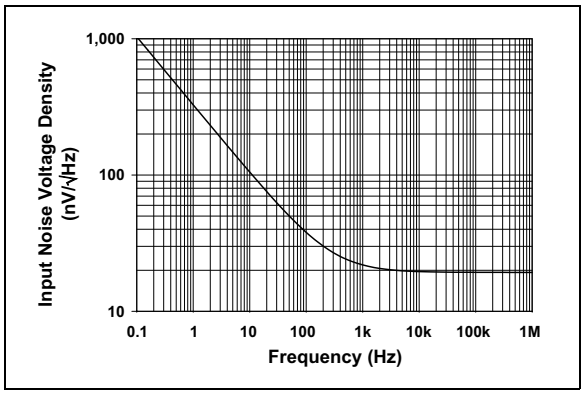

FIGURE 2-19: *Input Noise Voltage Density vs. Frequency.*

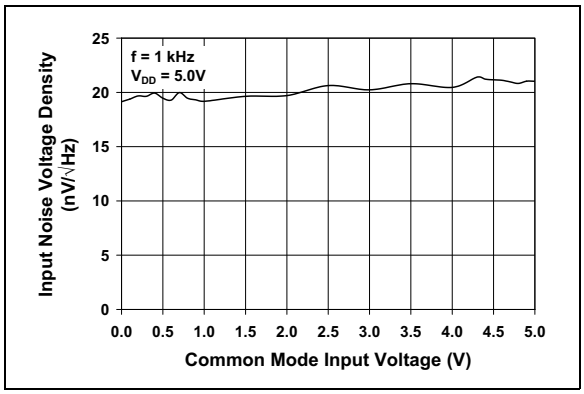

FIGURE 2-22: *Input Noise Voltage Density vs. Common Mode Input Voltage at 1 kHz.*

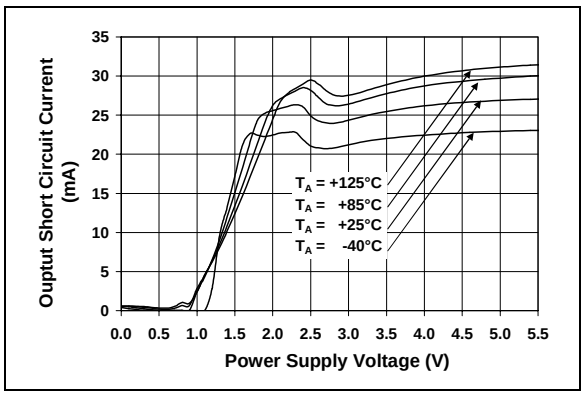

FIGURE 2-20: *Output Short-Circuit Current vs. Power Supply Voltage.*

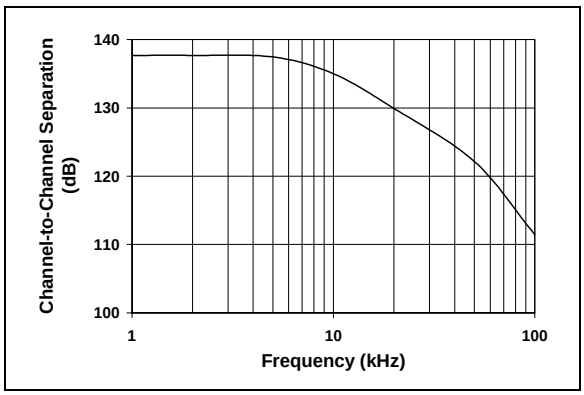

FIGURE 2-23: *Channel-to-Channel Separation vs. Frequency (MCP6272 and MCP6274).*

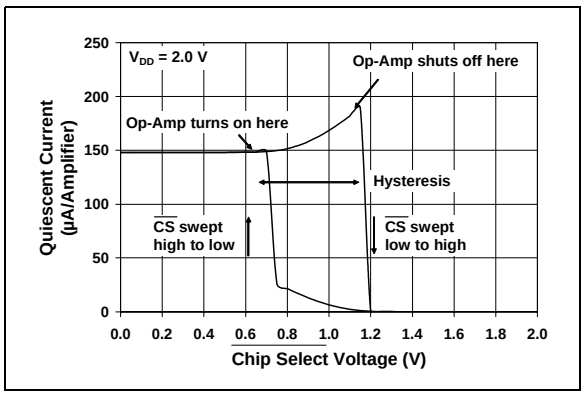

FIGURE 2-21: *Quiescent Current vs. Chip Select (CS) Voltage at V_{DD} = 2.0V (MCP6273 and MCP6275 only).*

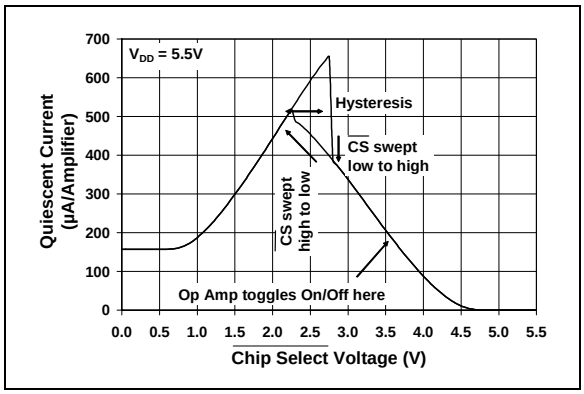

FIGURE 2-24: *Quiescent Current vs. Chip Select (CS) Voltage at V_{DD} = 5.5V (MCP6273 and MCP6275 only).*

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TYPICAL PERFORMANCE CURVES (Continued)

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

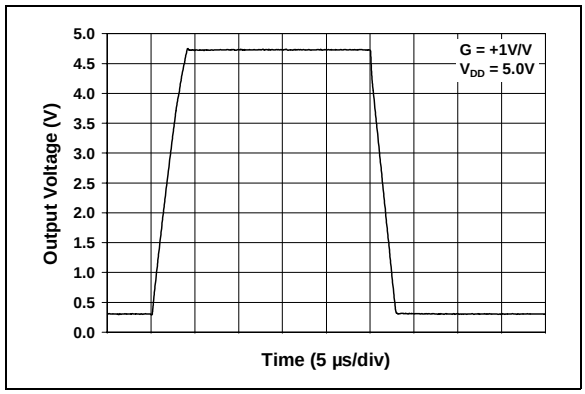

FIGURE 2-25: *Large-Signal Non-inverting Pulse Response.*

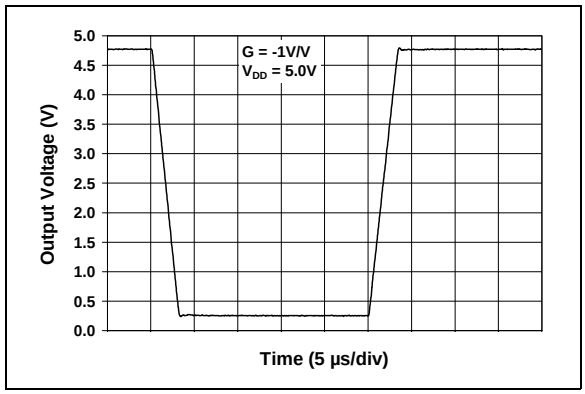

FIGURE 2-28: *Large-Signal Inverting Pulse Response.*

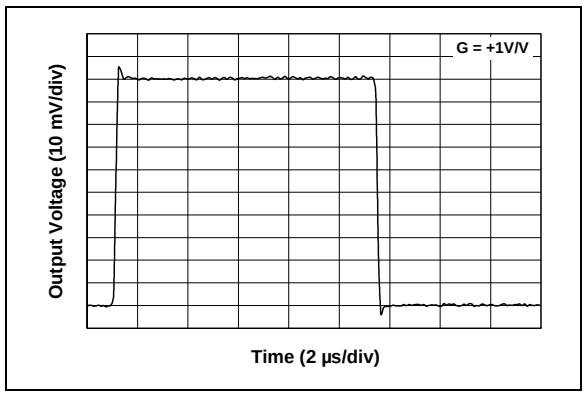

FIGURE 2-26: *Small-Signal Non-inverting Pulse Response.*

FIGURE 2-29: *Small-Signal Inverting Pulse Response.*

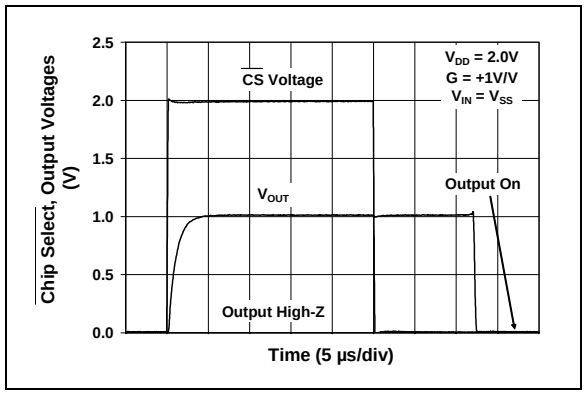

FIGURE 2-27: *$\overline{\text{Chip Select}}$ ($\overline{CS}$) to Amplifier Output Response Time at V_{DD} = 2.0V (MCP6273 and MCP6275 only).*

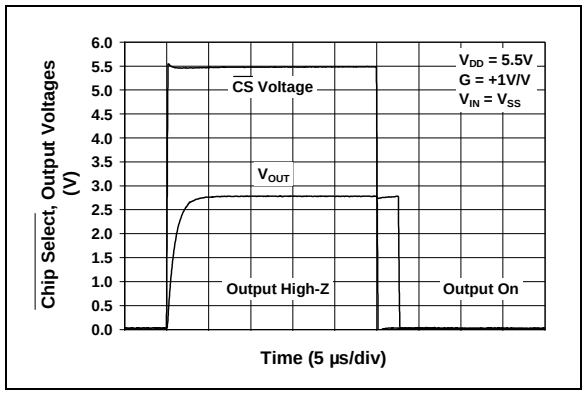

FIGURE 2-30: *$\overline{\text{Chip Select}}$ ($\overline{CS}$) to Amplifier Output Response Time at V_{DD} = 5.5V (MCP6273 and MCP6275 only).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1 (single op amps) and Table 3-2 (dual and quad op amps).

TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS

MCP6271 (PDIP, SOIC, MSOP)	**MCP6271** (SOT-23-5)	**MCP6271R** (SOT-23-5)	**MCP6273** (PDIP, SOIC, MSOP)	**MCP6273** (SOT-23-6)	**Symbol**	**Description**
6	1	1	6	1	V_{OUT}	Analog Output
2	4	4	2	4	$V_{IN}-$	Inverting Input
3	3	3	3	3	$V_{IN}+$	Non-inverting Input
7	5	2	7	6	V_{DD}	Positive Power Supply
4	2	5	4	2	V_{SS}	Negative Power Supply
—	—	—	8	5	$\overline{CS}$	$\overline{\text{Chip Select}}$
1,5,8	—	—	1,5	—	NC	No Internal Connection

TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS.

MCP6272	**MCP6274**	**MCP6275**	**Symbol**	**Description**
1	1	—	V_{OUTA}	Analog Output (op amp A)
2	2	2	$V_{INA}-$	Inverting Input (op amp A)
3	3	3	$V_{INA}+$	Non-inverting Input (op amp A)
8	4	8	V_{DD}	Positive Power Supply
5	5	—	$V_{INB}+$	Non-inverting Input (op amp B)
6	6	6	$V_{INB}-$	Inverting Input (op amp B)
7	7	7	V_{OUTB}	Analog Output (op amp B)
—	8	—	V_{OUTC}	Analog Output (op amp C)
—	9	—	$V_{INC}-$	Inverting Input (op amp C)
—	10	—	$V_{INC}+$	Non-inverting Input (op amp C)
4	11	4	V_{SS}	Negative Power Supply
—	12	—	$V_{IND}+$	Non-inverting Input (op amp D)
—	13	—	$V_{IND}-$	Inverting Input (op amp D)
—	14	—	V_{OUTD}	Analog Output (op amp D)
—	—	1	V_{OUTA} / $V_{INB}+$	Analog Output (op amp A)/Non-inverting Input (op amp B)
—	—	5	$\overline{CS}$	$\overline{\text{Chip Select}}$

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 MCP6275's $V_{OUTA}/V_{INB}+$ Pin

For the MCP6275 only, the output of op amp A is connected directly to the non-inverting input of op amp B; this is the $V_{OUTA}/V_{INB}+$ pin. This connection makes it possible to provide a $\overline{CS}$ pin for duals in 8-pin packages.

3.4 $\overline{CS}$ Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low-power mode of operation.

3.5 Power Supply (V_{SS} and V_{DD})

The positive power supply (V_{DD}) is 2.0V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These parts need to use a bulk capacitor (within 100 mm), which can be shared with nearby analog parts.

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4.0 APPLICATION INFORMATION

The MCP6271/2/3/4/5 family of op amps is manufactured using Microchip's state-of-the-art CMOS process, specifically designed for low-cost, low-power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6271/2/3/4/5 ideal for battery-powered applications.

4.1 Rail-to-Rail Inputs

The MCP6271/2/3/4/5 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 4-1 shows the input voltage exceeding the supply voltage without any phase reversal.

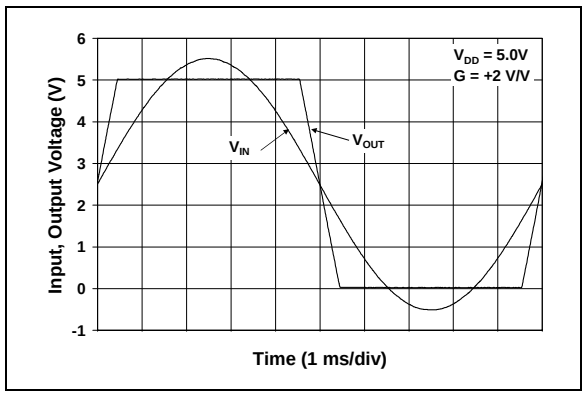

FIGURE 4-1: *The* MCP6271/2/3/4/5 *Show No Phase Reversal.*

The input stage of the MCP6271/2/3/4/5 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}) and the other at high V_{CM}. With this topology, the device operates with V_{CM} up to 0.3V above V_{DD} and 0.3V below V_{SS}. The Input Offset Voltage (V_{OS}) is measured at $V_{CM} = V_{SS} – 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

Input voltages that exceed the absolute maximum voltage ($V_{SS} – 0.3V$ to $V_{DD} + 0.3V$) can cause excessive current to flow into or out of the input pins. Current beyond ±2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 4-2.

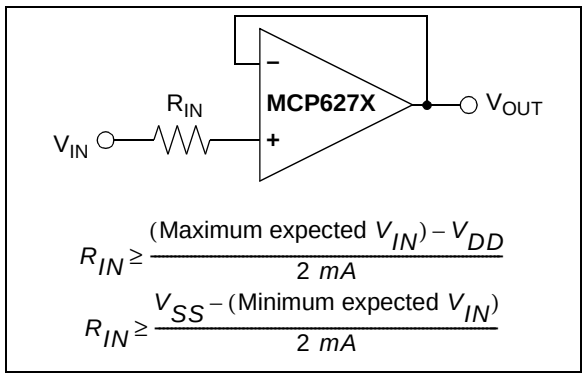

FIGURE 4-2: *Input Current Limiting Resistor (R_{IN}).*

4.2 Rail-to-Rail Output

The output voltage range of the MCP6271/2/3/4/5 op amps is $V_{DD} – 15$ mV (min.) and $V_{SS} + 15$ mV (max.) when $R_L = 10\ k\Omega$ is connected to $V_{DD}/2$ and $V_{DD} = 5.5V$. Refer to Figure 2-16 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage-feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

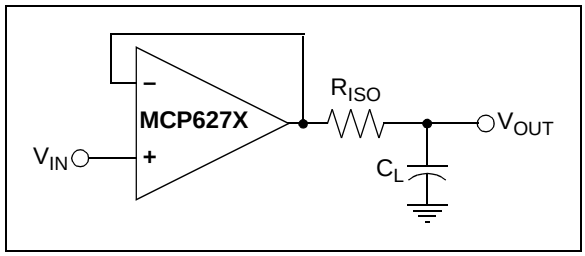

FIGURE 4-3: *Output Resistor, R_{ISO} stabilizes large capacitive loads.*

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

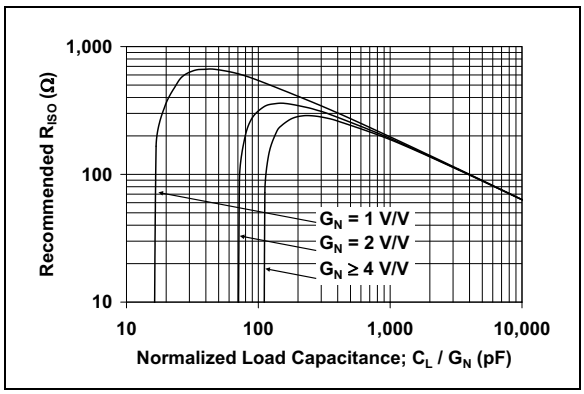

FIGURE 4-4: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6271/2/3/4/5 SPICE macro model are helpful.

4.4 MCP6273/5 Chip Select ($\overline{CS}$)

The MCP6273 and MCP6275 are single and dual op amps with Chip Select ($\overline{CS}$), respectively. When $\overline{CS}$ is pulled high, the supply current drops to 0.7 µA (typ.) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier may not operate properly. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

4.5 Cascaded Dual Op Amps (MCP6275)

The MCP6275 is a dual op amp with Chip Select ($\overline{CS}$). The Chip Select input is available on what would be the non-inverting input of a standard dual op amp (pin 5). This pin is available because the output of op amp A connects to the non-inverting input of op amp B, as shown in Figure 4-5. The Chip Select input, which can be connected to a microcontroller I/O line, puts the device in Low-power mode. Refer to **Section 4.4 "MCP6273/5 Chip Select ($\overline{CS}$)"**.

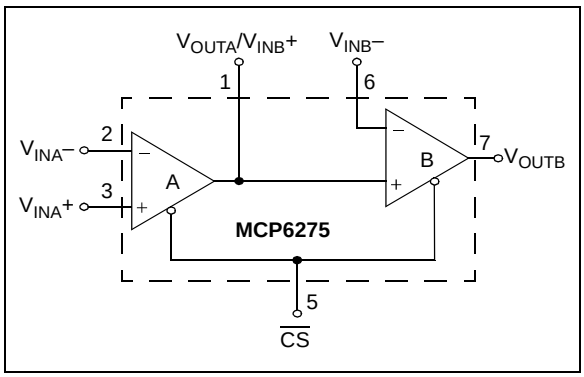

FIGURE 4-5: *Cascaded Gain Amplifier.*

The output of op amp A is loaded by the input impedance of op amp B, which is typically $10^{13}\Omega \,||\, 6$ pF, as specified in the DC specification table (Refer to **Section 4.3 "Capacitive Loads"** for further details regarding capacitive loads).

The common mode input range of these op amps is specified in the data sheet as V_{SS} – 300 mV and V_{DD} + 300 mV. However, since the output of op amp A is limited to V_{OL} and V_{OH} (20 mV from the rails with a 10 kΩ load), the non-inverting input range of op amp B is limited to the common mode input range of V_{SS} + 20 mV and V_{DD} – 20 mV.

4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good, high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.7 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface-leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6271/2/3/4/5 family's bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is illustrated in Figure 4-6.

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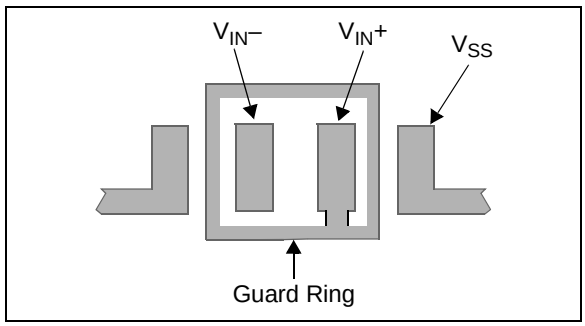

FIGURE 4-6: *Example Guard Ring Layout for Inverting Gain.*

1. For Inverting Gain and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b. Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.
2. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common mode input voltage.

4.8 Application Circuits

4.8.1 ACTIVE FULL-WAVE RECTIFIER

The MCP6271/2/3/4/5 family of amplifiers can be used in applications such as an Active Full-Wave Rectifier or an Absolute Value circuit, as shown in Figure 4-7. The amplifier and feedback loops in this active voltage rectifier circuit eliminate the diode drop problem that exists in a passive voltage rectifier. This circuit behaves as a follower (the output follows the input) as long as the input signal is more positive than the reference voltage. If the input signal is more negative than the reference voltage, however, the circuit behaves as an inverting amplifier. Therefore, the output voltage will always be above the reference voltage, regardless of the input signal.

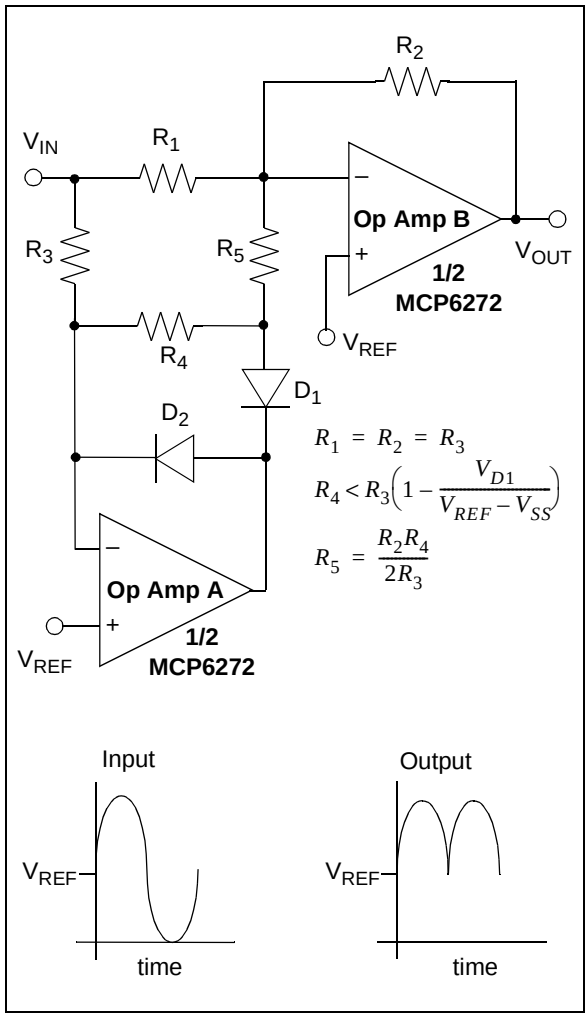

FIGURE 4-7: *Active Full-wave Rectifier.*

The design equations give a gain of ±1 from V_{IN} to V_{OUT}, and produce rail-to-rail outputs.

FIGURE 4-10: *Cascaded Gain Circuit Configuration.*

4.8.3.3 Difference Amplifier

Figure 4-11 shows op amp A configured as a difference amplifier with $\overline{\text{Chip Select}}$. In this configuration, it is recommended that well-matched resistors (e.g., 0.1%) be used to increase the Common Mode Rejection Ratio (CMRR). Op amp B can be used to provide additional gain and isolate the load from the difference amplifier.

FIGURE 4-11: *Difference Amplifier Circuit.*

4.8.3.4 Inverting Integrator with Active Compensation and $\overline{\text{Chip Select}}$

Figure 4-12 uses an active compensator (op amp B) to compensate for the non-ideal op amp characteristics introduced at higher frequencies. This circuit uses op amp B as a unity-gain buffer to isolate the integration capacitor C_1 from op amp A and drives the capacitor with a low-impedance source. Si(83.5(buf.1(c0impe).8(io))-039)tr0.680414.680414. a.e Tw [(int)i 5((end)12-0 buf.1(c)183(C)5.)-0.4c

4.8.3.6 Second-Order Sallen-Key with an Extra Pole-Zero Pair

Figure 4-14 is a second-order Sallen-Key low-pass filter with Chip Select. Use the Filterlab® software from Microchip to determine the R and C values for op amp A's second-order filter. Op amp B can be used to add a pole-zero pair using C_3, R_5 and R_6.

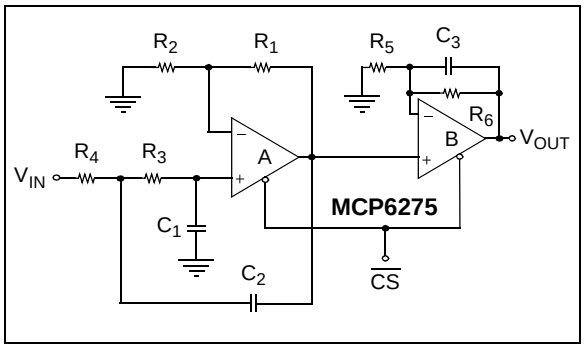

FIGURE 4-14: *Second-Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair and Chip Select.*

4.8.3.7 Capacitorless Second-Order Low-Pass filter with Chip Select

The low-pass filter shown in Figure 4-15 does not require external capacitors and uses only three external resistors; the op amp's GBWP sets the corner frequency. R_1 and R_2 are used to set the circuit gain. R_3 is used to set the Q. To avoid gain-peaking in the frequency response, Q needs to be low (lower values need to be selected for R_3). Note that the amplifier bandwidth varies greatly over temperature and process. This configuration, however, provides a low-cost solution for applications with high bandwidth requirements.

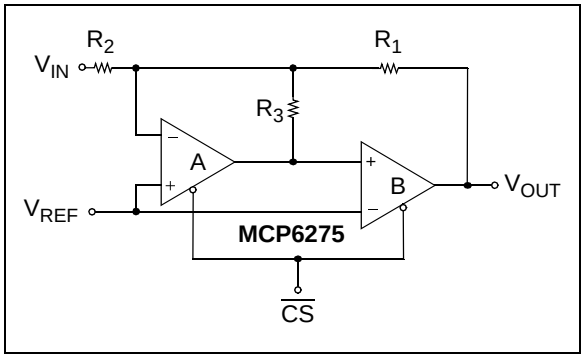

FIGURE 4-15: *Capacitorless Second-Order Low-Pass Filter with Chip Select.*

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5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6271/2/3/4/5 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6271/2/3/4/5 op amps is available on our web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation at room temperature. See the macro model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

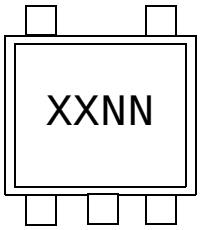
5.2 FilterLab® Software

Microchip's FilterLab software is an innovative tool that simplifies analog active filter (using op amps) design. It is available free of charge from our web site at www.microchip.com. The FilterLab software tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

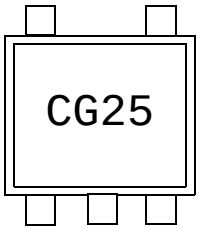
5-Lead SOT-23 (**MCP6271 and MCP6271R**)



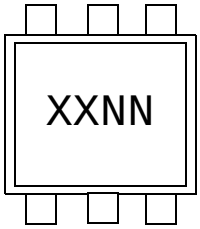
Device	Code
MCP6271	CGNN
MCP6271R	ETNN

Note: Applies to 5-Lead SOT-23

Example:

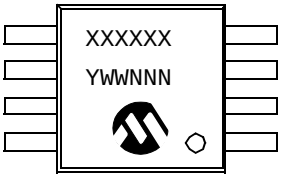


6-Lead SOT-23 (**MCP6273**)

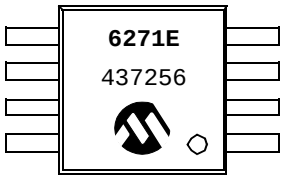


Example:

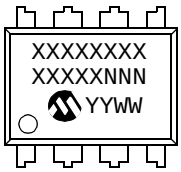
8-Lead MSOP



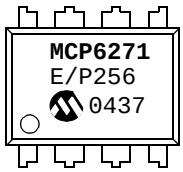
Example:



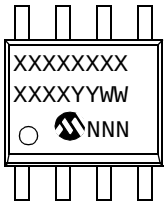
8-Lead PDIP (300 mil)



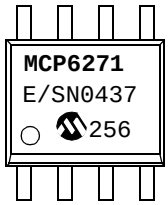
Example:



8-Lead SOIC (150 mil)



Example:



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

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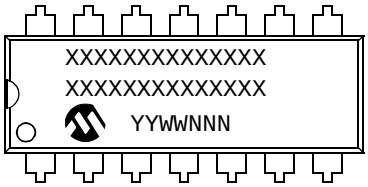
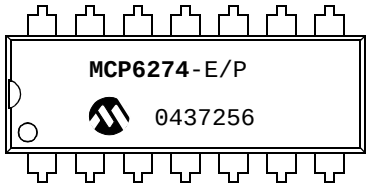
Package Marking Information (Continued)

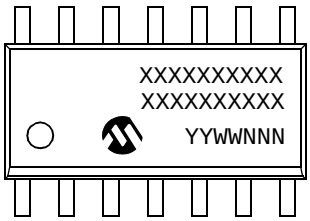
14-Lead PDIP (300 mil) **(MCP6274)**



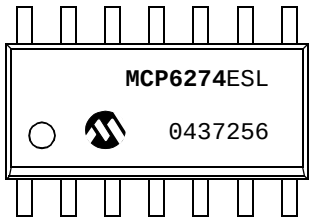
Example:



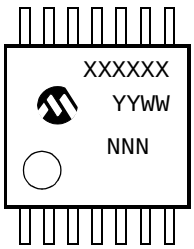
14-Lead SOIC (150 mil) **(MCP6274)**



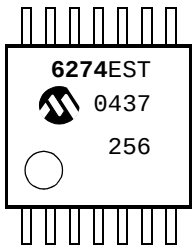
Example:



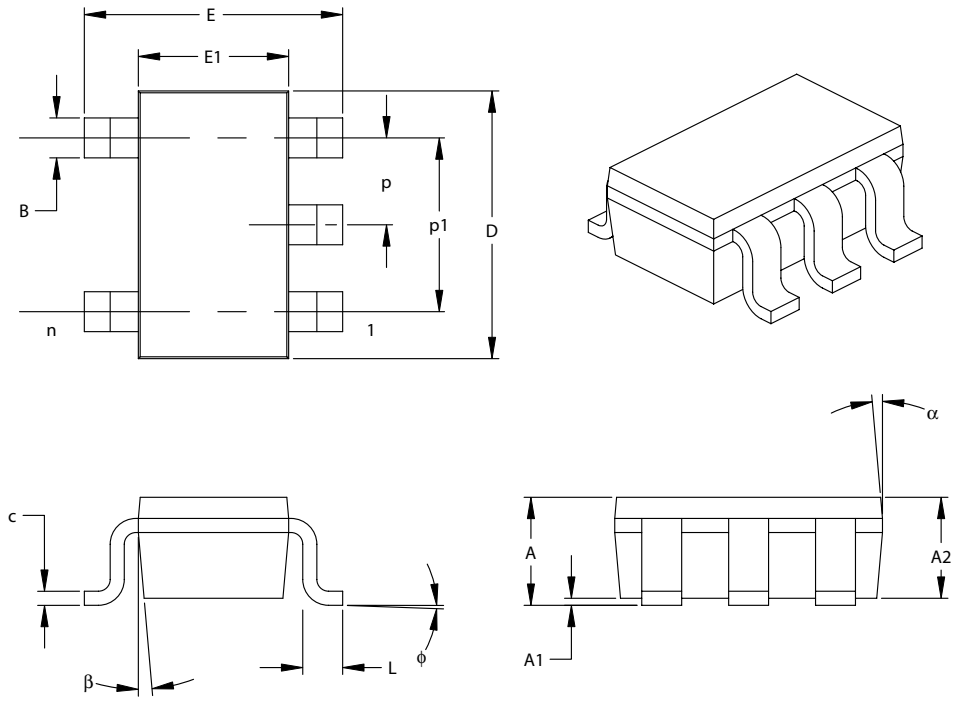
14-Lead TSSOP **(MCP6274)**



Example:



5-Lead Plastic Small Outline Transistor (OT) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

EIAJ Equivalent: SC-74A

Drawing No. C04-091

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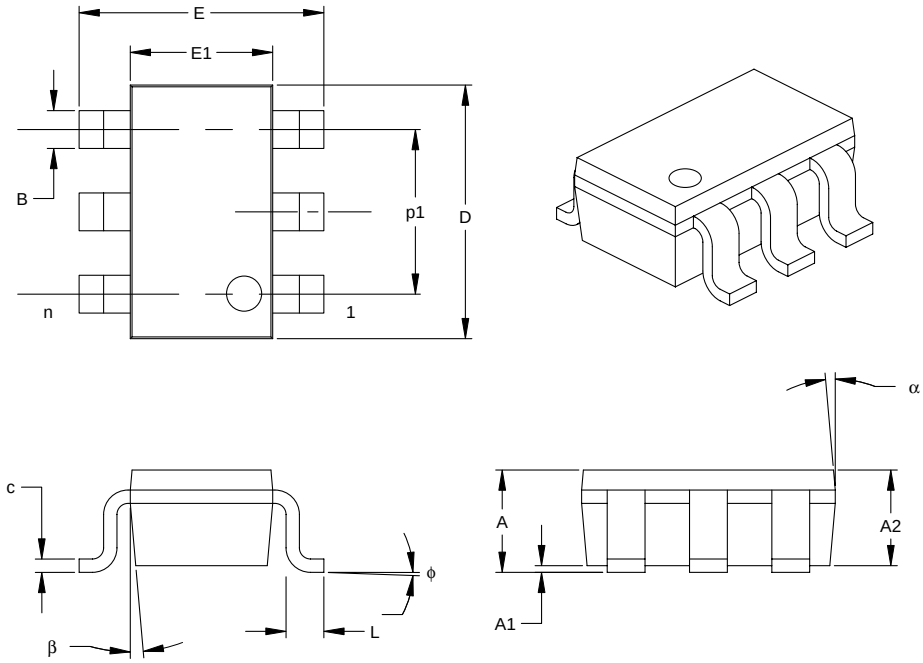
6-Lead Plastic Small Outline Transistor (CH) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		6			6	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

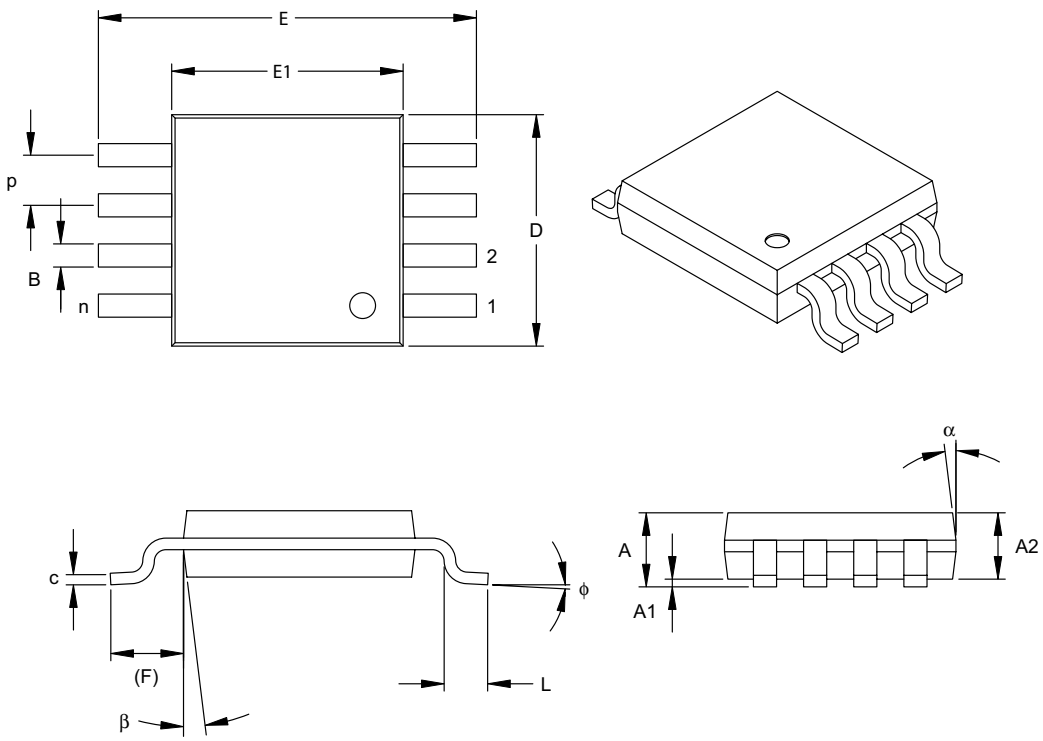
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

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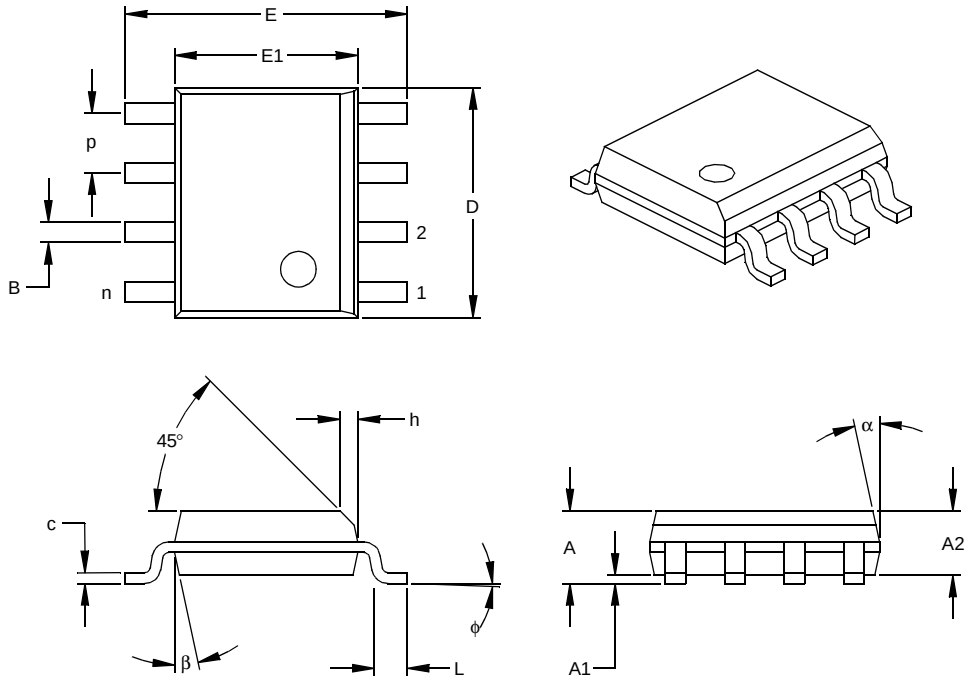
d Plastic Dual In-line (P) – 300 mil (PDIP)

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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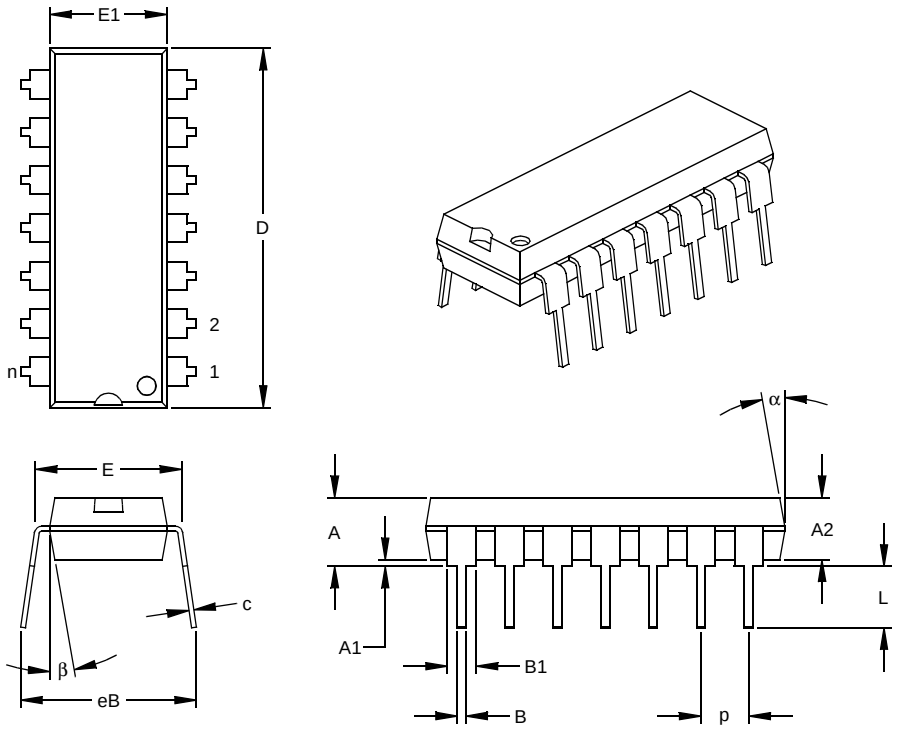
14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

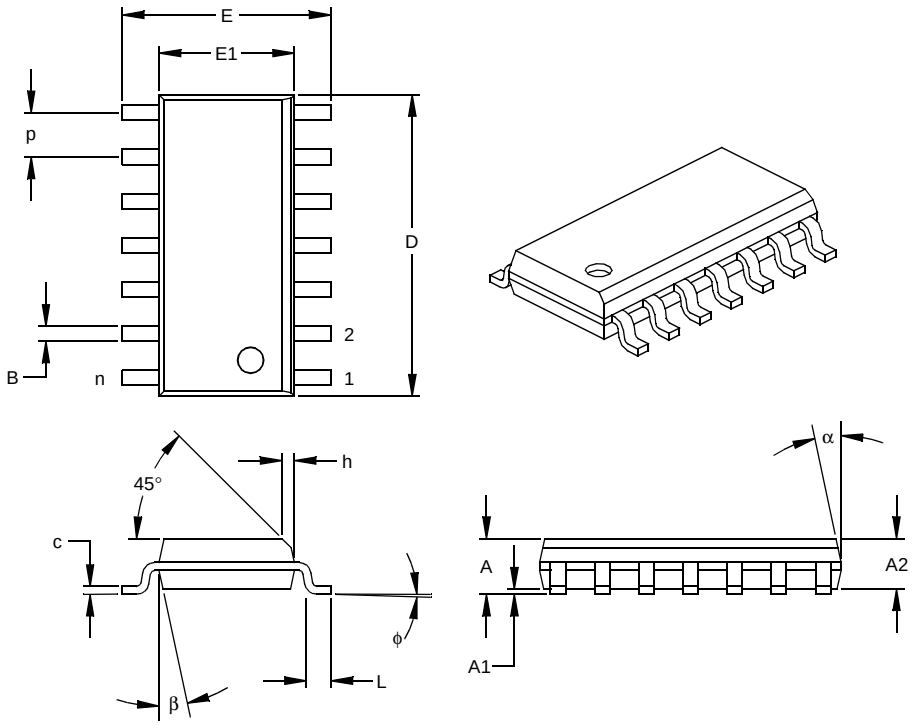


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

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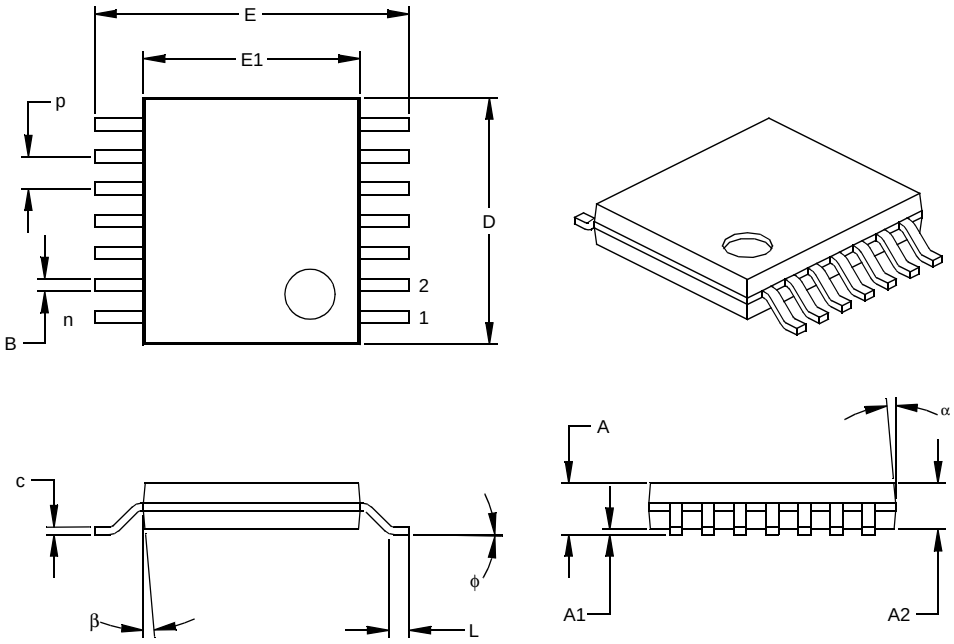
14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (June 2003)

Original data sheet release.

Revision B (October 2003)

Revision C (June 2004)

Revision D (December 2004)

The following is the list of modifications:

1. Added SOT-23-5 packages for the MCP6271 and MCP6271R single op amps.
2. Added SOT-23-6 packages for the MCP6273 single op amp.
3. Added **Section 3.0 “Pin Descriptions”**.
4. Corrected application circuits (**Section 4.8 “Application Circuits”**).
5. Added SOT-23-5 and SOT-23-6 packages and corrected package marking information (**Section 6.0 “Packaging Information”**).
6. Added Appendix A: Revision History.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	X	/XX
Device		Temperature Range	Package

Device:	MCP6271:	Single Op Amp
	MCP6271T:	Single Op Amp (Tape and Reel) (SOIC, MSOP, SOT-23-5)
	MCP6271RT:	Single Op Amp (Tape and Reel) (SOT-23-5)
	MCP6272:	Dual Op Amp
	MCP6272T:	Dual Op Amp (Tape and Reel) (SOIC, MSOP)
	MCP6273:	Single Op Amp with Chip Select
	MCP6273T:	Single Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP, SOT-23-6)
	MCP6274:	Quad Op Amp
	MCP6274T:	Quad Op Amp (Tape and Reel) (SOIC, TSSOP)
	MCP6275:	Dual Op Amp with Chip Select
	MCP6275T:	Dual Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP)
Temperature Range:	E = -40°C to +125°C	
Package:	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6271, MCP6271R)
	CH =	Plastic Small Outline Transistor (SOT-23), 6-lead (MCP6273)
	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC, (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	ST =	Plastic TSSOP (4.4mm Body), 14-lead

Examples:

a)	MCP6271-E/SN:	Extended Temperature, 8LD SOIC package.
b)	MCP6271-E/MS:	Extended Temperature, 8LD MSOP package.
c)	MCP6271-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6271T-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.
a)	MCP6272-E/SN:	Extended Temperature, 8LD SOIC package.
b)	MCP6272-E/MS:	Extended Temperature, 8LD MSOP package.
c)	MCP6272-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6272T-E/SN:	Tape and Reel, Extended Temperature, 8LD SOIC package.
a)	MCP6273-E/SN:	Extended Temperature, 8LD SOIC package.
b)	MCP6273-E/MS:	Extended Temperature, 8LD MSOP package.
c)	MCP6273-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6273T-E/CH:	Extended Temperature, 6LD SOT-23 package.
a)	MCP6274-E/P:	Extended Temperature, 14LD PDIP package.
b)	MCP6274T-E/SL:	Tape and Reel, Extended Temperature, 14LD SOIC package.
c)	MCP6274-E/SL:	Extended Temperature, 14LD SOIC package.
d)	MCP6274-E/ST:	Extended Temperature, 14LD TSSOP package.
a)	MCP6275-E/SN:	Extended Temperature, 8LD SOIC package.
b)	MCP6275-E/MS:	Extended Temperature, 8LD MSOP package.
c)	MCP6275-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6275T-E/SN:	Tape and Reel, Extended Temperature, 8LD SOIC package.

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