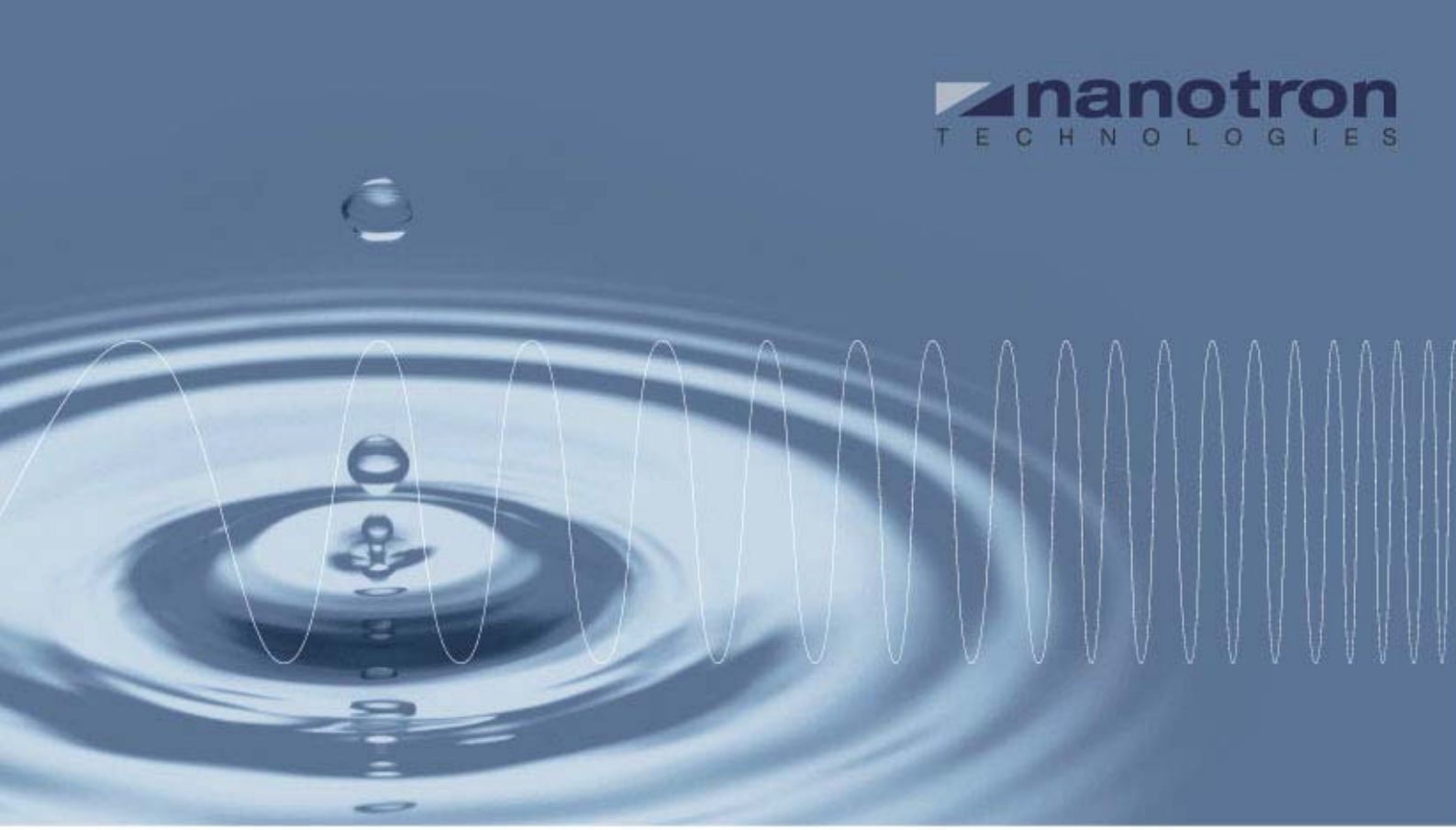

nanoLOC TRX Transceiver (NA5TR1)

Datasheet

Version 1.02

NA-06-0230-0388-1.02

This document contains information on a pre-engineering chip. Specifications and information herein are subject to change without notice.

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CAUTION! Electrostatic Sensitive Device. Precaution should be used when handling the device in order to prevent permanent damage.

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1 Chip Summary

1.1 Key Features

- Integrated 2.45 GHz ISM RF transceiver, including:
  - Ranging (link distance estimation) support in hardware
  - FDMA (Frequency Division Multiplex Access) with 3 non-overlapping frequency channels and 7 overlapping frequency channels
  - 0 dBm nominal output power
  - System RF sensitivity equal to ≤-95 dBm @ BER=0.001 at nominal conditions
  - System RF sensitivity equal to ≤-97 dBm @ BER=0.001 at nominal conditions, except FEC is on.
  - RSSI sensitivity to –95 dBm (for matched chirp only) at nominal conditions
- Extended operating temperature range (industrial): $T_{ambient}$ = -40°C ... +85°C
- In-band Carrier to Interference Ratio (C/I): C/I = 0 … 3 dB @ 250 kbps @ C = -80 dBm
- Allows unregulated 2.3 V…2.7 V supply voltage
- Power down mode for increased current saving
- Extremely low shut down current ≤2 µA (typical)
- Software controlled power supply for external microcontroller allows further energy saving
- 32768 Hz clock available for external microcontroller. Other frequencies also available (feature clock)
- Integrated fast SPI interface (32 Mbps, slave mode only)
- Integrated frame buffering
- Integrated microcontroller management function
- General purpose 4-bit digital I/Os for easy connection to sensors and actors
- Hardware MAC accelerators for time critical and computation intensive tasks

1.2 Simplified Block Diagram

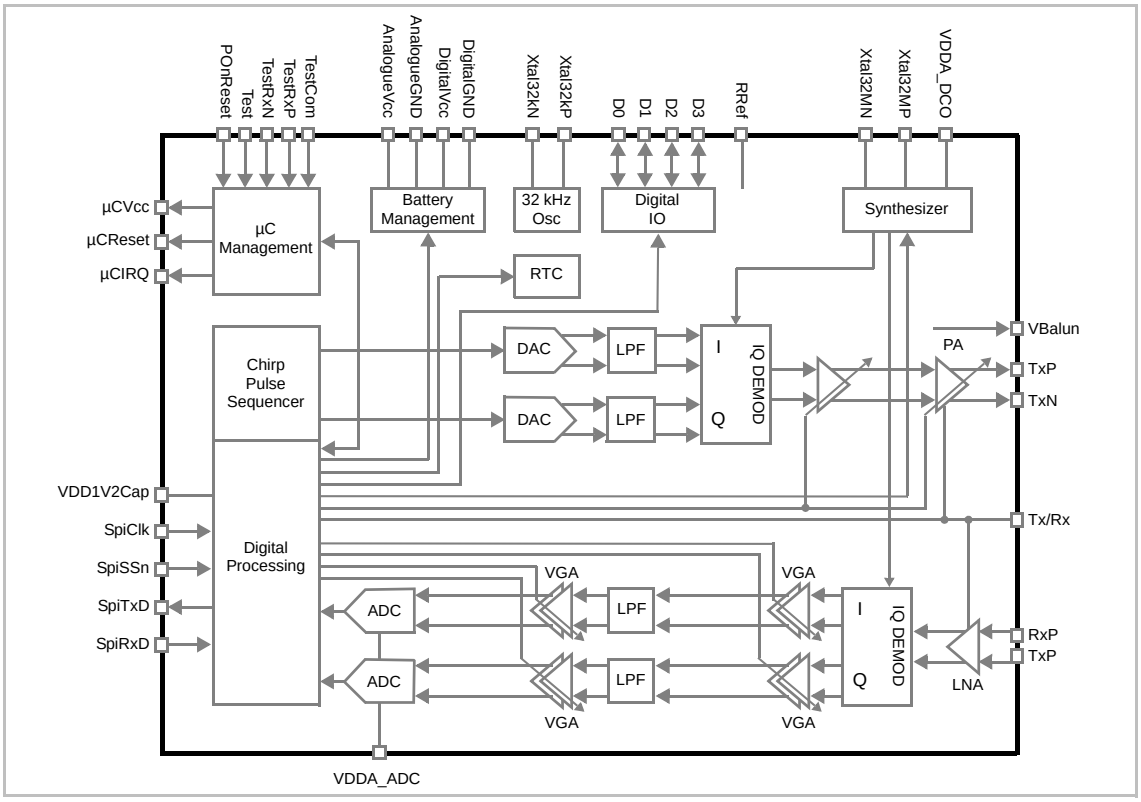

Figure 1: nanoLOC block diagram (simplified)

1.3 Target Applications

- Logistics: Active RFID / RTLS for asset tracking
- Industrial monitoring and control
- Medical applications
- Security / Government applications

1.4 Sample Application Showing Recommended Circuitry

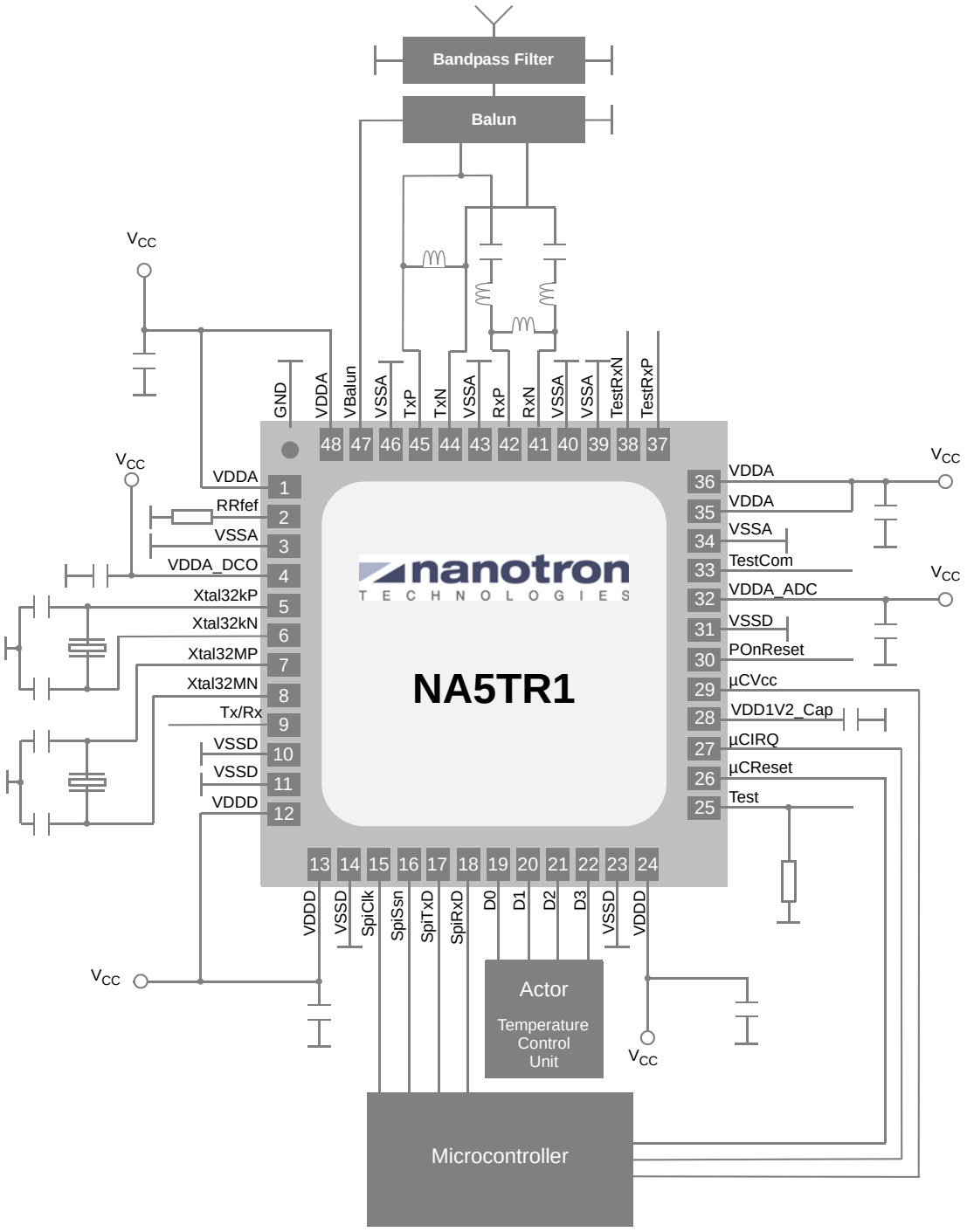

Figure 2: Sample application showing recommended circuitry

2 Product Features

MAC / PHY Features	

■ Fully Integrated 2.45 GHz ISM RF transceiver
  ■ Full hardware supported Ranging (link distance estimation) capability, in standard or increased accuracy modes, based on SDS-TWR
  ■ Built-In IEEE 802.15.4a compatibility
  ■ FDMA (Frequency Division Multiplex Access) with frequency channels selectable by application software
  ■ Two independent channel (non-overlapping frequency band) allocations, with one for Europe and one for USA
  ■ Seven additional FDMA channels (overlapping frequency bands) are available
■ CSMA/CA, TDMA
■ Low C/I (Carrier to Interference) Ratio
■ Programmable digital support block
■ Output RF power control (controlled in several steps) between -33 dBm to 0 dBm
	■ Link distances (in-door, outdoors, and free space) for EIRP=1 mW (PEP): 10 m, 100 m, 300 m respectively (at nominal conditions)
	■ Receiver sensitivity (at nominal conditions) in the range of –93 dBm @ BER = 0.001
	■ Low radiated power: -33 dBm for 10 m link distance in free space, with isotropic antennas, and at nominal conditions
	■ Internal hardware accelerators for all time critical and computing intensive tasks
	■ RSSI (Radio Signal Strength Indicator) used by CSMA protocol, radiated power management, and bit error rate estimation procedure
	■ Asynchronous (even single bit detection possible without synchronization) or synchronous system
	■ Immunity against Doppler effect

Power Consumption	
■ Extremely low current consumption ■ Battery operation ■ Sleep-mode/wake-up operation to expand battery lifetime and reduce human exposure	■ Software controlled, switchable power supply for external microcontroller for further energy saving ■ Main analog signal processing – simplicity, cheap, low power consumption

Transmit and Receive	
■ Configurable transmit and receive buffers ■ 4 kbit receive/transmit buffers to store several frames	■ Several receive and transmit frames can be stored simultaneously in the buffers

Data Rates	
■ Data rates selectable between 125 kbit/s and 1 Mbit/s (2 Mbit/s for special cases) ■ Low data rate over air interface in relationship with theoretical data rate for this particular modulation	■ Big processing gain implicates improved noise immunity ■ Low data rate of the network traffic in relationship with the data rate over air interface – simple protocols with high overhead are acceptable

Required Additional Components	
■ Very few external components required	■ CDDL integrated into chip (no external filters required)

Digital I/O Interface	
■ Simple, flexible interface	■ Fast (32 Mbps) worldwide accepted Serial Peripheral Interface (SPI) interface (slave mode only)

Radiated Power	
■ Reduced radiated power to absolute minimum reduces human exposure. ■ Additionally chirp modulation dramatically reduces power spectral density of emitted signal	■ Reduced power spectral density of the signal directly reduces human exposure.

nanoLOC Networks	
■ Network topology not limited by hardware implementation	■ Proposed network topology (if any)

Package	
■ Small size	■ 7mm x 7mm x 1mm Leadless Leadframe package

Additional Features	
■ Development tools available ■ Simple API access to chip registers using nTRX drivers	■ Easy to use evaluation boards for testing nanoLOC in any environment ■ Ready to customize development boards for quick application development

3 Applications

The nanoLOC TRX transceiver is ideal for extremely low-cost, battery-operated applications that require a non-licensed robust wireless link over short distances. These applications can be installed either indoors or outdoors. This chip is also ideal for applications that require low human exposure, and for developers, simplicity.

Target applications are primarily in the capital goods market, in particular, OEM customers that install transceivers into their industrial application products.

Logistics: Active RFID / RTLS for Asset Tracking	
■ Asset Identification and tracking	■ Inventory Management
■ Visitor/Employee Identification and tracking	■ Logistics applications (location)

Medical	
■ Medical monitoring	■ Medical personnel monitoring
■ Medical equipment tracking	■ Medical control applications that require reduced human exposure to RF energy
■ Patient monitoring	

Industrial Monitoring and Control	
■ Sensor networks and Actor RF Networks	■ Actor networks
■ Manufacturing and production processing equipment	■ Heating, ventilation, and air conditioning (HVAC)

Security / Government	
■ Fire Fighting	■ Security
■ Police	■ Ambulance Services

3.1 Application Software and Hardware

Nanotron offers a generic set of application software that can be used to quickly develop custom applications based on nanoLOC.

Contact Nanotron Sales for an Evaluation Kit based on nanoLOC to evaluate and prove nanoLOC technology in an environment of your own choosing, as well as a Development Kit for fast application development using nanoLOC.

4 Quick Reference Data

Table 1: Quick reference data

Parameter	Value	Unit
Maximum supply voltage	2.7	V
Minimum supply voltage	2.3	V
Maximum output power	0	dBm
Maximum data rate	2	Mbps
Sensitivity at nominal conditions	-95	dBm
Sensitivity at nominal conditions and FEC on	-97	dBm
Supply Current		
In transmit mode @ -10 dBm output power & nominal conditions	25	mA
In transmit mode @ 0 dBm output power & nominal conditions	30	mA
In receive mode & nominal conditions	33	mA
In shut-down mode	2	µA
Operating temperature range	-40 to +85	°C
Frequency Channels (FDMA Mode, non-overlapping channels)		
Number of frequency channels	3	Number
Center frequency of channel no. 1 (Europe)	2412	MHz
Center frequency of channel no. 2 (Europe)	2442	MHz
Center frequency of channel no. 3 (Europe)	2472	MHz
Center frequency of channel no. 1 (USA)	2412	MHz
Center frequency of channel no. 2 (USA)	2437	MHz
Center frequency of channel no. 3 (USA)	2462	MHz
Frequency Channels (FDMA Mode, overlapping channels)		
Number of frequency channels	7	Number
Center frequency of channel no. 1 (overlapping)	2412	MHz
Center frequency of channel no. 2 (overlapping)	2422	MHz
Center frequency of channel no. 3 (overlapping)	2432	MHz
Center frequency of channel no. 4 (overlapping)	2442	MHz
Center frequency of channel no. 5 (overlapping)	2452	MHz
Center frequency of channel no. 6 (overlapping)	2462	MHz
Center frequency of channel no. 7 (overlapping)	2472	MHz

Table 1: Quick reference data (Continued)

Parameter	Value	Unit
Nominal frequency bandwidth of the channel @ -30 dBr	22	MHz
Nominal frequency bandwidth for ranging @ -30 dBr	83	MHz
Typical Operational Voltages		
Typical Power supply voltage V_{DDA} (analogue block)	2.5	V
Typical Power supply voltage V_{DDD} (digital block)	2.5	V

4.1 Nominal Conditions

Nominal conditions are as specified below, except otherwise noted:

- Reference design has been used.
- T_{junct} = 30°C
- V_{SSA} = V_{SSD} = GND
- V_{DDA} = V_{DDD} = +2.5 V
- Transmission / reception @ 250 kbps
- Nominal frequency bandwidth of the channel B = 22 MHz @ -30 dBr
- Raw data mode
- No CRC
- No FEC
- No encryption
- Bit scrambling
- No ranging
- BER = 0.001 during receive mode
- RF output power (PEP) during transmit phase = 0 dBm EIRP measured during continuous transmission
- Nominal process
- All RF ports are impedance matched according to the specification.
- All RF power are measured on the IC terminals (pins)
- For link distance measurement, two identical nanoLOC systems are used

5 The nanoLOC System

Ranging Capabilities Based on SDS-TWR

An important feature of the nanoLOC system is its ranging capabilities, which are based on a ranging technique developed by Nanotron – Symmetrical Double-Sided Two Way Ranging, or SDS-TWR. This technique estimates the link distance between two communicating nanoLOC nodes. SDS-TWR is based on precise time measurements of the signals propagating forward and backwards between two nodes. This feature can be performed using expanded frequency bandwidth for increased distance measurement accuracy. The nanoLOC system provides two Ranging accuracy levels:

- Standard Ranging Accuracy

  Data transmission is combined with ranging.

- Improved Ranging Accuracy

  Only Ranging is performed, as the entire available ISM frequency bandwidth is used.

  RF communication can be resumed by switching back to Standard Ranging Mode.

FDMA (Frequency Division Multiple Access)

This system utilizes the 2.4 GHz licence-free ISM band, which is allocated worldwide for Industrial, Scientific and Medical applications. Notably, home equipment such as microwave ovens also operate in this band. Consequently, other services operating in this band, such as wireless communication, must accept and tolerate potential interferences and disturbances. As a means of counteracting in-band and out-of-band disturbances, nanoLOC provides FDMA (Frequency Division Multiple Access), which divides the 2.4 GHz bandwidth into different frequency bands:

- Two independent channel (non-overlapping frequency bands) allocations: one for Europe and one for USA

- Seven additional FDMA channels (overlapping frequency bands) are available

Low C/I (Carrier to Interference) Ratio

The ISM frequency band is very “noisy” as it often has many non-wanted signals (noise) that detract from the potential quality of the wanted signals (carrier). Due to nanoLOC’s high processing gain, the carrier to interference ratio is extremely low and operates effectively in this “noisy” ISM band.

For example. with nanoLOC, RF communication (with increased error rate) is possible with the following configuration:

- Communication link between two nanoLOC devices of about 25 m
- Active microwave oven is approximately 1 to 2 m from the nanoLOC receiver.

Such a scenario would be typical for home applications.

6 The nanoLOC IC

The nanoLOC IC is a extremely low power, highly integrated mixed signal chip utilizing Chirp Spread Spectrum, a novel wireless communication technology developed by Nanotron.

Fully Integrated Chip

nanoLOC is a fully integrated single chip transceiver with ranging capabilities. It consists of:

- Complete analog receiver (from antenna output to the demodulated digital data output) with minimal number of external elements.
- Complete transmitter (from digital data input to output from RF power amplifier, which can be directly connected to the antenna input).
- Programmable support block including power management, battery voltage monitor, and much more. All important functions of this block can be setup and controlled by application software.

Built-In IEEE 802.15.4a Compatibility

The nanoLOC IC has been designed with the new IEEE 802.15.4a standard as a guide, which is the utilization of sub-chirps. In this standard, the PHY layer employs an 8-ary Differentially Bi-Orthogonal Chirp Spread Spectrum (DBO-CSS) modulation technique.

Programmable Digital Support Block

This programmable digital support block communicates with an external microcontroller via a Serial Peripheral Interface (SPI). This block performs several service functions including RF-front-end control and calibration for the analogue part of the IC. Additionally, this block includes support for some fundamental protocol stack functions of the MAC. These include MAC Frame coding, frame buffering, bit processing (such as CRC generation/checking and en/decryption), as well as MAC protocol handling (such as medium access control and automatic acknowledgement-frame transmission). Additional functions of this block include support for Ranging, Real Time Clock maintenance, and power-down/wake-up management. All functions of this block can be setup and controlled by application software, which is executed by a microcontroller connected to the chip by means of the SPI interface.

Robust, Short Distance Wireless Networks

This nanoLOC IC is designed to build up robust, short distance wireless networks operating in the 2.45 GHz ISM band that also require extremely low power consumption over a wide range of the operating temperatures. For battery operating applications requiring a long battery life (for several years, for example), this IC offers an ideal solution.

Chirp Spread Spectrum

For communication over the air, the nanoLOC chip uses chirp technology developed by Nanotron – Chirp Spread Spectrum (CSS). A chirp pulse is a frequency modulated pulse that changes monotonic from a lower value to a higher value (Upchirp) or from a higher value to a lower value (Downchirp) In nanoLOC, Upchirps and Downchirps have a symbol duration t_{symbol} = 1 µs, 2 µs, 4 µs and a frequency bandwidth B_{chirp} = 22 MHz. Application software can define and select different data rates between 125 kbit/s and 1 Mbit/s. For special cases 2 Mbit/s can be selected.

Receiver Sensitivity

The sensitivity of the nanoLOC chip is defined by the raw data mode (when data is not coded) where BER = 0.001. The sensitivity is $P_{sensitivity}$ = -95 dBm or better, which is achieved at nominal conditions. Link budget is equal to A_{link_budget} = 95 dB.

If both transceivers that are establishing a wireless communication link are equipped with an identical patch antenna (each with gain G_A = 3 dBi) then (for BER = 0.001) the maximum link attenuation between antennas is equal to:

$$A_{path\text{-}att\text{-}max} = P_{transmitted\text{-}max} + 2*G_A + P_{sensitivity} = 101 \text{ dB}$$

To increase the Link Budget value and/or increase the quality of the wireless link (for example, reduce BER value) FEC can be activated. When FEC is on (activated) the receiver's sensitivity $P_{sensitivity\text{-}FEC}$ = -97 dBm or better, which is achieved at nominal conditions, except FEC is on. For this scenario, maximum link attenuation is increased to:

$$A_{path\_att\_max\_fec} = 103 \text{ dB}.$$

Maximum Transmission Output Power

The maximum transmission power of the nanoLOC chip is $P_{transmitted\text{-}max}$ = 0 dBm at nominal conditions. The transmission power can be programmed by the application software and can be stepwise reduced (from maximum 0 dBm) in several steps. The transmission power can vary from –33 dBm to 0 dBm (without any additional external power amplifier, attenuator, etc.).

Frame Buffers

Due to nanoLOC's use of frame buffers, even a very slow microcontroller can work with this "high speed" chip. nanoLOC's 4 kbit receive or transmit buffers can store several frames (depending of the frame length). For instance, several receive and transmit frames can be stored simultaneously in the buffers. This eliminates the problem of different peak data rates between the following two interfaces:

- Digital interface between a microcontroler and the nanoLOC chip
- Air interface between nanoLOC nodes

Minimum External Components Required

The chip is designed in such a way that only a minimum number of external elements are required to build up a fully operational bi-directional wireless communication node.

Additional Chip Features

The chip also includes the following additional features:

- Power management module
- Wake-up circuitry
- Real Time Clock
- Low battery alarm
- Encryption/decryption
- CRC (Cyclic Redundancy Checksum) generation/check block
- FEC (Forward Error Correction) block
- Radio Signal Strength Indicator (RSSI).

These features are supported and controlled by the application software.

For example, the RSSI value can be used to indicate when the air interface is free or busy – this information is required when CSMA (Carrier Sense Multiplex Access) is used.

7 Block Diagram

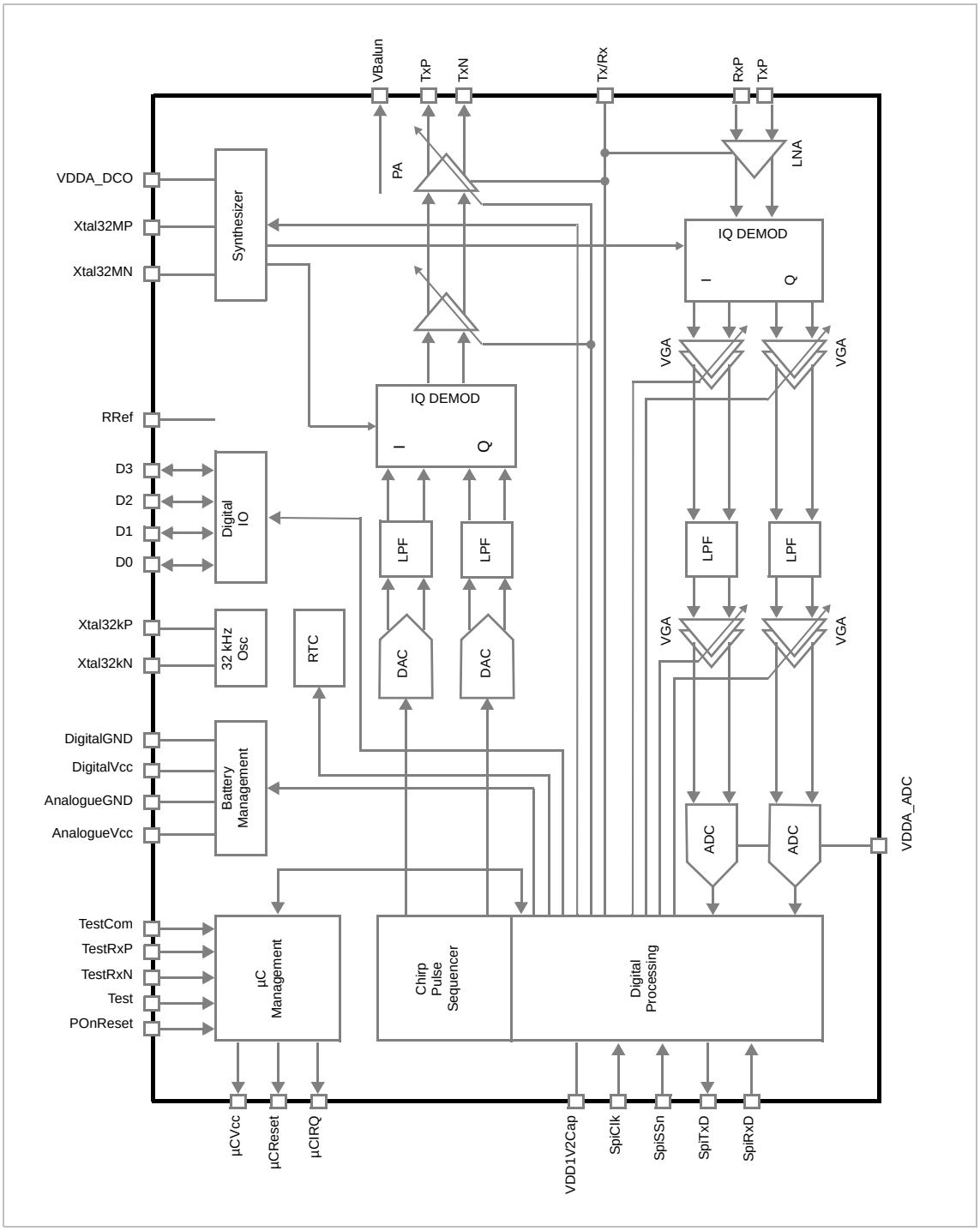

Figure 3: nanoLOC TRX Transceiver (NA5TR1) block diagram (simplified)

8 Absolute Maximum Ratings

Table 2: Absolute maximum ratings

Parameter	Value[1]	Unit
Temperature		
Maximum operating temperature	85	°C
Maximum junction temperature	95	°C
Maximum storage temperature	125	°C
Reflow solder temperature (lead-free package)	242	°C
Voltages		
Power supply voltage VDDA (analogue block)	2.7	V
Power supply voltage VDDD (digital block)	2.7	V
Power		
Total power dissipation FDMA-CSS mode	130	mW
Total power dissipation CSS Ranging mode	172	mW
Electrostatic Discharge Protection (ESD Protection)		
Maximum ESD input potential, Human Body Model	1000	V

1. It is critical that the ratings provided in Absolute Maximum Ratings be carefully observed. Stress exceeding one or more of these limiting values may cause permanent damage to the device.

9 Pin Connections

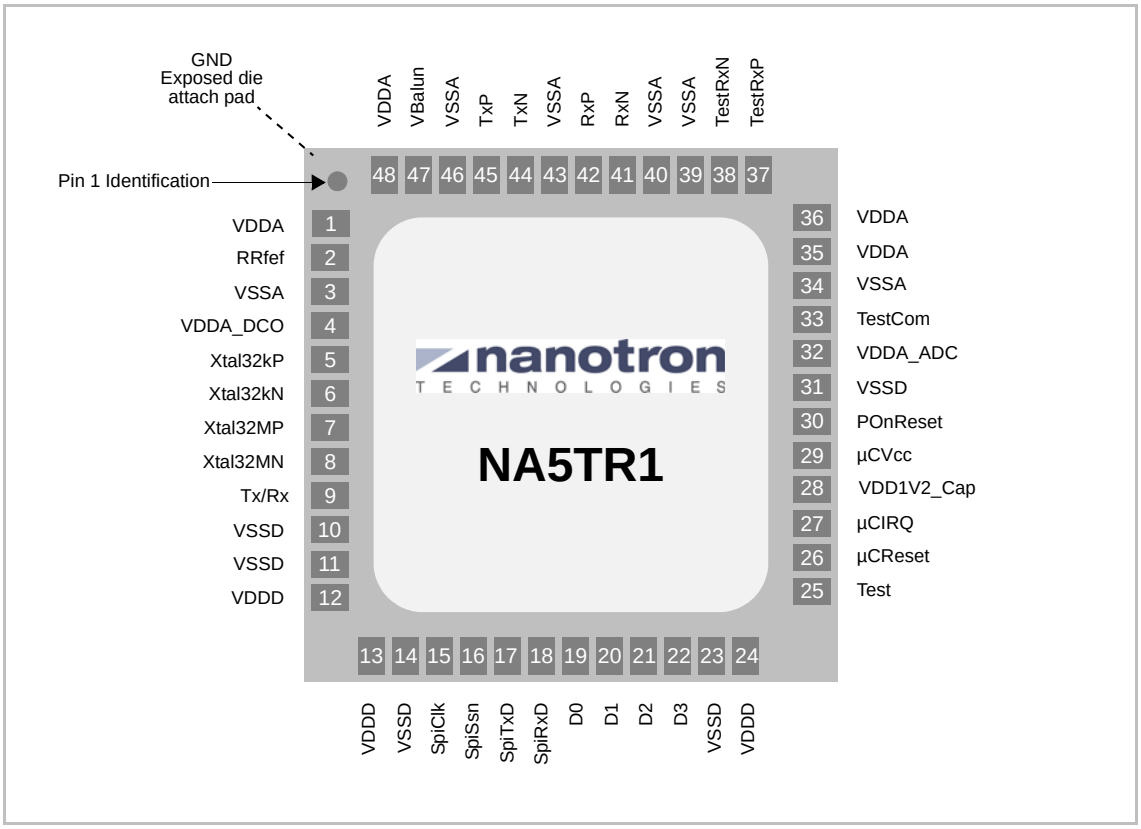

Figure 4: nanoLOC TRX Transceiver (NA5TR1) pin assignment (top view)

9.1 Pin Descriptions

Table 3: Pin description

Pin	Name	Type	Description
–	GND	Ground (analog)	Exposed die attach pad: must be connected to solid ground plane.
1	VDDA	Supply	Power supply for analog parts.
2	RRef	Analog IO	External precise reference resistor. See Electrical Specifications for details.
3	VSSA	Supply	Power supply for analog parts.
4	VDDA_DCO	Supply	Power supply for DCO.
5	Xtal32kP	Analog IO	32.768 kHz crystal oscillator pin 1 or input for an external 32.768 kHz clock generator. Used to connect crystal or active frequency reference
6	Xtal32kN	Analog IO	32.768 kHz crystal oscillator pin 2.
7	Xtal32MP	Analog IO	32 MHz crystal oscillator pin 1 or input for an external 32 MHz clock generator. Usage: Connect crystal or active frequency reference
8	Xtal32MN	Analog IO	32 MHz kHz crystal oscillator pin 2.

Table 3: Pin description (Continued)

Pin	Name	Type	Description
9	Tx/Rx	Digital Output	Distinguishes between the TX and RX phase. Can also be used to provide an external power amplifier control. Active Low during TX, otherwise High.
10	VSSD	Supply	Power supply for digital parts.
11	VSSD	Supply	Power supply for digital parts.
12	VDDD	Supply	Power supply for digital parts.
13	VDDD	Supply	Power supply for digital parts.
14	VSSD	Supply	Power supply for digital parts.
15	SpiClk	Digital Input	SPI Clock.
16	SpiSSn	Digital Input	SPI Slave Selected; Active Low.
17	SpiTxD	Digital Output	SPI Transmit Data (MISO).
18	SpiRxD	Digital Input	SPI Receive Data (MOSI).
19	D0	Digital IO	General purpose Digital Input or Output line 0. For usage, see *nanoLOC TRX User Guide*.
20	D1	Digital IO	General purpose Digital Input or Output line 1. For usage, see *nanoLOC TRX User Guide*.
21	D2	Digital IO	General purpose Digital Input or Output line 2. For usage, see *nanoLOC TRX User Guide*.
22	D3	Digital IO	General purpose Digital Input or Output line 3. For usage, see *nanoLOC TRX User Guide*.
23	VSSD	Supply	Power supply for digital parts.
24	VDDD	Supply	Power supply for digital parts.
25	Test	N.A	Internal test pin; connect to GND.
26	µCReset	Digital Output	Used to reset an external microcontroller at power-up and wake-up. Active Low during normal operation.
27	µCIRQ	Digital Output	Interrupt Request. Can be used to send an interrupt request to an external microcontroller. Logic levels can be programmed (For details, see *nanoLOC TRX User Guide*).
28	VDD1V2_Cap	Supply	1.2 V digital power supply decoupling. See Electrical Specifications for details.
29	µCVcc	DC Output	Switchable power supply for external microcontroller.
30	POnReset	Digital Input	Power on reset signal. See Electrical Specifications for details.
31	VSSD	Supply	Power supply for digital parts.
32	VDDA_ADC	Supply	Power supply for analog parts (Rx ADC).
33	TestCom	N.A.	Internal test pin; must not be connected.
34	VSSA	Supply	Power supply for analog parts.
35	VDDA	Supply	Power supply for analog parts.

Table 3: Pin description (Continued)

Pin	Name	Type	Description
36	VDDA	Supply	Power supply for analog parts.
37	TestRxP	N.A.	Internal test pin; must not be connected.
38	TestRxN	N.A.	Internal test pin; must not be connected.
39	VSSA	Supply	Power supply for analog parts.
40	VSSA	Supply	Power supply for analog parts.
41	RxN	RF Input	Differential receiver input (inverted).
42	RxP	RF Input	Differential receiver input.
43	VSSA	Supply	Power supply for analog parts.
44	TxN	RF Output	Differential transmitter output (Inverted).
45	TxP	RF Output	Differential transmitter output.
46	VSSA	Supply	Power supply for analog parts.
47	VBalun	DC Output	DC voltage for RF output stage. See Electrical Specifications for details.
48	VDDA	Supply	Power supply for analog parts.

10 Electrical Specifications

In this section, the fundamental electrical specification of the major blocks of the nanoLOC (NA5TR1) chip are specified. The typical values represent the mean production values (nominal process) at nominal operating conditions. The min/max values are guaranteed values over the entire operating range (unless otherwise stated). For a balanced signal, all impedances, signal voltages, etc., refer to the differential signal.

10.1 General / DC Parameters

Table 4: General / DC Parameters

Parameter	Value	Unit
Operating frequency range	2.4 GHz ISM Band	–
Supply voltage range	2.3 … 2.7	V
Modulation method	Chirp	–
Operating temperature range	-40 … +85	°C
Supply current for individual blocks:		
Tx block (P_{out} = 0 dBm)	23	mA
Tx block, ranging with increased accuracy (P_{out} = 0 dBm)	30	mA
Rx block	27	mA
Rx block, ranging with increased accuracy	34	mA
Digital part, Tx mode	7	mA
Digital part, Tx mode, ranging with increased accuracy	9	mA
Digital part, Rx mode	6	mA
Digital part, Rx mode, ranging with increased accuracy	10	mA
Total supply current:		
Tx Mode (P_{out} = 0 dBm)	30	mA
Tx Mode, ranging with increased accuracy (P_{out} = 0 dBm)	39	mA
Rx Mode	33	mA
Rx Mode, ranging with increased accuracy	44	mA
VDD1V2_Cap (Pin 28): 1.2 V digital power supply decoupling.		
Decoupling capacitance (typical)	100	nF
VBalun (Pin 47): DC voltage for RF output stage. This must be fed to TxN and TxP using bias-Tees or a balun transformer with center tap. Min and max Values for decoupling bypass capacitor are shown below. (It is not a block capacitor). See also the reference design.		
Decoupling bypass capacitor Min	27	pF
Decoupling bypass capacitor Max	47	pF
µCVcc (pin 29): Switchable power supply for external microcontroller.		

Table 4: General / DC Parameters (Continued)

Parameter	Value	Unit
Maximum capacitive load	10	µF
Maximum output current	10	mA
RRef (pin 2): External precise reference resistor.		
Resistance	10	kΩ
Recommended resistance tolerance	1	%

10.2 Transmitter (TX)

10.2.1 General Parameters

Table 5: Transmitter – general parameters

Parameter	Value	Unit
Transmitter nominal output power	0	dBm
Dynamic for output power control	≥ 33	dB
Number of steps for output power control	64	Number
Load impedance	200	Ohm
Type of load	Balanced	–
Transmitter spurious outputs (1 GHz ... 12.5 GHz)	-80	dBm/Hz
Transmitter carrier suppression	-20	dBc
Number of frequency channels (FDMA Mode, non-overlapping channels), according to IEEE 802.15.4a standard	3	Number
Centre frequency of FDMA channel no. 1 (Europe)	2412	MHz
Center frequency of FDMA channel no. 2 (Europe)	2442	MHz
Centre frequency of FDMA channel no. 3 (Europe)	2472	MHz
Centre frequency of FDMA channel no. 1 (USA)	2412	MHz
Centre frequency of FDMA channel no. 2 (USA)	2437	MHz
Centre frequency of FDMA channel no. 3 (USA)	2462	MHz
Number of frequency channels (FDMA Mode, overlapping channels), according to IEEE 802.15.4a standard	7	Number
Center frequency of channel no. 1 (overlapping)	2412	MHz
Center frequency of channel no. 2 (overlapping)	2422	MHz
Center frequency of channel no. 3 (overlapping)	2432	MHz
Center frequency of channel no. 4 (overlapping)	2442	MHz
Center frequency of channel no. 5 (overlapping)	2452	MHz

Table 5: Transmitter – general parameters (Continued)

Parameter	Value	Unit
Center frequency of channel no. 6 (overlapping)	2462	MHz
Center frequency of channel no. 7 (overlapping)	2472	MHz
Carrier frequency accuracy (relative), CSS mode	± 70	ppm
Carrier frequency accuracy (absolute), CSS mode	± 171	ppm
VBalun (Pin 47): DC voltage for RF output stage. This must be fed to TxN and TxP using bias-Tees or a balun / transformer with center tap. Min and max Values for decoupling bypass capacitor are shown below. RF ceramic type with low serial inductance is recommended. See also the reference design.		
Decoupling bypass capacitor min capacitance	27	pF
Decoupling bypass capacitor max capacitance	47	pF

10.2.2 Programmable RAM for Chirp Sequencer

Table 6: Transmitter – Programmable RAM for Chirp Sequencer

Parameter	Value	Unit
Memory type	Single port RAM	–
Memory organization	24 x 256	Number
Number of memory banks	2	Number
Width of output data bus for each memory bank	6	Bit
Number of memory cells in one bank	256	Number
Width of address bus	8	Bit

10.2.3 Chirp Specification (CSS)

Table 7: Transmitter – Chirp specification (CSS)

Parameter	Value	Unit
Chirp duration (programmable)	1, 2 and 4	µs
Symbol rate:		
Nominal	1	Mbaud
Reduced	0.5 and 0.25	Mbaud
Chirp Sequencer Clock Frequency f_{Chirp}, FDMA-CSS mode	32	MHz
Chirp Sequencer Clock Frequency f_{Chirp}, CSS Ranging mode	244.175	MHz

10.3 Receiver (RX)

10.3.1 General Parameters

Table 8: Receiver – general parameters

Parameter	Value	Unit
Receiver sensitivity for CSS, 250 kbps @ BER=10^{-3}, nominal conditions	-95	dBm
Receiver sensitivity for CSS, 250 kbps @ BER=10^{-3}, nominal conditions, except FEC on	-97	dBm
Input impedance	200	Ohm
Type of RX input	Balanced	–
Typical noise figure	3.5	dB
Maximum noise figure	5	dB
Maximum input CSS signal @ BER=10^{-3}	-20	dBm
Number of frequency channels (FDMA Mode, non-overlapping channels), according to IEEE 802.15.4a standard	3	Number
Centre frequency for FDMA channel no. 1 (Europe)	2412	MHz
Centre frequency for FDMA channel no. 2 (Europe)	2442	MHz
Centre frequency for FDMA channel no. 3 (Europe)	2472	MHz
Centre frequency for FDMA channel no. 1 (USA)	2412	MHz
Centre frequency for FDMA channel no. 2 (USA)	2437	MHz
Centre frequency for FDMA channel no. 3 (USA)	2462	MHz
Number of frequency channels (FDMA Mode, overlapping channels), according to IEEE 802.15.4a standard	7	Number
Center frequency of channel no. 1 (overlapping)	2412	MHz
Center frequency of channel no. 2 (overlapping)	2422	MHz
Center frequency of channel no. 3 (overlapping)	2432	MHz
Center frequency of channel no. 4 (overlapping)	2442	MHz
Center frequency of channel no. 5 (overlapping)	2452	MHz
Center frequency of channel no. 6 (overlapping)	2462	MHz
Center frequency of channel no. 7 (overlapping)	2472	MHz
Nominal frequency bandwidth of the channel @ -30 dB	22	MHz
LO frequency accuracy (relative), CSS mode	± 70	ppm
LO frequency accuracy (absolute), CSS mode	± 171	kHz

10.3.2 Radio Signal Strength Indicator (RSSI)

Table 9: Receiver – RSSI

Parameter	Value	Unit
Absolute accuracy	± 6	dB
Resolution	± 2	dB

10.4 Dynamic Performance

Table 10: Dynamic performance

Parameter	Value	Unit
RX initialization time	≤60	µs
TX initialization time	≤24	µs
Switch TX-RX, ACK to DATA Mode	≤3	µs
Switch TX-RX, DATA to DATA Mode	≤3	µs
Switch TX-RX, DATA to ACK Mode	≤3	µs
Switch RX-TX, ACK to DATA Mode	≤24	µs
Switch RX-TX, DATA to DATA Mode	≤24	µs
Switch RX-TX, DATA to ACK Mode	≤8	µs
Start-up time for 32 MHz reference oscillator	≤5	ms
Start-up time for 32768 Hz RTC oscillator	≤2	s

10.5 Quartz Controlled Oscillator for Reference Frequency

Table 11: Quartz controlled oscillator for reference frequency

Parameter	Value	Unit
Frequency f_{REF}	32	MHz
Oscillation type of the reference quartz resonator	Fundamental	–
Recommended max. frequency temperature coefficient of the reference quartz resonator, CSS mode only	± 20	ppm
Recommended max. frequency tolerance of the reference quartz resonator, CSS mode only	± 10	ppm
Recommended max. aging of the reference quartz resonator in 10 years, CSS mode only	± 10	ppm
Accuracy of the reference quartz resonator, CSS and 15.4a compatible mode, including temperature coefficient, frequency tolerance aging, etc.	40	ppm
Maximum equivalent serial resistance of the reference quartz resonator	40	Ohm

Table 11: Quartz controlled oscillator for reference frequency (Continued)

Parameter	Value	Unit
Recommended load capacitance	12	pF
Input for external signal with frequency f_{REF}	Yes	–
Pin name for external signal with frequency f_{REFTC}	Xtal32MP	–

10.6 Quartz Controlled Oscillator for Real Time Clock (RTC)

Table 12: Quartz Controlled Oscillator for Real Time Clock (RTC)

Parameter	Value	Unit
Frequency f_{RTC}	32768	Hz
Oscillation type of the RTC quartz resonator	Fundamental	—
Recommended accuracy of the quartz resonator	± 20	ppm
Maximum equivalent serial resistance of the RTC quartz resonator	80	kOhm
Recommended load capacitance	12.5	pF
Input for external signal with frequency f_{RTC}	Yes	–
Pin name for external signal with frequency f_{RTC}	Xtal32kP	–

10.7 Local Oscillator (LO)

Table 13: Local Oscillator (LO)

Parameter	Value	Unit
Number of frequency channels (FDMA Mode, non-overlapping channels), according to IEEE 802.15.4a standard	3	Number
Nominal LO frequency f_{LO1E} for FDMA channel no. 1 (Europe)	2412	MHz
Nominal LO frequency f_{LO2E} for FDMA channel no. 2 (Europe)	2442	MHz
Nominal LO frequency f_{LO3E} for FDMA channel no. 3 (Europe)	2472	MHz
Nominal LO frequency f_{LO1U} for FDMA channel no. 1 (USA)	2412	MHz
Nominal LO frequency f_{LO2U} for FDMA channel no. 2 (USA)	2437	MHz
Nominal LO frequency f_{LO3U} for FDMA channel no. 3 (USA)	2462	MHz
Number of frequency channels (FDMA Mode, overlapping channels), according to IEEE 802.15.4a standard	7	Number
Center frequency of channel no. 1 (overlapping)	2412	MHz
Center frequency of channel no. 2 (overlapping)	2422	MHz
Center frequency of channel no. 3 (overlapping)	2432	MHz
Center frequency of channel no. 4 (overlapping)	2442	MHz

Table 13: Local Oscillator (LO) (Continued)

Parameter	Value	Unit
Center frequency of channel no. 5 (overlapping)	2452	MHz
Center frequency of channel no. 6 (overlapping)	2462	MHz
Center frequency of channel no. 7 (overlapping)	2472	MHz
Accuracy of the LO frequency, typical CSS mode	± 70	ppm
Accuracy of the LO frequency, worst case, CSS mode	± 100	ppm
Accuracy of the LO frequency, typical 15.4a mode	TBD	ppm
Accuracy of the LO frequency, worst case, 15.4a mode	40	ppm
Minimum LO frequency adjustment range	83.5	MHz
LO noise rejection	-40	dBm

10.8 Digital Interface to Sensor / Actor

Table 14: Digital Interface to Sensor / Actor

Parameter	Value	Unit
Number of general purpose input/outputs	4	Number
Width of each interface	1	Bit
Direction	In/Out (bi-directional, open-drain with pull-up	–
Type	Programmable	–
Logic Input Capacitance	1.5	pF
Output High Level	(0.8 … 1.0) x V_{DDD}	V
Output Low Level	(0 … 0.2) x V_{DDD}	V
Minimum value of Input High Level	(0.6 … 0.7) x V_{DDD}	V
Maximum value of Input Low Level	(0.3 … 0.4) x V_{DDD}	V

10.9 Interface to Digital Controller

Table 15: Interface to digital controller

Pin Name	Parameter	Specification
µCIRQ	Push-pull	Power down mode, leakage current (GND)[1] << 1 µA, slow
SpiTxD, SpiClk, SpiSSn	Input	LVC[2], power down mode, leakage current (GND)* << 1 µA, slow
SpiTxD	Push-pull	LVC[2], power down mode, leakage current (GND)* << 1 µA, slow

1. Sum of all leakage currents plus internal stand-by consumption must not exceed the total stand-by power consumption
2. LVC, V_{DDD} = 2.3 V, V_{OH} = 2.0 V, V_{IH} = 1.7 V, V_{OL} = 0.2 V, V_{IL} = 0.7 V, V_{DDD} = 2.3 … 2.7 V, V_{OH} = 2.4 V, V_{IH} = 1.7...2.0 V, V_{OL} = 0.2 V, V_{IL} = 0.8 V

10.10 Power Supply for the External Digital Microcontroller

Table 16: Power supply for external digital microcontroller

Parameter	Value	Unit
Typical Output Voltage @ I_{Load} = 10mA	VDD-0.04 [1]	V
Maximum Capacitive Load at µCVcc	10	µF
Maximum Output Current	10	mA
Typical Start-Up Time @ I_{Load} = 10mA, C_{Load} = 10uF	1.5	ms

1. *VDD=2.3 … 2.7 V*

11 nanoLOC Package (VFQFPN-48)

11.1 *Micro*LeadFrame® QFN

The nanoLOC TRX Transceiver uses the MicroLeadFrame (MLF®), Quad Flat No-lead (QFN) package. It is a leadless leadframe based Chip Scale Package (CSP) that enhances chip speed, reduces thermal impedance, and reduces the printed circuit board area required for mounting. The small size and very low profile make it ideal for the nanoLOC chip.

MicroLeadFrame® (QFN - Quad Flat No-Lead package) is a near CSP plastic encapsulated package with a copper leadframe substrate. This package uses perimeter lands on the bottom of the package to provide electrical contact to the PCB. The package also offers Exposed Pad technology as a thermal enhancement by having the die attach paddle exposed on the bottom of the package surface to provide an efficient heat path when soldered directly to the PCB. This enhancement also enables stable ground by use of down bonds or by electrical connection through a conductive die attach material.

The basic construction and view of the MLF® package is shown below:

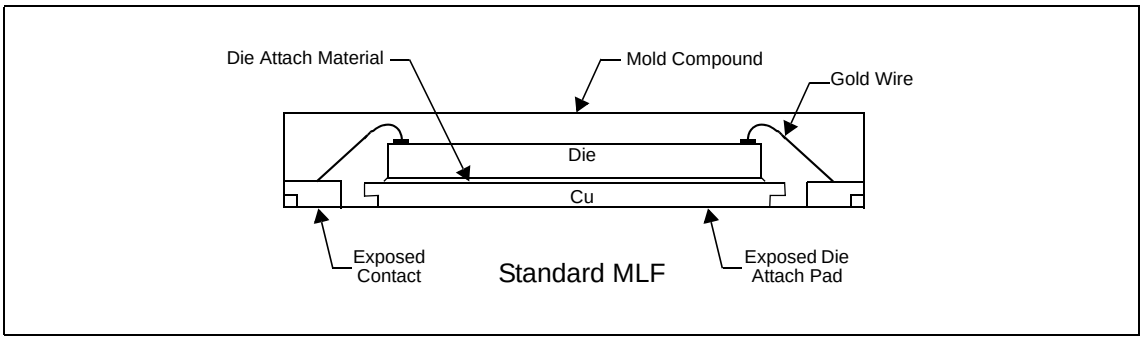

Figure 5: Basic construction of standard MLF package

11.2 VFQFPN-48 Package (7 x 7 x 1.0mm)

The VFQFPN-48 package is used for the nanoLOC TRX Transceiver (NA5TR1). This indicates a thermally enhanced **V**ery thin **F**ine pitch **Q**uad **F**lat **P**ackage **N**o lead chip with 48 pins.

The following figure shows the dimensions of the VFQFPN-48 package.

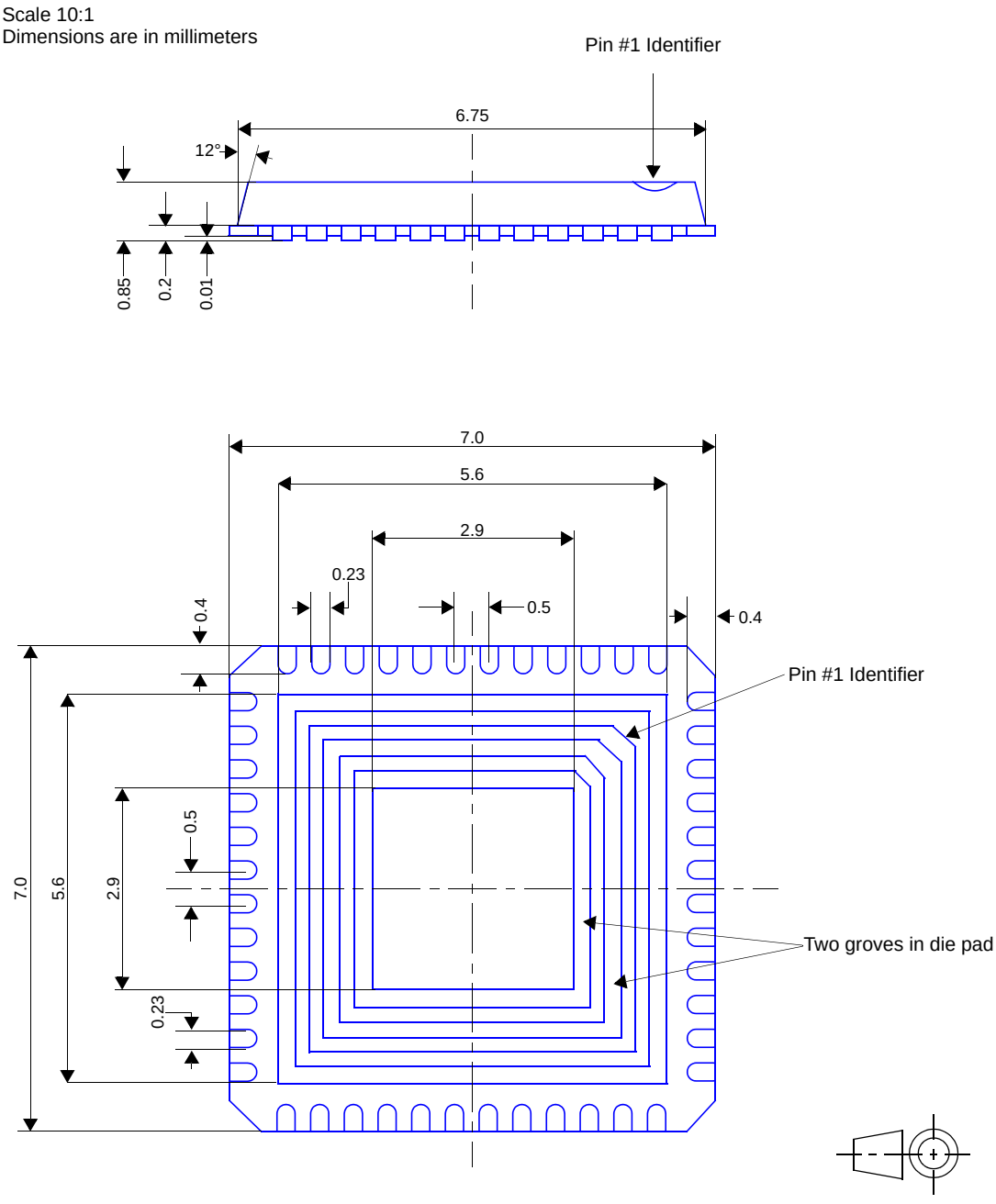

Figure 6: VFQFPN2-48 package dimensions

11.3 Recommended Footprint Dimensions

Recommended footprint data (dimensions) for the NA5TR1 (nanoLOC) chip are shown in the following figure.

Scale 10:1
Dimensions are in millimeters

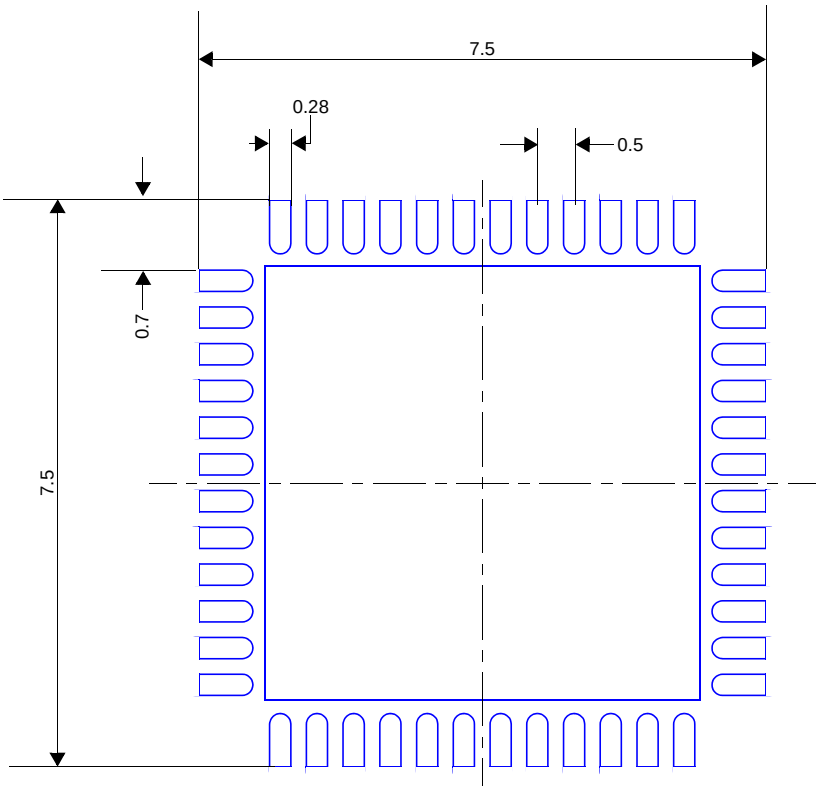

Figure 7: Package VFQFPN2-48 recommended footprint dimensions

12 Abbreviations

µA	Microampere (unit of electrical current)
µC	Microcontroller
µCIrq	External microprocessor interrupt request
µCReset	External microprocessor reset
µCVcc	External microprocessor battery supply voltage
µCVccExt	External microprocessor power supply voltage
µF	Microfarad (unit of electrical capacitance)
µH	MicroHenry (unit of electrical resistance)
µs	Microseconds (unit of time)
Ω	Ohm (unit of electrical resistance)
AC	Alternating Current
Ack	Acknowledgement packet type
ADC	Analogue to Digital Converter
ADD	Actor/sensor
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
ASIC	Application Specific-IC
B	Battery
B	Frequency bandwidth
BA	Balun (See BALUN)
BALUN	Balun Unbalanced
BCH	Bose-Chaudhuri-Hochquenghem
BER	Bit Error Rate
BOM	Bill of Materials
bps	Bits per second (unit of data throughput)
C	Capacitor
C	Power of signal carrier
°C	Celsius (unit of temperature)
CCITT	Comité Consultatif International Téléphonique et Télégraphique
CDDL	Complementary Dispersive Delay Line
C/I	Carrier to Interference Ratio
Clk	Clock
CRC	Cyclic Redundancy Check
CMMR	Common Mode Rejection Ratio
CMOS	Complementary Metal Oxide Semiconductor
CS	Chip Select
CSMA	Carrier Sense Multiple Access
CSMA/CA	Carrier Sense Multiple Access/Collision Avoidance
CSS	Chirp Spread Spectrum
DAC	Digital to Analog Converter
Data	Data packet type
dB	Decibel (ratio between two values, such as signal power, voltage, or current levels in logarithmic scale)
dBi	Gain referenced to isotropic antennae
DBO-CSS	Differentially Bi-Orthogonal Chirp Spread Spectrum
dBm	dB referenced to one milliwatt (10^{-3}W = 1mW)
dBr	Decibels relative to reference level
DC	Direct Current
DiIO	Digital Input/Output
DPA	Differential Power Amplifier
DPD	Differential Peak Detector
DUT	Device Under Test
E_b	Energy of bit
EIRP	Effective Isotropic Radiated Power
ESD	Electrostatic Discharge
FCD	Folded Chirp Detector
FCM	Folded Chirp Mixer
FDMA	Frequency Division Multiplex Access
FEC	Forward Error Correction
FET	Field Effect Transistor
FHSS	Frequency Hopping Spread Spectrum
FIFO	First In First Out
FS	Full Scale
GBWP	Gain Bandwidth Product
GHz	Gigahertz (unit of frequency)
GND	Ground
HBM	Human Body Model
I	Inline
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IF	Intermediate Frequency
I/O	Input/Output
I_{OH}	Output current high
I_{OL}	Output current low
IRQ	Interrupt request
IQ	In-phase, Quadrature
ISM	Industrial Scientific Medical
ISO	International Organization for Standardization
kΩ	KiloOhms (unit of electrical resistance)
kHz	KiloHertz (unit of frequency)
kpbs	Kilobits per second (unit of data throughput)
L	Inductance
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
ΛΣB	Λεαστ Σιγνιφιχαντ Βιτ
MΩ	MegaOhms (unit of electrical resistance)
mA	Milliampere (unit of electrical current)
Mbaud	Megabauds
Mbps	Megabits per second (unit of data throughput)
MAC	Medium Access Control
MHz	MegaHertz (unit of frequency)
MISO	Master In, Slave Out
MIX	Mixer
MLF	Micro Lead Frame Package
MOD	Modulator
MOSI	Master Out Slave In
MUX	Multiplexer
mW	milliwatt (unit of power)
NC	Not Connected
nF	Nanofarad (unit of electrical capacitance)
nH	NanoHenry (unit of electrical inductance)
N_o	Power spectral density of thermal noises
ns	Nanosecond (unit of time)
OEM	Original Equipment Manufacturer
OSC	Oscillator
OP	Operational Amplifier
OTA	Operational Transconductance Amplifier

PA	Power Amplifier
PAE	Power Added Efficiency
PAMP	Power amplifier
PDK	Process Development Kit
PEP	Peak Envelope Power
pF	Picofarad (unit of electrical capacitance)
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
P_{out}	Power Out
ppm	parts per million
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PGC	Power Gain Control
POMD	Peak Over Mean Detector
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
Q	Quadrature
QFN	Quad Flat No-lead
R	Resistor
RF	Radio Frequency
RFID	Radio Frequency IDentification
ROM	Read Only Memory
RSSI	Radio Signal Strength Indicator
RTC	Real Time Clock
RX	Receiver
S	Switch/button
SAR	Successive Approximation Register
SAW	Surface Acoustic Wave
SDS-TWR	Symmetrical Double Sided Two Way Ranging
SLNA	Symmetric Low Noise Amplifier
SMIX	Symmetric Mixer
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SpiClk	Serial peripheral interface Clock
SpiSsn	Serial peripheral interface Slave select
SpiRxD	Serial peripheral interface Receive Data
SpiTxD	Serial peripheral interface Transmit Data
SRAM	Static RAM
SSB	Single Side Band
t	Time constant
T	Duration time of the chirp waveform
TBD	To Be Determined
TDMA	Time Division Multiple Access
T_{junct}	Temperature of junction
THD	Total Harmonic Distortion
TRL	Transmission Line
TRX	Transceiver
TTL	Transistor-Transistor Logic
TX	Transmitter
V	Volts (unit of electrical potential)
V_{IH}	Input voltage for High level
V_{IL}	Input voltage for Low level
V_{OH}	Output voltage for High level
V_{OL}	Output voltage for Low level
VCA	Voltage Controlled Amplifier
V_{CC}	Battery supply voltage
VCO	Voltage Controlled Oscillator
V_{DDA}	Power supply for analog part
V_{DDD}	Power supply for digital part
VFQFPN	Very thin Fine pitch Quad Flat Pack Nolead Package
VGA	Variable Gain Amplifier
V_{SSA}	Analog ground
V_{SSD}	Digital ground
VSWR	Voltage Standing Wave Ratio
XTAL	Crystal
XCO	Xtal (crystal) Controlled Oscillator

12.1 Special Symbols

C_{DS}	Drain-source capacitance
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance
C_r	Feedback capacitance
D	Drain
E_G	Energy gap
f_T	Transit frequency
G	Gate, Gradient
GaAs	Gallium-Arsenide
Ge	Germanium
g_m	Short-circuit forward transconductance
H	Hybrid parameter
I_{DSS}	Drain current with V_{GS}=0
k	Boltzmann constant, $1.38 \cdot 10^{-23}$J/K or stability factor
q	Electron charge, $1.602 \cdot 10^{-19}$As
r_{DS}	Differential drain-source-resistance
RMS	Root Mean Square
R_{th}	Thermal resistance in K/W
S	Source
S_{ij}	Scattering parameters
Si	Silicon
T	Period
T_j	Junction Temperature
TC	Temperature coefficient, e.g. TK(IDSS)
V_{pp}	Peak-to-Peak Voltage
V_D	Diffusion voltage
V_{DS}	Drain-Source voltage
V_{GS}	Gate-Source voltage
V_T	Thermal voltage, V_T=kT/q
V_{TO}	Threshold voltage, Turn-on voltage
a	Angle
b	Current gain
d	Partial derivative
e_o	Dielectric constant of a vacuum
ε_r	Dielectric constant relative to a vacuum
ε_{reff}	Effective relative dielectric constant
G	Reflection coefficient
μ_o	Permeability of a vacuum
μ_o	Permeability relative to a vacuum
m	Charge carrier mobility
w	Angular frequency
D	Difference
S	Sum

13 Ordering Information

To order the product described in this datasheet, use the following information.

Table 17: nanoLOC TRX Transceiver (NA5TR1) Ordering Information

Part Description	Part Number	Additional Information
nanoLOC TRX Transceiver	NLSG0501A	nanoLOC Development Kit, nanoLOC Evaluation Kit, and nanoLOC Driver are available upon request.

A1 Example Application

A1.1 Schematics

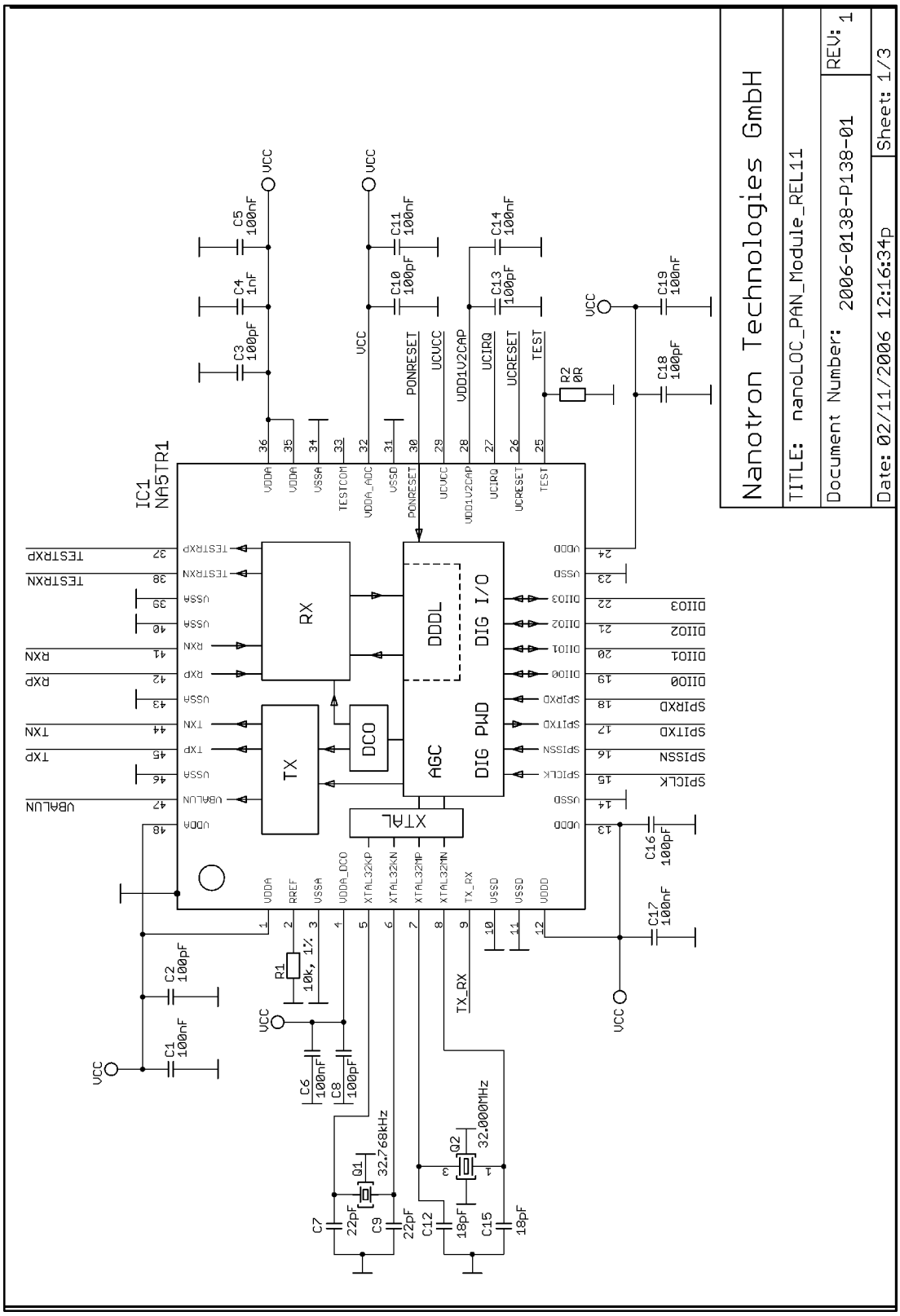

Figure 8: Example Application: schematics part 1

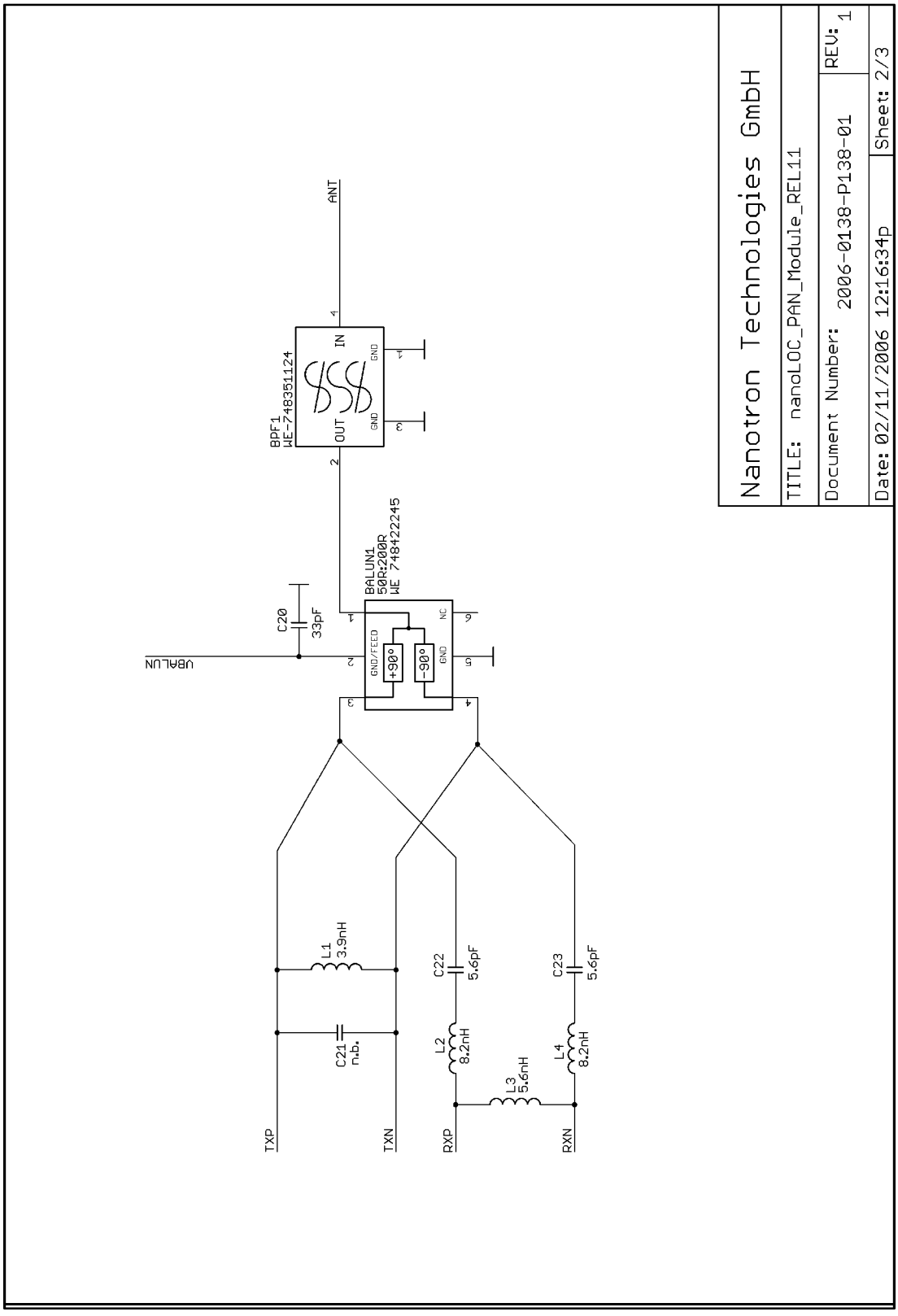

Figure 9: Example Application: schematics part 2

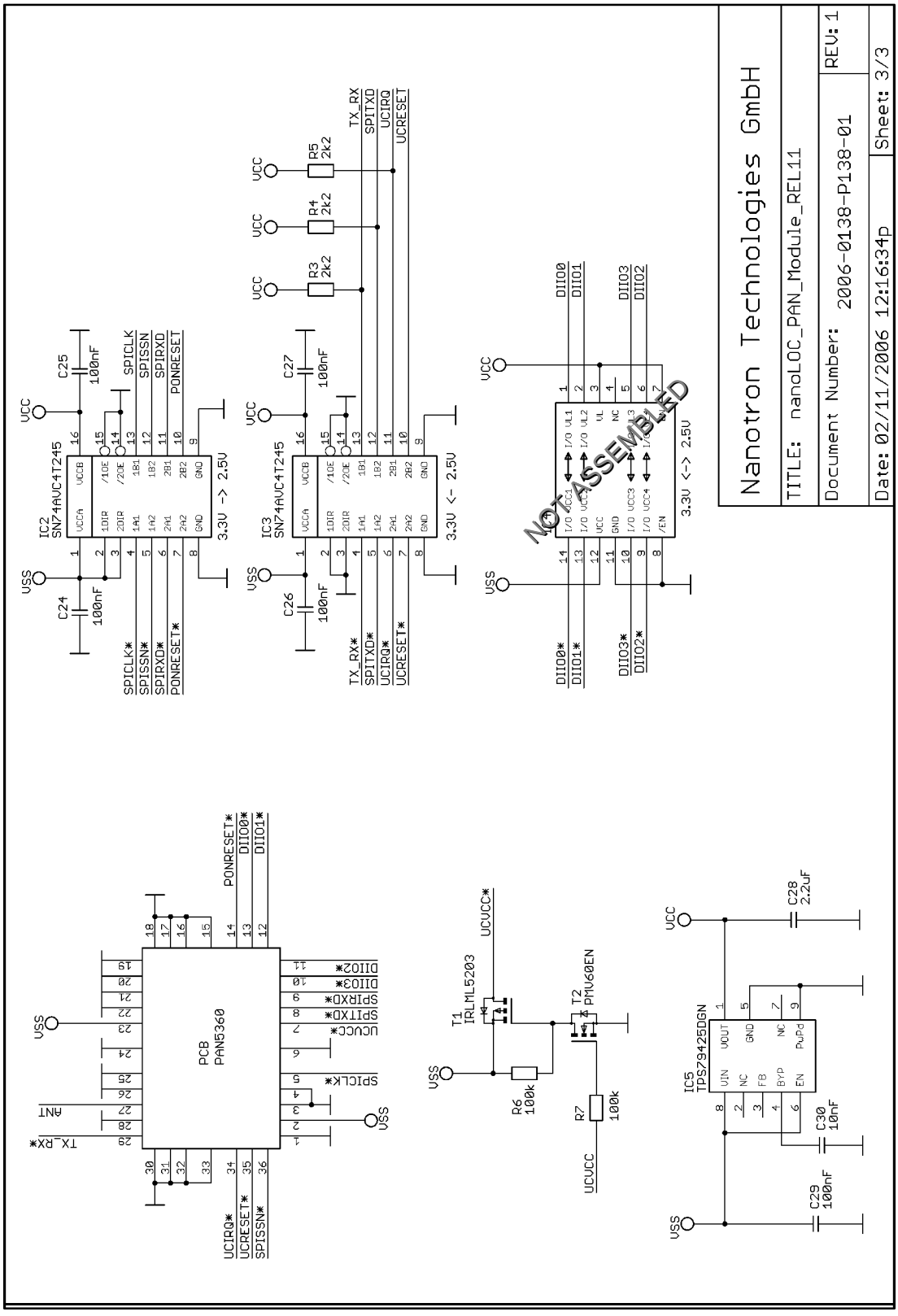

Figure 10: Example Application: schematics part 3

A1.2 PCB Layout

Note: As this example application includes level shifters, it can be used in a variety of 3 volt environments, controllers, other circuits. To work in a 2.5 volt environment, voltage converters are not required.

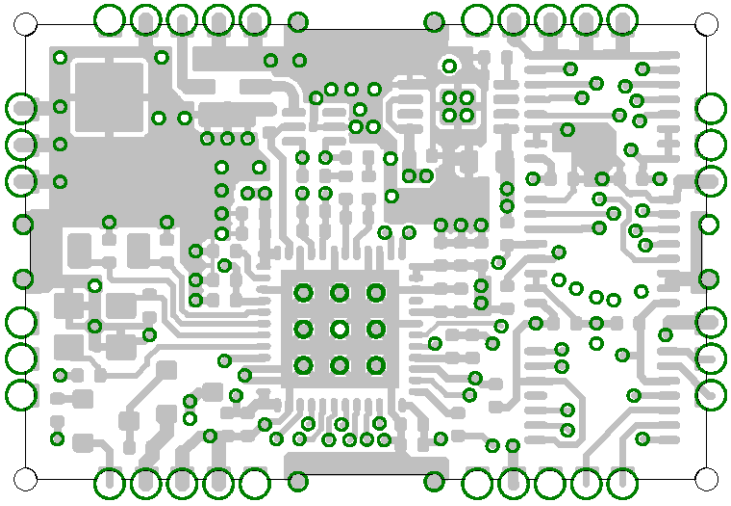

Figure 11: Example Application: top layer (enlarged 3X)

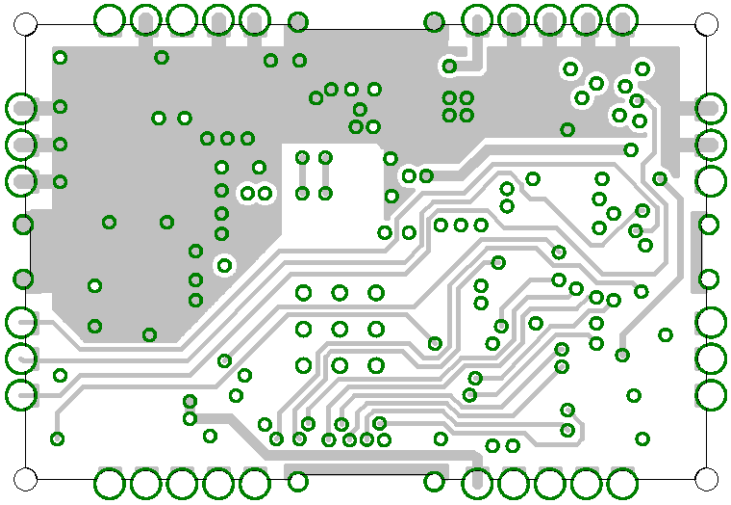

Figure 12: Example Application: 2nd layer (enlarged 3X)

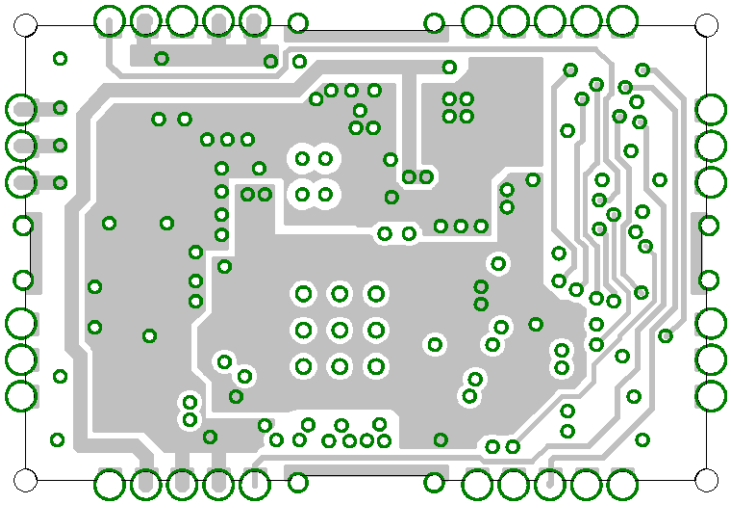

Figure 13: Example Application: 3rd layer (enlarged 3X)

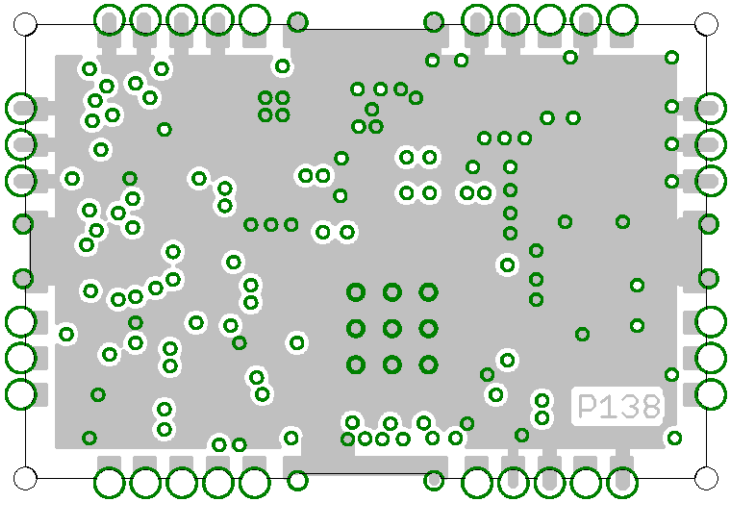

Figure 14: Example Application: bottom layer (inverted and enlarged 3X)

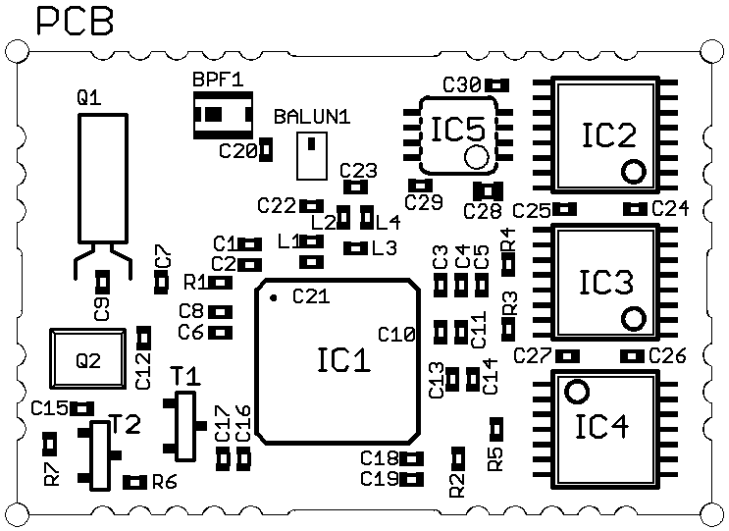

Figure 15: Example Application: top components (enlarged 3X)

A1.3 Example Application Bill of Materials

Table 18: Example Application bill of materials

Part Description	Label	Value	Qty	Package	Remarks	Supplier/Order No.
Resistor	R2	0R	1	0402	Not specified	Not specified
	R3, R4, R5	2k2	3	0402	63mW, ±5%	Not specified
	R1	10k, 1%	1	0402	63mW, ±1%	Not specified
	R6, R7	100k	2	0402	63mW, ±5%	Not specified
Capacitor	C21	n.a.	\	0402	Not specified	Not specified
	C22, C23	5.6pF	2	0402	NPO, 50V, ±5%	Not specified
	C7, C9	22pF	2	0402	NPO, 50V, ±5%	Not specified
	C12, C15	18pF	2	0402	NPO, 50V, ±5%	Not specified
	C20	33pF	1	0402	NPO, 50V, ±5%	Not specified
	C2, C3, C8, C10, C13, C16, C18	100pF	7	0402	NPO, 50V, ±5%	Not specified
	C4	1nF	1	0402	NPO, 50V, ±5%	Not specified
	C30	10nF	1	0402	X7R, 10V, ±10%	Not specified
	C1, C5, C6, C11, C14, C17, C19, C24, C25, C26, C27, C29	100nF	12	0402	X7R, 10V, ±10%	Not specified
	C28	2.2uF	1	0603	X5R, 6.3V, ±10%	Not specified
Inductor	L1	3.9nH	1	0402	WE-MK	Wuerth Elektronik WE 744784039
	L3	5.6nH	1	0402	WE-MK	Wuerth Elektronik WE 744 784056
	L2, L4	8.2nH	2	0402	WE-MK	Wuerth Elektronik WE 744 784082
Balun 50R:200R	BALUN1	WE 748422245	1	BAL0805	ISM 2.44GHz, 50R:200R	Wuerth Elektronik WE 748422245
Bandpass Filter 2.4GHz	BPF1	WE-748351124	1	WE-BPF1008	ISM 2.44GHz	Wuerth Elektronik WE 748351124
Clock Crystal	Q1	32.768kHz	1	MS1V-TK	±20ppm, -40× ... +85×C, CL =12.5pF	GOLLEDGE MS1V-T1K 32.768kHz±20ppm
	Q2	32.000MHz	1	32SMX	±30ppm @-40 ...+85×, CL=16pF	SMI 32 M 320 -16

Table 18: Example Application bill of materials (Continued)

Part Description	Label	Value	Qty	Package	Remarks	Supplier/Order No.
P-Channel MOS-FET	T1	IRLML5203	1	SOT-23	µTrenchMOS enhancement mode FET	International Rectifier IRLML5203PbF
N-Channel MOS-FET	T2	PMV60EN	1	SOT-23	HEXFET Power MOSFET	Philips Semiconductor PMV60EN
nanoLOC Trans-ceiver	IC1	NA5TR1	1	VFQFPN48	nanoLOC Transceiver	Nanotron Technologies NA5TR1
Level Shifter	IC2, IC3	SN74AVC4T245	2	TSSOP16	4 Bit Dual Supply Bus trans-ceiver	Texas Instruments SN74AVC4T245PWT
Level Shifter	IC4	NOT ASSEMBLED				
Voltage Regulator	IC5	TPS79425DGN	1	MSOP-8	LD Voltage Regulator	Texas Instruments TPS79425DGNT
PCB	PCB	P138	1	30 x 20 mm	Not specified	Nanotron Technologies P138

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A2 RF Test Board Design for Measurements

A2.1 Overview

The following RF Test Module was designed for testing and measurement purposes only. It was used during measurements and simulations to determine parameters published in this document, unless otherwise specified.

The electrical interface between the RF Test Module and automatic test equipment utilizes the 3.3 V CMOS level standard. However, to interface with the nanoLOC chip, a 2.5 V CMOS level is required. Therefore, a proper interconnection between both voltage domains is required (for example, level shifters, which are implemented in this design).

Note: Level shifters are needed only due to interface requirements of Automatic Test equipment, not by the nanoLOC chip itself. No level shifters are needed if 2.5 V power supply design is used.

For conducting tests purposes, the RF Test Module includes a 50 Ω coaxial SMA connector.

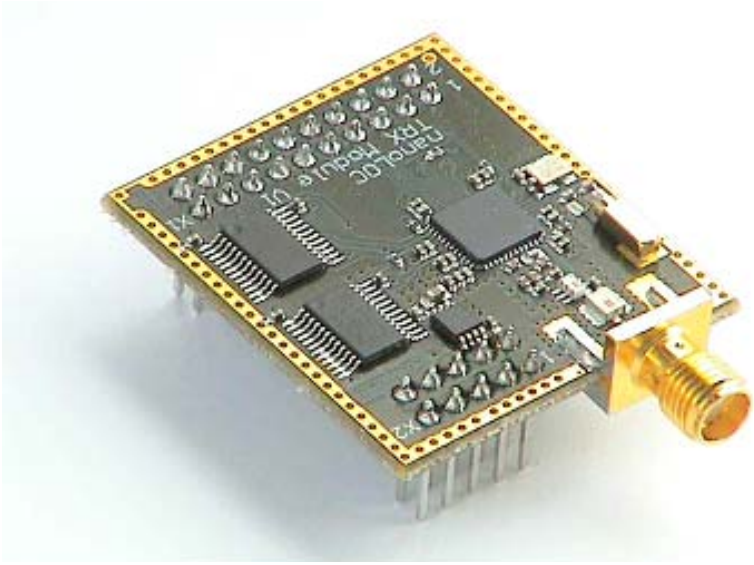

Figure 16: RF Test Module for nanoLOC chip: top view

Figure 17: RF Test Module for nanoLOC chip: bottom view

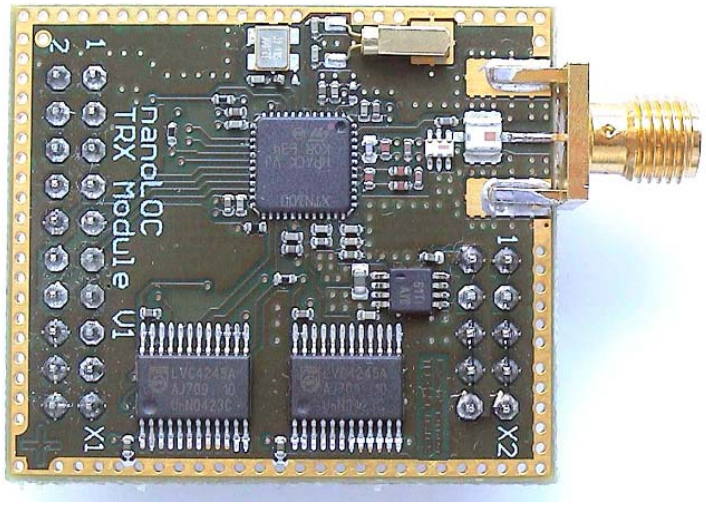

Figure 18: RF Test module for nanoLOC chip: component side

A2.2 Schematics

The following schematics represents the following major blocks of the design:

- Schematic 1: Power supply for nanoLOC chip and connection with crystal resonators.
- Schematic 2: RF interface between nanoLOC chip and SMA connector (impedance matching circuitry for Rx and Tx, balun, ISM Band Pass Filter).
- Schematic 3: Interface to the Automatic Test Equipment (level shifters, connectors).

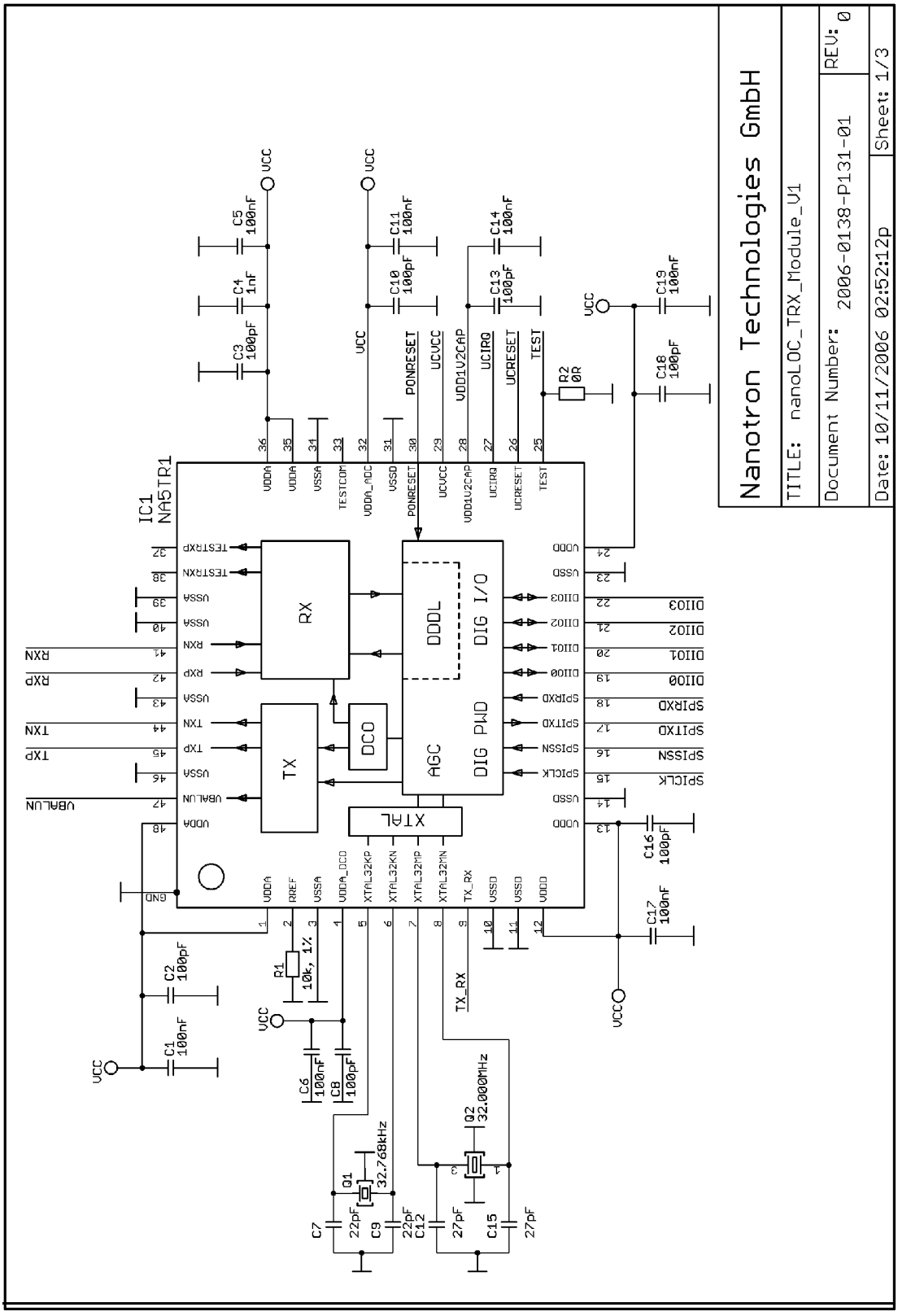

Figure 19: RF Test Module: schematics 1

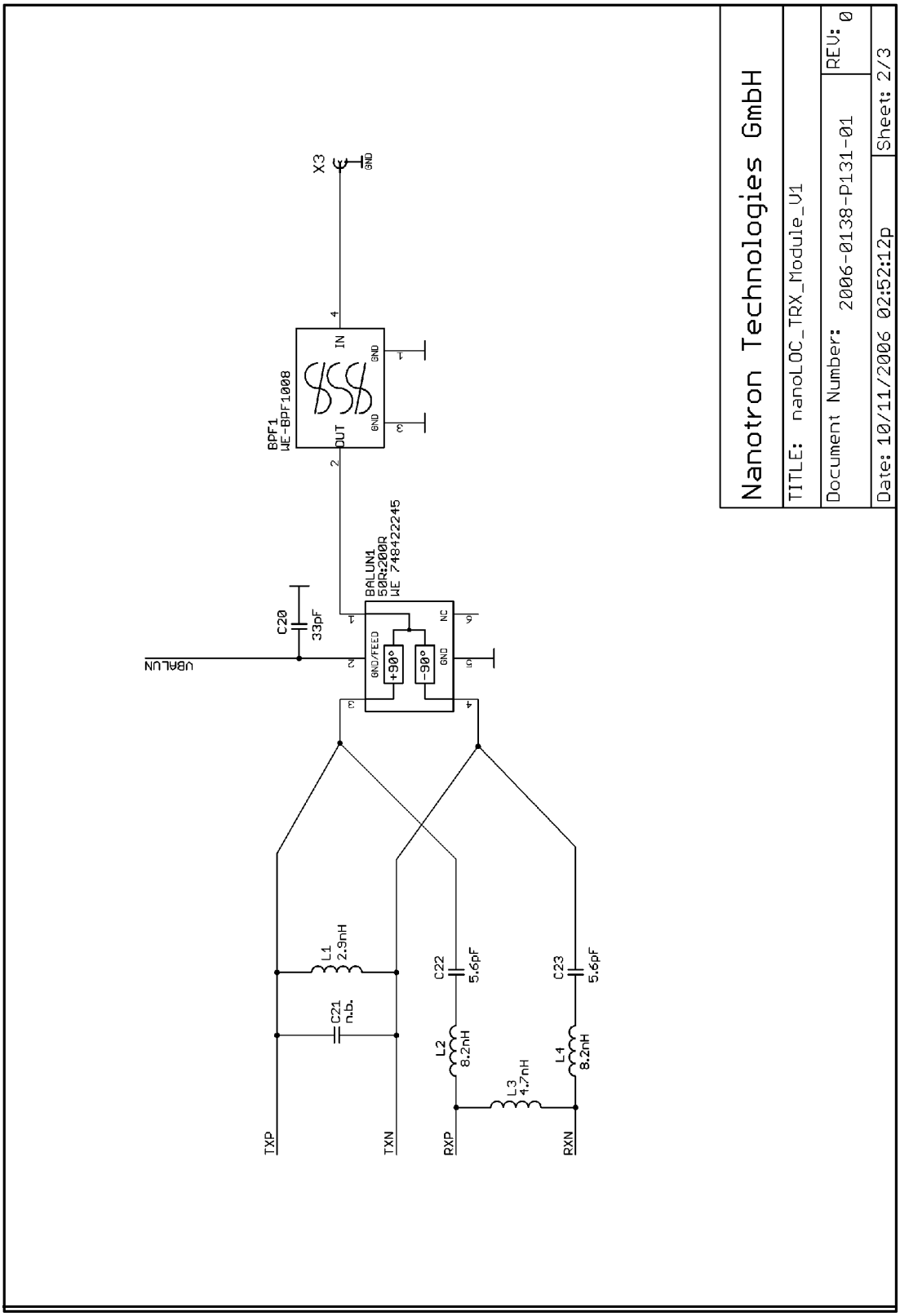

Figure 20: RF Test Module: schematics 2

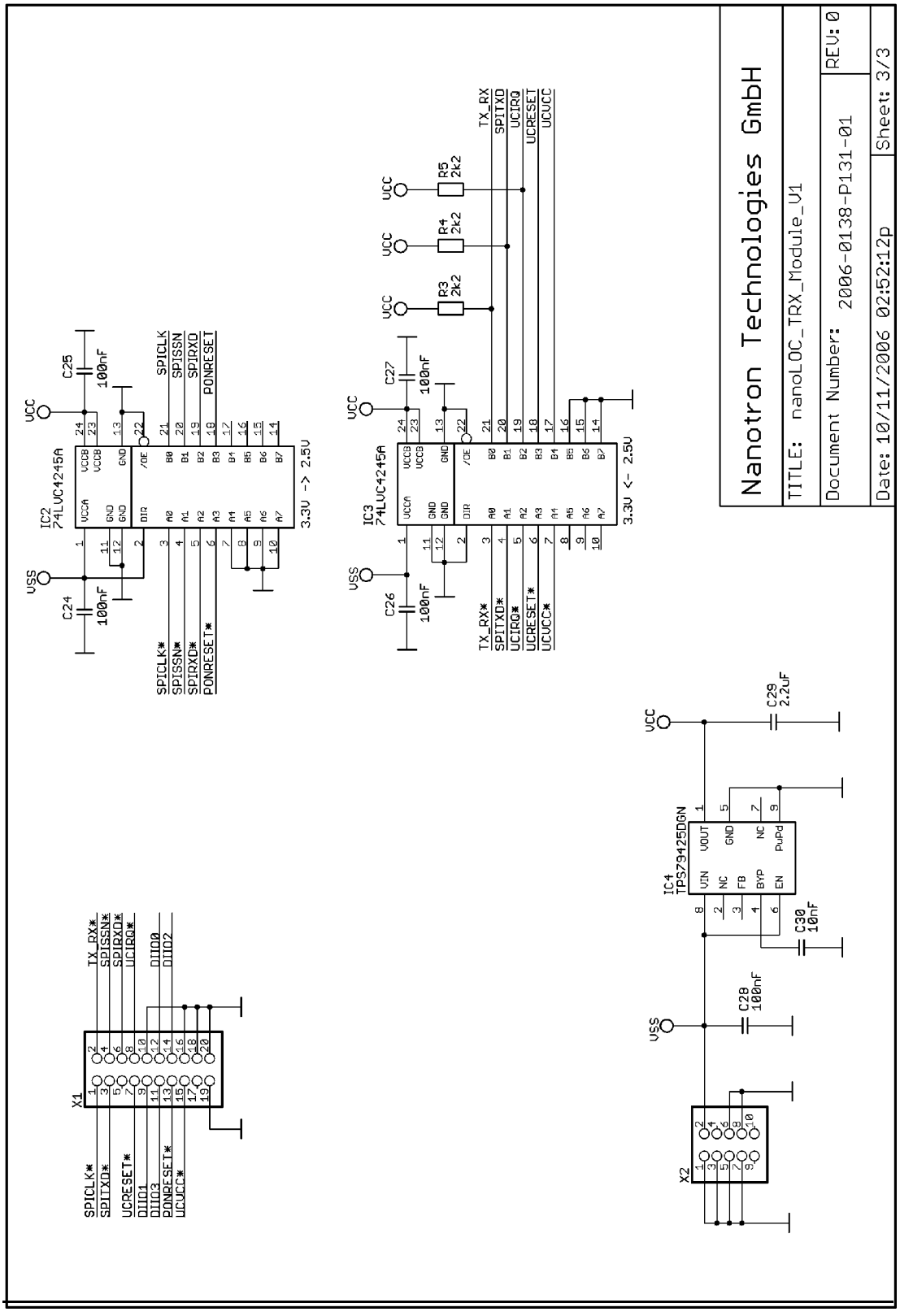

Figure 21: RF Test Module: schematics 3

A2.3 PCB Layout

Note: As the RF Test Module includes level shifters, it can be used in a variety of 3 volt environments, controllers, and other circuits. To work in a 2.5 volt environment, voltage converters are not required.

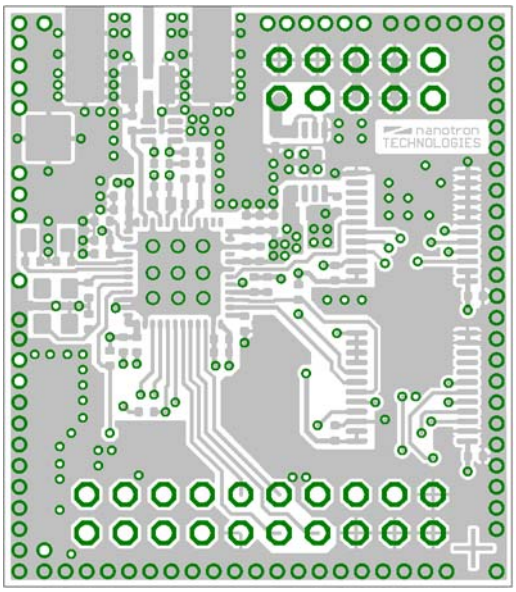

Figure 22: RF Test Module: top layer (enlarged 2X)

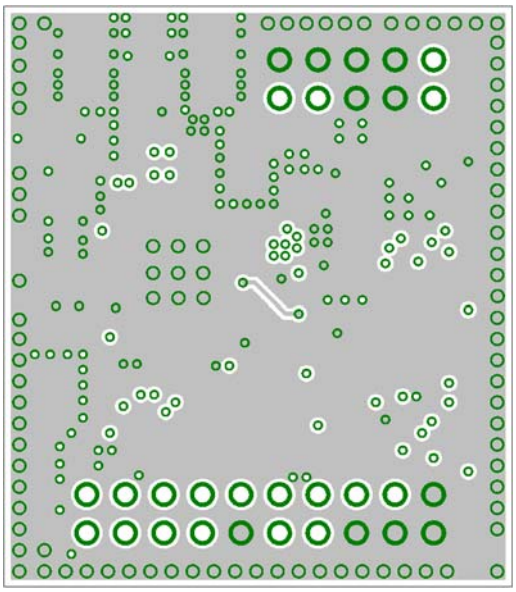

Figure 23: RF Test Module: 2nd layer (enlarged 2X)

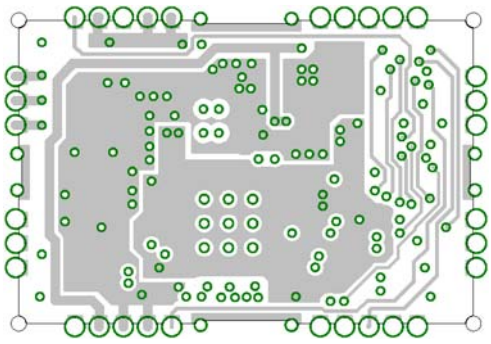

Figure 24: RF Test Module: 3rd layer (enlarged 2X)

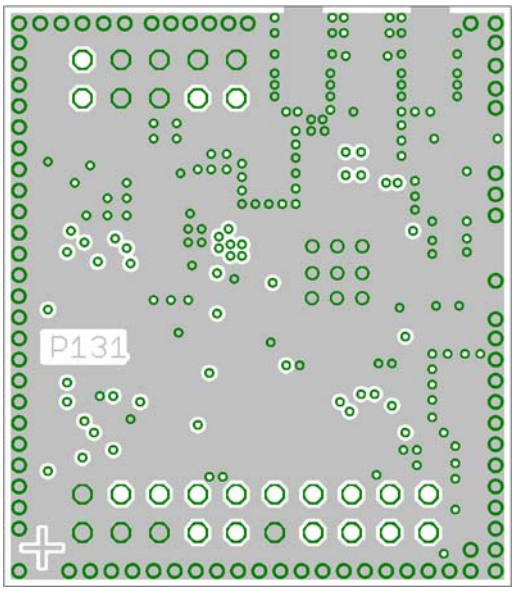

Figure 25: RF Test Module: bottom layer (inverted and enlarged 2X)

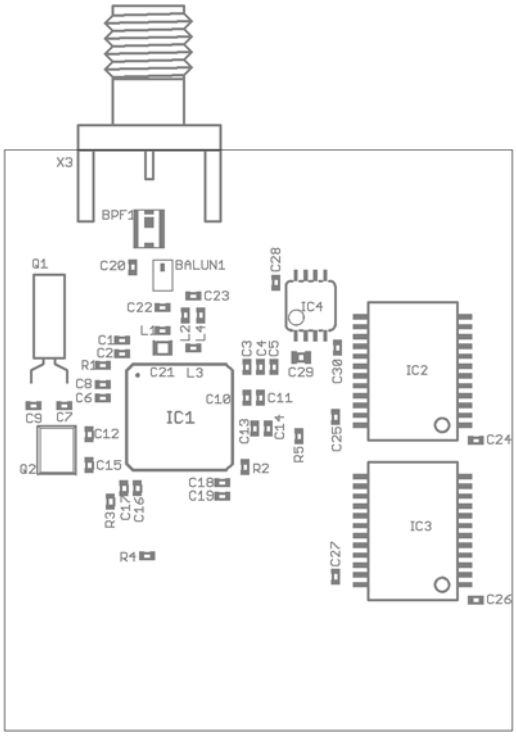

Figure 26: RF Test Module: top components (enlarged 2X)

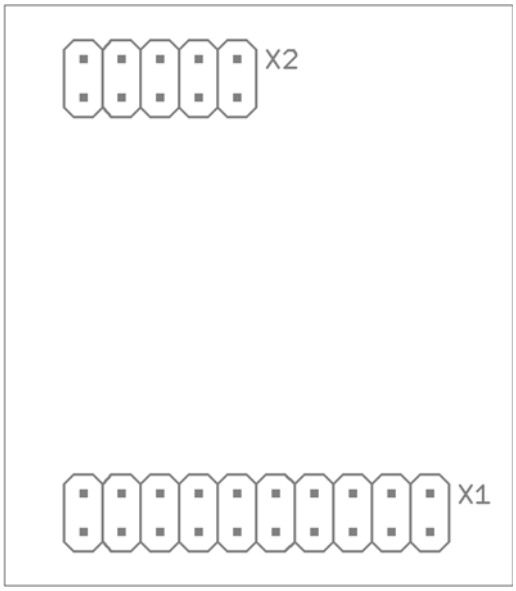

Figure 27: RF Test Module: bottom components (inverted and enlarged 2X)

A2.4 RF Test Module Bill of Materials (BOM)

Table 19: RF Test Module bill of materials

Part Description	Label	Value	Qty	Package	Remarks	Supplier/Order No.
Resistor	R2	0R	1	0402	63mW, ±5%, 50V	PHYCOMP 2322 705 91001
	R3, R4, R5	2k2	3	0402	63mW, ±5%, 50 V	MEGGITT CRG0402J2K2-10
	R1	10k,1%	1	0402	63mW, ±1%, 50 V	PHYCOMP 232270671003
Capacitor	C21	n.b.	\	0402	Not specified	Not specified
	C22, C23	5.6pF	2	0402	ACCU-P 25V, ±1.8%	AVX 04023J5R6BBWTR
	C20	15pF	1	0402	NPO, 50V, ±5%	Not specified
	C7, C9	22pF	2	0402	NPO, 50V, ±5%	PHYCOMP 2238 869 15229
	C12, C15	27pF	2	0402	NPO, 50V, ±5%	Not specified
	C2, C3, C8, C10, C13, C16, C18	100pF	7	0402	NPO, 50V, ±5%	PHYCOMP 2238 869 15101
	C4	1nF	1	0402	X7R, 50V, ±10%	PHYCOMP 2238 587 15623
	C30	10nF	1	0402	X7R, 16V, ±10%	PHYCOMP 2238 787 15636
	C1, C5, C6, C11, C14, C17, C19, C24, C25, C26, C27, C28	100nF	12	0402	Y5V, 16V, +80/-20%	PHYCOMP2238 787 19849
	C29	2.2uF	1	0603	X5R, 6.3V, ±10%	KEMET C0603C225K8PAC7867
Inductor	L1	2.7nH	1	0402	WE-MK	Wuerth WE 744784027
	L3	4.7nH	1	0402	WE-MK	Wuerth WE 744784047
	L2,L	8.2nH	2	0402	WE-MK	Wuerth WE 744784082
SMD - Balun 50R:200R	BALUN1	WE 748422245	1	BAL0805	ISM 2.44GHz, 50R:200R	Wuerth WE 748422245
Band pass filter 2.4GHz	BPF1	WE 748351124	1	WE-BPF1008	ISM 2.44GHz	Wuerth WE 748351124
Clock crystal 32.768 kHz	Q1	32.768kHz	1	MS1V-TK	±20ppm, -40× ... +85×C, CL =12.5pF	GOLLEDGE MS1V-T1K 32.768kHz±20ppm
Clock crystal 32.000 MHz	Q2	32.000MHz	1	32SMX	±30ppm @-40 ...+85×, CL=12pF	EPSON TSX-3225 32.000MHz, CL=12pF

Table 19: RF Test Module bill of materials (Continued)

Part Description	Label	Value	Qty	Package	Remarks	Supplier/Order No.
nanoLOC Transceiver	IC1	NA5TR1	1	VFQFPN48	nanoLOC Transceiver	Nanotron Technologies NA5TR1
Level Shifter	IC2, IC3	74LVC4245A	2	SSOP24	Not specified	Philips Semiconductors 74LVC4245A
Voltage Regulator	IC4	TPS79425DGN	1	MSOP-8	Vout = 2.5V LD Voltage Regulator	Texas Instruments TPS79425DGNT
Connector, 2-row, 5pin	X2	n.a	1	2X05	n.a	WINSLOW Adaptics W82110T3825
Connector, 2-ow, 10pin	X1	n.a.	1	2X10	n.a	WINSLOW Adaptics W82120T3825
SMA Connector	X3	JOHNSON_ JACK_GND_2	1	JOHNSON_JACK_ GND_2		Johnson Components 142-0711-851

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Revision History

Date	Version	Description/Changes
1.00	2006-08-29	Pre-engineering preliminary document.
1.01	2006-11-03	Pre-engineering preliminary document. Specifications, pin description, reference design, product descriptions added. Errata: Nominal conditions include Bit scrambling; $A_{path\text{-}att\text{-}max}$ = 101 dB; $A_{path\_att\_max\_fec}$ = 103 dB.
1.02	2007-02-21	Minor text edits and corrections.

About Nanotron Technologies GmbH

Nanotron Technologies GmbH develops world-class wireless products for demanding applications based on its patented Chirp transmission system - an innovation that guarantees high robustness, optimal use of the available bandwidth, and low energy consumption. Since the beginning of 2005, Nanotron's Chirp technology has been a part of the IEEE 802.15.4a draft standard for wireless PANs which require extremely robust communication and low power consumption.

ICs and RF modules include the nanoNET TRX, the nanoLOC TRX, and ready-to-use or custom wireless solutions. These include, but are not limited to, industrial monitoring and control applications, medical applications (Active RFID), security applications, and Real Time Location Systems (RTLS). nanoNET is certified in Europe, United States, and Japan and supplied to customers worldwide.

Headquartered in Berlin, Germany, Nanotron Technologies GmbH was founded in 1991 and is an active member of IEEE and the ZigBee alliance.

Further Information

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