

---

## *DABiC-5 8-Bit Serial Input Latched Sink Drivers*

---

### **Last Time Buy**

This part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: November 1, 2010

Deadline for receipt of LAST TIME BUY orders: April 30, 2011

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, contact Allegro Sales.*

---

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

---

*Allegro MicroSystems, Inc. reserves the right to make, from time to time, revisions to the anticipated product life cycle plan for a product to accommodate changes in production capabilities, alternative product availabilities, or market demand. The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.*

---

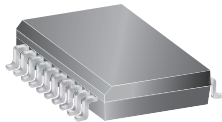
## DABiC-5 8-Bit Serial Input Latched Sink Drivers

### Features and Benefits

- 3.3 to 5 V logic supply range
- Power-on reset (POR)
- To 10 MHz data input rate
- CMOS, TTL compatible inputs
- -40°C operation available
- Low-power CMOS logic and latches
- Schmitt trigger inputs for improved noise immunity
- High-voltage current-sink outputs
- Internal pull-up/pull-down resistors
- Output transient-protection diodes
- Single or split supply operation

### Packages:

*Not to scale*



20-pin SOICW (package LW)  
(drop-in replacement for discontinued 18-pin SOIC variants)



18-pin DIP (Package A)

### Description

The merging of low-power CMOS logic and bipolar output power drivers using the proprietary DABiC-5 fabrication process permit the A6841 integrated circuits to be used in a wide variety of peripheral power driver applications. Each device has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers. The 500 mA, NPN Darlington outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids, and other inductive loads.

All package variations of the A6841 offer premium performance with a minimum output-breakdown voltage rating of 50 V (35 V sustaining). All drivers can be operated with a split supply where the negative supply is up to -20 V.

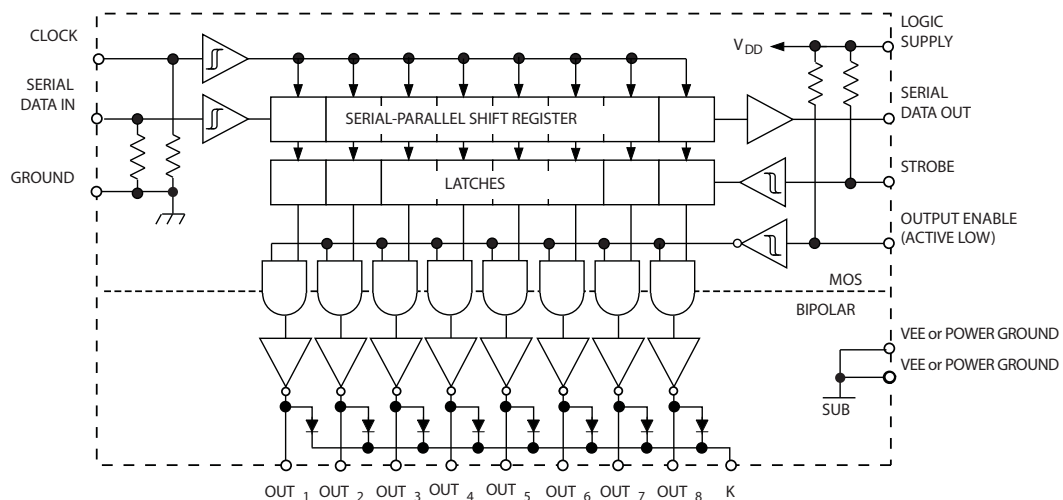
The CMOS inputs are compatible with standard CMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, drivers can be cascaded for interface applications requiring additional drive lines.

The A6841 is provided in an 18-pin plastic DIP (suffix A), and a 20-pin wide-body SOIC (suffix LW) with improved thermal characteristics compared to the 18-pin SOIC version it replaces (100% pin-compatible electrically). These devices are lead (Pb) free, with 100% matte tin plated leadframes.

Applications include:

- Relays
- Solenoids
- Inductive loads

### Functional Block Diagram



### Selection Guide

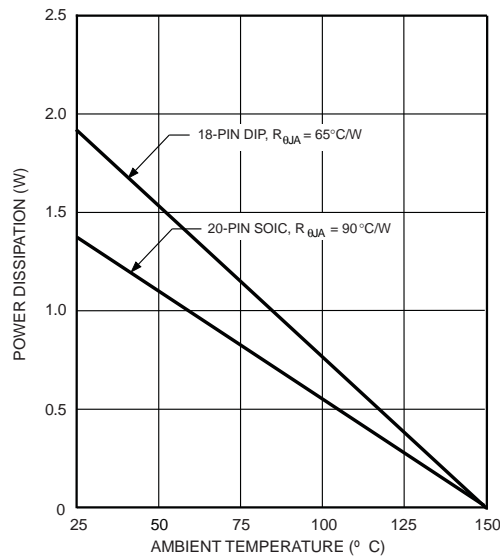
Part Number	Package	Packing	Ambient
A6841SA-T	18-pin DIP	21 pieces per tube	-20°C to 85°C
A6841SLWTR-20-T	20-pin wide body SOIC	1000 pieces per reel	

### Absolute Maximum Ratings\*

Characteristic	Symbol	Notes	Rating	Units
Logic Supply Voltage	$V_{DD}$		7	V
Emitter Supply Voltage	$V_{EE}$		-20	V
Input Voltage Range	$V_{IN}$		-0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_{CE}$		50	V
	$V_{CE(SUS)}$	For inductive load applications	35	V
Continuous Output Current	$I_{OUT}$	Each output	500	mA
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	°C
		Range S	-20 to 85	°C
Maximum Junction Temperature	$T_J(max)$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

### Allowable Package Power Dissipation, $P_D$



**ELECTRICAL CHARACTERISTICS**<sup>1</sup> Unless otherwise noted: T<sub>A</sub> = 25°C, V<sub>EE</sub> = 0 V, logic supply operating voltage V<sub>DD</sub> = 3.0 to 5.5 V

Characteristic	Symbol	Test Conditions	V <sub>dd</sub> = 3.3 V			V <sub>dd</sub> = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I <sub>CEX</sub>	V <sub>OUT</sub> = 50 V	–	–	10	–	–	10	µA
Output Sustaining Voltage	V <sub>CE(SUS)</sub>	I <sub>OUT</sub> = 350 mA, L = 3 mH	35	–	–	35	–	–	V
Collector–Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>OUT</sub> = 100 mA	–	–	1.1	–	–	1.1	V
		I <sub>OUT</sub> = 200 mA	–	–	1.3	–	–	1.3	V
		I <sub>OUT</sub> = 350 mA	–	–	1.6	–	–	1.6	V
Input Voltage	V <sub>IN(1)</sub>		2.2	–	–	3.3	–	–	V
	V <sub>IN(0)</sub>		–	–	1.1	–	–	1.7	V
Input Resistance	R <sub>IN</sub>		50	–	–	50	–	–	kΩ
Serial Data Output Voltage	V <sub>OUT(1)</sub>	I <sub>OUT</sub> = –200 µA	2.8	3.05	–	4.5	4.75	–	V
	V <sub>OUT(0)</sub>	I <sub>OUT</sub> = 200 µA	–	0.15	0.3	–	0.15	0.3	V
Maximum Clock Frequency <sup>2</sup>	f <sub>c</sub>		10	–	–	10	–	–	MHz
Logic Supply Current	I <sub>DD(1)</sub>	One output on, OE = L, ST = H	–	–	2.0	–	–	2.0	mA
	I <sub>DD(0)</sub>	All outputs off, OE = H, ST = H, P1 through P8 = L	–	–	100	–	–	100	µA
Clamp Diode Leakage Current	I <sub>r</sub>	V <sub>r</sub> = 50 V	–	–	50	–	–	50	µA
Clamp Diode Forward Voltage	V <sub>f</sub>	I <sub>f</sub> = 350 mA	–	–	2	–	–	2	V
Output Enable-to-Output Delay	t <sub>dis(BQ)</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	t <sub>en(BQ)</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Strobe-to-Output Delay	t <sub>p(STH-QL)</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	t <sub>p(STH-QH)</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Fall Time	t <sub>f</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Rise Time	t <sub>r</sub>	V <sub>CC</sub> = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Clock-to-Serial Data Out Delay	t <sub>p(CH-SQX)</sub>	I <sub>OUT</sub> = ±200 µA	–	50	–	–	50	–	ns

<sup>1</sup>Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.

<sup>2</sup>Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

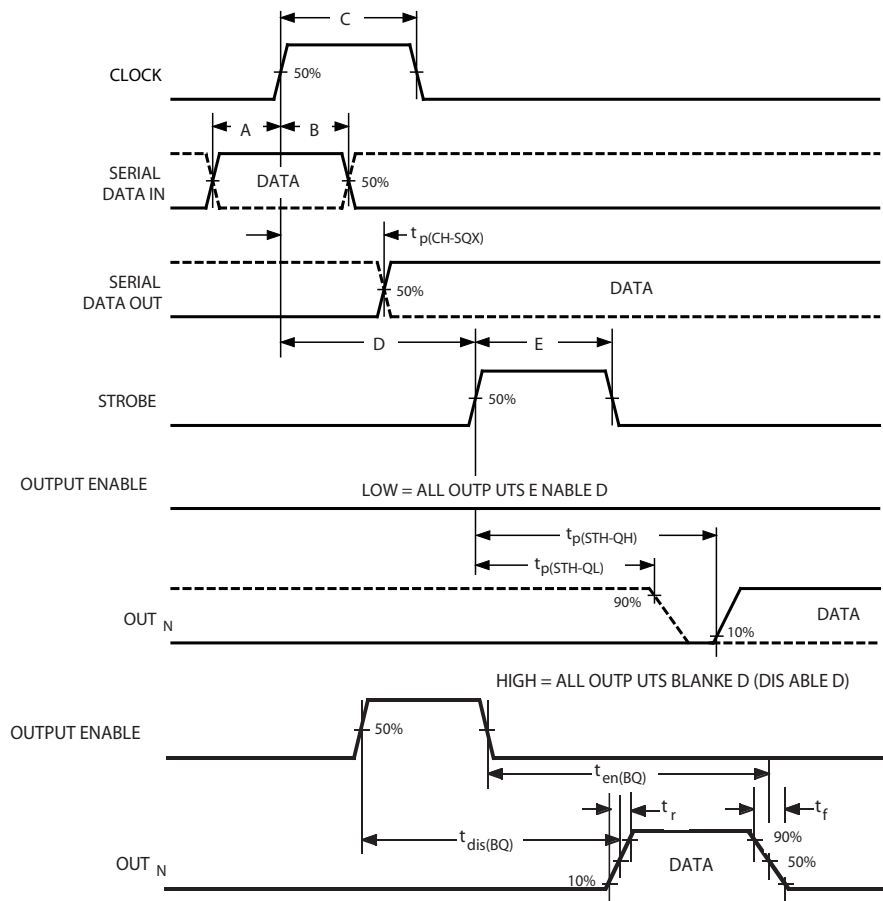
Truth Table

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable Input	Output Contents								
		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>8</sub>	R <sub>1</sub>			R <sub>2</sub>	R <sub>3</sub>	...	R <sub>8</sub>	I <sub>1</sub>	I <sub>2</sub>		I <sub>3</sub>	...	I <sub>8</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>8</sub>	
H	⌋	H	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>7</sub>	R <sub>7</sub>																		
L	⌋	L	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>7</sub>	R <sub>7</sub>																		
X	⌋	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>8</sub>	R <sub>8</sub>																		
		X	X	X	...	X	X	L			R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>8</sub>										
		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>8</sub>	P <sub>8</sub>	H			P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>8</sub>	L									
					...						X	X	X	...	X	H									

L = Low Logic Level  
H = High Logic Level  
X = Irrelevant

P = Present State  
R = Previous State

Timing Requirements and Specifications  
(Logic Levels are  $V_{DD}$  and Ground)



Key	Description	Symbol	Time (ns)
A	Data Active Time Before Clock Pulse (Data Set-Up Time)	$t_{su(D)}$	25
B	Data Active Time After Clock Pulse (Data Hold Time)	$t_h(D)$	25
C	Clock Pulse Width	$t_w(CH)$	50
D	Time Between Clock Activation and Strobe	$t_{su(C)}$	100
E	Strobe Pulse Width	$t_w(STH)$	50

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

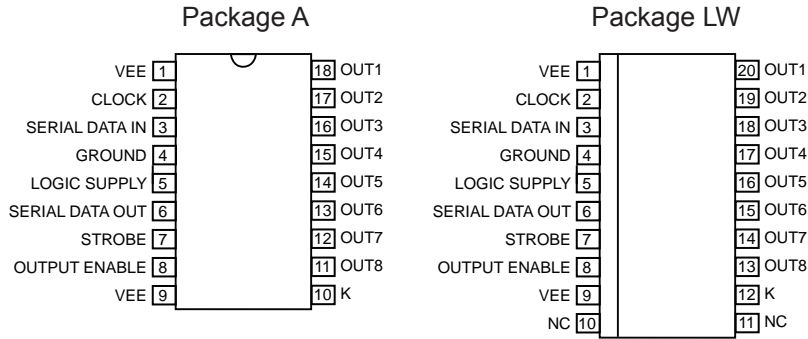
Powering-on with the inputs in the low state ensures that the registers and latches power-on in the low state (POR).

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The serial data must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF). The information stored in the latches or shift register is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

Pin-out Diagrams

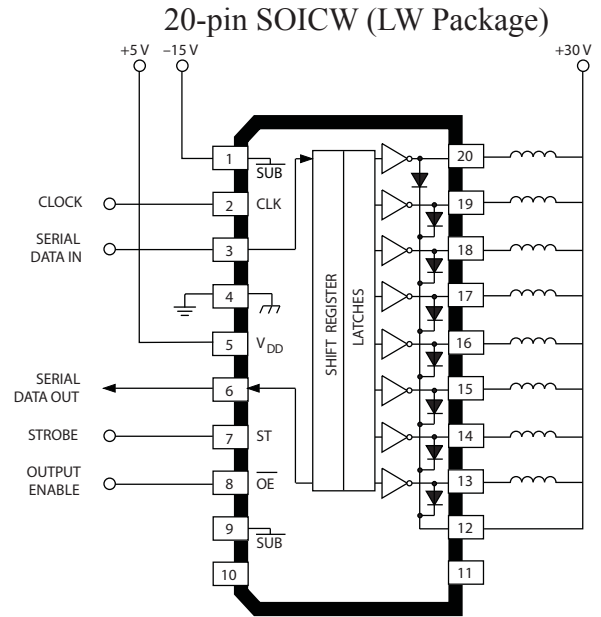
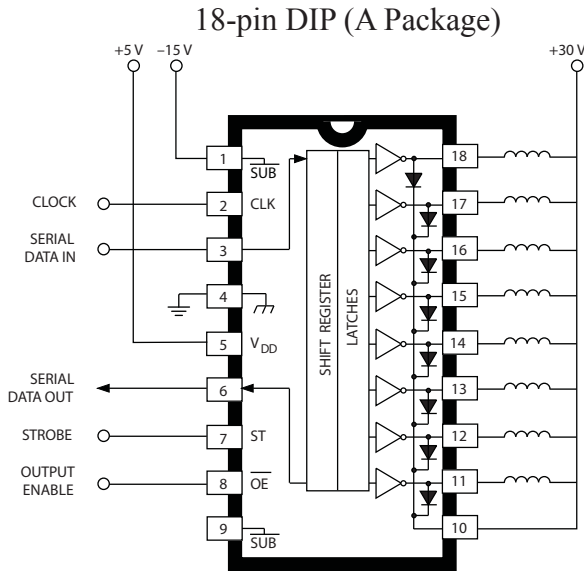


(NC pins, 10 and 11, not present on discontinued 18-pin LW package)

Terminal List Table

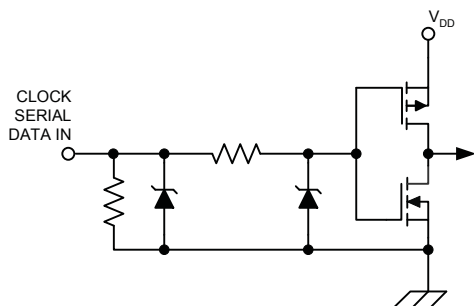
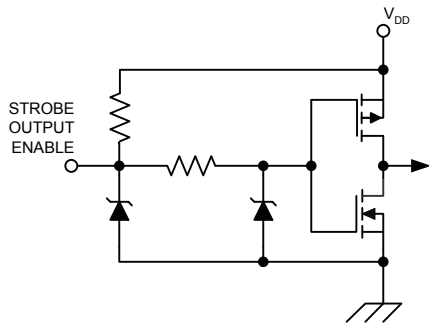
Name	Description	Number	
		Package A	Package LW
VEE	Power Ground to substrate	1, 9	1, 9
CLOCK	Clock	2	2
SERIAL DATA IN	Serial Data In	3	3
GROUND	Logic Ground	4	4
VDD	Logic Supply	5	5
SERIAL DATA OUT	Serial Data Out, for cascading devices	6	6
STROBE	Strobe	7	7
OUTPUT ENABLE	Output Enable (active low)	8	8
K	Common to +V <sub>L</sub> , for inductive loads	10	12
NC	Not internally connected	–	10, 11
OUT8	Sink Output 8	11	13
OUT7	Sink Output 7	12	14
OUT6	Sink Output 6	13	15
OUT5	Sink Output 5	14	16
OUT4	Sink Output 4	15	17
OUT3	Sink Output 3	16	18
OUT2	Sink Output 2	17	19
OUT1	Sink Output 1	18	20

Typical Application  
Relay/solenoid driver using split supply

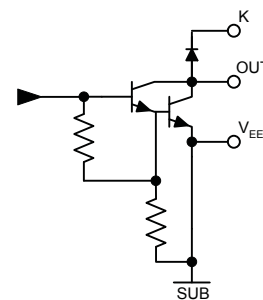


Pins 10 and 11 can float; other pins match discontinued 18-pin SOIC: 1 to 9 same, pins 12 to 20 match pins 10 to 18

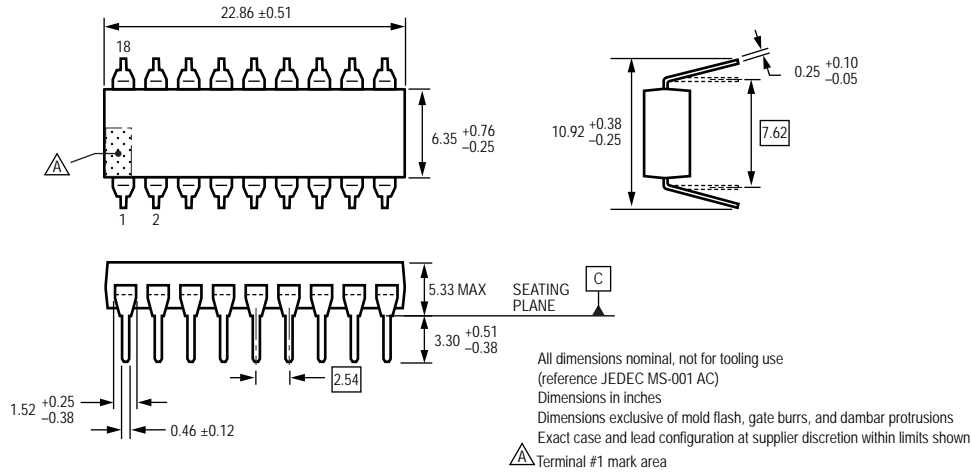
Typical Input Circuits



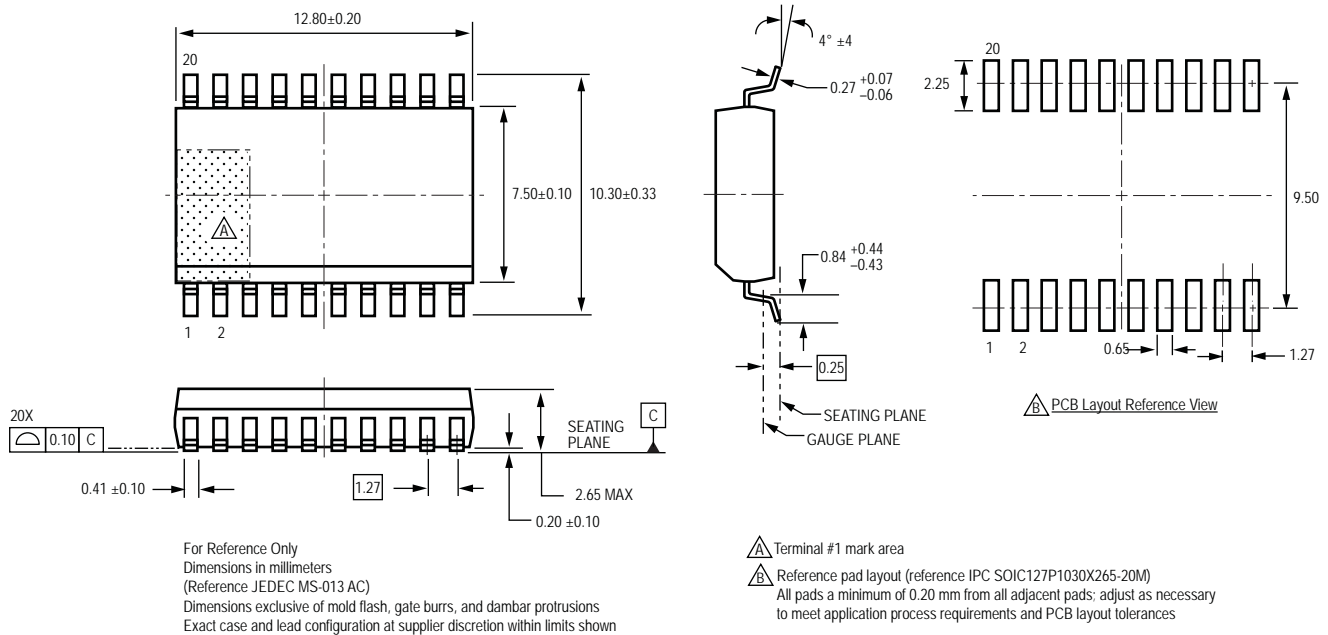
Typical Output Driver



Package A, 18-Pin DIP



Package LW, 20-Pin SOICW





Copyright ©2004-2010 Allegro MicroSystems, Inc.

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:

[www.allegromicro.com](http://www.allegromicro.com)

