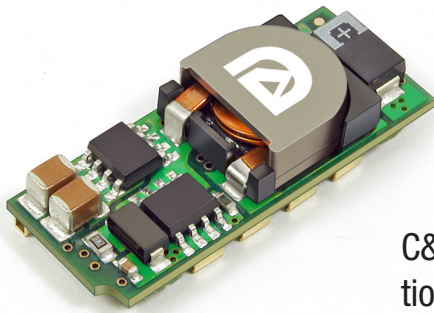


Typical Unit



C&D's miniature POL switching DC/DC converters are ideal regulation and supply elements for distributed power and intermediate bus architectures.

FEATURES

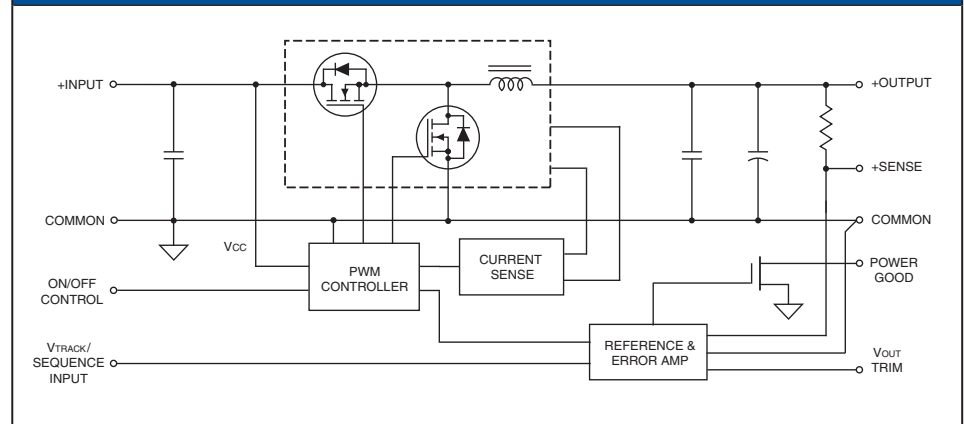
- Point-of-load (POL) converters for distributed bus architectures
- 5V & 12V wide input ranges
- 6, 10 or 16 Amp maximum outputs
- DOSA compatible SMT package
- Double lead free to RoHS standards
- Phased start up sequencing and tracking
- Extensive self-protection
- Starts up into pre-biased loads

PRODUCT OVERVIEW

They are fully compatible with the Distributed-power Open Standards Alliance specification (www.dosapower.com). LSM2's can power CPU's, programmable logic and mixed voltage systems with little heat and low noise. A typical application uses a master isolated 12 or 5 Volt DC supply and individual LSM2 converters for local 1.8 and 3.3 Volt DC supplies. All system isolation resides in the

central supply, leaving lower cost POL regulation right at the load. Unlike linear regulators, the LSM2's can deliver very high power (up to 52 Watts) in a tiny area with no heat sinking and no external components needed. They feature quick transient response (to 25µsec) and very fast current slew rates (to 20A/µsec).

SIMPLIFIED SCHEMATIC



Typical topology is shown



PERFORMANCE SPECIFICATIONS AND ORDERING GUIDE ^①													
Root Model ^⑦	Output						Input			Efficiency		Package (Case/ Pinout)	
	V _{OUT} (Volts)	I _{OUT} (Amps)	Power (Watts)	R/N (mVp-p) ^②		Regulation ^③		V _{IN} Nom. (Volts)	Range ^⑥ (Volts)	I _{IN} ^④ (mA/A)	Min.		Typ.
				Typ.	Max.	Line	Load				Min.		Typ.
LSM2-T/6-W3	0.75-3.3	6	19.8	20	40	±0.11%	±0.075%	5	2.4-5.5	50/4.15	93%	95.5%	C63, P67
LSM2-T/6-D12	0.75-5	6	30.0	30	90	±0.075%	±0.15%	12	8.3-13.2	70/2.68	91.9%	93.4%	C63, P67
LSM2-T/10-W3	0.75-3.3	10	33.0	58	79	±0.15%	±0.075%	5	2.4-5.5	75/6.91	94%	95.5%	C62, P66
LSM2-T/10-D12	0.75-5	10	50.0	62	80	±0.07%	±0.15%	12	8.3-13.2	100/4.35	94.8%	95.8%	C62, P66
LSM2-T/16-W3	0.75-3.3	16	52.8	83	110	±0.1%	±0.075%	5	2.4-5.5	70/11.15	92.8%	94.7%	C62, P66
LSM2-T/16-D12 ^⑤	0.75-5	16	80.0	90	125	±0.1%	±0.21%	12	8.3-13.2	100/7.1	93%	94%	C62, P66

- ① Typical at T_A = +25°C under nominal line voltage and full-load conditions, unless noted.
- ② Ripple/Noise (R/N) is tested/specified over a 20MHz bandwidth and may be reduced with external filtering. See I/O Filtering and Noise Reduction for details.
- ③ These devices have no minimum-load requirements and will regulate under no-load conditions. Regulation specifications describe the output-voltage deviation as the line voltage or load is varied from its nominal/midpoint value to either extreme.

- ④ Nominal line voltage, no-load/full-load conditions.
- ⑤ LSM2-T16-D12 efficiencies are shown at 5V_{OUT}.
- ⑥ V_{IN} must be ≥0.5V greater than V_{OUT}.
- ⑦ These are not complete model numbers. Please refer to the Part Number Structure when ordering.

PART NUMBER STRUCTURE

Output Configuration:

L = Unipolar
Low Voltage

Non-Isolated SMT

Nominal Output Voltage:

0.75-3.3 Volts (W3)
0.75-5 Volts (D12)

Maximum Rated Output
Current in Amps

LSM2 - T / 16 - D12 N G - C

RoHS-6 compliant*

Power Good Output: **

Blank = Omitted
G = Installed

On/Off Polarity:

Blank = Positive polarity
N = Negative polarity

Input Voltage Range:

D12 = 8.3-14 Volts (12V nominal)
W3 = 2.4-5.5 Volts (5V nominal)

Note:
Not all model number combinations are available. Contact DATEL.

* Contact C&D Technologies (DATEL) for availability.

** The Power Good option is not available for LSM2-T/10-D12 and LSM2-T/16-D12. Models without Power Good do not install pad 8 (10/16 Amp). For 6 Amp models, pad 7 is only installed for "G" models.

Performance/Functional Specifications ⁽¹⁾

INPUT	
Input Voltage Range	See Ordering Guide
Isolation	Not isolated, input and output commons are internally connected
Start-Up Threshold	
W3 Models	2.2 Volts
12V Models	8 Volts
Undervoltage Shutdown	
W3 Models	2.0 Volts
12V Models	7.5 Volts
Overvoltage Shutdown	None
Reflected (Back) Ripple Current ⁽²⁾	20-70mA _{p-p} (model dependent)
Internal Input Filter Type	Capacitive
Reverse Polarity Protection	See fuse information
Input Current:	
Full Load Conditions	See Ordering Guide
Inrush Transient	0.1-0.4A ² sec (model dependent)
Shutdown Mode (Off, UV, OT)	5mA
Output Short Circuit	60mA
No Load	
W3 models	50mA
12V models	100mA
Low Line (VIN = VMIN)	
LSM2-T/6-W3	5.54 Amps
LSM2-T/6-D12	3.79 Amps
LSM2-T/10-W3	9.14 Amps
LSM2-T/10-D12	6.31 Amps
LSM2-T/16-W3	14.63 Amps
LSM2-T/16-D12	10.2 Amps
Remote On/Off Control: ⁽⁵⁾	
Positive Logic (no model suffix)	OFF = ground pin to +0.3V max. ON = open pin or +VIN max.
Negative Logic ("N" model suffix)	ON = ground pin to +0.3V max. OFF = open pin to +VIN max.
Current	1mA max.
OUTPUT	
Voltage Output Range	See Ordering Guide
Minimum Loading	No minimum load
Accuracy (50% load)	±2% of V _{NOM}
Voltage Adjustment Range ⁽¹³⁾	See Ordering Guide
Temperature Coefficient	±0.02% of V _{OUT} range per °C
Ripple/Noise (20 MHz bandwidth)	See Ordering Guide and ⁽⁸⁾
Line/Load Regulation (See Tech Notes)	See Ordering Guide and ⁽¹⁰⁾
Efficiency	See Ordering Guide
Maximum Capacitive Loading: ⁽¹⁴⁾	
LSM2-T/6 models:	
Cap-ESR = 0.001 to 0.01Ω	3000μF
Cap-ESR >0.01Ω	5000μF
LSM2-T/10 and -T/16 models:	
Cap-ESR = 0.001 to 0.01Ω	5000μF
Cap-ESR >0.01Ω	10,000μF
Current Limit Inception: (98% of V _{OUT})	
LSM2-T/6 models	11 Amps (cold startup) 10 Amps (after warm up)
LSM2-T/10 models	18.75 Amps (cold startup) 16.75 Amps (after warm up)
LSM2-T/16 models	24 Amps (cold startup) 21 Amps (after warm up)
Short Circuit Mode ⁽⁶⁾	
Short Circuit Current Output Protection Method ⁽¹⁶⁾	600mA Hiccup autorecovery on overload removal
Short Circuit Duration	Continuous, no damage (output shorted to ground)

Prebias Startup ⁽¹⁵⁾	Converter will start up if the external output voltage is less than V _{NOM}
Sequencing	
Slew Rate	2V max. per millisecond
Startup delay until sequence start	10 milliseconds
Tracking accuracy, rising input	V _{OUT} = ±100mV of Sequence In
Tracking accuracy, falling input	V _{OUT} = ±200mV of Sequence In
Sequence pin input impedance	400kΩ to 1MΩ
Remote Sense to V_{OUT}	0.5V max. ⁽⁷⁾
Power Good Output ⁽¹⁷⁾	TRUE (OK) = open drain
("G" suffix)	FALSE (not OK) = Signal Ground to 0.4V
Power_Good Configuration	MOSFET to ground with external user pullup, 10mA max. sink

DYNAMIC CHARACTERISTICS

Dynamic Load Response 25μsec to ±2% of final value
(50-100-50% load step, di/dt = 20A/msec)

Start-Up Time 7msec for V_{OUT} = nominal
(V_{IN} on to V_{OUT} regulated or On/Off to V_{OUT})

Switching Frequency

LSM2-T/6 models	315kHz
LSM2-T/10 and -T/16 models	230kHz

ENVIRONMENTAL

Calculated MTBF ⁽⁴⁾ TBC Hours

Operating Temperature Range (Ambient)

No derating, natural convection	-40 to +63°C ⁽⁹⁾
With derating	See Derating Curves

Operating PC Board Temperature -40 to +100°C max. ⁽¹²⁾

Storage Temperature Range -55 to +125°C

Thermal Protection/Shutdown +115°C

Relative Humidity to 85% / +85°C, non-condensing

PHYSICAL

Outline Dimensions See Mechanical Specifications

Removable Heat Shield Nylon 46

Weight 0.28 ounces (7.8 grams)

Lead Material Tin-plated copper alloy

Electromagnetic Interference (conducted and radiated) FCC part 15, class B, EN55022 (may need external filter)

Safety UL/cUL 60950 CSA-C22.2 No.234
IEC/EN 60950

Flammability UL94V-0

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Continuous or transient)

W3 models	+7 Volts
12V models	+15 Volts

On/Off Control -0.3V min. to +VIN max.

Input Reverse Polarity Protection See Fuse section

Output Current ⁽⁷⁾ Current-limited. Devices can withstand sustained short circuit without damage.

Storage Temperature -55 to +125°C

Lead Temperature (soldering 10 sec. max.) +280°C

These are stress ratings. Exposure of devices to any of these conditions may adversely affect long-term reliability. Proper operation under conditions other than those listed in the Performance/Functional Specifications Table is not implied.

Performance/Functional Specification Notes:

- (1) All models are tested and specified with external 1 || 10 μ F ceramic/tantalum output capacitors and a 22 μ F external input capacitor. All capacitors are low ESR types. These capacitors are necessary to accommodate our test equipment and may not be required to achieve specified performance in your applications. All models are stable and regulate within spec under no-load conditions.
General conditions for Specifications are +25°C, V_{IN} = nominal, V_{OUT} = nominal, full load. "Nominal" output voltage is +5V for D12 models and +3.3V for W3 models.
- (2) Input Back Ripple Current is tested and specified over a 5-20MHz bandwidth. Input filtering is C_{IN} = 2 x 100 μ F tantalum, C_{BUS} = 1000 μ F electrolytic, L_{BUS} = 1 μ H.
- (3) Note that Maximum Power Derating curves indicate an average current at nominal input voltage. At higher temperatures and/or lower airflow, the DC/DC converter will tolerate brief full current outputs if the total RMS current over time does not exceed the derating curve.
- (4) Mean Time Before Failure is calculated using the Telcordia (Belcore) SR-332 Method 1, Case 3, ground fixed conditions, $T_{PCBOARD}$ = +25°C, full output load, natural air convection.
- (5) The On/Off Control may be driven with external logic or by applying appropriate external voltages which are referenced to -Input Common. The On/Off Control Input should use either an open collector/open drain transistor or logic gate which does not exceed + V_{IN} . A 68K Ω external pullup resistor to + V_{IN} will cause the "ON" state for negative logic models.
- (6) Short circuit shutdown begins when the output voltage degrades approximately 2% from the selected setting.
- (7) If Sense is connected remotely at the load, up to 0.5 Volts difference is allowed between the Sense and + V_{OUT} pins to compensate for ohmic voltage drop in the power lines. A larger voltage drop may cause the converter to exceed maximum power dissipation.
- (8) Output noise may be further reduced by adding an external filter. See I/O Filtering and Noise Reduction.
- (9) All models are fully operational and meet published specifications, including "cold start" at -40°C.
- (10) Regulation specifications describe the deviation as the line input voltage or output load current is varied from a nominal midpoint value to either extreme.
- (11) Other input or output voltage ranges are available under scheduled quantity special order.
- (12) Maximum PC board temperature is measured with the sensor in the center.
- (13) Do not exceed maximum power specifications when adjusting the output trim.
- (14) The maximum output capacitive loads depend on the the Equivalent Series Resistance (ESR) of the external output capacitor.
- (15) Do not use Pre-bias startup and sequencing together. See Technical Notes below.
- (16) After short circuit shutdown, if the load is partially removed such that the load still exceeds the overcurrent (OC) detection, the converter will remain in hiccup restart mode.
- (17) When Sequencing is not used, the Power Good output is TRUE at any time the output is within approximately $\pm 10\%$ of the voltage set point. Power Good basically indicates if the converter is in regulation. Power Good detects Over Temperature if the PWM has shut down due to OT. Power Good does not directly detect Over Current.
If Sequencing is in progress, Power Good will falsely indicate TRUE (valid) before the output reaches its setpoint. Ignore Power Good if Sequencing is in transition.

TECHNICAL NOTES

I/O Filtering and Noise Reduction

All models in the LSM2 Series are tested and specified with external 1 || 10 μ F ceramic/tantalum output capacitors and a 22 μ F tantalum input capacitor. These capacitors are necessary to accommodate our test equipment and may not be required to achieve desired performance in your application. The LSM2's are designed with high-quality, high-performance internal I/O caps, and will operate within spec in most applications with no additional external components.

In particular, the LSM2's input capacitors are specified for low ESR and are fully rated to handle the units' input ripple currents. Similarly, the internal output capacitors are specified for low ESR and full-range frequency response.

In critical applications, input/output ripple/noise may be further reduced using filtering techniques, the simplest being the installation of external I/O caps.

External input capacitors serve primarily as energy-storage devices. They minimize high-frequency variations in input voltage (usually caused by IR drops in conductors leading to the DC/DC) as the switching converter draws pulses of current. Input capacitors should be selected for bulk capacitance (at appropriate frequencies), low ESR, and high rms-ripple-current ratings. The switching nature of modern DC/DC's requires that the dc input voltage source have low ac impedance at the frequencies of interest. Highly inductive source impedances can greatly affect system stability. Your specific system configuration may necessitate additional considerations.

Output ripple/noise (also referred to as periodic and random deviations or PARD) may be reduced below specified limits with the installation of additional external output capacitors. Output capacitors function as true filter elements and should be selected for bulk capacitance, low ESR, and appropriate frequency response. Any scope measurements of PARD should be made directly at the DC/DC output pins with scope probe ground less than 0.5" in length. All external capacitors should have appropriate voltage ratings and be located as close to the converters as possible. Temperature variations for all relevant parameters should be taken into consideration.

The most effective combination of external I/O capacitors will be a function of your line voltage and source impedance, as well as your particular load and layout conditions. Our Applications Engineers can recommend potential solutions and discuss the possibility of our modifying a given device's internal filtering to meet your specific requirements. Contact our Applications Engineering Group for additional details.

Input Fusing

Most applications and or safety agencies require the installation of fuses at the inputs of power conversion components. The LSM2 Series are not internally fused. Therefore, if input fusing is mandatory, either a normal-blow or a fast-blow fuse with a value no greater than twice the maximum input current should be installed within the ungrounded input path to the converter.

As a rule of thumb however, we recommend to use a normal-blow or slow-blow fuse with a typical value of about twice the maximum input current, calculated at low line with the converter's minimum efficiency.

Safety Considerations

LSM2 SMT's are non-isolated DC/DC converters. In general, all DC/DC's must be installed, including considerations for I/O voltages and spacing/separation requirements, in compliance with relevant safety-agency specifications (usually UL/IEC/EN60950).

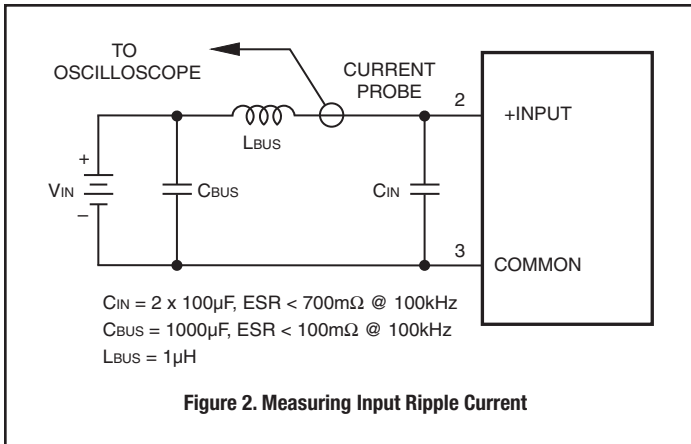
In particular, for a non-isolated converter's output voltage to meet SELV (safety extra low voltage) requirements, its input must be SELV compliant. If the output needs to be ELV (extra low voltage), the input must be ELV.

Input Overvoltage and Reverse-Polarity Protection

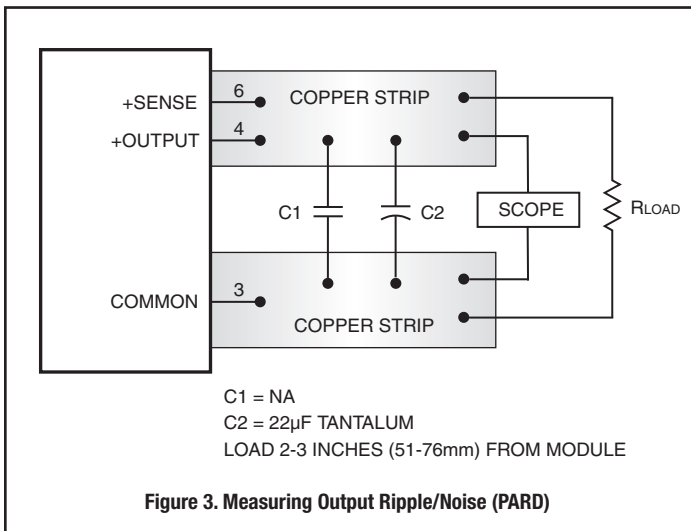
LSM2 SMT Series DC/DC's do not incorporate either input overvoltage or input reverse-polarity protection. Input voltages in excess of the specified absolute maximum ratings and input polarity reversals of longer than "instantaneous" duration can cause permanent damage to these devices.

Start-Up Time

The V_{IN} to V_{OUT} Start-Up Time is the interval between the time at which a



ramping input voltage crosses the lower limit of the specified input voltage range and the fully loaded output voltage enters and remains within its specified accuracy band. Actual measured times will vary with input source impedance, external input capacitance, and the slew rate and final value of the input voltage as it appears to the converter.



The On/Off to V_{OUT} Start-Up Time assumes the converter is turned off via the On/Off Control with the nominal input voltage already applied to the converter. The specification defines the interval between the time at which the converter is turned on and the fully loaded output voltage enters and remains within its specified accuracy band. See Typical Performance Curves.

Remote Sense

LSM2 Series offer an output sense function. The sense function enables point-of-use regulation for overcoming moderate IR drops in conductors and/or cabling. Since these are non-isolated devices whose inputs and outputs usually share the same ground plane, sense is provided only for the +Output.

The remote sense line is part of the feedback control loop regulating the DC/DC converter's output. The sense line carries very little current and consequently requires a minimal cross-sectional-area conductor. As such,

it is not a low-impedance point and must be treated with care in layout and cabling. Sense lines should be run adjacent to signals (preferably ground), and in cable and/or discrete-wiring applications, twisted-pair or similar techniques should be used. To prevent high frequency voltage differences between V_{OUT} and Sense, we recommend installation of a 1000pF capacitor close to the converter.

The sense function is capable of compensating for voltage drops between the +Output and +Sense pins that do not exceed 10% of V_{OUT} .

$$[V_{OUT}(+) - \text{Common}] - [\text{Sense}(+) - \text{Common}] \leq 10\%V_{OUT}$$

Power derating (output current limiting) is based upon maximum output current and voltage at the converter's output pins. Use of trim and sense functions can cause the output voltage to increase, thereby increasing output power beyond the LSM2's specified rating. Therefore:

$$(V_{OUT} \text{ at pins}) \times (I_{OUT}) \leq \text{rated output power}$$

The internal 10.5Ω resistor between +Sense and +Output (see Figure 1) serves to protect the sense function by limiting the output current flowing through the sense line if the main output is disconnected. It also prevents output voltage runaway if the sense connection is disconnected.

Note: If the sense function is not used for remote regulation, +Sense must be tied to +Output at the DC/DC converter pins.

Sense Input

Use the Sense input with caution. Many applications do not need the Sense connection. Sense is intended to correct small output accuracy errors caused by the resistive ohmic drop in output wiring as output current increases. This output drop (the difference between Sense and V_{OUT} when measured at the converter) should not be allowed to exceed 0.5V. Consider using heavier wire if this drop is excessive.

Sense is connected at the load and corrects for resistive errors only. Be careful where it is connected. Any long, distributed wiring and/or significant inductance introduced into the Sense control loop can adversely affect overall system stability. If in doubt, test the application, and observe the DC/DC's output transient response during step loads. There should be no appreciable ringing or oscillation. You may also adjust the output trim slightly to compensate for voltage loss in any external filter elements. Do not exceed maximum power ratings.

On/Off Control

The On/Off Control pin may be used for remote on/off operation. Positive logic LSM2 Series DC/DC converters are designed so that they are enabled when the control pin is left open (open collector) and disabled when the control pin is pulled low (to less than +0.3V relative to Common). As shown in Figure 4, all models have an internal pull-up current source to V_{IN} (+Input).

Dynamic control of the on/off function is best accomplished with a mechanical relay or open-collector/open-drain drive circuit (optically isolated if appropriate). The drive circuit should be able to sink appropriate current when activated and withstand appropriate voltage when deactivated.

Applying an external voltage to the On/Off Control pin when no input power is applied to the converter can cause permanent damage to the converter. The on/off control function, however, is designed such that the converter can be disabled (control pin pulled low) while input voltage is ramping up and then "released" once the input has stabilized (see also power-up sequencing).

Power-up sequencing

If a controlled start-up of one or more LSM2 Series DC/DC converters is required, or if several output voltages need to be powered-up in a given sequence, the On/Off control pin can be driven with an external open collector device as per Figure 4.

Leaving the input of the on/off circuit closed during power-up will have the output of the DC/DC converter disabled. When the input to the external open collector is pulled high, the DC/DC converter's output will be enabled.

Output Overvoltage Protection

LSM2 SMT Series DC/DC converters do not incorporate output overvoltage protection. In the extremely rare situation in which the device's feedback loop is broken, the output voltage may run to excessively high levels ($V_{OUT} = V_{IN}$). If it is absolutely imperative that you protect your load against any and all possible overvoltage situations, voltage limiting circuitry must be provided external to the power converter. Output Overcurrent Detection

Overloading the power converter's output for an extended time will invariably cause internal component temperatures to exceed their maximum ratings and eventually lead to component failure. High-current-carrying components such as inductors, FET's and diodes are at the highest risk. LSM2 SMT Series DC/DC converters incorporate an output overcurrent detection and shutdown function that serves to protect both the power converter and its load.

If the output current exceeds its maximum rating by typically 50% or if the output voltage drops to less than 98% of its original value, the LSM2's internal overcurrent-detection circuitry immediately turns off the converter, which then goes into a "hiccup" mode. While hiccupping, the converter will continuously attempt to restart itself, go into overcurrent, and then shut down. Once the output short is removed, the converter will automatically restart itself. Output

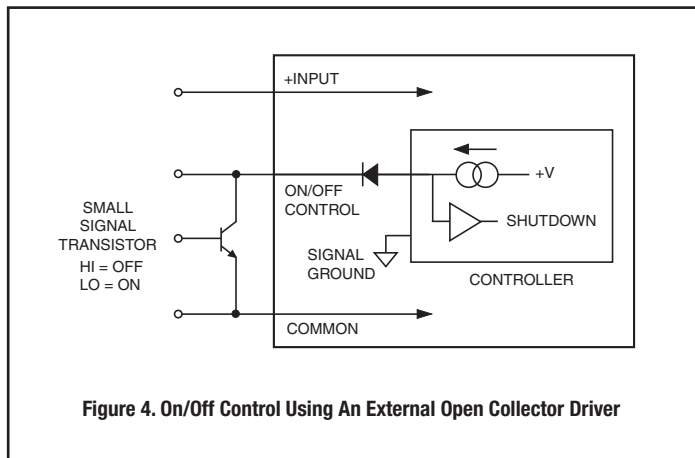


Figure 4. On/Off Control Using An External Open Collector Driver

Reverse Conduction

Many DC/DC's using synchronous rectification suffer from Output Reverse Conduction. If those devices have a voltage applied across their output before a voltage is applied to their input (this typically occurs when another power supply starts before them in a power-sequenced application), they will either fail to start or self destruct. In both cases, the cause is the "freewheeling" or "catch" FET biasing itself on and effectively becoming a short circuit.

LSM2 SMT DC/DC converters do not suffer from Output Reverse Conduction. They employ proprietary gate drive circuitry that makes them immune to

moderate applied output overvoltages.

Thermal Considerations and Thermal Protection

The typical output-current thermal-derating curves shown below enable designers to determine how much current they can reliably derive from each model of the LSM2 SMT's under known ambient-temperature and air-flow conditions. Similarly, the curves indicate how much air flow is required to reliably deliver a specific output current at known temperatures.

The highest temperatures in LSM2 SMT's occur at their output inductor, whose heat is generated primarily by I^2R losses. The derating curves were developed using thermocouples to monitor the inductor temperature and varying the load to keep that temperature below +110°C under the assorted conditions of air flow and air temperature. Once the temperature exceeds +115°C (approx.), the thermal protection will disable the converter. Automatic restart occurs after the temperature has dropped below +110°C.

As you may deduce from the derating curves and observe in the efficiency curves on the following pages, LSM2 SMT's maintain virtually constant efficiency from half to full load, and consequently deliver very impressive

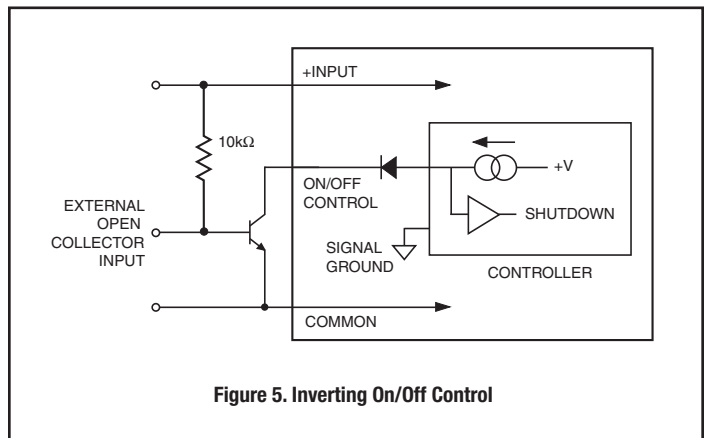


Figure 5. Inverting On/Off Control

temperature performance even if operating at full load.

Lastly, when LSM2 SMT's are installed in system boards, they are obviously subject to numerous factors and tolerances not taken into account here. If you are attempting to extract the most current out of these units under demanding temperature conditions, we advise you to monitor the output-inductor temperature to ensure it remains below +110°C at all times.

Start Up Considerations

When power is first applied to the DC/DC converter, operation is different than when the converter is running and stabilized. There is some risk of start up difficulties if you do not observe several application features. Lower output voltage converters may have more problems here since they tend to have higher output currents. Operation is most critical with any combination of the following external factors:

- 1 - Low initial input line voltage and/or poor regulation of the input source.
- 2 - Full output load current on lower output voltage converters.
- 3 - Slow slew rate of input voltage.
- 4 - Longer distance to input voltage source and/or higher external input source impedance.

- 5 - Limited or insufficient ground plane. External wiring that is too small.
- 6 - Too small external input capacitance. Too high ESR.
- 7 - High output capacitance causing a start up charge overcurrent surge.
- 8 - Output loads with excessive inductive reactance or constant current characteristics.

If the input voltage is already at the low limit before power is applied, the start up surge current may instantaneously reduce the voltage at the input terminals to below the specified minimum voltage. Even if this voltage depression is very brief, this may interfere with the on-board controller and possibly cause a failed start. Or the converter may start but the input current load will now drive the input voltage below its running low limit and the converter will shut down.

If you measure the input voltage before start up with a Digital Voltmeter (DVM), the voltage may appear to be adequate. Limited external capacitance and/or too high a source impedance may cause a short downward spike at power up, causing an instantaneous voltage drop. Use an oscilloscope not a DVM to observe this spike. The converter's soft-start controller is sensitive to input voltage. What matters here is the actual voltage at the input terminals at all times.

Symptoms of start-up difficulties may include failed started, output oscillation or brief start up then overcurrent shutdown. Since the input voltage is never absolutely constant, the converter may start up at some times and not at others.

Solutions

To improve start up, review the conditions above. One of the better solutions is to place a moderate size capacitor very close to the input terminals. You may need two parallel capacitors. A larger electrolytic or tantalum cap supplies the surge current and a smaller parallel low-ESR ceramic cap gives low AC impedance. Too large an electrolytic capacitor may have higher internal impedance (ESR) and/or lower the start up slew rate enough to upset the DC/DC's controller. Make sure the capacitors can tolerate reflected switching current pulses from the converter.

The capacitors will not help if the input source has poor regulation. A converter which starts successfully at 3.3 Volts will turn off if the input voltage decays to below the input voltage threshold, regardless of external capacitance.

Increase the input start up voltage if possible to raise the downward voltage spike. Also, make sure that the input voltage ramps up in a reasonably short time (less than a few milliseconds). If possible, move the input source closer to the converter to reduce ohmic losses in the input wiring. Remember that the input current is carried both by the wiring and the ground plane return. Make sure the ground plane uses adequate thickness copper. Run additional bus wire if necessary.

Any added output capacitor should use just enough capacitance (and no more) to reduce output noise at the load and to avoid marginal threshold noise problems with external logic. An output cap will also "decouple" inductive reactance in the load. Certain kinds of electronic loads include "constant current" characteristics which destabilize the output with insufficient capacitance. If the wiring to the eventual load is long, consider placing this decoupling cap at the load. Use the Remote Sense input to avoid ohmic voltage drop errors.

An elegant solution to start up problems is to apply the input voltage with the Remote On/Off control first in the off setting (for those converters with an On/Off Control). After the specified start-up delay (usually under 20 mSec), turn on

the converter. The controller will have already been stabilized. The short delay will not be noticed in most applications. Be aware of applications which need "power management" (phased start up).

Finally, it is challenging to model some application circuits with absolute fidelity. How low is the resistance of your ground plane? What is the inductance (and distributed capacitance) of external wiring? Even a detailed mathematical model may not get all aspects of your circuit. Therefore it is difficult to give cap values which serve all applications. Some experimentation may be required.

Pre-Biased Startup

Newer systems with multiple power voltages have an additional problem besides startup sequencing. Some sections have power already partially applied (possibly because of earlier power sequencing) or have leakage power present so that the DC/DC converter must power up into an existing voltage. This power may either be stored in an external bypass capacitor or supplied by an active source.

This "pre-biased" condition can also occur with some types of programmable logic or because of blocking diode leakage or small currents passed through forward biased ESD diodes. Conventional DC/DC's may fail to start up correctly if there is output voltage already present. And some external circuits are adversely affected when the low side MOSFET in a synchronous rectifier converter sinks current at start up.

The LSM2 series includes a pre-bias startup mode to prevent these initialization problems. Essentially, the converter acts as a simple buck converter until the output reaches its set point voltage at which time it converts to a synchronous rectifier design. This feature is variously called "monotonic" because the voltage does not decay (from low side MOSFET shorting) or produce a negative transient once the input power is applied and the startup sequence begins.

Don't Use Pre-Biasing and Sequencing Together

Normally, you would use startup sequencing on multiple DC/DC's to solve the Pre-Bias problem. By causing all power sources to ramp up together, no one source can dominate and force the others to fail to start. For most applications, do not use startup sequencing in a Pre-Bias application, especially with an external active power source.

If you have active source pre-biasing, leave the Sequence input open so that the output will step up quickly and safely. A symptom of this condition is repeated failed starts. You can further verify this by removing the existing load and testing it with a separate passive resistive load which does not exceed full current. If the resistive load starts successfully, you may be trying to drive an external pre-biased active source.

It may also be possible to use pre-bias and sequencing together if the Pre-Bias source is in fact only a small external bypass capacitor slowly charged by leakage currents. Test your application to be sure.

Output Adjustments

The LSM2 series includes a special output voltage trimming feature which is fully compatible with competitive units. The output voltage may be varied using a single trim resistor from the Trim input to Power Common (pin 4) or an external DC trim voltage applied between the Trim input and Power Common. The output voltage range for W3 models is 0.75 to 3.3 Volts. For D12 models, the output range is 0.75 to 5 Volts.

IMPORTANT: On W3 models only, for outputs greater than 3 Volts up to 3.3 Volts maximum, the input supply must be 4.5 Volts minimum. To retain proper regulation, do not exceed the 3.3V output.

As with other trim adjustments, be sure to use a precision low-tempco resistor (± 100 ppm/ $^{\circ}$ C) mounted close to the converter with short leads. Also be aware that the output voltage accuracy is $\pm 2\%$ (typical) therefore you may need to vary this resistance slightly to achieve your desired output setting.

Two different trim equations are used for the W3 and D12 models.

W3 Models Resistor Trim Equation:

$$R_{TRIM} (W) = \frac{21070}{V_o - 0.7525} - 5110$$

The W3 models fixed trim resistors to set the output voltage are:

V _{OUT} (Typ.)	0.7525V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V
R _{TRIM} (k Ω)	Open	80.021	41.973	23.077	15.004	6.947	3.16

D12 Models Resistor Trim Equation:

$$R_{TRIM} (W) = \frac{10500}{V_o - 0.7525} - 1000$$

V _{OUT}	0.7525V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
R _{TRIM} (k Ω)	Open	41.424	22.46	13.05	9.024	5.009	3.122	1.472

Voltage Trim

The LSM2 Series may also be trimmed using an external voltage applied between the Trim input and Output Common. Be aware that the internal “load” impedance looking into trim pin is approximately 5 Kiloohms. Therefore, you may have to compensate for this in the source resistance of your external voltage reference.

Use a low noise DC reference and short leads. Mount the leads close to the converter. Consider using a small bypass capacitor (0.1 μ F ceramic) between trim and output common to avoid instability.

Two different trim equations are used for the W3 and D12 models.

W3 Models Voltage Trim Equation:

$$V_{TRIM} \text{ (in Volts)} = 0.7 - (0.1698 \times (V_o - 0.7525))$$

The LSM2 W3 fixed trim voltages to set the output voltage are:

V _{OUT} (Typ.)	0.7525V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V
V _{TRIM}	Open	0.6928V	0.624V	0.5731V	0.5221V	0.4033V	0.267V

D12 Models Voltage Trim Equation:

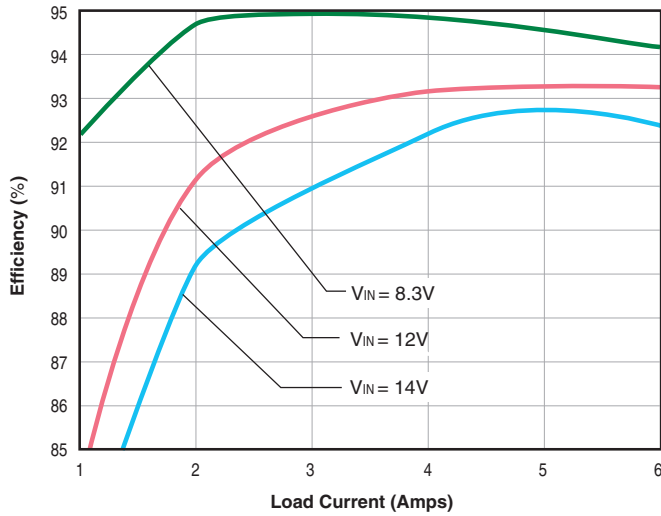
$$V_{TRIM} \text{ (in Volts)} = 0.7 - (0.0667 \times (V_o - 0.7525))$$

The LSM2 D12 fixed trim voltages to set the output voltage are:

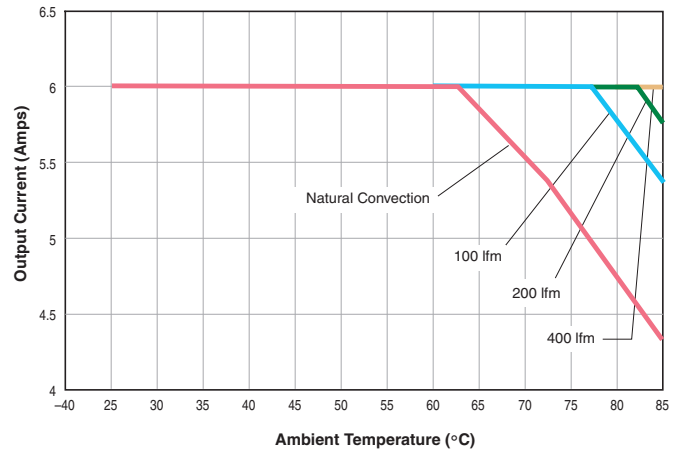
V _{OUT}	0.7525V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
V _{TRIM} (V)	Open	0.6835	0.670	0.650	0.630	0.583	0.530	0.4166

TYPICAL PERFORMANCE CURVES

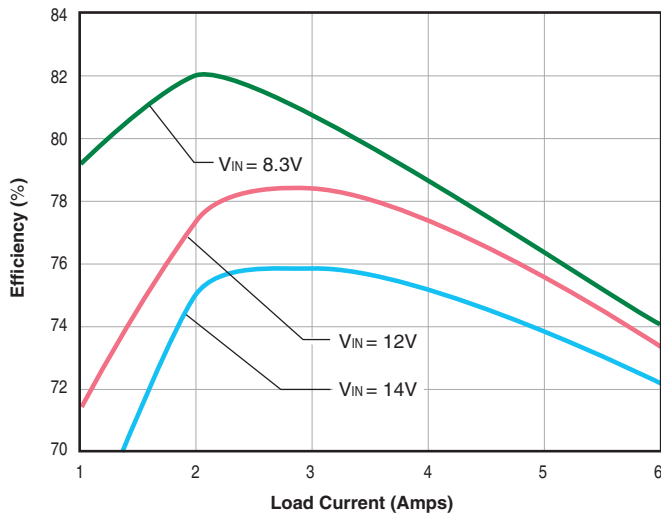
LSM2-T/6-D12
Efficiency vs. Line Voltage and Load Current @ 25°C (V_{out} = 5V)



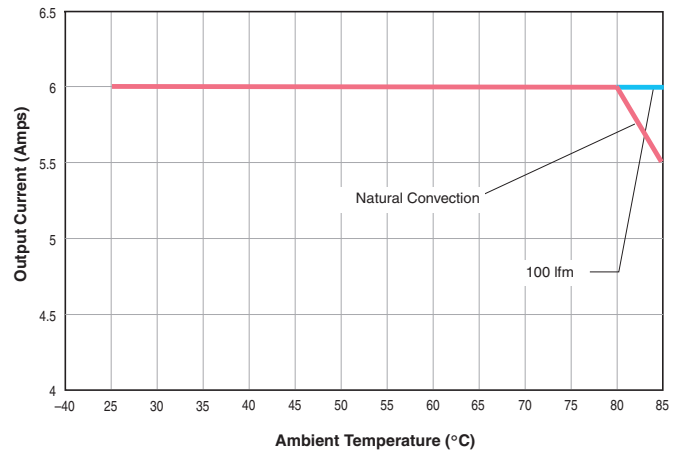
LSM2-T/6-D12 Maximum Current Temperature Derating
V_{out} = 5V (air flow from input to output)



LSM2-T/6-D12
Efficiency vs. Line Voltage and Load Current @ 25°C (V_{out} = 0.75V)



LSM2-T/6-D12 Maximum Current Temperature Derating
V_{out} = 0.75V (air flow from input to output)



Tape & Reel Surface Mount Package

DATEL's LSM2 series DC/DC converters are the only higher-current (16A) SMT DC/DC's that can be automatically "pick-and-placed" using standard vacuum-pickup equipment (nozzle size and style, vacuum pressure and placement speed may need to be optimized for automated pick and place) and subsequently reflowed using high-temperature, lead-free solder.

Virtually all SMT DC/DC's today are unprotected "open-frame" devices assembled by their vendors with high-temperature solder (usually Sn96.5/Ag3.5 with a melting point +221°C) so that you may attach them to your board using low-temperature solder (usually Sn63/Pb37 with a melting point of +183°C). Conceptually straightforward, this "stepped" solder approach has its limitations, and it is clearly out of step with an industry trending toward the broad use of lead-free solders. Are you to experiment and develop reflow profiles from other vendors that ensure the components on those DC/DC never exceed 215-216°C? If those components get too hot, "double-reflow" could compromise the reliability of their solder joints. Virtually all these devices demand you "cool down" the Sn63 profile you are likely using today.

DATEL is not exempted from the Laws of Physics, and we do not have magic solders no one else has. Nevertheless, we have a simple and practical, straightforward approach that works. We assemble our LSM2 SMT DC/DC's using a high-temperature (+216°C), lead-free alloy (Sn96.2%, Ag2.5%, Cu0.8%, Sb0.5%). The LSM2 design ensures co-planarity to within 0.004 inches (100µm) of the unit's tin-plated (150 micro-inches) copper leads. See Mechanical Data for additional information.

The disposable heat shield (patent pending), which has a cutaway exposing the package leads, provides thermal insulation to internal components during reflow and its smooth surface ideally doubles as the vacuum pick-up location also. The insulation properties of the heat shield are so effective that temperature differentials as high as 50°C develop inside-to-outside the shield. Oven temperature profiles with peaks of 250-260°C and dwell times exceeding 2 minutes above 221°C (the melting point of Sn96.5/Ag3.5) are easily achieved.

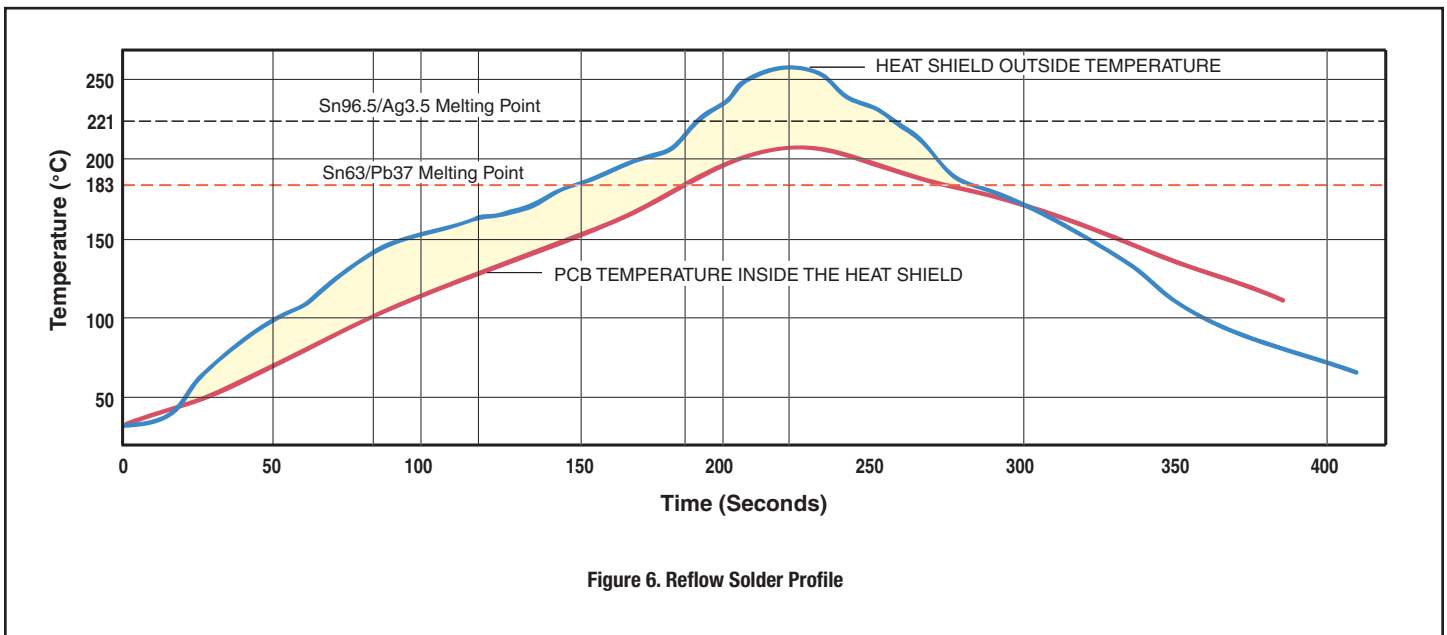


Figure 6. Reflow Solder Profile

LSM2 TAPE AND REEL SPECIFICATIONS

DATEL's new-generation LSM2 SMT DC/DC converters are shipped in quantities of 150 modules per tape and reel.

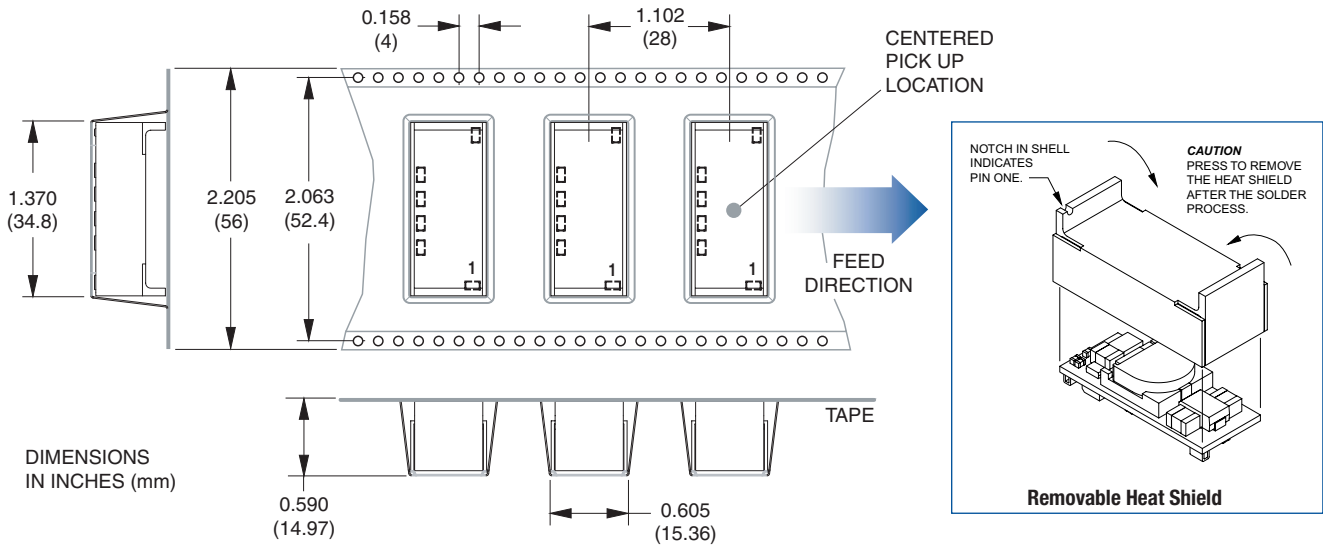


Figure 7. Tape Dimensions

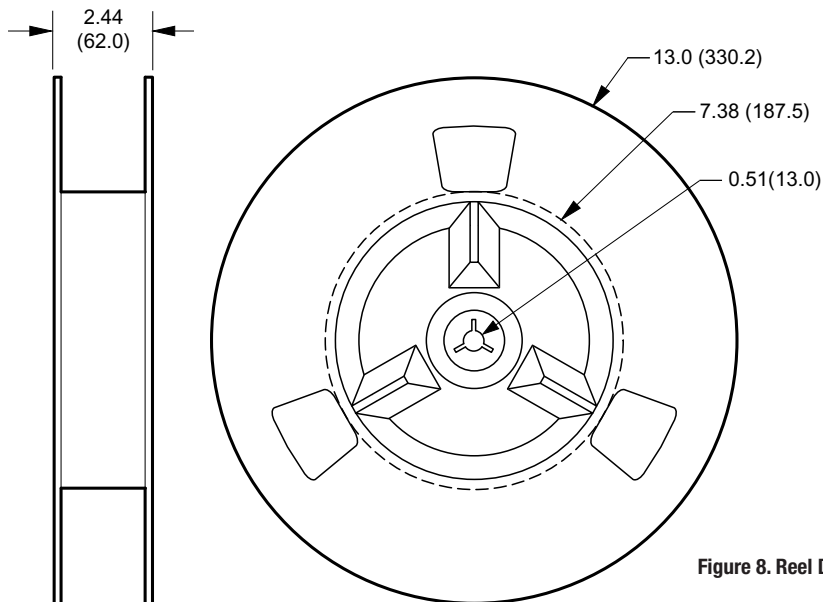


Figure 8. Reel Dimensions

LSM2 Power Sequencing

Whereas in the old days, one master switch simultaneously turned on the power for all parts of a system, many modern systems require multiple supply voltages for different on-board sections. Typically the CPU or microcontroller needs 1.8 Volts or lower. Memory (particularly DDR) may use 1.8 to 2.5 Volts. Interface “glue” and “chipset” logic might use +3.3Vdc power while Input/ Output subsystems may need +5V. Finally, peripherals use 5V and/or 12V.

Timing is Everything

This mix of system voltages is being distributed by several local power solutions including Intermediate Bus Architecture (IBA) bus converters, Point-of-load (POL) DC/DC converters and sometimes a linear regulator, all sourced from a master AC power supply. While this mix of voltages is challenging enough, a further difficulty is the start-up and shutdown timing relationship between these power sources and relative voltage differences between them.

For many systems, the CPU and memory must be powered up, boot-strap loaded and stabilized before the I/O section is turned on. This avoids uncommanded data bytes being transferred, compromising an active external network or placing the I/O section in an undefined mode. Or it keeps bad commands out of disk and peripheral controllers until they are ready to go to work.

Another goal for staggered power-up is to avoid an oversize load applied to the master source all at once. A more serious reason to manage the timing and voltage differences is to avoid either a latchup condition in programmable logic (a latchup might ignore commands or would respond improperly to them) or a high current startup situation (which may damage on-board circuits). And on the power down phase, inappropriate timing or voltages can cause interface logic to send a wrong “epitaph” command.

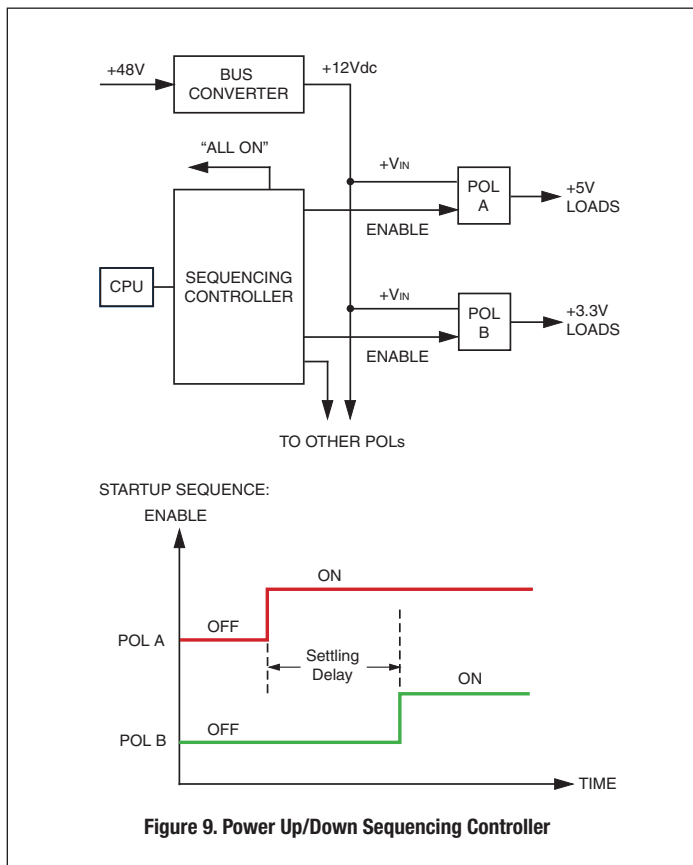


Figure 9. Power Up/Down Sequencing Controller

Two Approaches

There are two ways to manage these timing and voltage differences. Either the power up/down sequence can be controlled by discrete On/Off logic controls for each power supply (see Figure 9). Or the power up/down cycle is set by Sequencing or Tracking circuits. Some systems combine both methods.

The first system (discrete On/Off controls) applies signals from an already-powered logic sequencer or dedicated microcontroller which turns on each downstream power section in cascaded series. This of course assumes all POL's have On/Off controls. A distinct advantage of the sequencing controller is that it can produce an “All On” output signal to state that the full system is stable and ready to go to work. For additional safety, the sequencer can monitor the output voltages of all downstream POL's with an A/D converter system.

However the sequencer controller has some obvious difficulties besides extra cost, wiring and programming complexity. First, power is applied as a fast-rising, all-or-nothing step which may be unacceptable to certain circuits, especially large output bypass capacitors. These could force POL's into overcurrent shutdown. And some circuits (such as many linear regulators and some POL's) may not have convenient start-up controls. This requires designing and fabricating external power controls such as high-current MOSFET's.

If the power up/down timing needs to be closely controlled, each POL must be characterized for start-up and down times. These often vary—one POL may stabilize in 15 milliseconds whereas another takes 50 milliseconds. Another problem is that the sequencing controller itself must be “already running” and stabilized before starting up other circuits. If there is a glitch in the system, the power up/down sequencer could get out of step with possible disastrous results. Lastly, changing the timing may require reprogramming the logic sequencer or rewriting software.

Sequence/Track Input

A different power sequencing solution is employed on DATEL's LSM2 DC/DC converter. After external input power is applied and the converter stabilizes, a high impedance Sequence/Track input pin accepts an external analog voltage. The output power voltage will then track this Sequence/Track input at a one-to-one ratio up to the nominal set point voltage for that converter. This Sequencing input may be ramped, delayed, stepped or otherwise phased as needed for the output power, all fully controlled by the user's simple external circuits. As a direct input to the converter's feedback loop, response to the Sequence/Track input is very fast (milliseconds).

By properly controlling this Sequence pin, most operations of the discrete On/Off logic sequencer may be duplicated. The Sequence pin system does not use the converter's Enable On/Off control (unless it is a master emergency shut down system).

Power Phasing Architectures

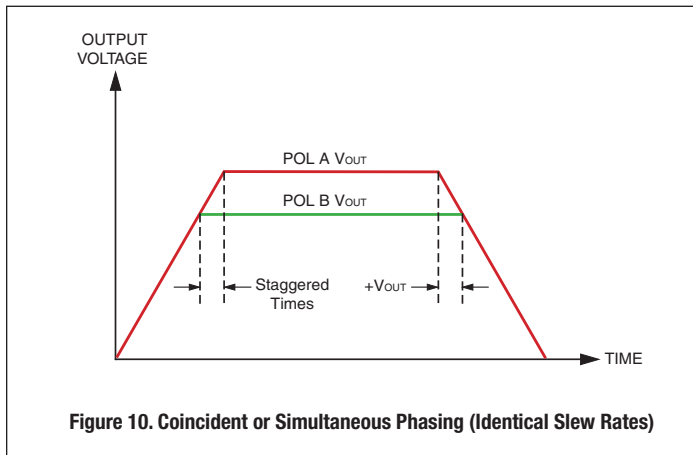
Observe the simplified timing diagrams below. There are many possible power phasing architectures and these are just some examples to help you analyze your system. Each application will be different. Multiple output voltages may require more complex timing than that shown here.

These diagrams illustrate the time and slew rate relationship between two typical power output voltages. Generally the Master will be a primary power voltage in the system which must be present first or coincident with any Slave power voltages. The Master output voltage is connected to the Slave's Sequence input, either by a voltage divider, divider-plus-capacitor or some other method. Several standard sequencing architectures are prevalent. They are concerned with three factors:

- The time relationship between the Master and Slave voltages
- The voltage difference relationship between the Master and Slave
- The voltage slew rate (ramp slope) of each converter's output.

For most systems, the time relationship is the dominant factor. The voltage difference relationship is important for systems very concerned about possible latchup of programmable devices or overdriving ESD diodes. Lower slew rates avoid overcurrent shutdown during bypass cap charge-up.

In Figure 10, two POL's ramp up at the same rate until they reach their different respective final set point voltages. During the ramp, their voltages are nearly identical. This avoids problems with large currents flowing between



logic systems which are not initialized yet. Since both end voltages are different, each converter reaches its setpoint voltage at a different time.

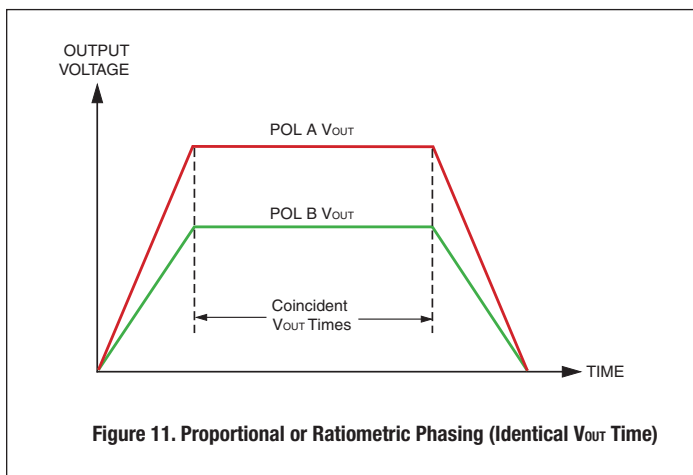


Figure 11 shows two POL's with different slew rates in order to reach differing final voltages at about the same time.

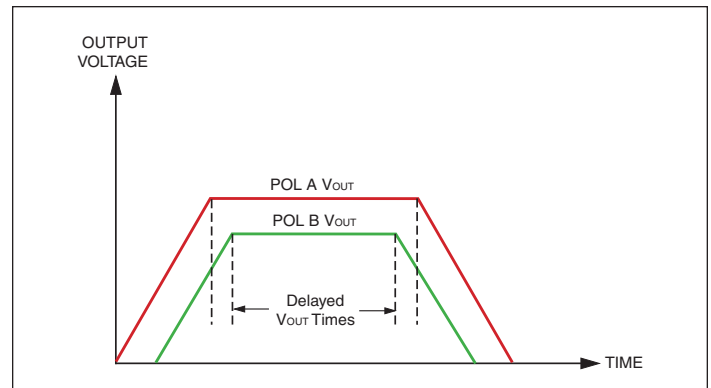
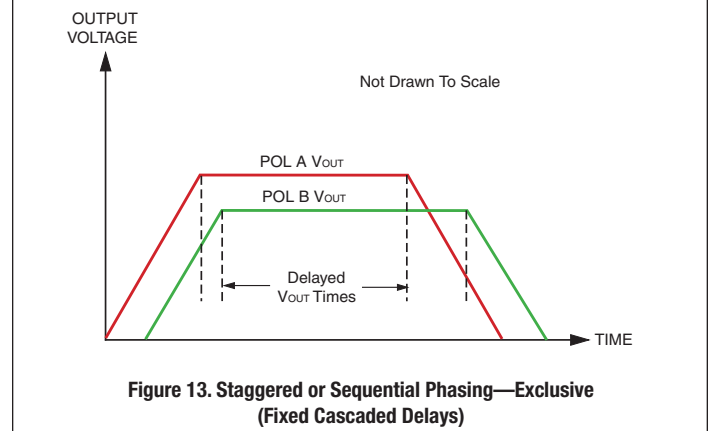


Figure 12. Staggered or Sequential Phasing—Inclusive (Fixed Delays)



Figures 12 and 13 show both delayed start up and delayed final voltages for two converters. Figure 12 is called "Inclusive" because the later starting POL finishes inside the earlier POL. The timing in Figure 12 is more easily built using a combined digital sequence controller and the Sequence/Track pin.

Figure 13 is the same strategy as Figure 12 but with an "exclusive" timing relationship staggered approximately the same at power-up and power-down.

Operation

To use the Sequence pin after power start-up stabilizes, apply a rising external voltage to the Sequence input. As the voltage rises, the output voltage will track the Sequence input (gain = 1). The output voltage will stop rising when it reaches the normal set point for the converter. The Sequence input may optionally continue to rise without any effect on the output. Keep the Sequence input voltage below the converter's input supply voltage.

Use a similar strategy on power down. The output voltage will stay constant until the Sequence input falls below the set point.

Any strategy may be used to deliver the power up/down ramps. The circuits below show simple RC networks but you may also use operational amplifiers, D/A converters, etc.

Circuits

The circuits shown in Figures 14 through 16 introduce several concepts when using these Sequencing controls on Point-of-Load (POL) converters. These circuits are only for reference and are not intended as final designs ready for your application. Also, numerous connections are omitted for clarity.

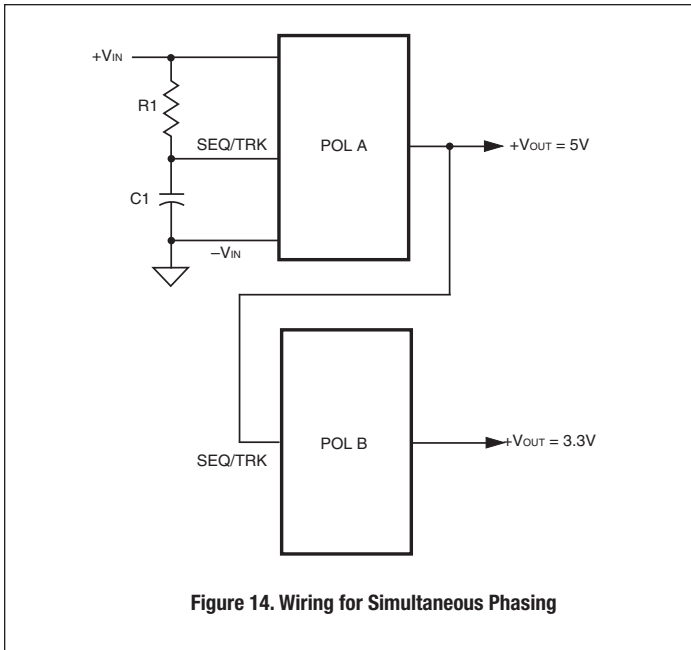


Figure 14. Wiring for Simultaneous Phasing

Figure 14 shows a basic Master (POL A) and Slave (POL B) connected so the POL B ramps up identically to POL A as shown in timing diagram, Figure 10. RC network R1 and C1 charge up at a rate set by the R1-C1 time constant, giving a roughly linear ramp. As POL A reaches 3.3V_{OUT} (the setpoint of POL B), POL B will stop rising. POL A then continues rising until it reaches 5V. R1 should be significantly smaller than the internal bias current resistor from the Sequence pin. Start with a 20kΩ value. We assume that the critical phase is only on power up therefore there is no provision for ramped power down.

Figure 15 shows a single POL and the same RC network. However, we have added a FET at Q1 as an up/down control. When V_{IN} power is applied to the POL, Q1 is biased on, shorting out the Sequence pin. When Q1's gate is biased off, R1 charges C1 and the POL's output ramps up at the R1-C1 slew rate. Note: Q1's gate would typically be controlled from some external digital logic.

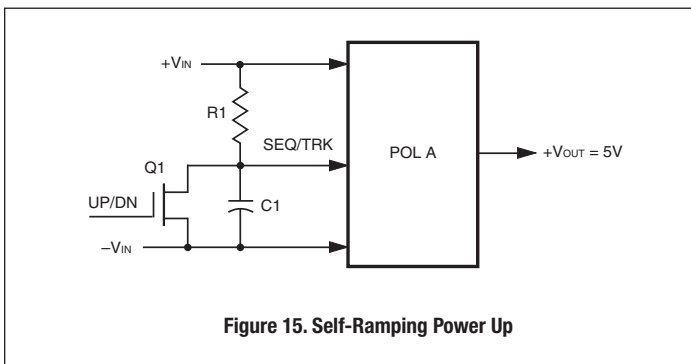


Figure 15. Self-Ramping Power Up

If you wish to have a ramped power down (rather than a step down), add a small resistor in series with Q1's drain.

Figure 16 shows both a RC ramp on Master POL A and a proportional tracking divider (R2 and R3) on POL B. We have also added an optional very small noise filter cap at C2. Figure 16's circuit corresponds roughly to Figure 11's timing for power up.

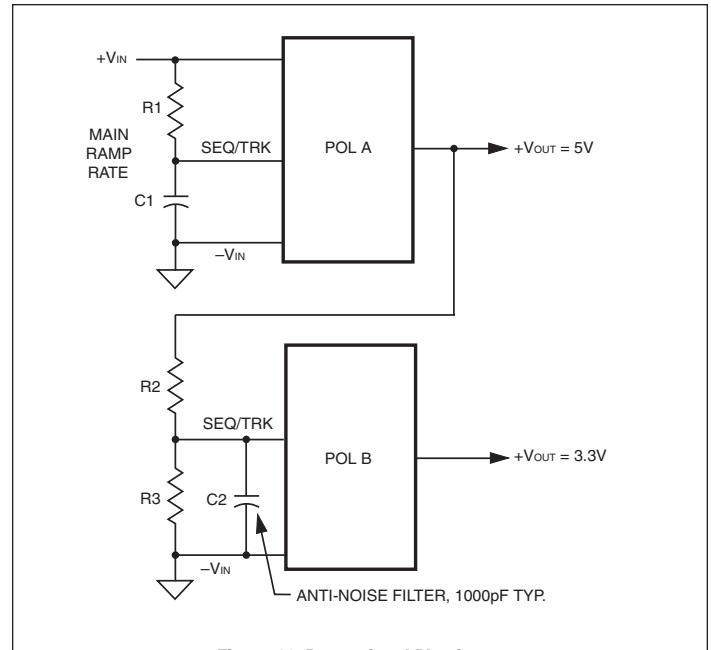


Figure 16. Proportional Phasing

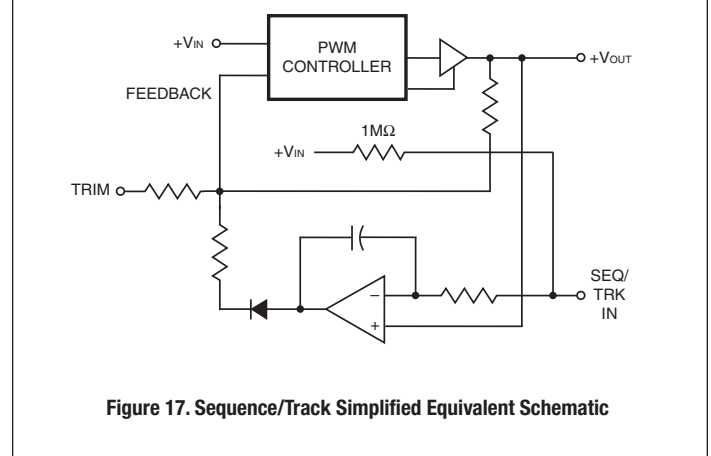


Figure 17. Sequence/Track Simplified Equivalent Schematic

Guidelines for Sequence/Track Applications

- [1] Leave the converter's On/Off Enable control (if installed) in the On setting. Normally, you should just leave the On/Off pin open.
- [2] Allow the converter to stabilize (typically less than 20 mS after +V_{IN} power on) before raising the Sequence input. Also, if you wish to have a ramped power down, leave +V_{IN} powered all during the down ramp. Do not simply shut off power.
- [3] If you do not use the Sequence/Track pin, leave it open or tied to +V_{IN}.
- [4] Observe the Output slew rate relative to the Sequence input. A rough guide is 2 Volts per millisecond maximum slew rate. If you exceed this slew rate on the Sequence pin, the converter will simply ramp up at its maximum output slew rate (and will not necessarily track the faster Sequence input). The reason to carefully consider the slew rate limitation is in case you want two different POL's to precisely track each other.

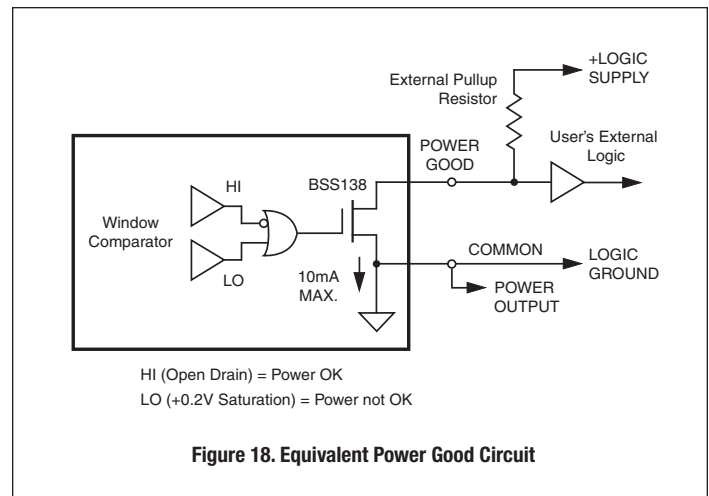
- [5] Be aware of the input characteristics of the Sequence pin. The high input impedance affects the time constant of any small external ramp capacitor. And the bias current will slowly charge up any external caps over time if they are not grounded. The internal pull-up resistor to $+V_{IN}$ is typically $400k\Omega$ to $1M\Omega$.
Notice in the simplified Sequence/Track equivalent circuit (Figure 17) that a blocking diode effectively disconnects this circuit when the Sequence/Track pin is pulled up to $+V_{IN}$ or left open.
- [6] Allow the converter to eventually achieve its full-rated setpoint output voltage. Do not remain in ramp up/down mode indefinitely. The converter is characterized and meets all its specifications only at the setpoint voltage (plus or minus any trim voltage). During the ramp-up phase, the converter is not considered fully in regulation. This may affect performance with excessive high current loads at turn-on.
- [7] The Sequence is a sensitive input into the feedback control loop of the converter. Avoid noise and long leads on this input. Keep all wiring very short. Use shielding if necessary. Consider adding a small parallel ceramic capacitor across the Sequence/Track input (see Figure 16) to block any external high frequency noise.
- [8] If one converter is slaving to another master converter, there will be a very short phase lag between the two converters. This can usually be ignored.
- [9] You may connect two or more Sequence inputs in parallel from two converters. Be aware of the increasing pull-up bias current and reduced input impedance.
- [10] Any external capacitance added to the converter's output may affect ramp up/down times and ramp tracking accuracy.

Power Good Output

The Power Good Output consists of an unterminated BSS138 small signal field effect transistor and a dual window comparator input circuit driving the gate of the FET. Power Good is TRUE (open drain, high impedance state) if the converter's power output voltage is within about $\pm 10\%$ of the setpoint. Thus, the PG TRUE condition indicates that the converter is approximately within regulation. Since an overcurrent condition occurs at about 2% output voltage reduction, the Power Good does not directly measure an output overcurrent condition at rated maximum output current. However, gross overcurrent or an output short circuit will set Power Good to FALSE ($+0.2V$ saturation, low impedance condition).

Using a simple connection to external logic (and returned to the converter's Common connection), the Power Good output is unterminated so that the user may adapt the output to a variety of logic families. The PG pin may therefore be used with logic voltages which are not necessarily the same as the input or output power voltages. Install an external pullup resistor to the logic supply voltage which is compatible with your logic system. When the Power Good is out of limit, the FET is at saturation, approximately $+0.2V$ output. Keep this LOW (FALSE) pulldown current to less than 10mA.

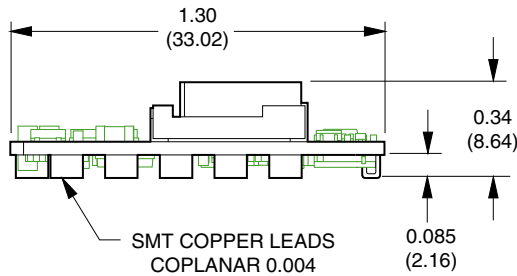
Please note that Power Good is briefly false during Sequence ramp-up. Ignore Power Good while in transition.



MECHANICAL SPECIFICATIONS

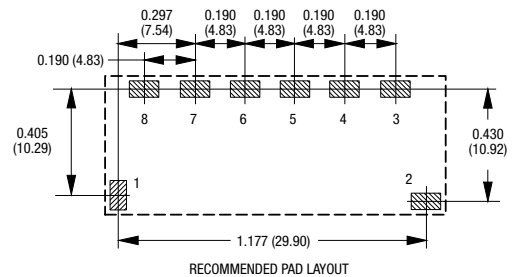
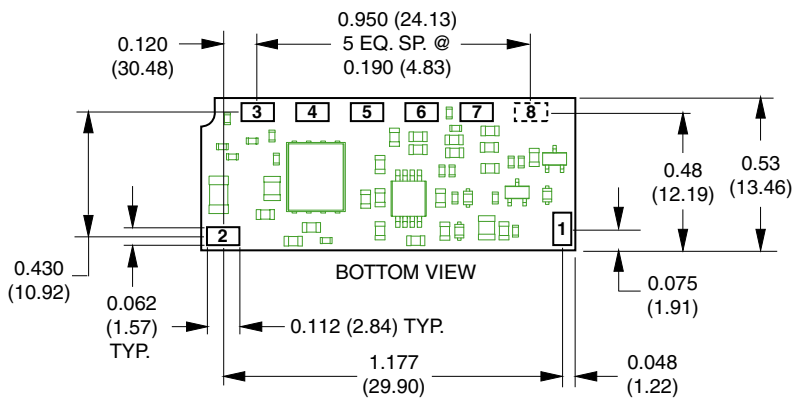
10/16 Amp Models

Case C62



I/O CONNECTIONS	
Pin	Function P66
1	On/Off Control
2	+Input
3	Seq./Track
4	Common
5	+Output
6	Trim
7	Sense
8	Power Good*

* Power Good is only installed for 10 and 16 Amp "G" W3 models, otherwise pad 8 is not installed.

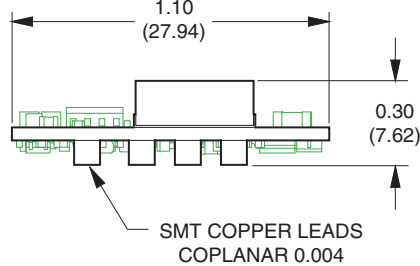


Recommended Pad Size: 0.15 x 0.10 (3.81 x 2.54)

DIMENSIONS ARE IN INCHES (MM)

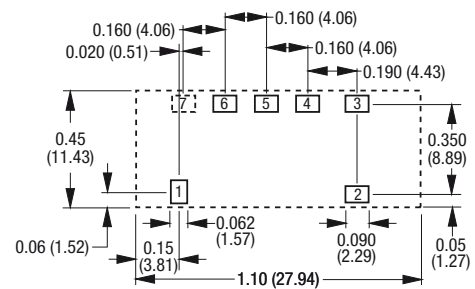
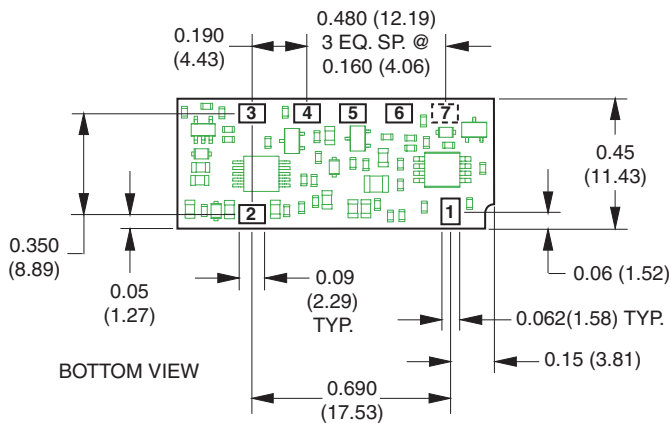
6 Amp Models

Case C63



I/O CONNECTIONS	
Pin	Function P67
1	On/Off Control
2	+Input
3	Seq./Track
4	Common
5	Trim
6	+Output
7	Power Good*

* Power Good is only included for 6 Amp "G" models. Otherwise pad 7 is not installed.



Recommended Pad Size: 0.15 x 0.10 (3.81 x 2.54)

Drawing not to scale

DIMENSIONS ARE IN INCHES (MM)

Drawing not to scale



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