National Semiconductor

October 24, 2008

LMV1089 Dual Input, Clarisound™ Far Field Noise Suppression Microphone Amplifier with Automatic Calibration Capability

General Description

The LMV1089 is a fully analog dual differential input, differential output, microphone array amplifier designed to reduce background acoustic noise, while delivering superb speech clarity in voice communication applications.

The LMV1089 preserves near-field voice signals within 4cm of the microphones while rejecting far-field acoustic noise greater than 50cm from the microphones. Up to 20dB of far-field rejection is possible in a properly configured and calibrated system.

Part of the Powerwise™ family of energy efficient solutions, the LMV1089 consumes only 1.1mA of supply current providing superior performance over DSP solutions consuming greater than ten times the power.

A quick calibration during the manufacturing test process of a product containing the LMV1089 compensates the entire microphone system. This calibration compensates for mismatch in microphone gain and frequency response, as well as acoustical path variances. The LMV1089 stores the calibration coefficients in the on-chip EEPROM. The calibration is initiated by an I²C command or by a logic pin control.

The dual microphone inputs and the processed signal output are differential to provide excellent noise immunity. The microphones are biased with an internal low-noise bias supply.

Key Specifications

■ Far Field Noise Suppression Electrical	33dB
■ Supply voltage	2.7V to 5.5V
■ Supply current	1.1mA (typ)
■ Standby current	0.7μA (typ)
■ Signal-to-Noise Ratio (A-weighted)	65dB (typ)
■ Total Harmonic Distortion + Noise	0.1% (typ)
■ PSRR (217Hz)	96dB (typ)

Features

- Low power consumption
- Shutdown function
- No added processing delay
- Differential outputs
- Automatic calibration
- Adjustable 6 - 48dB gain
- Excellent RF immunity
- Space-saving 36–bump micro SMD package

Applications

- Headset and Boom microphones
- Mobile and handheld two-way radios
- Bluetooth and other powered headsets
- Hand-held voice microphones
- Equalized stereo microphone preamplifier

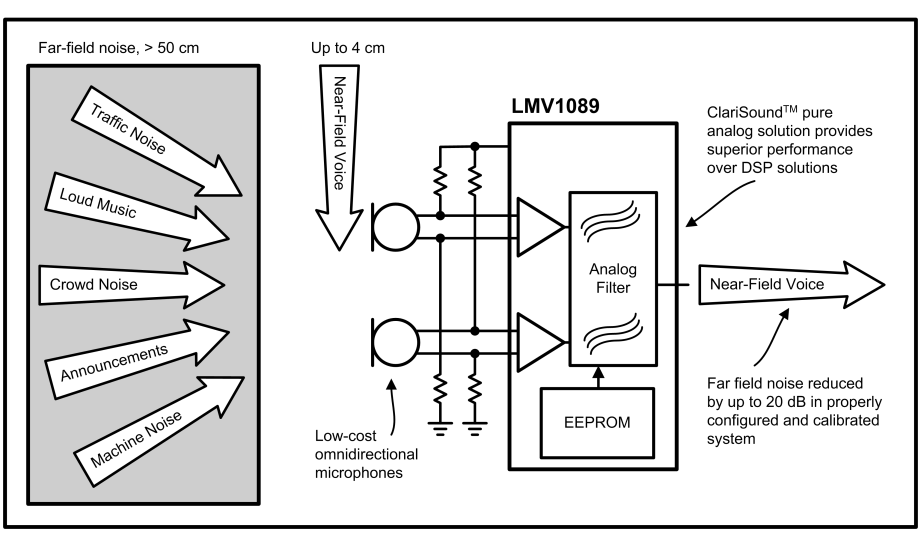
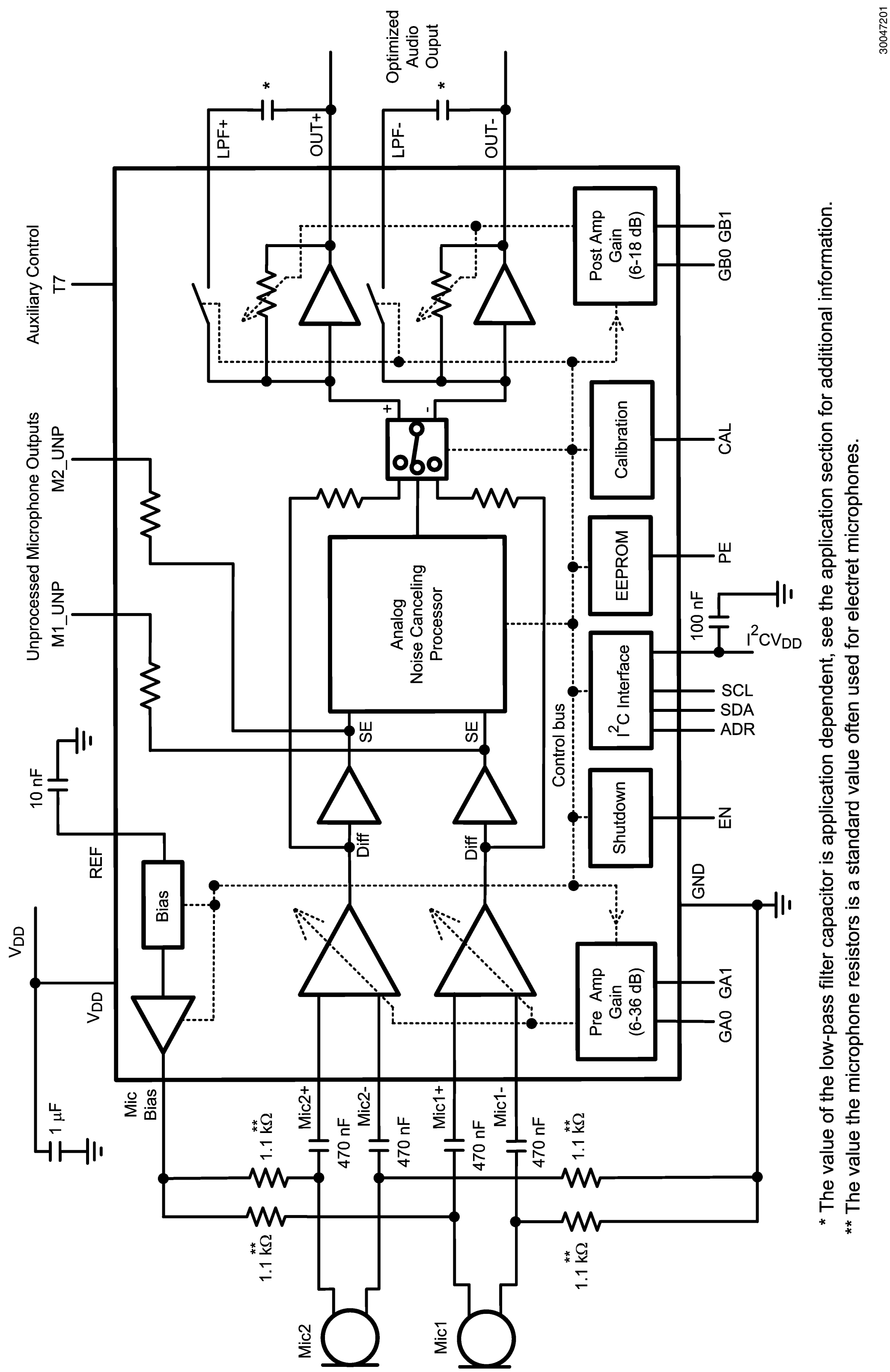


FIGURE 1.

LMV1089 Dual Input, Clarisound™ Far Field Noise Suppression Microphone Amplifier with Automatic Calibration Capability

Typical Application



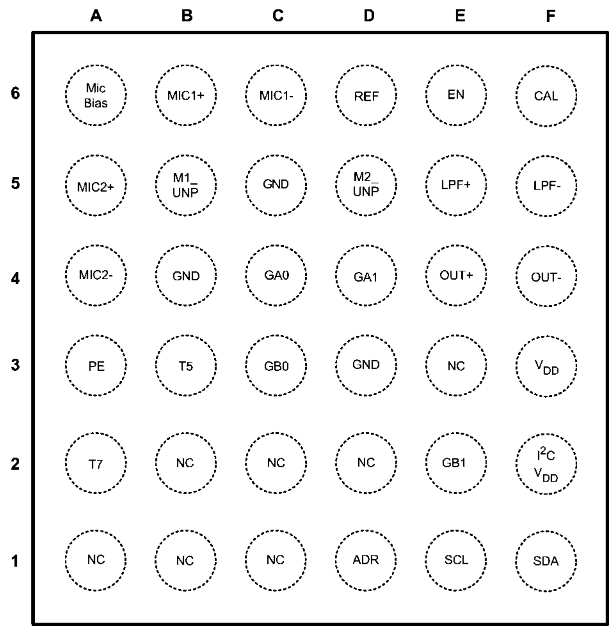
* The value of the low-pass filter capacitor is application dependent, see the application section for additional information.

** The value the microphone resistors is a standard value often used for electret microphones.

FIGURE 2. Typical Dual Microphone Far Field noise Cancelling Application

Connection Diagrams

36–Bump micro SMD package



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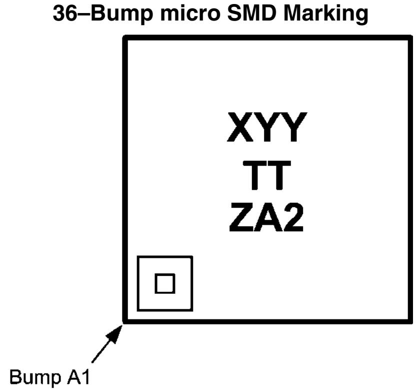
Top View
Order Number LMV1089RL
See NS Package Number RLA36TTA

36–Bump micro SMD Marking



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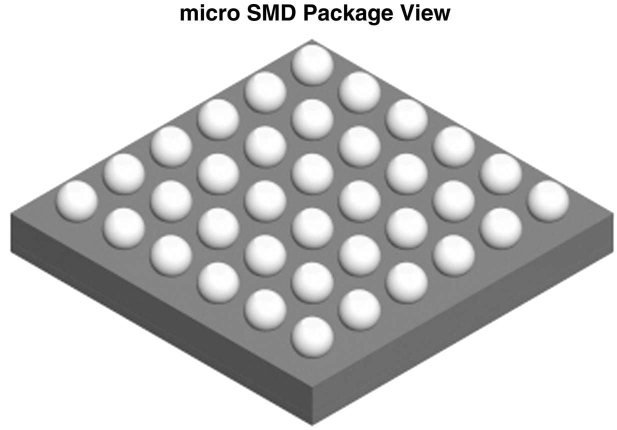
Top View
X = Plant Code
YY = Date Code
TT = Die Tracability
ZA2 = LMV1089RL

micro SMD Package View



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Bottom View

Ordering Information

Order Number	Package	Package Drawing Number	Device Marking	Transport Media
LMV1089RL	36 Bump μSMD	RLA36TTA	XYYTTZA2	250 units on tape and reel
LMV1089RLX	36 Bump μSMD	RLA36TTA	XYYTTZA2	1000 units on tape and reel

TABLE 1. Pin Name and Function

Bump Number	Pin Name	Pin Function	Pin Type
A1	NC	No connect	No Connect
A2	T7	Auxiliary Control Manual Calibration = GND Auto Calibration = V_{DD}	Digital Input
A3	PE	Program Enable EEPROM	Digital Input
A4	MIC2–	microphone 2 negative input	Analog Input
A5	MIC2+	microphone 2 positive input	Analog Input
A6	Mic Bias	Microphone Bias	Analog Output
B1	NC	No Connect	No Connect
B2	NC	No Connect	No Connect
B3	T5	Float (do not connect to GND)	Production Test
B4	GND	amplifier ground	Ground
B5	M1_UNP	microphone 1 unprocessed output	Analog Output
B6	MIC1+	microphone 1 positive input	Analog Input
C1	NC	No Connect	No Connect
C2	NC	No Connect	No Connect
C3	GB0	default Post Amp Gain 0	Digital Input
C4	GA0	default Pre Amp Gain 0	Digital Input
C5	GND	amplifier ground	Ground
C6	MIC1–	amplifier ground	Analog Input
D1	ADR	I^2C Address select	Digital Input
D2	NC	No Connect	No Connect
D3	GND	amplifier ground	Ground
D4	GA1	default Pre Amp Gain 1	Digital Input
D5	M2_UNP	microphone 2 unprocessed output	Analog Output
D6	REF	reference voltage de-coupling	Analog Reference
E1	SCL	I^2C clock	Digital Input
E2	GB1	default Post Amp Gain 1	Digital Input
E3	NC	No Connect	No Connect
E4	OUT+	positive optimized audio output	Analog Output
E5	LPF+	Low Pass Filter for positive output	Analog Input
E6	EN	chip enable	Digital Input
F1	SDA	I^2C data	Digital Input/Output
F2	I^2CV_{DD}	I^2C power supply	Supply
F3	V_{DD}	power supply	Supply
F4	OUT-	negative optimized audio output	Analog Output
F5	LPF-	Low Pass Filter for negative output	Analog Input
F6	CAL	calibration enable	Digital Input

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-85°C to +150°C
Power Dissipation (Note 3)	Internally Limited
ESD Rating (Note 4)	2000V
ESD Rating (Note 5)	200V
Junction Temperature (T_{JMAX})	150°C
Mounting Temperature Infrared or Convection (20 sec.)	235°C

Thermal Resistance

θ_{JA} (microSMD)	70°C/W

Soldering Information See AN-112 "microSMD Wafers Level Chip Scale Package."

Operating Ratings (Note 2)

Supply Voltage	$2.7V \leq V_{DD} \leq 5.5V$
I^2CV_{DD} Supply Voltage (Note 8)	$1.7V \leq I^2CV_{DD} \leq 5.5V$
Temperature Range	−40°C to 85°C
$T_{MIN} \leq T_A \leq T_{MAX}$	$-40°C \leq T_A \leq +85°C$

Electrical Characteristics 3.3V (Note 1)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V_{DD} = 3.3V$, $V_{IN} = 18mV_{P-P}$, f = 1kHz, EN = V_{DD}, pass through mode (Note 8), Pre Amp gain = 20dB, Post Amp gain = 6dB, $R_L = 100k\Omega$, and $C_L = 4.7pF$, $C_{REF} = 10nF$

Symbol	Parameter	Conditions	LMV1089 Typical (Note 6)	LMV1089 Limits (Note 7)	Units (Limits)
SNR	Signal-to-Noise Ratio	f = 1kHz, V_{IN} = 18mV_{P-P}	63		dB
		f = 1kHz, V_{IN} = 18mV_{P-P}, A-Weighted voice band (300 – 3400Hz)	65		dB
e_N	Input Referred Noise level	A-weighted	5		μV_{RMS}
V_{IN}	Maximum Input Signal	THD+N < 1%, Pre Amp Gain = 6dB	910	870	mV_{P-P} (min)
V_{OUT}	Maximum AC Output Voltage	f = 1kHz, Differential Out+, Out- THD+N < 1%	1.2	1.1	V_{RMS} (min)
	DC Level at Outputs	Out+, Out-	800		mV
THD+N	Total Harmonic Distortion + Noise	Differential Out+ and Out-	0.1	0.2	% (max)
Z_{IN}	Input Impedance		155	120 190	kΩ (min) kΩ (max)
Z_{OUT}	Output Impedance		300		Ω
Z_{LOAD}	Load Impedance (Out+, Out-)	R_{LOAD} C_{LOAD}		10 100	kΩ (min) pF (max)
A_M	Microphone Preamplifier Gain Range		6 – 36		dB
A_{MR}	Microphone Preamplifier Gain Adjustment Resolution	f = 1kHz	2	1.75 2.25	dB (min) dB (max)
A_P	Post Amplifier Gain Range	Pass Through Mode and Summing Mode	6 – 18		dB
A_{PR}	Post Amplifier Gain Resolution		3	2.6 3.4	dB (min) dB (max)
A_{CR}	Gain Compensation Range		±3		dB
A_{MD}	Maximum Gain Matching Difference After Calibration	f = 300Hz f = 1kHz f = 3kHz	0.5 0.25 0.5		dB dB dB
X_{Talk}	Crosstalk Attenuation between Mic1 and Mic2	Measured at M1_UNP and M2_UNP	52	41	dB (min)
T_{CAL}	Calibration Duration			790	ms (max)
$FFNS_E$	Far Field Noise Suppression Electrical	f = 1kHz (See Test Method) f = 300Hz (See Test Method)	27 33		dBV dBV
$SNRI_E$	Signal-to-Noise Ratio Improvement Electrical	f = 1kHz (See Test Method) f = 300Hz (See Test Method)	24 28		dBV dBV
PSRR	Power Supply Rejection Ratio	Input Referred, Input AC grounded			
		f_{RIPPLE} = 217Hz (V_{RIPPLE} = 100mV_{P-P})	96	85	dB (min)
		f_{RIPPLE} = 1kHz (V_{RIPPLE} = 100mV_{P-P})	91	80	dB (min)
CMRR	Common Mode Rejection Ratio	f = 1kHz	60		dB

V_{BM}	Microphone Bias Supply Voltage	I_{BIAS} = 1mA	2.0	1.85 2.15	V (min) V (max)
e_{VBM}	10nF capacitor on V_{REF} pin	A-Weighted, 10nF cap at V_{REF} pin	10		μV_{RMS}
I_{BM}	Total available Microphone Bias Current			1.2	mA (min)
I_{DDQ}	Supply Quiescent Current	V_{IN} = 0V	1.1	1.5	mA (max)
I_{DD}	Supply Current	$V_{IN} = 25mV_{P-P}$ both inputs, Noise cancelling mode	1.1		mA
I_{SD}	Shut Down Current	EN pin = GND	0.7	1	μA (max)
I_{DDCP}	Supply Current during Calibration and Programming	Calibrating or Programming EEPROM	30	40	mA (max)
$I_{DD}I^2C$	I^2C supply current	I^2C Idle Mode	25	100	nA (max)
T_{ON}	Turn On Time			40	ms (max)
T_{OFF}	Turn Off Time			60	ms (max)

Electrical Characteristics 5.0V (Note 1)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V_{DD} = 5V$, $V_{IN} = 18mV_{P-P}$, EN = V_{DD}, pass through mode (Note 8), Pre Amp gain = 20dB, Post Amp gain = 6dB, $R_L = 100k\Omega$, and $C_L = 4.7pF$.

Symbol	Parameter	Conditions	LMV1089 Typical (Note 6)	LMV1089 Limit (Note 7)	Units (Limits)
SNR	Signal-to-Noise Ratio	f = 1kHz, V_{IN} = 18mV_{P-P}	63		dB
		f = 1kHz, V_{IN} = 18mV_{P-P}, A-Weighted voice band (300 – 3400Hz)	65		dB
e_N	Input Referred Noise level	A-weighted	5		µV_{RMS}
V_{IN}	Maximum Input Signal	f = 1kHz, THD+N < 1%	918	870	mV_{P-P} (min)
V_{OUT}	Maximum AC Output Voltage	f = 1kHz, THD+N < 1% between differential output	1.2	1.1	V_{RMS} (min)
	DC Output Voltage		800		mV
THD+N	Total Harmonic Distortion + Noise	f = 1kHz V_{IN} = 18mV_{P-P}	0.1	0.2	% (max)
Z_{IN}	Input Impedance		155	120 190	kΩ (min) kΩ (max)
Z_{OUT}	Output Impedance		300		Ω
A_M	Microphone Preamplifier Gain Range	f = 1kHz	6 – 36		dB
A_{MR}	Microphone Preamplifier Gain Adjustment Resolution	f = 1kHz	2	1.75 2.25	dB (min) dB (max)
A_P	Post Amplifier Gain Range	f = 1kHz Pass Through Mode and Summing Mode	6 – 18		dB
A_{PR}	Post Amplifier Gain Adjustment Resolution	f = 1kHz	3	2.6 3.4	dB (min) dB (max)
A_{CR}	Gain Compensation Range	f = 1kHz	±3		dB
A_{MD}	Maximum Gain Matching Difference After Calibration	f = 300Hz f = 2kHz f = 3kHz	0.5 0.25 0.5		dB dB dB
T_{CAL}	Calibration Duration			790	ms (max)
$FFNS_E$	Far Field Noise Suppression Electrical	f = 1kHz (See Test Method) f = 300Hz (See Test Method)	27 33		dBV dBV
$SNRI_E$	Signal-to-Noise Ratio Improvement Electrical	f = 1kHz (See Test Method) f = 300Hz (See Test Method)	24 27		dBV dBV
PSRR	Power Supply Rejection Ratio	Input Referred, Input AC grounded			
		f_{RIPPLE} = 217Hz (V_{RIPPLE} = 100mV_{P-P})	96	85	dB (min)
		f_{RIPPLE} = 1kHz (V_{RIPPLE} = 100mV_{P-P})	91	80	dB (min)
CMRR	Common Mode Rejection Ratio	f = 1kHz	62		dB
V_{BM}	Microphone Bias Supply Voltage	I_{BIAS} = 1mA	2.0		V
e_{VBM}	10nF capacitor on V_{REF} pin	A-Weighted	10		µV_{RMS}
I_{BM}	Total Available Microphone Bias Current			1.2	mA (min)
I_{DDQ}	Supply Quiescent Current	V_{IN} = 0V	1.1	1.5	mA (max)
I_{DDCP}	Supply Current during Calibration and Programming	Calibrating or Programming EEPROM	30	40	mA (max)
I_{DD}	Supply Current	V_{IN} = 25mV_{P-P} both inputs, Noise cancelling mode	1.1		mA (max)
I_{SD}	Shut Down Current	EN pin = GND	1.6		µA
T_{ON}	Turn On Time			40	ms (max)
T_{OFF}	Turn Off Time			60	ms (max)

Digital Interface Characteristics (Notes 1, 8)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, I^2CV_{DD} within the Operating Rating (Note 8)

Symbol	Parameter	Conditions	LMV1089 Typical (Note 6)	LMV1089 Limit (Note 7)	Units (Limits)
V_{IH}	Logic High Input Level	EN, TM, SCL, SDA, ADR, CAL, PE		$0.75xI^2CV_{DD}$	V (min)
		GA0, GA1, GB0, GB1		$0.6xV_{DD}$	
V_{IL}	Logic Low Input Level	EN, TM, SCL, SDA, ADR, CAL, PE		$0.25xI^2CV_{DD}$	V (max)
		GA0, GA1, GB0		$0.4xV_{DD}$	
ts_{CAL}	CAL Setup Time		2		ms
th_{CAL}	CAL Hold time until calibration is finished			790	ms (min)
ts_{PEC}	PE Setup Time		2		ms
th_{PEC}	PE Hold until calibration is finished			790	ms (min)

Note 1: "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum* Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *The Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JC}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower. For the LMV1089, T_{JMAX} = 150°C and the typical θJA for this microSMD package is 70°C/W and for the LLP package θ_{JA} is 64°C/W Refer to the Thermal Considerations section for more information.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Typical values represent most likely parametric norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 7: Datasheet min/max specification limits are guaranteed by test, or statistical analysis.

Note 8: The voltage at I^2CV_{DD} must not exceed the voltage on V_{DD}.

Test Methods

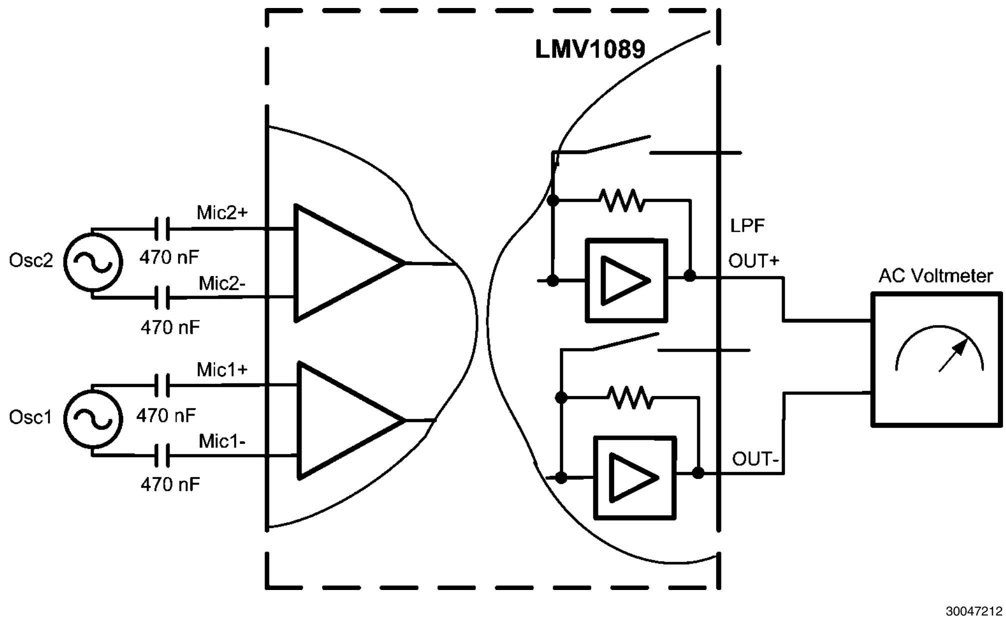


FIGURE 3. $FFNS_E$, $NFSL_E$, $SNRI_E$ Test Circuit

FAR FIELD NOISE SUPPRESSION ($FFNS_E$)

For optimum noise suppression the far field noise should be in a broadside array configuration from the two microphones (see Figure 15). Which means the far field sound source is equidistance from the two microphones. This configuration allows the amplitude of the far field signal to be equal at the two microphone inputs, however a slight phase difference may still exist. To simulate a real world application a slight phase delay was added to the $FFNS_E$ test. The block diagram from Figure 3 is used with the following procedure to measure the $FFNS_E$.

1. A sine wave with equal frequency and amplitude ($25mV_{P-P}$) is applied to Mic1 and Mic2. Using a signal generator, the phase of Mic 2 is delayed by 1.1° when compared with Mic1.
2. Measure the output level in dBV (X)
3. Mute the signal from Mic2
4. Measure the output level in dBV (Y)
5. $FFNS_E$ = Y - X dB

NEAR FIELD SPEECH LOSS ($NFSL_E$)

For optimum near field speech preservation, the sound source should be in an endfire array configuration from the two microphones (see Figure 16). In this configuration the speech signal at the microphone closest to the sound source will have greater amplitude than the microphone further away. Additionally the signal at microphone further away will experience a phase lag when compared with the closer microphone. To simulate this, phase delay as well as amplitude shift was added to the $NFSL_E$ test. The schematic from Figure 3 is used with the following procedure to measure the $NFSL_E$.

1. A $25mV_{P-P}$ and $17.25mV_{P-P}$ ($0.69*25mV_{P-P}$) sine wave is applied to Mic1 and Mic2 respectively. Once again, a signal generator is used to delay the phase of Mic2 by 15.9° when compared with Mic1.
2. Measure the output level in dBV (X)
3. Mute the signal from Mic2
4. Measure the output level in dBV (Y)
5. $NFSL_E$ = Y - X dB

SINGLE TO NOISE RATIO IMPROVEMENT ELECTRICAL ($SNRI_E$)

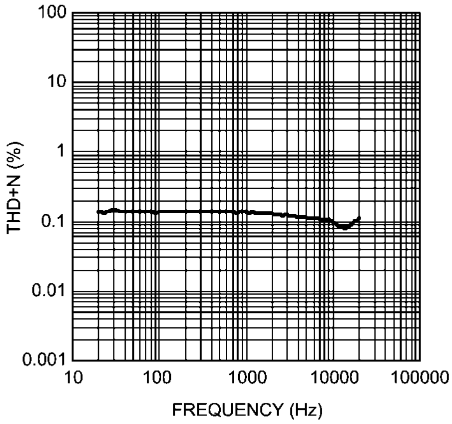
The $SNRI_E$ is the ratio of $FFNS_E$ to $NFSL_E$ and is defined as:

$$SNRI_E = FFNS_E - NFSL_E$$

Typical Performance Characteristics

Unless otherwise specified, T_J = 25°C, V_{DD} = 3.3V, Input Voltage = 18mV$_{P-P}$, f =1 kHz, pass through mode (Note 8), Pre Amp gain = 20dB, Post Amp gain = 6dB, R_L = 100kΩ, and C_L = 4.7pF.

THD+N vs Frequency
Mic1 = AC GND, Mic2 = 36mV$_{P-P}$
Noise Canceling Mode



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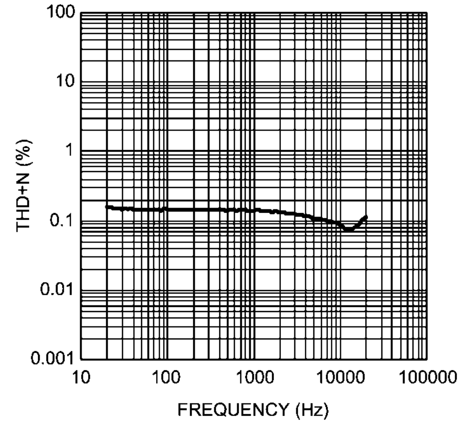
THD+N vs Frequency
Mic2 = AC GND, Mic1 = 36mV$_{P-P}$
Noise Canceling Mode



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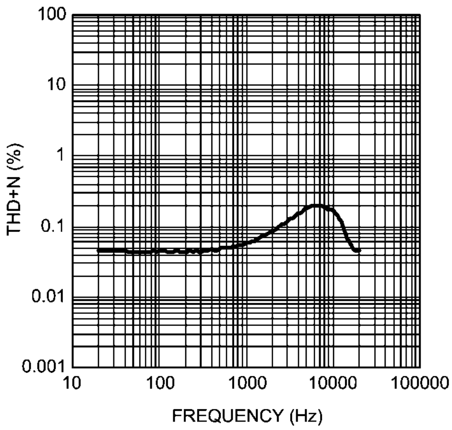
THD+N vs Frequency
Mic1 = 36mV$_{P-P}$
Mic1 Pass Through Mode



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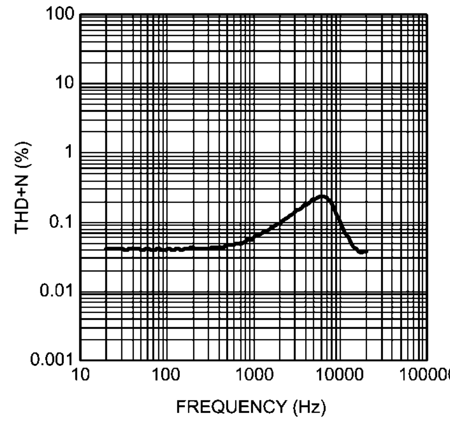
THD+N vs Frequency
Mic2 = 36mV$_{P-P}$
Mic2 Pass Through Mode



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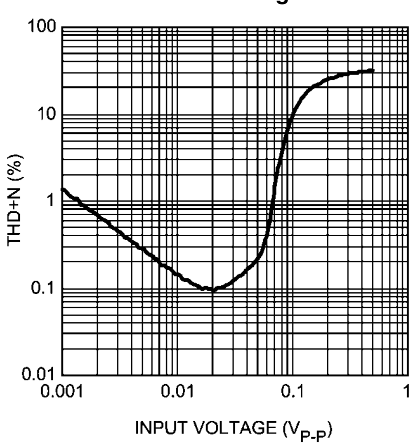
THD+N vs Input Voltage
Mic1 = AC GND, f = 1kHz
Mic2 Noise Canceling Mode



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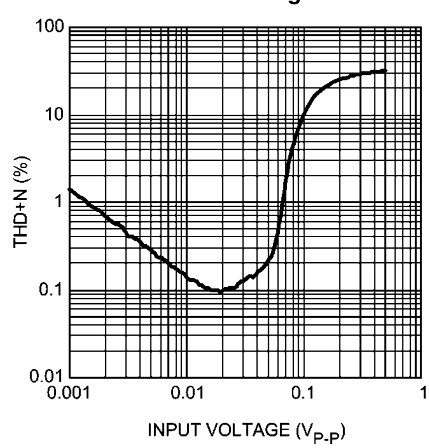
THD+N vs Input Voltage
Mic2 = AC GND, f = 1kHz
Mic1 Noise Canceling Mode



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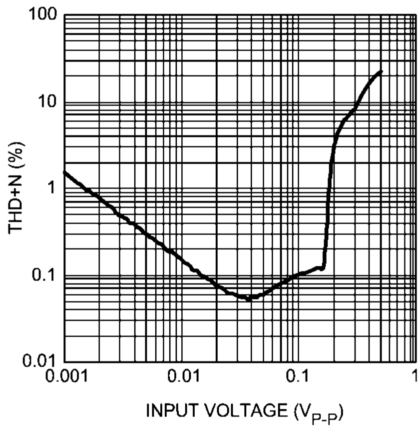
THD+N vs Input Voltage
f = 1kHz
Mic1 Pass Through Mode



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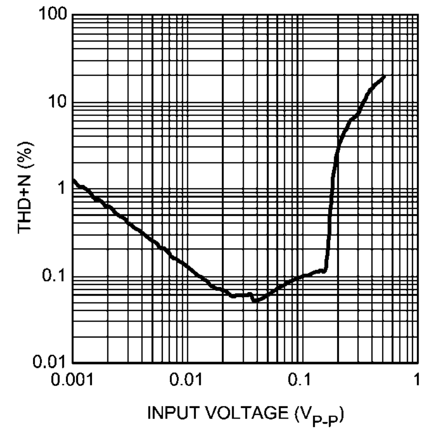
THD+N vs Input Voltage
f = 1kHz
Mic2 Pass Through Mode



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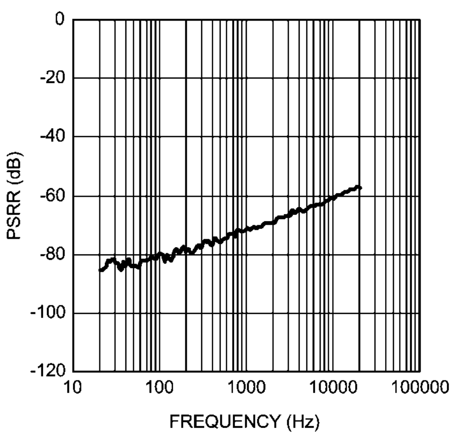
PSRR vs Frequency
Pre Amp Gain = 20dB, Post Amp Gain = 6dB
V_{RIPPLE} = 100mV_{P-P}, Mic1 = Mic2 = AC GND
Mic1 Pass Through Mode



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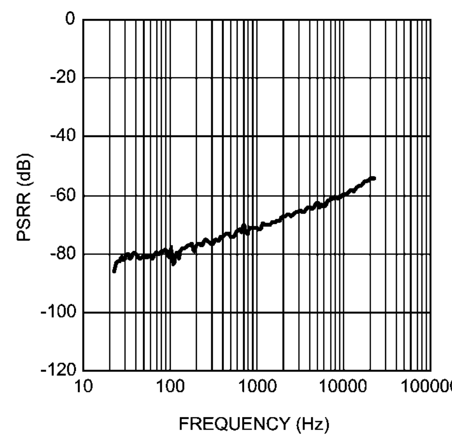
PSRR vs Frequency
Pre Amp Gain = 20dB, Post Amp Gain = 6dB
V_{RIPPLE} = 100mV_{P-P}, Mic1 = Mic2 = AC GND
Mic2 Pass Through Mode



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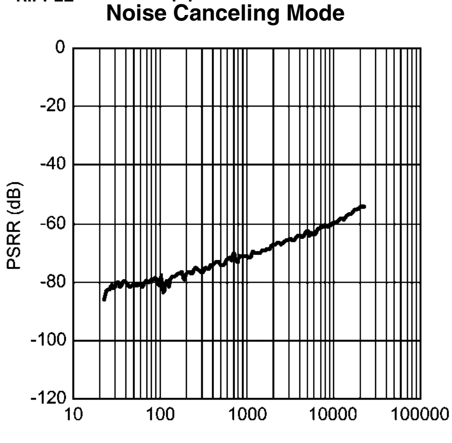
PSRR vs Frequency
Pre Amp Gain = 20dB, Post Amp Gain = 6dB
V_{RIPPLE} = 100mV_{P-P}, Mic1 = Mic2 = AC GND
Noise Canceling Mode



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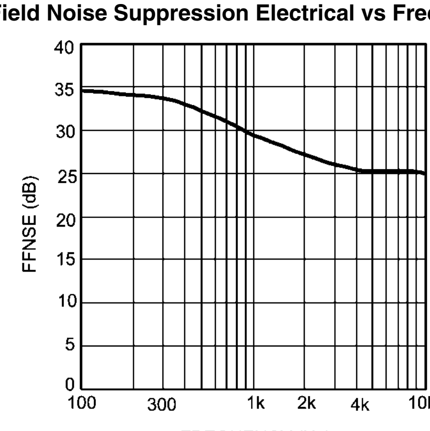
Far Field Noise Suppression Electrical vs Frequency



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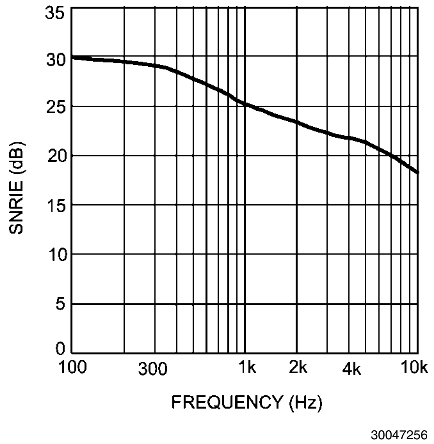
Signal-to-Noise Ratio Electrical vs Frequency



Application Data

INTRODUCTION

The LMV1089 is a fully analog single chip solution to reduce the far field noise picked up by microphones in a communication system. A simplified block diagram is provided in *Figure 4*.

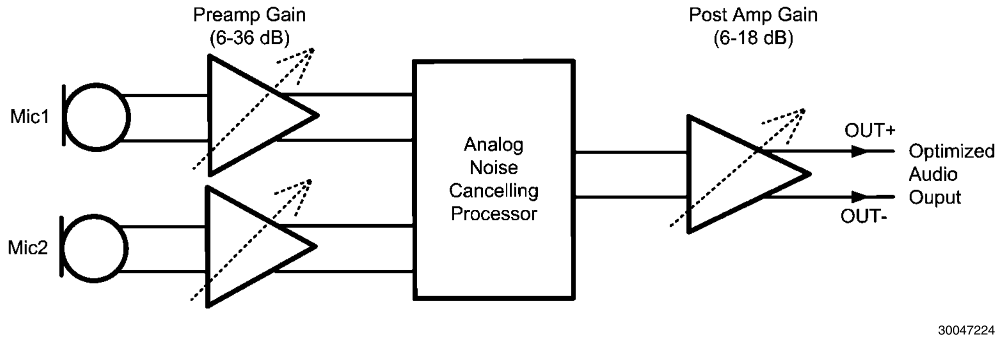


FIGURE 4. Simplified Block Diagram of the LMV1089

The output signal of the microphones is amplified by a preamplifier with adjustable gain between 6dB and 36dB. In the analog noise cancelling processor the gain and frequency response of the microphones and acoustical effects of the enclosure are matched through the auto-calibration function. After the signals are matched the analog noise cancelling suppresses the far field noise signal. The output of the analog noise cancelling processor is amplified in the post amplifier with adjustable gain between 6dB and 18dB. For optimum noise and EMI immunity, the microphones have a differential connection to the LMV1089 and the output of the LMV1089 is also differential. The adjustable gain functions can be controlled via I²C and four control pins. Both methods are described later in the application section.

Power Supply Circuits

A low drop-out (LDO) voltage regulator in the LMV1089 allows the device to be independent of supply voltage variations.

The Power On Reset (POR) circuitry in the LMV1089 requires the supply voltage to rise from 0V to V_{DD} in less than 100ms.

The Mic Bias output is provided as a low noise supply source for the electret microphones. The noise voltage on the Mic Bias microphone supply output pin depends on the noise voltage on the internal the reference node. The de-coupling capacitor on the V_{REF} pin determines the noise voltage on this internal reference. This capacitor should be larger than 1nF; having a larger capacitor value will result in a lower noise voltage on the Mic Bias output.

Most of the logic levels for the digital control interface are relative to I^2CV_{DD} voltage. This eases interfacing to the micro controller of the application containing the LMV1089. The supply voltage on the I^2CV_{DD} pin must never exceed the voltage on the V_{DD} pin.

Only the four pins that determine the default power up gain (as described in *SETTING ADJUSTABLE GAIN*) have logic levels relative to V_{DD}.

Shutdown Function

As part of the Powerwise™ family, the LMV1089 consumes only 1.1mA of current. In many applications the part does not need to be continuously operational. To further reduce the power consumption in the inactive period, the LMV1089 provides two individual microphone power down functions. When either one of the shutdown functions is activated the part will go into shutdown mode consuming only a few µA of supply current.

SHUTDOWN VIA HARDWARE PIN

The hardware shutdown function is operated via the EN pin. In normal operation the EN pin must be at a 'high' level (V_{DD}). Whenever a 'low' level (GND) is applied to the EN pin the part will go into shutdown mode disabling all internal circuits.

SHUTDOWN VIA I²C

The LMV1089 offers an additional shutdown function by reprogramming an I²C register (see *Table 6*). The LMV1089 will only consume power in a mode where it can perform its normal functions. So at least one of the microphone amplifier circuits must be enabled ('1'). Writing '0' to the both bit 4 and bit 5 of the I²C 'A' register (address 0x01h) of the LMV1089 will force the part into shutdown mode, even if the EN pin is 'High', the only part that remains active in this state is the I²C, which consumes neglectible power when compared to the standby current.

Adjustable Gain

The LMV1089 has two gain stages where the gain can be adjusted to meet the requirements for the application. There is a preamplifier and a post amplifier that can be varied independent of each other. In most applications the gain will be set via the I²C interface, see *Table 6*.

SETTING ADJUSTABLE GAIN

The LMV1089 provides four pins to set the default gain settings during power up of the device, which is convenient for applications without a micro controller . The default gain of the preamplifier is controlled by the GA0 and GA1 pins and can be set by wiring those pins to either V_{DD} or GND. In this way, one of the four possible values in the 12dB to 36dB range (see *Table 2*) can be chosen. The default post amplifier gain is set in the same way by connecting the GB0 and GB1 pins to either V_{DD} or GND to select a gain between 6dB and 15dB (see *Table 3*). Setting the gain of the preamplifier and post amplifier via the I²C interface (see *Table 6*) will override this default gain.

The default gain is only set during power up of the device. Toggling the logic level of the enable pin (EN) will not change the current gain setting of the part. Any gain setting done via the I²C interface will remain valid during activation of the function.

TABLE 2. Default preamplifier gain

GA1	GA0	Gain
0	0	12dB
0	1	20dB (Note 9)
1	0	28dB
1	1	36dB

TABLE 3. Default post amplifier gain

GB1	GB0	Gain
0	0	6dB (Note 9)
0	1	9dB
1	0	12dB
1	1	15dB

Note 9: Default value used for performance measurements

Gain Balance and Gain Budget

In systems where input signals have a high dynamic range, critical noise levels or where the dynamic range of the output voltage is also limited, careful gain balancing is essential for the best performance. Too low of a gain setting in the preamplifier can result in higher noise levels while too high of a gain setting in the preamplifier will result in clipping and saturation in the noise cancelling processor and output stages.

The gain ranges and maximum signal levels for the different functional blocks are shown in *Figure 5*. Two examples are given as a guideline on how to select proper gain settings.

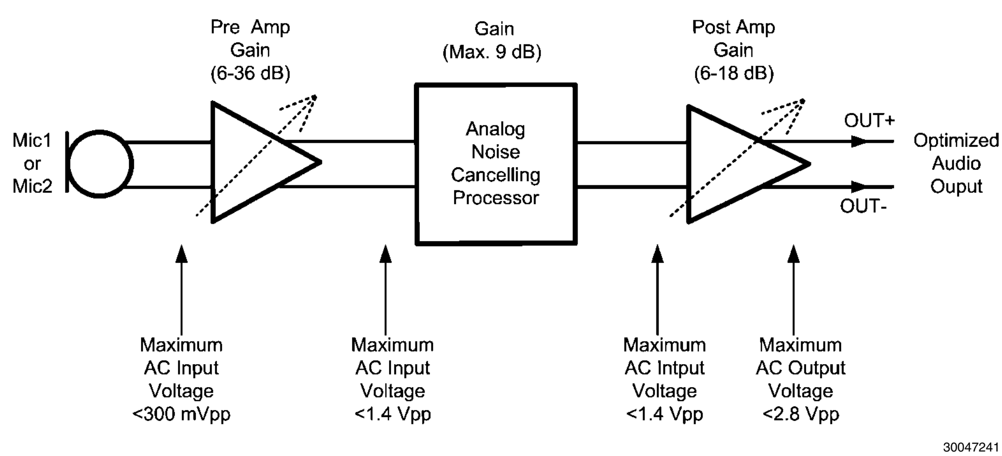


FIGURE 5. Maximum Signal Levels

Example 1

An application using microphones with $50mV_{P-P}$ maximum output voltage, and a baseband chip after the LMV1089 with $1.5V_{P-P}$ maximum input voltage.

For optimum noise performance, the gain of the input stage should be set to the maximum.

1. $50mV_{P-P}$ +36 dB = $3.1V_{P-P}$.
2. $3.1V_{P-P}$ is higher than the maximum $1.4V_{P-P}$ allowed for the Noise Cancelling Processor (NCP). This means a gain lower than 28.9dB should be selected.
3. Select the nearest lower gain from the gain settings shown in Table 2, 28dB is selected. This will prevent the NCP from being overloaded by the microphone. With this setting, the resulting output level of the Pre Amplifier will be $1.26V_{P-P}$.
4. The NCP can have a maximum processing gain of 9dB (depending on the calibration result) which will result in $3.5V_{P-P}$ at the output of the LMV1089. This level is higher then maximum level that is allowed at the input of the post amp of the LMV1089. Therefore the preamp gain has to be reduced, to $1.4V_{P-P}$ minus 9dB = $0.5V_{P-P}$. This limits the preamp gain to a maximum of 20dB.
5. The baseband chip limits the maximum output voltage to $1.5V_{P-P}$ with the minimum of 6dB post amp gain, this results in requiring a lower level at the input of the post amp of $0.75V_{P-P}$. Now calculating this for a maximum NCP gain of 9dB the output of the preamp must be $<266mV_{P-P}$.
6. Calculating the new gain for the preamp will result in <1.4dB gain.
7. The nearest lower gain will be 14dB.

So using preamp gain = 14dB and postamp gain = 6dB is the optimum for this application.

Example 2

An application using microphones with $10mV_{P-P}$ maximum output voltage, and a baseband chip after the LMV1089 with $3.3V_{P-P}$ maximum input voltage.

For optimum noise performance we would like to have the maximum gain at the input stage.

1. $10mV_{P-P}$ + 36dB = $631mV_{P-P}$.
2. This is lower than the maximum $1.4V_{P-P}$ so this is OK.
3. The NCP can have a maximum processing gain of 9dB (depending on the calibration result) which will result in $3.5V_{P-P}$ at the output of the LMV1089. This level is higher then maximum level that is allowed at the input of the Post Amp of the LMV1089. Therefore the Pre Amp gain has to be reduced, to $1.4V_{P-P}$ minus 9dB = $0.5V_{P-P}$. This limits the Pre Amp gain to a maximum of 34dB.
4. With a Post Amp gain setting of 6dB the output of the Post Amp will be $2.8V_{P-P}$ which is OK for the baseband.
5. The nearest lower Post Amp gain will be 6dB.

So using preamp gain = 34dB and postamp gain = 6dB is optimum for this application.

Unprocessed Output Pins

The LMV1089 provides two single ended output pins M1_UNP and M2_UNP. These pins provide the amplified output signal from the two differential microphone input amplifiers Mic1 and Mic2. When the application containing the LMV1089 is in a calibrated state the output level of the two microphone paths are matched. This makes these outputs suitable for stereo applications like video camera webcams and photo cameras. Low cost microphones with wider gain tolerance can be used because gain differences of the microphones will be compensated by the calibration system of the LMV1089. In this situation the default gain of the Pre Amplifiers is set by GA0 and GA1 as described in *Table 2*. This gain can be changed via I²C by writing register A as described in the *I²C Compatible Interface* section.

I²C Compatible Interface

I²C SIGNALS

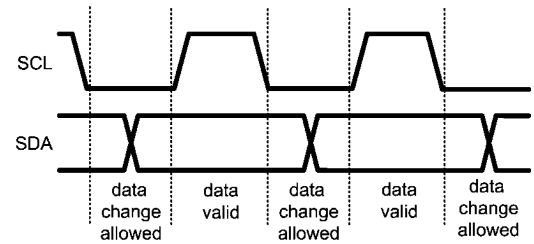
The LMV1089 pin Serial Clock (SCL) pin is used for the I²C clock and the Serial Data (SDA) pin is used for the I²C data. Both these signals need a pull-up resistor according to I²C specification. The LMV1089 can be controlled through two slave addresses. The digital I²C address pin selects the I²C address for LMV1089 as shown in *Table 4* .

TABLE 4. Chip Address

	D7	D6	D5	D4	D3	D2	D1	D0
1st Chip Address I²C Adress='0'	1	1	0	0	1	1	0	$\overline{W}$/R
2nd Chip Address I²C Adress='1'	1	1	0	0	1	1	1	$\overline{W}$/R

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when SCL is LOW.



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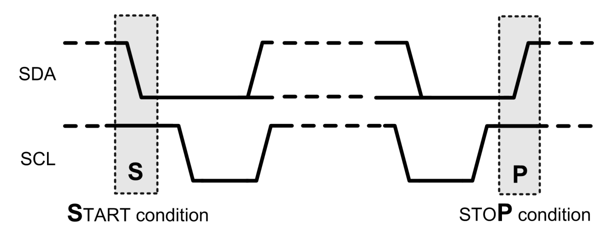
I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C data transmission session. START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.(Note 10)



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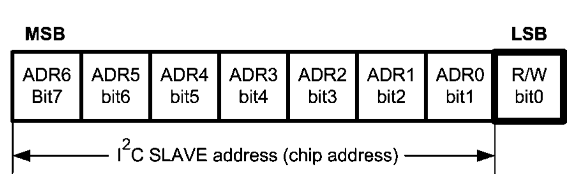
I²C Start Stop Conditions

Note 10: The master should issue STOP after no acknowledgment.

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge (ACK). A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LMV1089 address is **11001100_2** or **11001110_2**. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



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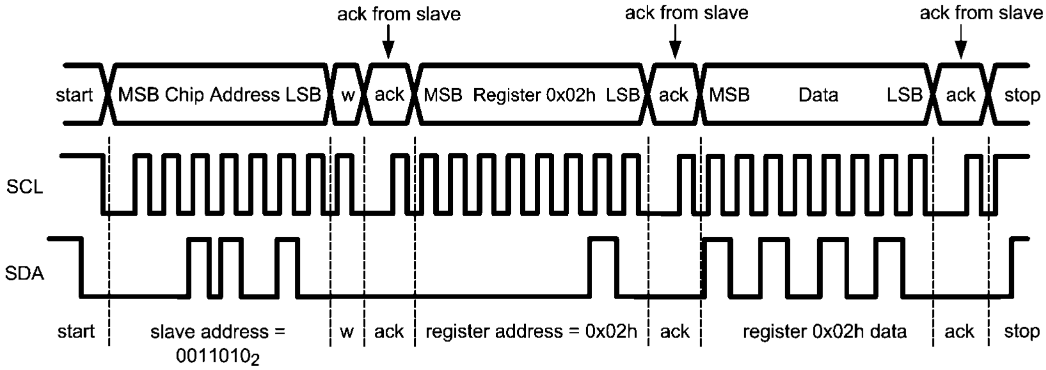
I²C Chip Address

Register changes take effect at the SCL rising edge during the last ACK from slave.

In *Figure 6*, a write example is shown, for a device with a randomly chosen address'**00110100_2**'.



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w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

FIGURE 6. Example I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform. *Figure 7* shows this read example for a randomly chosen address'**00110101_2**.

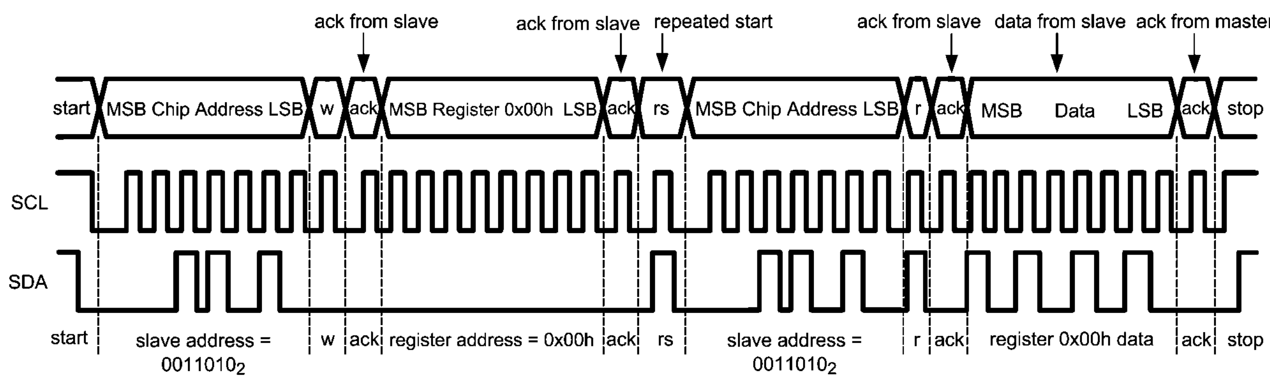

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FIGURE 7. Example I²C Read Cycle

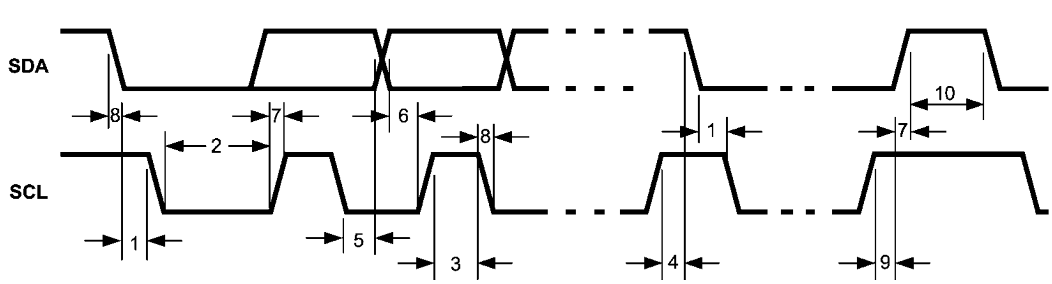

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FIGURE 8. I²C Timing Diagram

TABLE 5. I²C Timing Paramters

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		μs
2	Clock Low Time	1.3		μs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LMV1089)	300	1100	ns
5	Data Hold Time (Input direction, delay generated by the Master)	0	1100	ns
6	Data Setup Time	300		ns
7	Rise Time of SDA and SCL	20	300	ns
8	Fall Time of SDA and SCL	15	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		μs
C_b	Capacitive Load for Each Bus Line	10	200	pF

NOTE: Data guaranteed by design

TABLE 6. I²C Register Description

Address	Reg.	Bits	Description			Default
0x01h	A	[3:0]	Microphone preamplifier gain from 6dB up to 36dB in 2dB steps.			See Table 2
			0000	6dB		
			0001	8dB		
			0010	10dB		
			0011	12dB		
			0100	14dB		
			0101	16dB		
			0110	18dB		
			0111	20dB		
			1000	22dB		
			1001	24dB		
			1010	26dB		
			1011	28dB		
			1100	30dB		
			1101	32dB		
			1110	34dB		
			1111	36dB		
	A	[5:4]	A4 = mute mic1 and A5 = mute mic2. (0 = microphone on)			00(on)
	A	[7:6]	Mic enable bits, A6 = enable Mic1, A7 = enable Mic2 (1 = enable), A6 and A7 both 0 = Shutdown Mode			11(on)

<table>
<tr><th>Address</th><th>Reg.</th><th>Bits</th><th colspan="4">Description</th><th>Default</th></tr>
<tr><td rowspan="15">0x02h</td><td rowspan="9">B</td><td rowspan="9">[2:0]</td><td colspan="4">Gain setting for the post amplifier from (3dB steps)</td><td rowspan="9">See Table 3</td></tr>
<tr><td>000</td><td>6db</td><td></td><td></td></tr>
<tr><td>001</td><td>9dB</td><td></td><td></td></tr>
<tr><td>010</td><td>12dB</td><td></td><td></td></tr>
<tr><td>011</td><td>15dB</td><td></td><td></td></tr>
<tr><td>100</td><td>18dB</td><td></td><td></td></tr>
<tr><td>101</td><td>18dB</td><td></td><td></td></tr>
<tr><td>110</td><td>18dB</td><td></td><td></td></tr>
<tr><td>111</td><td>18dB</td><td></td><td></td></tr>
<tr><td rowspan="5">B</td><td rowspan="5">[4:3]</td><td colspan="4">Mic select bits</td><td rowspan="5">00</td></tr>
<tr><td>0</td><td>0</td><td colspan="2">Noise cancelling mode</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">Only Mic1 enabled</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">Only Mic2 enabled</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Mic1 + Mic2</td></tr>
<tr><td>B</td><td>[7:5]</td><td colspan="4">Not Used</td><td>000</td></tr>
<tr><td>0x0Ch</td><td>L</td><td>[7:0]</td><td colspan="4">reads the output of the EEPROM</td><td>read only</td></tr>
<tr><td>0x0Dh</td><td>M</td><td>[7:0]</td><td colspan="4">reads the output of the EEPROM</td><td>read only</td></tr>
<tr><td rowspan="2">0x0Efh</td><td>N</td><td>[6:0]</td><td colspan="4">reads the output of the EEPROM</td><td>read only</td></tr>
<tr><td>N</td><td>[7]</td><td colspan="4">Reads the “ready” signal. This give the status of the program cycle.
1 = ready ; 0 = program cycle in progress</td><td>read only</td></tr>
</table>

<table>
<tr><th>Address</th><th>Reg.</th><th>Bits</th><th colspan="3">Description</th><th>Default</th></tr>
<tr><td rowspan="34">0x0Fh</td><td rowspan="34">O</td><td rowspan="17">[3:0]</td><td colspan="4">Control the gain compensation between the two mics at 3kHz</td></tr>
<tr><td>0000 (0)</td><td>0.0dB</td><td></td><td rowspan="16">0000</td></tr>
<tr><td>0001 (1)</td><td>0.5dB</td><td></td></tr>
<tr><td>0010 (2)</td><td>1.0dB</td><td></td></tr>
<tr><td>0011 (3)</td><td>1.5dB</td><td></td></tr>
<tr><td>0100 (4)</td><td>2.0dB</td><td></td></tr>
<tr><td>0101 (5)</td><td>2.5dB</td><td></td></tr>
<tr><td>0110 (6)</td><td>3.0dB</td><td></td></tr>
<tr><td>0111 (7)</td><td>3.0dB</td><td></td></tr>
<tr><td>1000 (8)</td><td>0dB</td><td></td></tr>
<tr><td>1001 (9)</td><td>–0.5dB</td><td></td></tr>
<tr><td>1010 (A)</td><td>–1.0dB</td><td></td></tr>
<tr><td>1011 (B)</td><td>–1.5dB</td><td></td></tr>
<tr><td>1100 (C)</td><td>–2.0dB</td><td></td></tr>
<tr><td>1110 (D)</td><td>–2.5dB</td><td></td></tr>
<tr><td>1110 (E)</td><td>–3.0dB</td><td></td></tr>
<tr><td>1111 (F)</td><td>–3.0dB</td><td></td></tr>
<tr><td rowspan="17">[7:4]</td><td colspan="4">Control the gain compensation between the two mics at 300Hz</td></tr>
<tr><td>0000 (0)</td><td>0.0dB</td><td></td><td rowspan="16">0000</td></tr>
<tr><td>0001 (1)</td><td>0.5dB</td><td></td></tr>
<tr><td>0010 (2)</td><td>0.0dB</td><td></td></tr>
<tr><td>0011 (3)</td><td>1.5dB</td><td></td></tr>
<tr><td>0100 (4)</td><td>2.0dB</td><td></td></tr>
<tr><td>0101 (5)</td><td>2.5dB</td><td></td></tr>
<tr><td>0110 (6)</td><td>3.0dB</td><td></td></tr>
<tr><td>0111 (7)</td><td>3.0dB</td><td></td></tr>
<tr><td>1000 (8)</td><td>0dB</td><td></td></tr>
<tr><td>1001 (9)</td><td>–0.5dB</td><td></td></tr>
<tr><td>1010 (A)</td><td>–1.0dB</td><td></td></tr>
<tr><td>1011 (B)</td><td>–1.5dB</td><td></td></tr>
<tr><td>1100 (C)</td><td>–2.0dB</td><td></td></tr>
<tr><td>1101 (D)</td><td>–2.5dB</td><td></td></tr>
<tr><td>1110 (E)</td><td>–3.0dB</td><td></td></tr>
<tr><td>1111 (F)</td><td>–3.0dBd</td><td></td></tr>
</table>

Address	Reg.	Bits	Description			Default
0x10h	P	[3:0]	Control compensation gain for left channel at ALL frequencies			
			0000 (0)	–3.0dB		1111
			0001 (1)	–3.0dB		
			0010 (2)	–2.5dB		
			0011 (3)	–2.0dB		
			0100 (4)	–1.5dB		
			0101 (5)	–1.0dB		
			0110 (6)	–0.5dB		
			0111 (7)	0.0dB		
			1000 (8)	0.0dB		
			1001 (9)	0.5dB		
			1010 (A)	1.0dB		
			1011 (B)	1.5dB		
			1100 (C)	2.0dB		
			1101 (D)	2.5dB		
			1110 (E)	3.0dB		
			1111 (F)	3.0dB		
		[7:4]	Control compensation gain for right channel at ALL frequencies			
			0000 (0)	–3.0dB		1111
			0001 (1)	–3.0dB		
			0010 (2)	–2.5dB		
			0011 (3)	–2.0dB		
			0100 (4)	–1.5dB		
			0101 (5)	–1.0dB		
			0110 (6)	–0.5dB		
			0111 (7)	0.0dB		
			1000 (8)	0.0dB		
			1001 (9)	0.5dB		
			1010 (A)	1.0dB		
			1011 (B)	1.5dB		
			1100 (C)	2.0dB		
			1101 (D)	2.5dB		
			1110 (E)	3.0dB		
			1111 (F)	3.0dB		
0x11h	Q	[6:0]	Values are clocked into EEPROM registers once “newdata” pulse is generated			
		[7]	StoreBar signal StoreBar = 0 enables EEPROM programming StoreBar = 1 data clock into EEPROM registers			1
0x12h	R	[0]	Start Calibration via I2C ‘0’ to ‘1’ = start calibration (keep ‘1’ during calibration)			0
		[7]	Internal test			0000000

Calibration

Automatic calibration should only be required once, when the product containing the LMV1089 has completed manufacture, and prior to application packaging. The product containing the LMV1089 will be calibrated to the microphones, the microphone spacings, and the acoustical properties of the final design.

The compensation or calibration technology is achieved via memory stored coefficients when the FFNS circuitry activates the calibration sequence. The purpose of the calibration sequence is to choose the optimized coefficients for the FFNS circuitry for the given microphones, spacing, and acoustical design of the product containing the LMV1089.

A basic calibration can be performed with a single 1kHz tone, however to take full advantage of this calibration feature a three tone calibration (See *PERFORMING A THREE TONE CALIBRATION*) is preferred .

The automatic calibration process can be initiated from either a digital interface CALIBRATE pin (CAL) or via the I²C interface.

The logic level at the PROGRAM ENABLE (PE) pin determines if the result of the calibration is volatile or permanent. To make the result of the calibration permanent (stored in the EEPROM) the PROGRAM ENABLE (PE) pin must be high during the automatic calibration process.

AUTOMATIC CALIBRATION VIA CAL PIN

To initiate the automatic calibration via the CAL pin, the following procedure is required. See timing diagram Figure 11:

- From the initial condition where both PE and CAL are at 'low' level
- bring PE to a 'high' level (enable EEprom write)
- bring CAL to a 'high' level to start Calibration
- Apply Audio stimulus (single tone 1kHz or three tone sequence as described in *PERFORMING A THREE TONE CALIBRATION*) (see Figure 12).
- Hold CAL 'high' for at least 790ms
- Remove Audio stimulus
- bring CAL to a 'low' level to stop Calibration
- bring PE to a 'low' level (disable EEprom write)

A tone may be applied prior to the rising of CAL and PE. Signals applied to the microphone inputs before rising of CAL and PE are ignored by the calibration system.

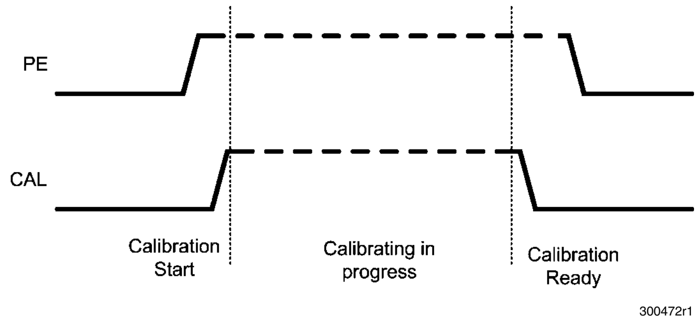


FIGURE 9. Automatic Calibration via CAL pin

Note: When the I²C is operated, make sure that register 'R' (address 0x12) bit 0 is '0' before operating the CAL pin (default value for this bit). When this bit is set '1' the calibration engine of the LMV1089 is started and will remain active with a higher supply current than normal operation. The state of the calibration remains active until this bit is reset, '0". With the bit set the 'low' to' high' transfer of the CAL pin will be ignored.

AUTOMATIC CALIBRATION VIA I2C COMMAND

To initiate the automatic calibration via the I2C interface, the following procedure is required:

- From the initial condition where PE is 'low' level
- Bring PE to a 'high' level (enable EEprom write)
- Write '1' into I2C register 'R' (address 0x12) bit 0 to start calibration
- Apply Audio stimulus (single tone 1kHz or three tone sequence as described in *PERFORMING A THREE TONE CALIBRATION*)
- Wait at least 790ms
- Remove Audio stimulus
- Write '0' into I2C to finish calibration
- Bring PE to a 'low' level (disable EEprom write)

A tone may be applied prior to the rising of PE or setting the I2C calibration bit . Signals applied to the microphone inputs before rising of PE or setting the I2C calibration bit are ignored by the calibration system.

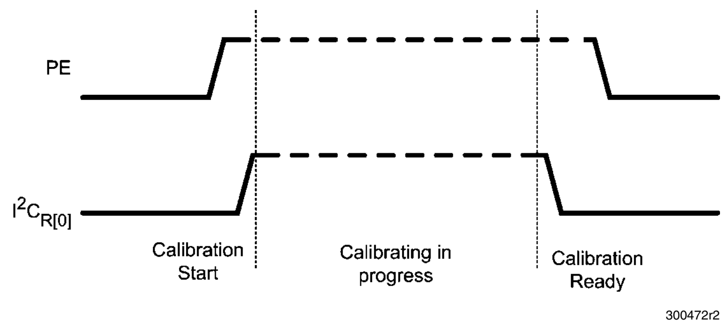


FIGURE 10.

PERFORMING THE AUTOMATIC CALIBRATION

Automatic calibration can be performed as 'one tone' or as 'three tone' calibration. Three tone calibration is preferred because the three tone calibration not only compensates for differences in the gain between the two microphones, but this function also corrects for differences in the frequency response between in the two microphones and compensates for the acoustical effects of the enclosure.

The one tone calibration only compensates for the gain difference between the two microphones at 1kHz and can lead to less far field noise reduction when compared to three tone calibration.

PERFORMING A ONE TONE CALIBRATION

The easiest way to perform an automatic calibration with the LMV1089 uses a 1kHz tone. This tone can be a steady state tone or a 1kHz tone that is switched on and off using the timing from *Figure 11*.

To perform a one tone calibration, a 1kHz test tone is required right after the PE and CAL inputs are brought to a logic high level and that tone should be stable during the time as indicated in *Table 7*. At the end of this sequence the calibration data is automatically stored in the internal EEPROM (see Figure 12).

A tone may be applied prior to the rising of CAL start signal and PE. Signals applied to the microphone outside the limits shown in *Figure 11* and *Table 7* are ignored by the calibration system.

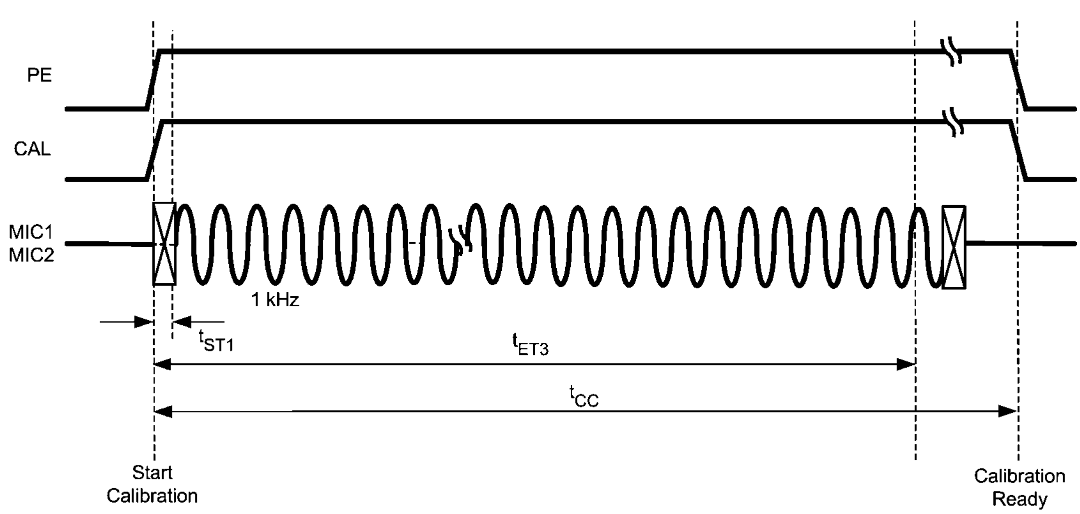


FIGURE 11. One Tone Calibration Timing

PERFORMING A THREE TONE CALIBRATION

In a system with two microphones in an enclosure there will always be a difference in the transfer function in both gain and frequency response between the two channels. The LMV1089 has the capability to perform an automatic calibration function to minimize these differences. To perform this calibration, a test sequence of three tones is required right after the PE and CAL inputs are brought to a logic high level. At the end of this sequence the calibration data is automatically stored in the internal EEPROM.

The three tones have to be applied as follows (see Figure 12):

- A first tone with a frequency of 1kHz
- A second tone with a frequency of 300Hz
- A third tone with a frequency of 3kHz

A tone may be applied prior to the rising of CAL start signal and PE. Signals applied to the microphone outside the limits shown in *Figure 12* and *Table 7* are ignored by the calibration system.

Between each tone pair there is a small time, indicated by a cross, to change the frequency. During that time the input tone is ignored by the calibration system.

The total calibration sequence requires less than 790ms.

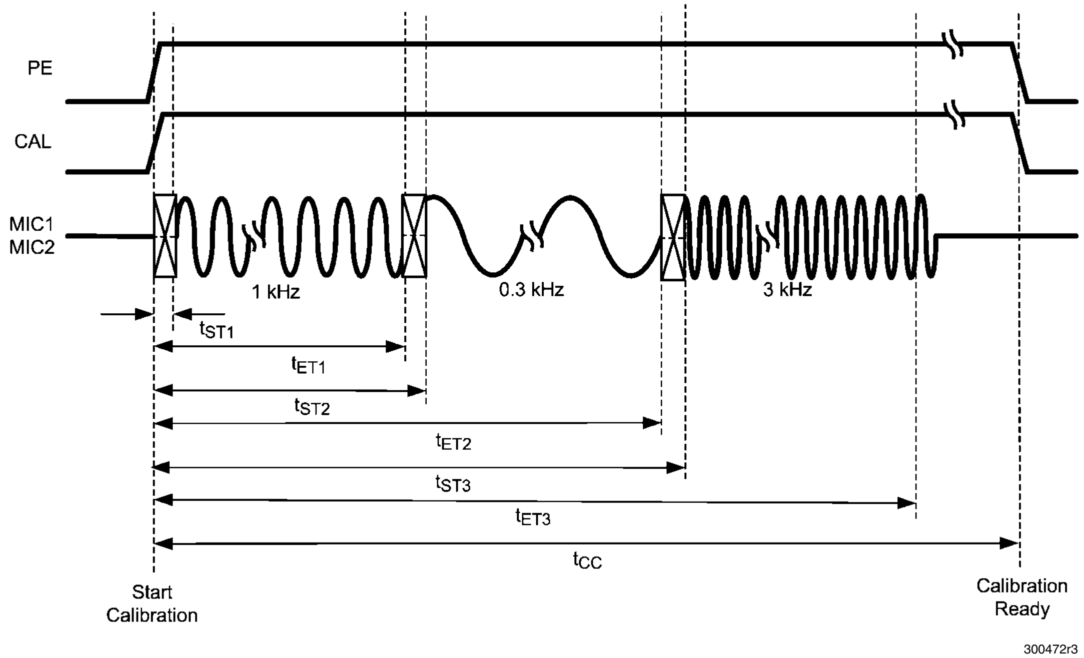


FIGURE 12. Calibration Timing

TABLE 7. Automatic Calibration Timing Parameters

Symbol	Parameter	Limits		Unitis
		Min	Max	
t_{ST1}	Calibration Start Tone 1		10	ms
t_{ET1}	Calibration End Tone 1	200		ms
t_{ST2}	Calibration Start Tone 2		210	ms
t_{ET2}	Calibration End Tone 2	400		ms
t_{ST3}	Calibration Start Tone 3		410	ms
t_{ET3}	Calibration End Tone 3	600		ms
t_{CC}	Calibration Complete	790		ms

NOTE: Data guaranteed by design

AUTOMATIC CALIBRATION SETUP

A calibration test setup consists of a test room (acoustical box) with a loudspeaker (acoustical source) driven with the test tone sequence from *Figure 12*. The test setup is shown in *Figure 13*. The distances between the source and microphone 1 and microphone 2 must be equal and the sound must travel without any obstacle from source to both microphones.

The sound will travel with the limited speed of 300m/s from the loudspeaker source to the microphones. When creating the calibration signals this time should not be ignored, 30cm distance will cause 1ms delay.

For an optimum automatic calibration the output level of the microphones and preamp gain must be set so that the resulting signal at the output of the preamplifier is $100mV_{P-P} \pm 6dB$

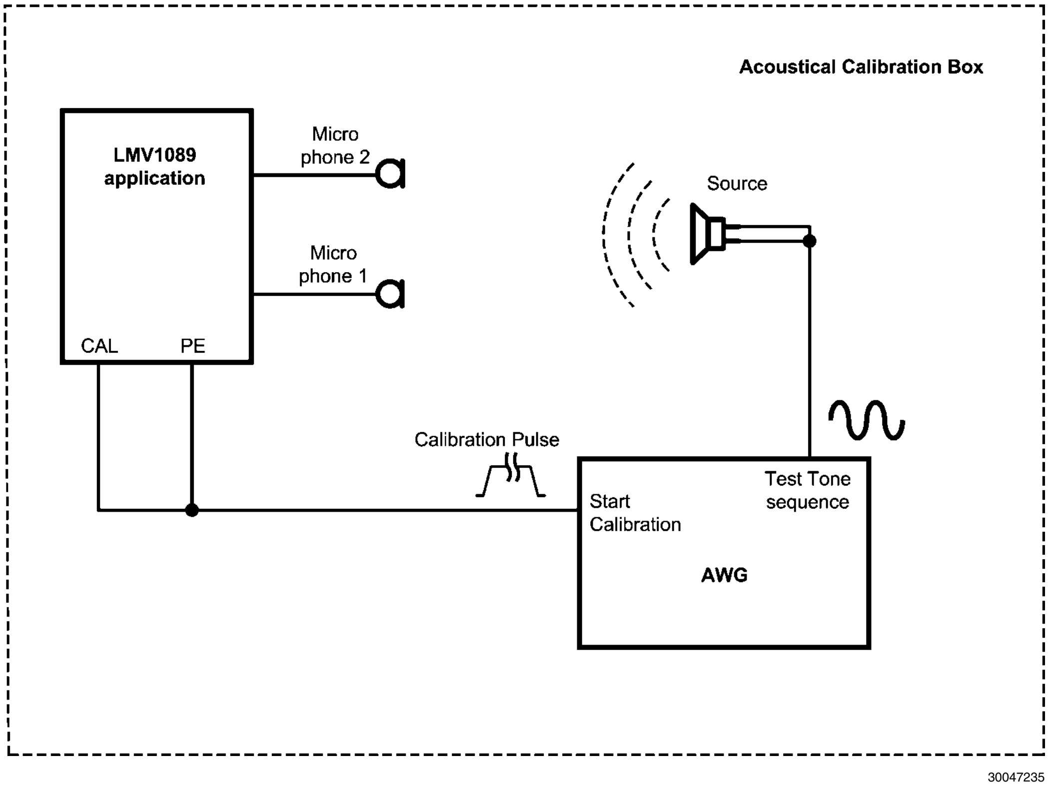


FIGURE 13. Calibration Test setup

MANUAL CALIBRATION

You can manually program the gain compensation of the two mic inputs on the LMV1089 using the I²C interface. *Table 5* shows the control bits for I²C Register O and P with the corresponding gains. This can be easily done by doing the following:

1) READ contents of the I²C register N immediately after powering up.

2) Set PE pin and T7 pin to Vdd.

3) WRITE to I²C register O and P to choose the calibration settings.

Bits O<7:4> control the two mics at 300Hz and bits O<3:0> control the two mics at 3kHz.

Bits P<7:4> control the right channel gain and bits P<3:0> control the left channel gain

4) WRITE a ‘0’ to I²C register Q<7> bit (storeBar) and the bits from I²C register N<6:0> to I²C register Q<6:0>

5) When I²C register N<7> (ready) goes high, then the EEPROM programming is complete. Now PE pin and T7 pin should be set to GND and I²C register Q<7> (storeBar) should be returned to ‘1’.

SUPPLY CURRENT DURING CALIBRATION

The calibration function performs two main tasks in a sequence. First the AC characteristics of the microphones are matched. Then in the second stage, if the PE pin is high, the on-chip EEPROM is programmed.

During the first stage of this sequence the supply current on the LMV1089 will increase to about 2.5mA. During the writing of the EEPROM the supply current will rise for about 215 ms to about 30mA. This increased current is used for the on chip charge pump which generates the high voltages that are required for programming the EEPROM.

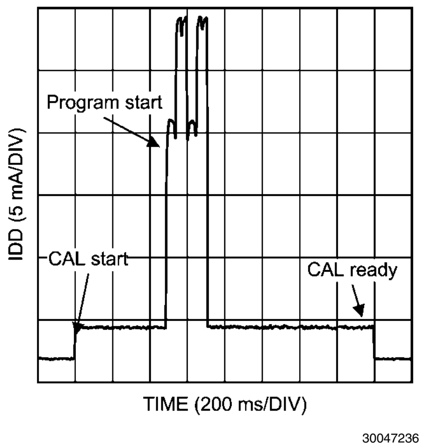


FIGURE 14. Supply current during calibration and programming

Microphone Placement

Because the LMV1089 is a microphone array Far Field Noise Reduction solution, proper microphone placement is critical for optimum performance. Two things need to be considered: The spacing between the two microphones and the position of the two microphones relative to near field source

If the spacing between the two microphones is too small, near field speech will be canceled along with the far field noise. Conversely, if the spacing between the two microphones is large, the far field noise reduction performance will be degraded. The optimum spacing between Mic 1 and Mic 2 is 1.5-2.5cm. This range provides a balance of minimal near field speech loss and maximum far field noise reduction.

If the spacing between the two microphones is too small near field speech will be canceled along with the far field noise. Conversely, if the spacing between the two microphones is large, the far field noise reduction performance will be degraded. The optimum spacing between Mic 1 and Mic 2 is 1.5-2.5cm. This range provides a balance of minimal near field speech loss and maximum far field noise reduction. The microphones should be in line with the desired sound source 'near speech' and configured in an endfire array (see *Figure 16*) orientation from the sound source. If the 'near speech' (desired sound source) is equidistant to the source like a broadside array (see *Figure 15*) the result will be a great deal of near field speech loss.

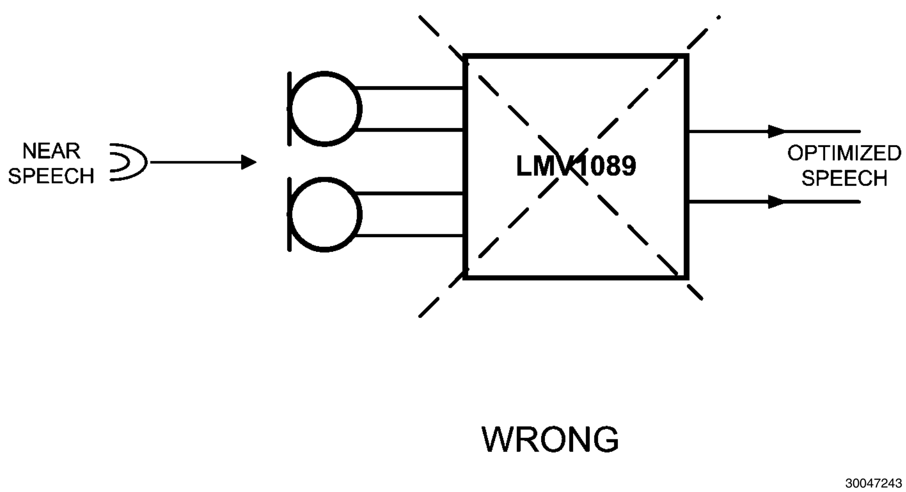


FIGURE 15. Broadside Array (WRONG)

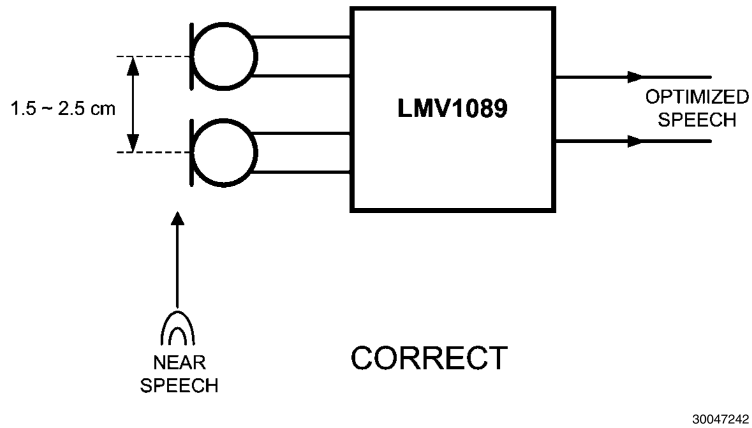


FIGURE 16. Endfire Array (CORRECT)

Low-Pass Filter At The Output

At the output of the LMV1089 there is a provision to create a 1st order low-pass filter (only enabled in 'Noise Cancelling' mode). This low-pass filter can be used to compensate for the change in frequency response that results from the noise cancellation process. The change in frequency response resembles a first-order high-pass filter, and for many of the applications it can be compensated by a first-order low-pass filter with cutoff frequency between 1.5kHz and 2.5kHz.

The transfer function of the low-pass filter is derived as:

$$H(s) = \frac{\text{Post Amplifier gain}}{sR_fC_f+1}$$

This low-pass filter is created by connecting a capacitor between the LPF pin and the OUT pin of the LMV1089. The value of this capacitor also depends on the selected output gain. For different gains the feedback resistance in the low-pass filter network changes as shown in *Table 8*.

TABLE 8. Low-Pass Filter Internal Impedance

Post Amplifier Gain Setting (dB)in Pass Through mode	Feedback Resistance R_f (kΩ)
6	20
9	29
12	40
15	57
18	80

This will result in the following values for a cutoff frequency of 2000 Hz:

TABLE 9. Low-Pass Filter Capacitor For 2kHz

Post Amplifier Gain Setting (dB)	R_f (kΩ)	C_f (nF)
6	20	3.9
9	29	2.7
12	40	2.0
15	57	1.3
18	80	1.0

Measurement Setup

Because of the nature of the calibration system it is not possible to predict the absolute gain in the two microphone channels of the Far Field Noise Cancelling System. This is because, after the calibration function has been operated, the noise cancelling circuit will compensate for the difference in gain between the microphones. In Noise Cancelling mode, this can result in a final gain offset of max 3dB between the gain set in the registers (A[3:0] and B[2:0]) and the actual measured gain between input and output of the LMV1089. After performing a calibration the frequency characteristic of the microphone channels will be matched for the two microphones. As a result of this matching there can be a slight slope in the frequency characteristic in one or both amplifiers.

A-WEIGHTED FILTER

The human ear is sensitive for acoustic signals within a frequency range from about 20Hz to 20kHz. Within this range the sensitivity of the human ear is not equal for each frequency. To approach the hearing response, weighting filters are introduced. One of those filters is the A-weighted filter.

The A-weighted filter is used in signal to noise measurements, where the wanted audio signal is compared to device noise and distortion.

The use of this filter improves the correlation of the measured values to the way these ratios are perceived by the human ear.

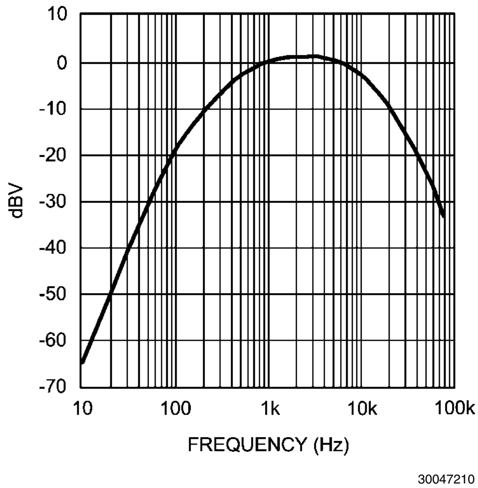


FIGURE 17. A-Weighted Filter

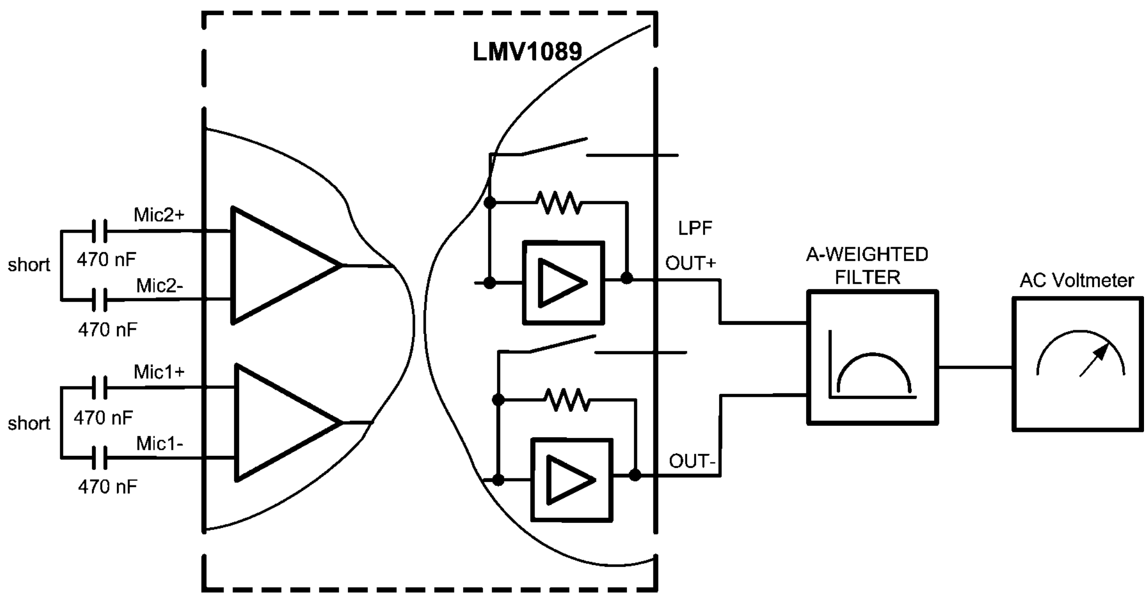


FIGURE 18. Noise Measurement Setup

MEASURING NOISE AND SNR

The overall noise of the LMV1089 is measured within the frequency band from 10Hz to 22kHz using an A-weighted filter. The Mic+ and Mic- inputs of the LMV1089 are AC shorted between the input capacitors, see *Figure 18*.

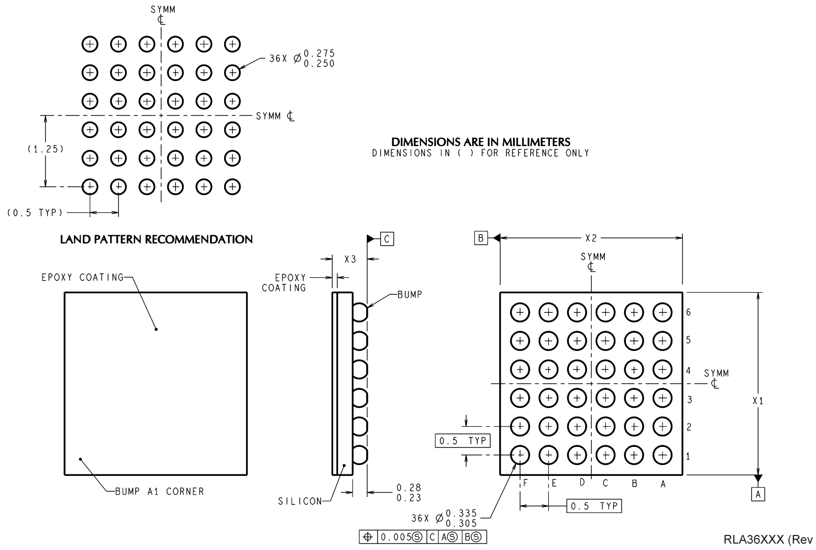
For the signal to noise ratio (SNR) the signal level at the output is measured with a 1kHz input signal of 18mV$_{P-P}$ using an A-weighted filter. This voltage represents the output voltage of a typical electret condenser microphone at a sound pressure level of 94dB SPL, which is the standard level for these measurements. The LMV1089 is programmed for 26dB of total gain (20dB preamplifier and 6dB postamplifier) with only Mic1 or Mic2 used. (See also *I²C Compatible* Interface).

The input signal is applied differentially between the Mic+ and Mic-. Because the part is in Pass Through mode the low-pass filter at the output of the LMV1089 is disabled.

Revision History

Rev	Date	Description
1.0	09/24/08	Initial release.
1.01	09/30/08	Text edits.
1.02	10/14/08	Text edits.
1.03	10/24/08	Text edits.

Physical Dimensions inches (millimeters) unless otherwise noted



36 Bump micro SMD Technology
NS Package Number RLA36TTA
X_1 = 3.459±0.03(mm), X_2 = 3.459(mm)±0.03, X_3 = 0.66±0.075(mm)

Notes

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