

74LCX32

Low Voltage Quad 2-Input OR Gate with 5V Tolerant Inputs

General Description

The LCX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX32 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 2.3V–3.6V V_{CC} specifications provided
- 5.5 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance:
 - Human body model > 2000V
 - Machine model > 150V
- Leadless Pb-Free DQFN package

Ordering Code:

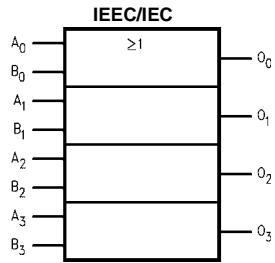
Order Number	Package Number	Package Description
74LCX32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX32MX_NL (Note 2)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX32SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX32BQX (Note 1)	MLP014A	Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74LCX32MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LCX32MTCX_NL (Note 2)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: DQFN package available in Tape and Reel only.

Note 2: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol

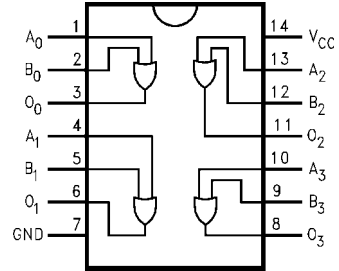


Pin Descriptions

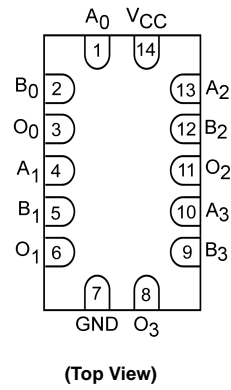
Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Connection Diagrams

Pin Assignments for SOIC, SOP, and TSSOP



Pad Assignment for DQFN



Absolute Maximum Ratings ^(Note 3)						
Symbol	Parameter	Value	Conditions	Units		
V _{CC}	Supply Voltage	-0.5 to +7.0		V		
V _I	DC Input Voltage	-0.5 to +7.0		V		
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	Output in HIGH or LOW State (Note 4)	V		
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA		
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA		
		+50	V _O > V _{CC}			
I _O	DC Output Source/Sink Current	±50		mA		
I _{CC}	DC Supply Current per Supply Pin	±100		mA		
I _{GND}	DC Ground Current per Ground Pin	±100		mA		
T _{STG}	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions ^(Note 5)						
Symbol	Parameter	Min	Max	Units		
V _{CC}	Supply Voltage	Operating	2.0	3.6	V	
		Data Retention	1.5	3.6		
V _I	Input Voltage	0	5.5	V		
V _O	Output Voltage	0	V _{CC}	V		
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V - 3.6V		±24	mA	
		V _{CC} = 2.7V - 3.0V		±12		
		V _{CC} = 2.3V - 2.7V		±8		
T _A	Free-Air Operating Temperature	-40	85	°C		
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V-2.0V, V _{CC} = 3.0V	0	10	ns/V		
<p>Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p>Note 4: I_O Absolute Maximum Rating must be observed.</p> <p>Note 5: Unused inputs must be held HIGH or LOW. They may not float.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V _{IL}	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 - 3.6	V _{CC} - 0.2		V
		I _{OH} = -8 mA	2.3	1.8		
		I _{OH} = -12 mA	2.7	2.2		
		I _{OH} = -18 mA	3.0	2.4		
		I _{OH} = -24 mA	3.0	2.2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 - 3.6		0.2	V
		I _{OL} = 8 mA	2.3		0.6	
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 - 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 - 3.6		10	μA
		3.6V ≤ V _I ≤ 5.5V	2.3 - 3.6		±10	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 - 3.6		500	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to }+85^\circ\text{C}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50\text{ pF}$		$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	5.5	1.5	6.2	1.5	6.6	ns
t_{PLH}		1.5	5.5	1.5	6.2	1.5	6.6	
t_{OSHL}	Output to Output		1.0					ns
t_{OSLH}	Skew (Note 6)		1.0					

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$ $C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	3.3 2.5	0.8 0.6	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$ $C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	3.3 2.5	-0.8 -0.6	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10\text{ MHz}$	25	pF

AC Loading and Waveforms Generic for LCX Family

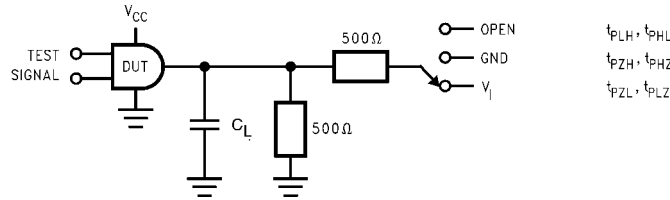


FIGURE 1. AC Test Circuit
(C_L includes probe and jig capacitance)

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND

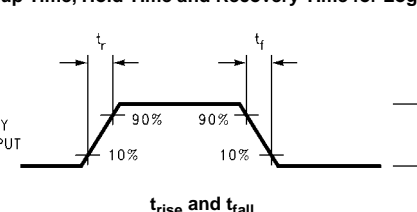
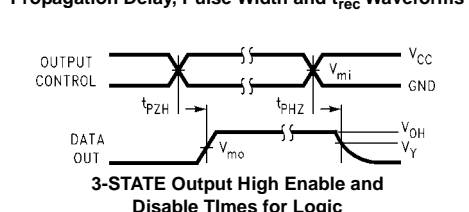
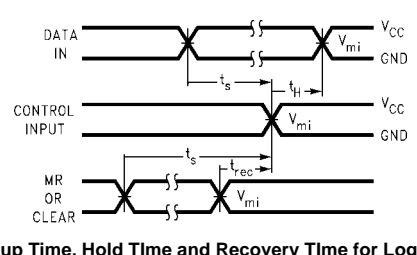
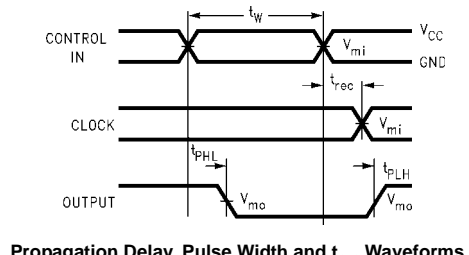
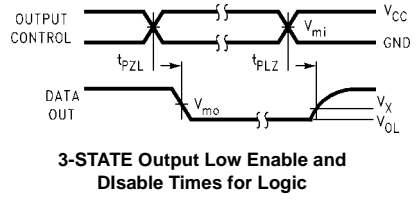
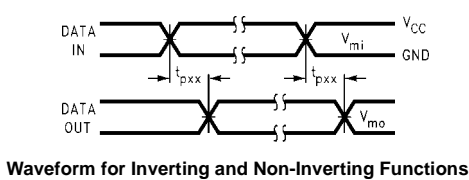


FIGURE 2. Waveforms
(Input Pulse Characteristics; $f = 1MHz, t_r = t_f = 3ns$)

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

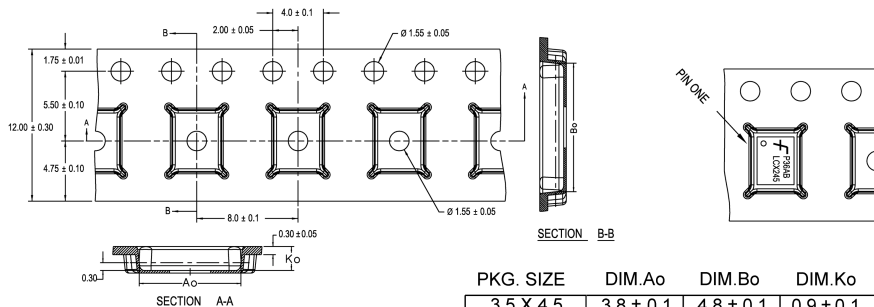


Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



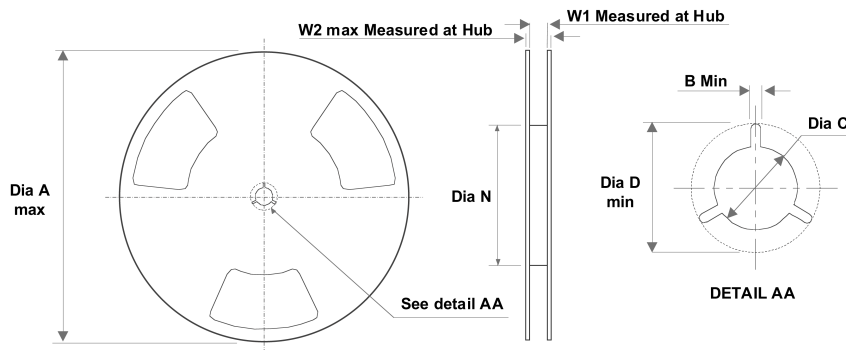
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

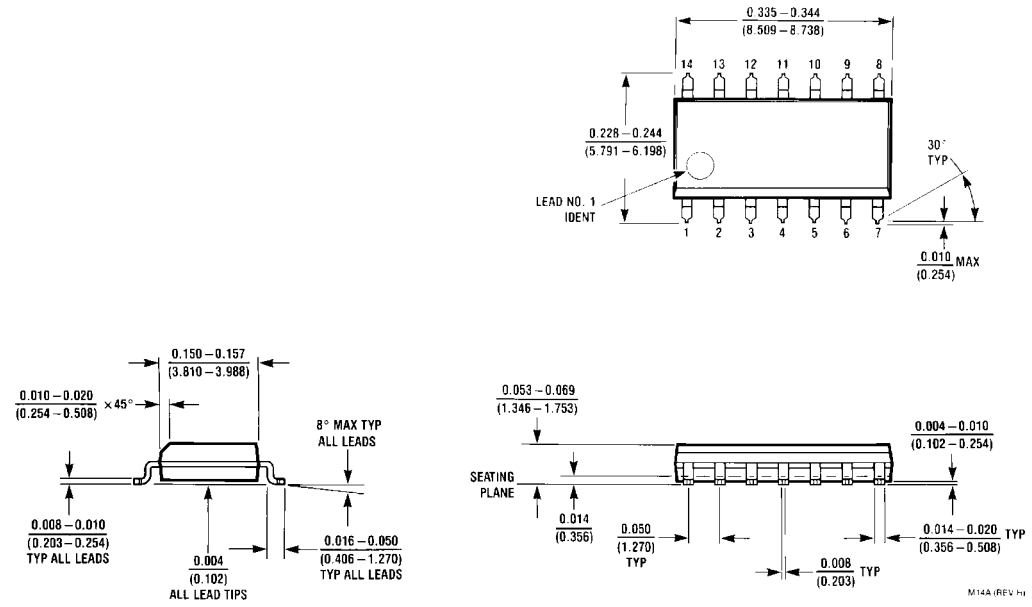
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is $\pm 0.002[0.05]$ for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

REEL DIMENSIONS inches (millimeters)



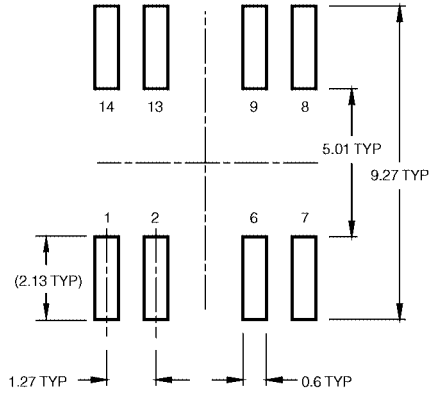
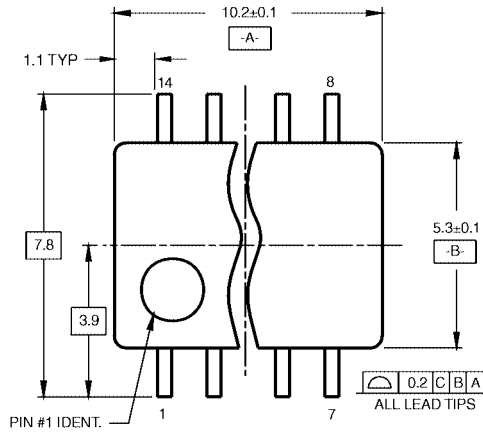
Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions inches (millimeters) unless otherwise noted

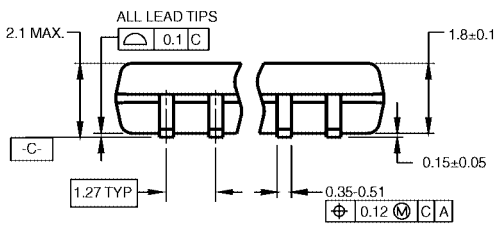


**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

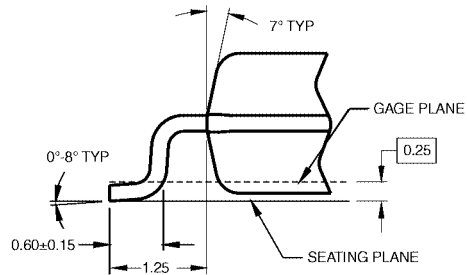
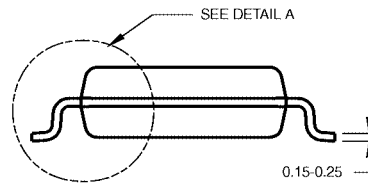
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



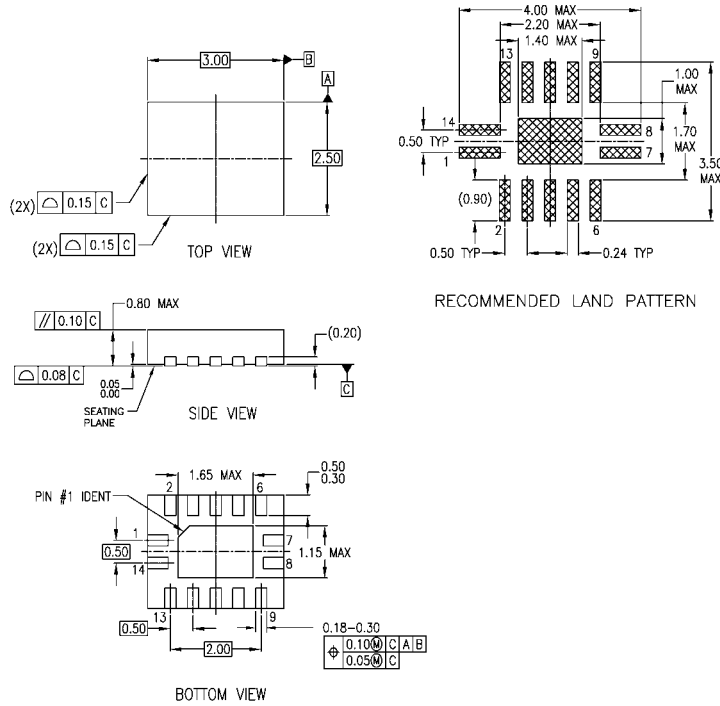
DETAIL A

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



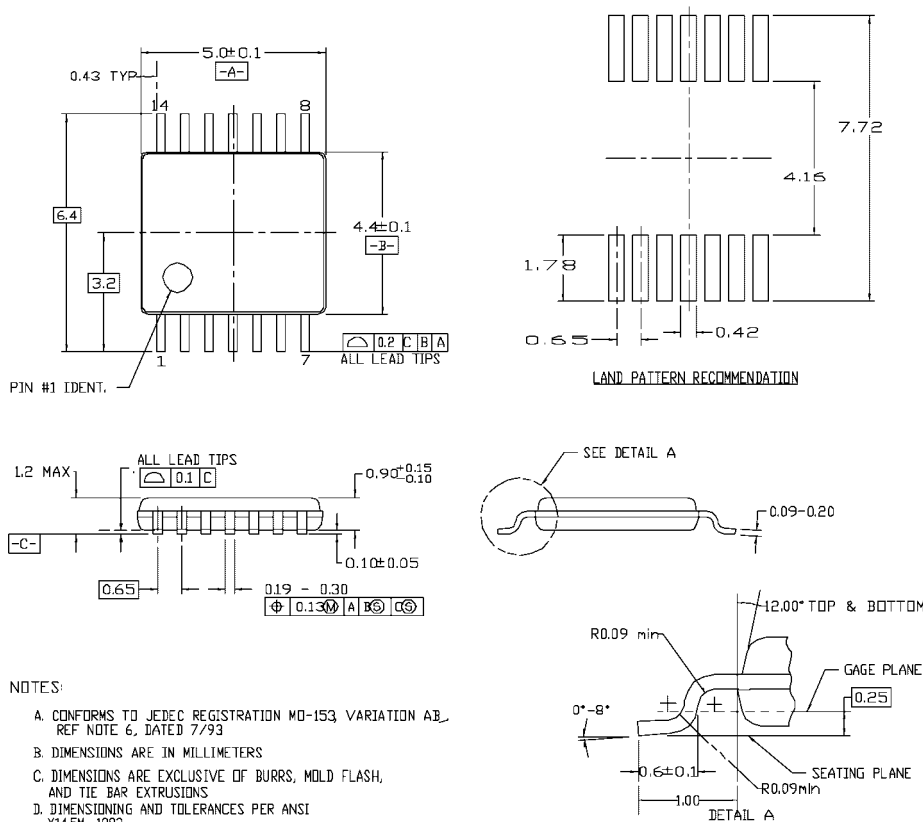
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP014ArevA

**Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
Package Number MLP014A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
 - B. DIMENSIONS ARE IN MILLIMETERS
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

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