



# STP9NC60 STP9NC60FP

## N - CHANNEL 600V - 0.6Ω - 9A TO-220/TO-220FP PowerMESH™ II MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP9NC60	600 V	< 0.75 Ω	9.0 A
STP9NC60FP	600 V	< 0.75 Ω	5.2 A

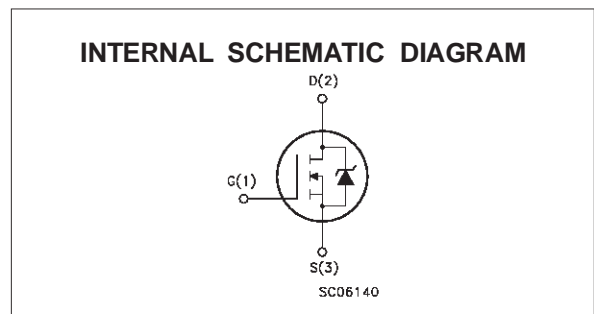
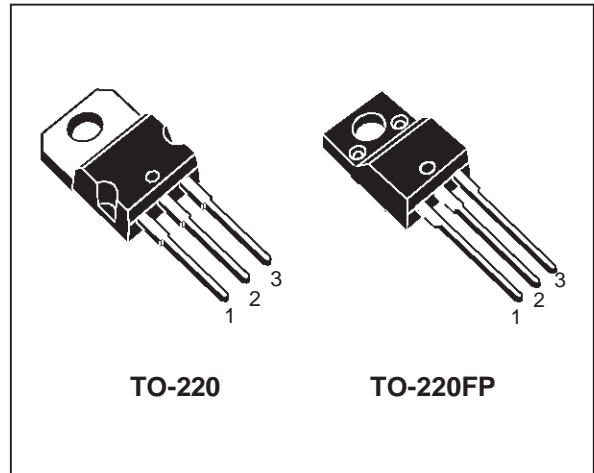
- v TYPICAL R<sub>DS(on)</sub> = 0.6 Ω
- v EXTREMELY HIGH dv/dt CAPABILITY
- v 100% AVALANCHE TESTED
- v NEW HIGH VOLTAGE BENCHMARK
- v GATE CHARGE MINIMIZED

### DESCRIPTION

The PowerMESH™ II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron\*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

### APPLICATIONS

- v HIGH CURRENT, HIGH SPEED SWITCHING
- v SWITCH MODE POWER SUPPLIES (SMPS)
- v DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVER



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP9NC60	STP9NC60FP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600		V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 kΩ)	600		V
V <sub>GS</sub>	Gate-source Voltage	± 30		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	9.0	5.2	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	5.7	3.3	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	36	36	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	125	40	W
	Derating Factor	1.0	0.32	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4.5	4.5	V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	—	2000	V
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 9A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

## STP9NC60/FP

### THERMAL DATA

		TO-220	TO-220FP		
$R_{thj-case}$	Thermal Resistance Junction-case	Max	1.0	3.12	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5		$^{\circ}\text{C}/\text{W}$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	0.5		$^{\circ}\text{C}/\text{W}$
$T_l$	Maximum Lead Temperature For Soldering Purpose		300		$^{\circ}\text{C}$

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max, $\delta < 1\%$ )	9	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	850	mJ

### ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ $V_{GS} = 0$	600			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30\text{ V}$			$\pm 100$	nA

#### ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 4\text{ A}$		0.6	0.75	$\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	9.0			A

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 4\text{ A}$		10		S
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		1400		pF
$C_{oss}$	Output Capacitance			196		pF
$C_{rss}$	Reverse Transfer Capacitance			31		pF

**ELECTRICAL CHARACTERISTICS** (continued)  
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300\text{ V}$ $I_D = 4.5\text{ A}$		28		ns
$t_r$	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, see fig. 3)		15		ns
$Q_g$	Total Gate Charge	$V_{DD} = 480\text{ V}$ $I_D = 9.0\text{ A}$ $V_{GS} = 10\text{ V}$		44	62	nC
$Q_{gs}$	Gate-Source Charge			10.5		nC
$Q_{gd}$	Gate-Drain Charge			19.5		nC

SWITCHING OFF

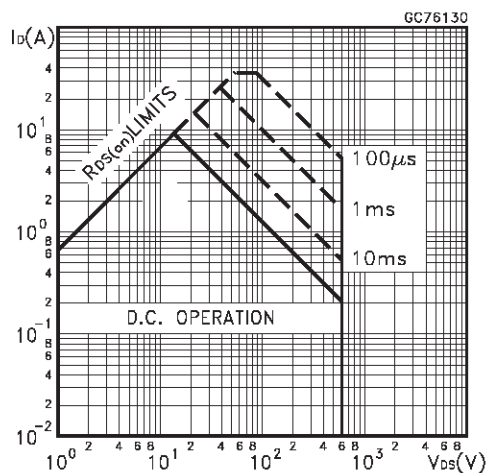
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 300\text{ V}$ $I_D = 4.5\text{ A}$		53		ns
$t_f$	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, see fig. 3)		30		ns
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 480\text{ V}$ $I_D = 9.0\text{ A}$		15		ns
$t_f$	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		12		ns
$t_c$	Cross-over Time	(Inductive Load, see fig. 5)		24		ns

SOURCE DRAIN DIODE

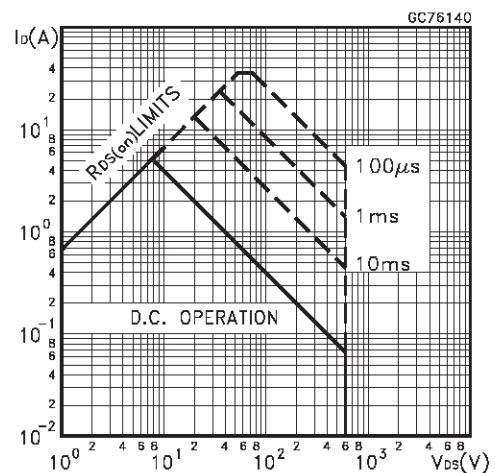
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				9.0	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				36	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 9\text{ A}$ $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 9\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		610		ns
$Q_{rr}$	Reverse Recovery Charge			5.4		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current			17		A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %  
( $\bullet$ ) Pulse width limited by safe operating area

Safe Operating Area for TO-220

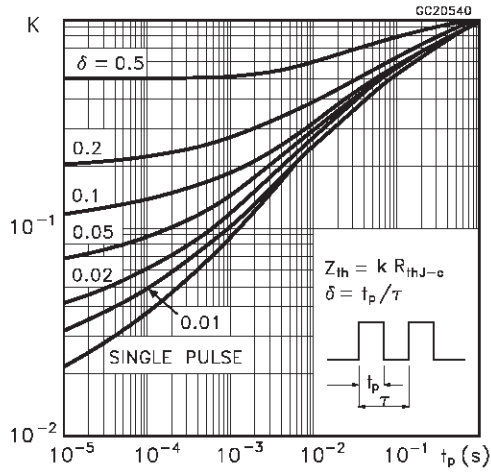


Safe Operating Area for TO-220FP

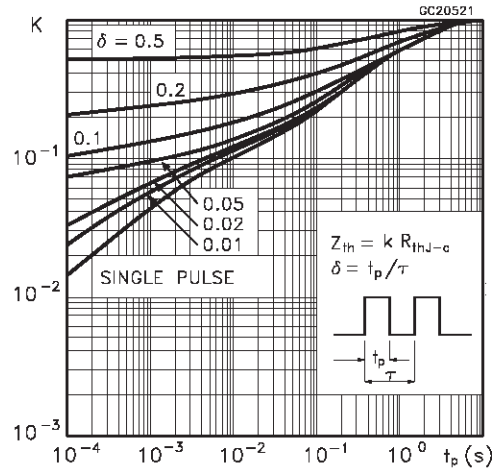


# STP9NC60/FP

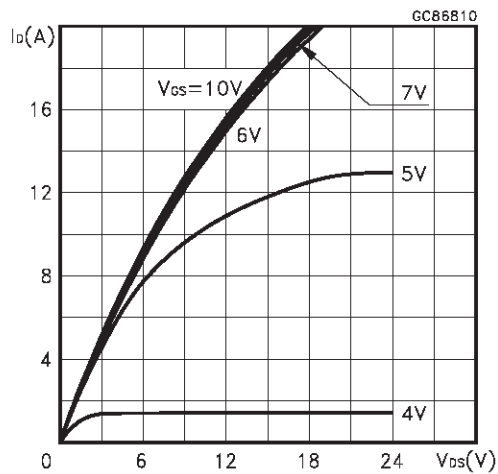
Thermal Impedance for TO-220



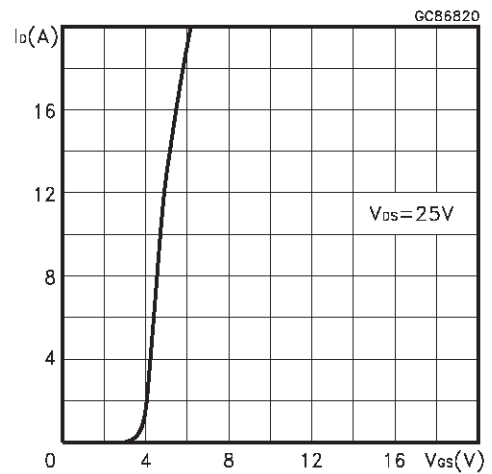
Thermal Impedance for TO-220FP



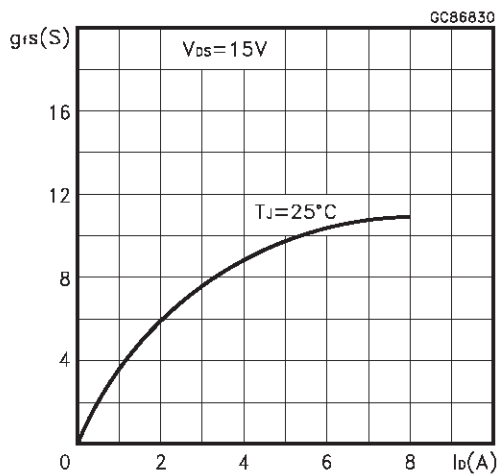
Output Characteristics



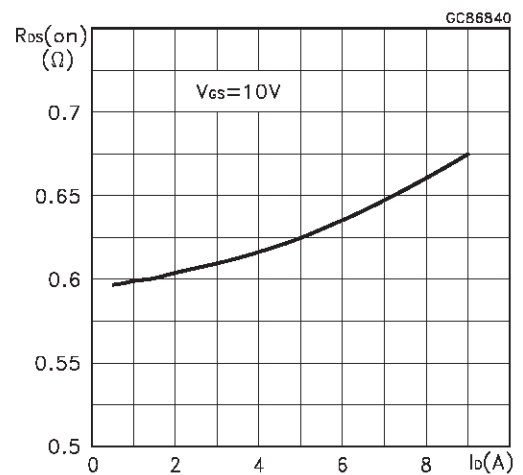
Transfer Characteristics



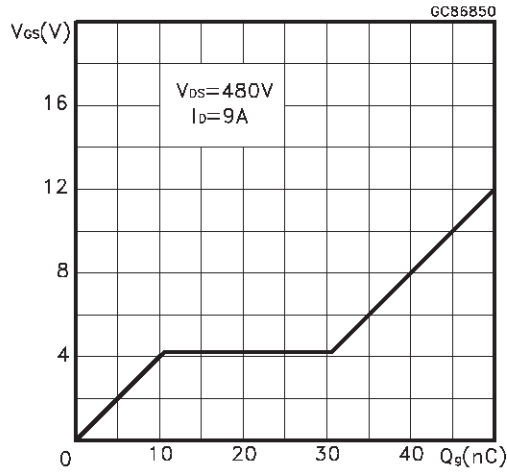
Transconductance



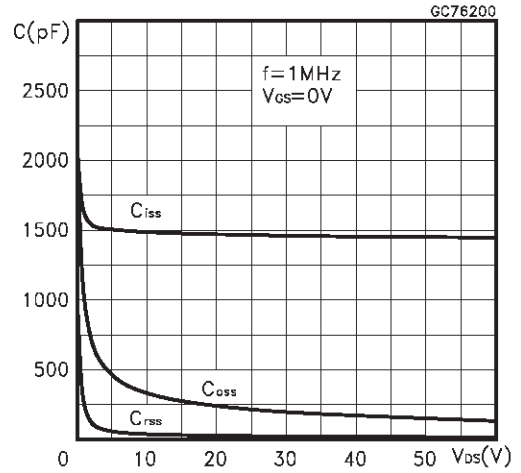
Static Drain-source On Resistance



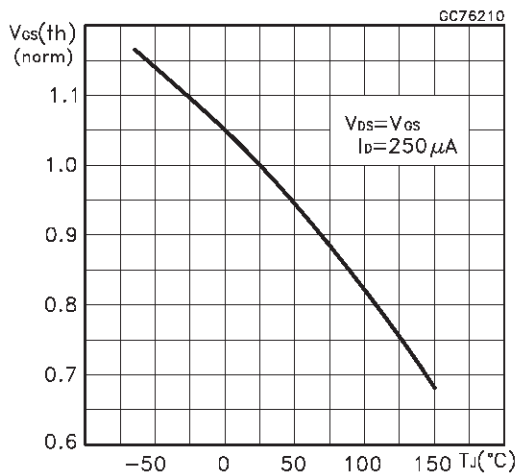
Gate Charge vs Gate-source Voltage



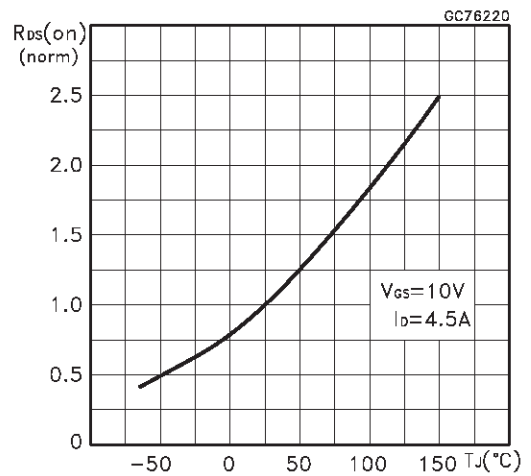
Capacitance Variations



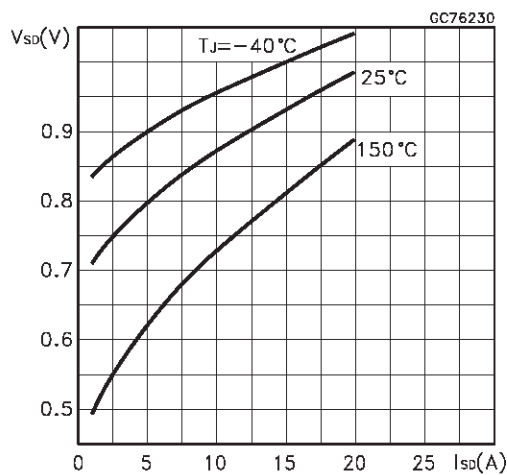
Normalized Gate Threshold Voltage vs Temperature



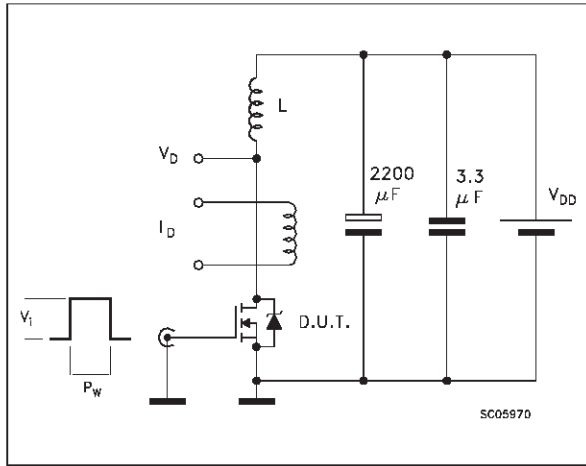
Normalized On Resistance vs Temperature



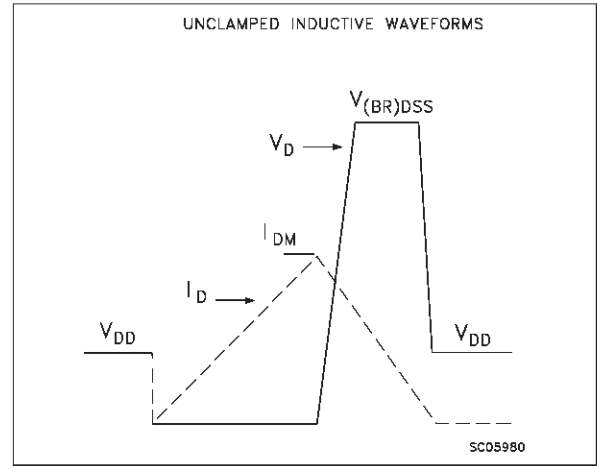
Source-drain Diode Forward Characteristics



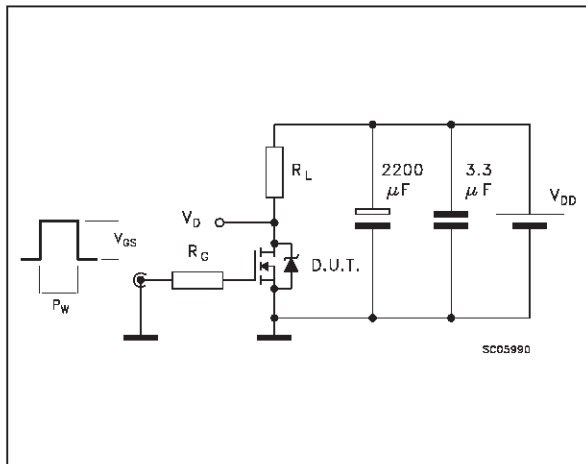
**Fig. 1: Unclamped Inductive Load Test Circuit**



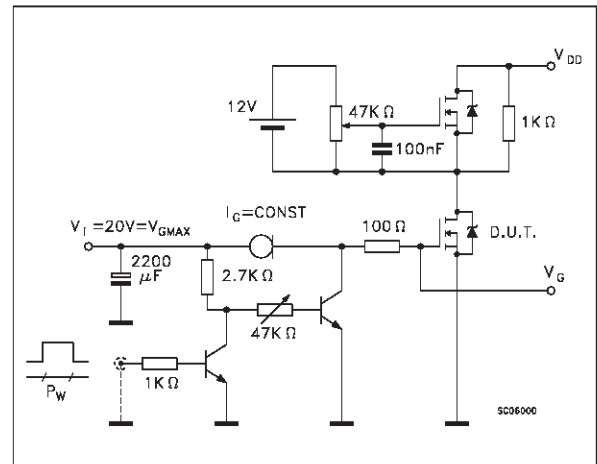
**Fig. 2: Unclamped Inductive Waveform**



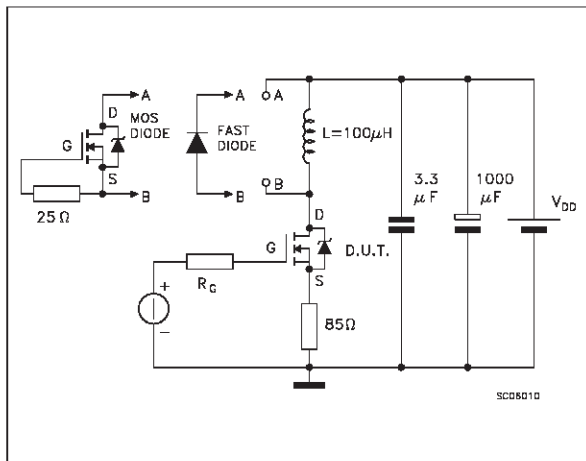
**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

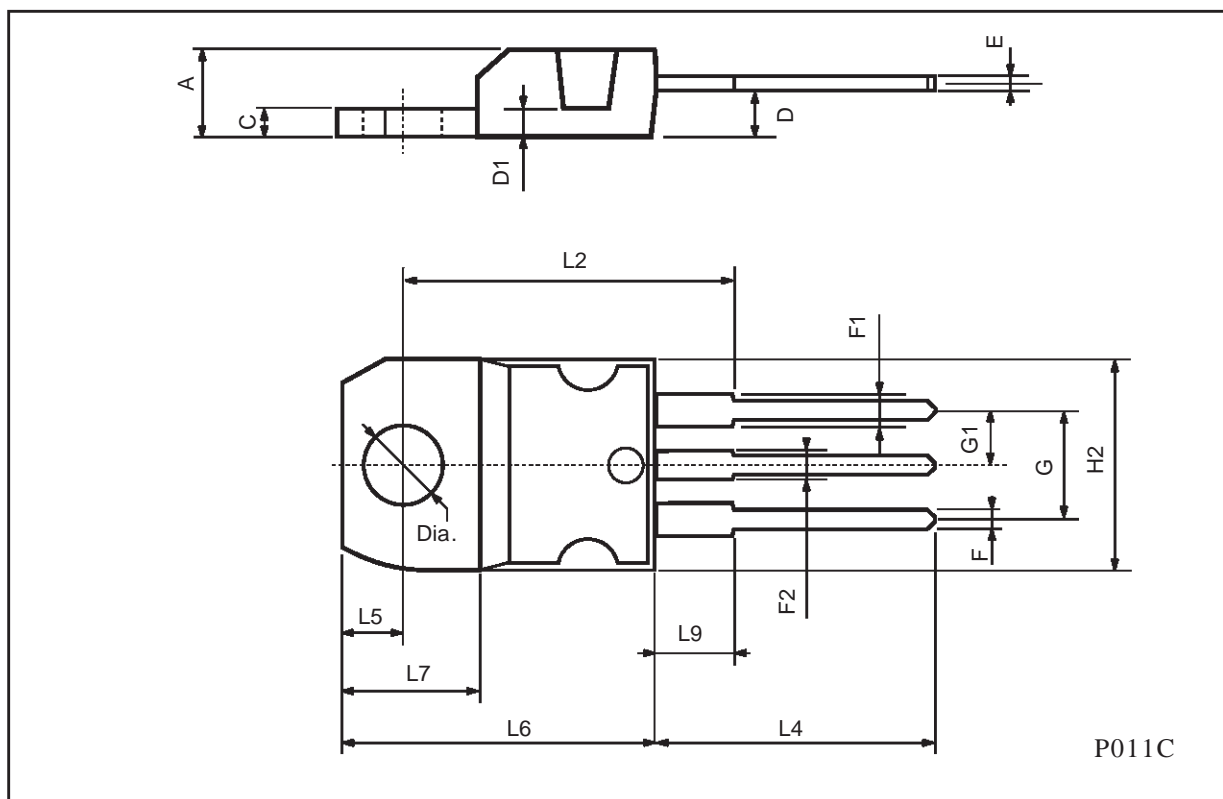


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



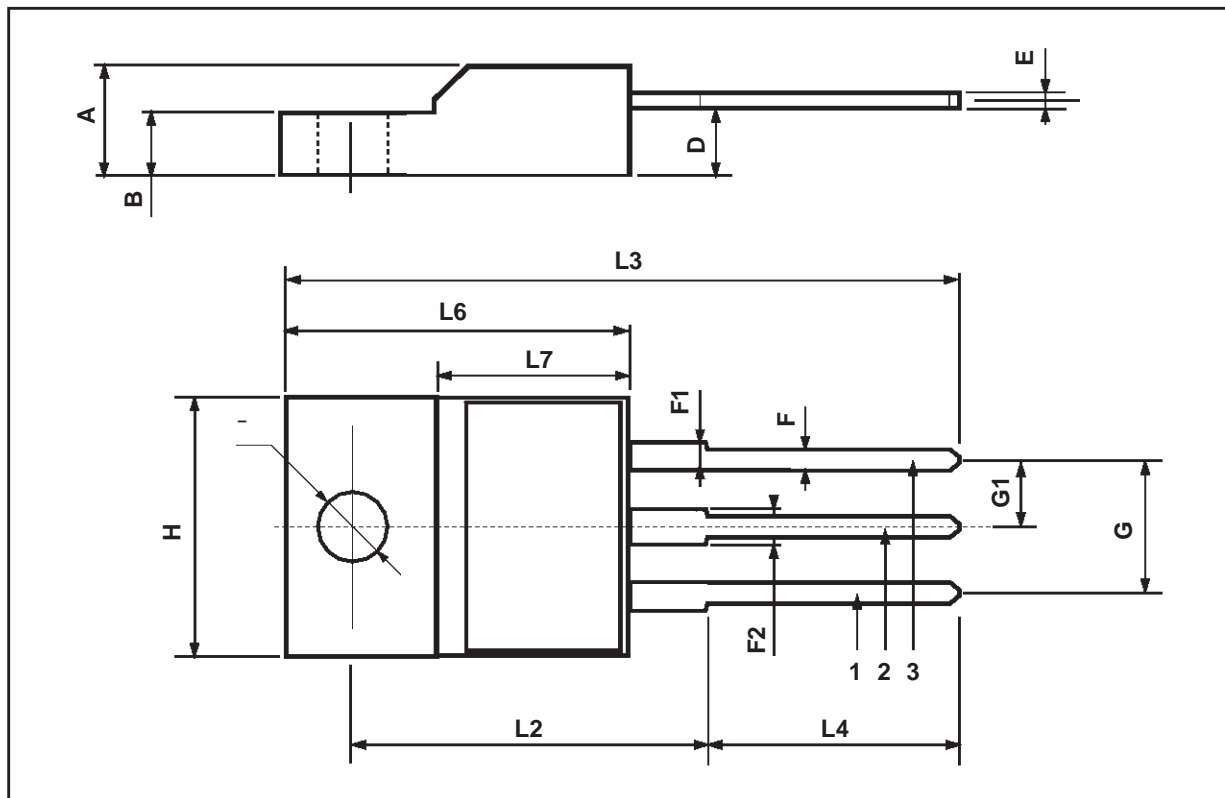
## TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



## TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126





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