



FDD5614P

# FDD5614P

## 60V P-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

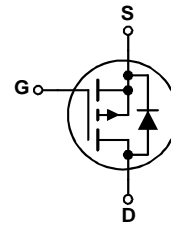
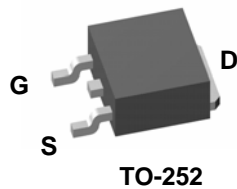
This 60V P-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

### Applications

- DC/DC converter
- Power management
- Load switch

### Features

- -15 A, -60 V.  $R_{DS(ON)} = 100\text{ m}\Omega$  @  $V_{GS} = -10\text{ V}$   
 $R_{DS(ON)} = 130\text{ m}\Omega$  @  $V_{GS} = -4.5\text{ V}$
- Fast switching speed
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units	
$V_{DSS}$	Drain-Source Voltage	-60	V	
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V	
$I_D$	Drain Current – Continuous (Note 3)	-15	A	
	– Pulsed (Note 1a)	-45		
$P_D$	Power Dissipation for Single Operation (Note 1)	(Note 1a)	42	W
		(Note 1b)	3.8	
		(Note 1b)	1.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$	

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD5614P	FDD5614P	13"	16mm	2500 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain-Source Avalanche Ratings (Note 1)</b>						
$W_{DSS}$	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = -30\text{ V}, I_D = -4.5\text{ A}$			90	mJ
$I_{AR}$	Maximum Drain-Source Avalanche Current				-4.5	A
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-49		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.9\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}, T_J = 125^\circ\text{C}$		76 99 137	100 130 185	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -3\text{ A}$		8		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V},$		759		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		90		pF
$C_{riss}$	Reverse Transfer Capacitance			39		pF
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30\text{ V}, I_D = -1\text{ A},$		7	14	ns
$t_r$	Turn-On Rise Time	$V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			19	34	ns
$t_f$	Turn-Off Fall Time			12	22	ns
$Q_g$	Total Gate Charge	$V_{DS} = -30\text{ V}, I_D = -4.5\text{ A},$		15	24	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = -10\text{ V}$		2.5		nC
$Q_{gd}$	Gate-Drain Charge			3.0		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-3.2	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -3.2\text{ A}$ (Note 2)		-0.8	-1.2	V

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $R_{\theta JA} = 40^{\circ}\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b)  $R_{\theta JA} = 96^{\circ}\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

3. Maximum current is calculated as: 
$$\sqrt{\frac{P_D}{R_{DS(on)}}}$$

where  $P_D$  is maximum power dissipation at  $T_C = 25^{\circ}\text{C}$  and  $R_{DS(on)}$  is at  $T_{J(max)}$  and  $V_{GS} = 10\text{V}$ . Package current limitation is 21A

Typical Characteristics

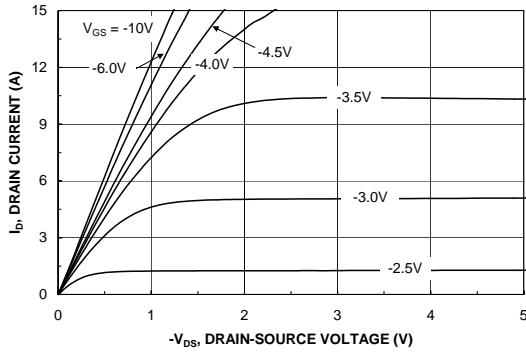


Figure 1. On-Region Characteristics.

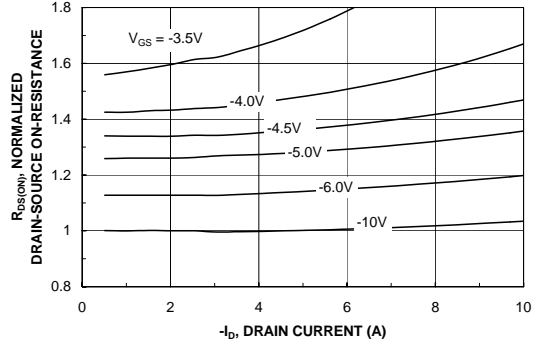


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

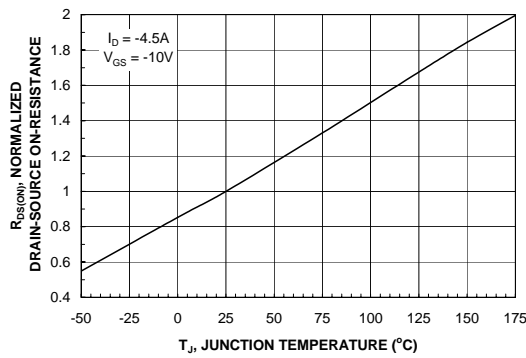


Figure 3. On-Resistance Variation with Temperature.

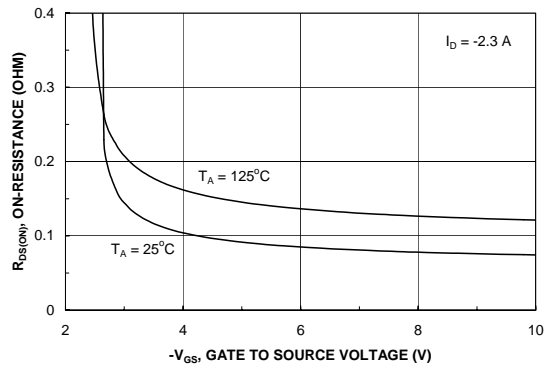


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

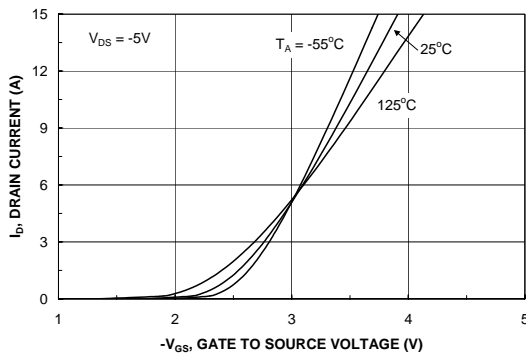


Figure 5. Transfer Characteristics.

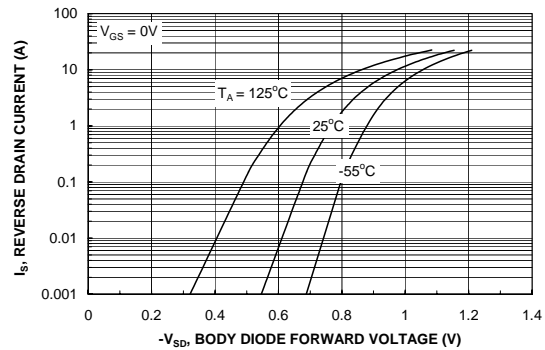


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

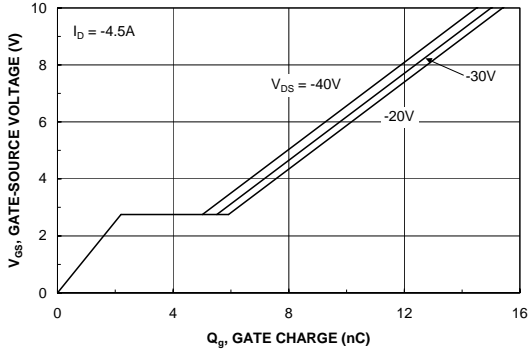


Figure 7. Gate Charge Characteristics.

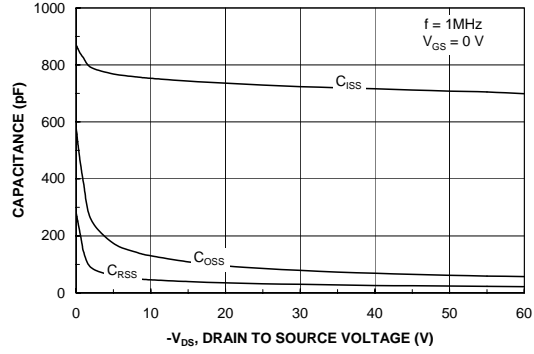


Figure 8. Capacitance Characteristics.

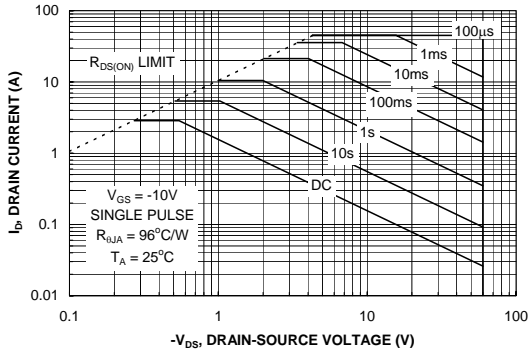


Figure 9. Maximum Safe Operating Area.

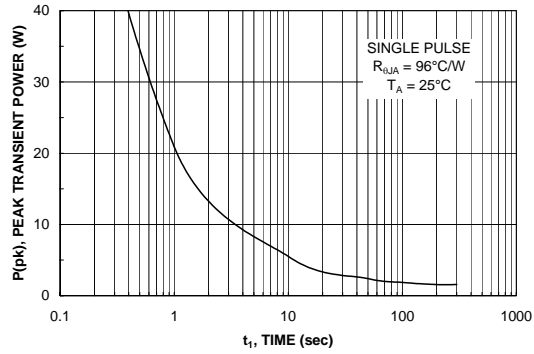


Figure 10. Single Pulse Maximum Power Dissipation.

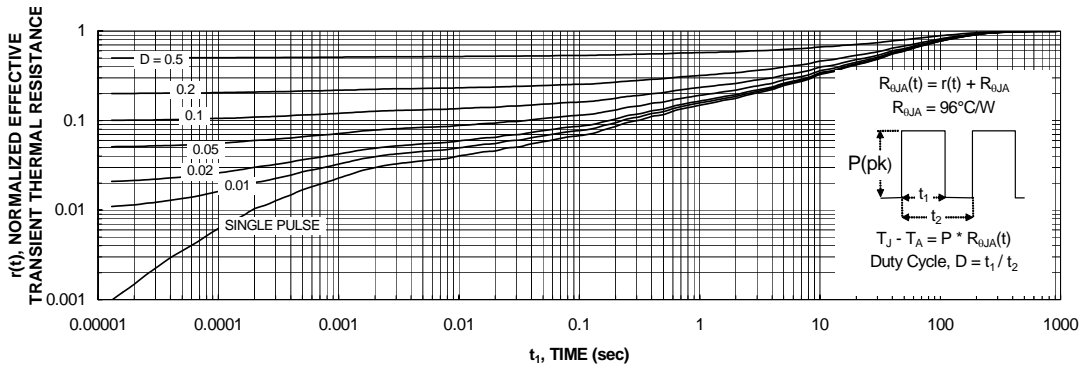
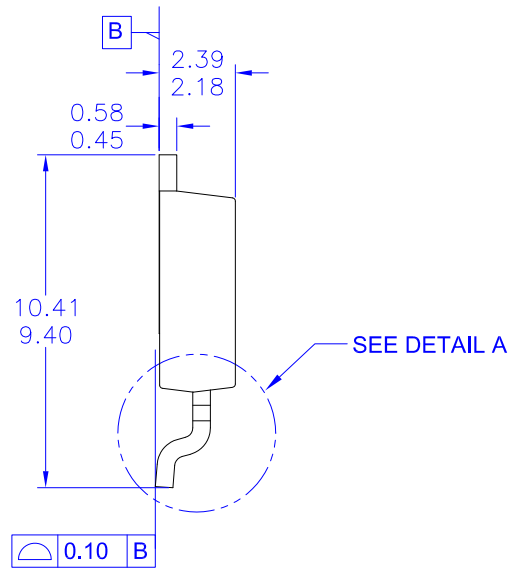
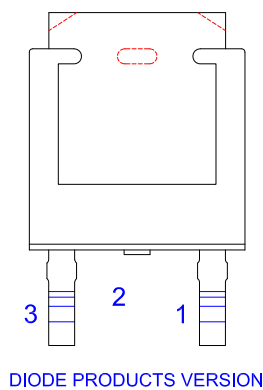
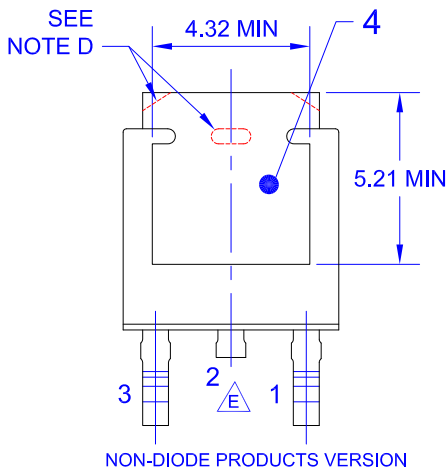
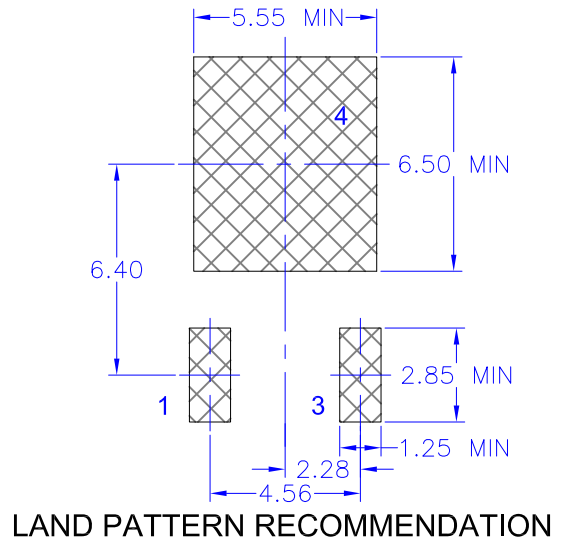
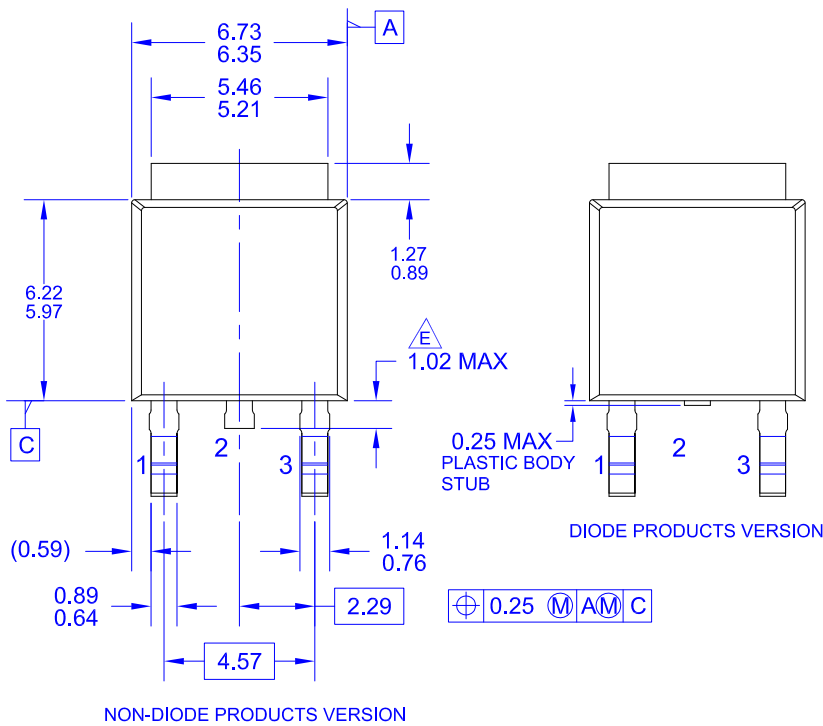
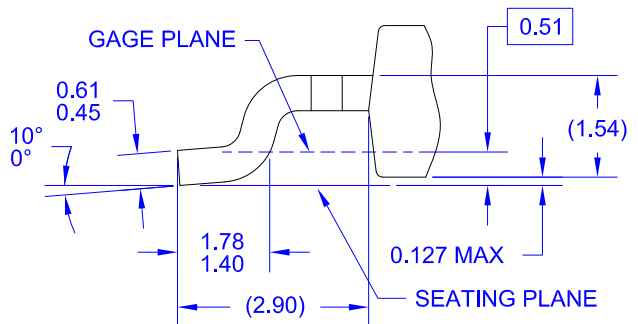


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10



DETAIL A  
(ROTATED -90°)  
SCALE: 12X





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