Product Change Notification / SYST-13LRGR126

Date:

14-Apr-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATtiny804/806/807/1604/1606/1607 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-13LRGR126_Affected_CPN_04142021.pdf
SYST-13LRGR126_Affected_CPN_04142021.csv

Notification Text:

SYST-13LRGR126

Microchip has released a new Product Documents for the ATtiny804/806/807/1604/1606/1607 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATtiny804/ 806/ 807/ 1604/ 1606/ 1607 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
1) Initial document release
The content of the document has been restructured from:
• ATtiny804/1604 Silicon Errata and Data Sheet Clarification
• ATtiny806/1606 Silicon Errata and Data Sheet Clarification
• ATtiny807/1607 Silicon Errata and Data Sheet Clarification
to:
• ATtiny804/806/807/1604/1606/1607 Silicon Errata and Data Sheet Clarification (this document)

Refer to 4.2 Appendix - Obsolete Revision History for further details.
The following items are referring to changes between the latest revisions of the obsolete documents and this document:
• Added new errata:
    – Device: 2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

– CCL: 2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT
– TCA: 2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode
– TCB: 2.7.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode
– USART:
  • 2.8.2 Open-Drain Mode Does Not Work When TXD is Configured as Output
  • 2.8.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode
  • Removed old data sheet clarifications, as the corresponding data sheet has been updated with correct information

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 14 Apr 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATtiny804/ 806/ 807/ 1604/ 1606/ 1607 Silicon Errata and Data Sheet Clarification

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Affected Catalog Part Numbers (CPN)

ATTINY1604-SSF
ATTINY1604-SSFR
ATTINY1604-SSN
ATTINY1604-SSNR
ATTINY1606-MF
ATTINY1606-MFR
ATTINY1606-MN
ATTINY1606-MNR
ATTINY1606-SF
ATTINY1606-SFR
ATTINY1606-SN
ATTINY1606-SNR
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ATtiny804/806/807/1604/1606/1607

Silicon Errata and Data Sheet Clarification

The ATtiny804/806/807/1604/1606/1607 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002312), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny804/806/807/1604/1606/1607 devices.

Notes:
- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002312) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

-	Erratum is not applicable.
X	Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. A
Device	2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X
ADC	2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode	X
	2.3.2 Pending Event Stuck When Disabling the ADC	X
	2.3.3 ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X
	2.3.4 ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X
CCL	2.4.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'	X
	2.4.2 D-latch is Not Functional	X
	2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT	X
RTC	2.5.1 Disabling the RTC Stops the PIT	X
	2.5.2 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	X
TCA	2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	2.7.1 The TCA Restart Command Does Not Force a Restart of TCB	X
	2.7.2 Minimum Event Duration Must Exceed the Selected Clock Period	X
	2.7.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X
USART	2.8.1 TXD Pin Override Not Released When Disabling the Transmitter	X
	2.8.2 Open-Drain Mode Does Not Work When TXD is Configured as Output	X
	2.8.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X

2. Silicon Errata Issues

2.1 Errata Details

-   Erratum is not applicable.

X   Erratum is applicable.

2.2 Device

2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around
Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCK in CLKCTRL.OSC20MCALIBB to '1'.

Affected Silicon Revisions

Rev. A
X

2.3 ADC - Analog-to-Digital Converter

2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around
Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. A
X

2.3.2 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work Around
Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. A

X

2.3.3 ADC Performance Degrades with CLK$_{ADC}$ Above 1.5 MHz and V$_{DD}$ < 2.7V

The ADC INL performance degrades if CLK$_{ADC}$ > 1.5 MHz and ADCn.CALIB.DUTYCYC set to '0' for V$_{DD}$ < 2.7V.

Work Around
None.

Affected Silicon Revisions

Rev. A
X

2.3.4 ADC Functionality Cannot be Ensured with CLK$_{ADC}$ Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK$_{ADC}$ > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work Around
If ADC is operated with CLK$_{ADC}$ > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. A
X

2.4 CCL - Configurable Custom Logic

2.4.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'

Connecting the LUTs in linked mode requires LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work Around
Use an event channel to link the LUTs, or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. A
X

2.4.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work Around
None.

Affected Silicon Revisions

Rev. A
X

2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL peripheral must be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around

None

Affected Silicon Revisions

Rev. A
X

2.5 RTC - Real-Time Counter

2.5.1 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work Around

Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. A
X

2.5.2 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the 15-bit prescaler resulting in a longer period on the current count or period.

Work Around

None.

Affected Silicon Revisions

Rev. A
X

2.6 TCA - 16-Bit Timer/Counter Type A

2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. A
X

2.7 TCB - 16-Bit Timer/Counter Type B

2.7.1 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force restarting the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around
None.

Affected Silicon Revisions

Rev. A
X

2.7.2 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Work Around
Ensure that the high/low period of input events is equal to or longer than the selected clock source (CLKSEL in TCBn.CTRLA) period.

Affected Silicon Revisions

Rev. A
X

2.7.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB operates in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around
Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A
X

2.8 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.8.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work Around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. A
X

2.8.2 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A
X

2.8.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception.

The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This results in the Start-of-Frame Detector being triggered and falsely detecting the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data.

Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Enable it again by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A
X

3.   Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002312).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1   None

There are no known data sheet clarifications as of this publication date.

4.   Document Revision History

Note: The document revision is independent of the silicon revision.

4.1   Revision History

Doc. Rev.	Date	Comments

A	04/2021	• Initial document release
		
		The content of the document has been restructured from:
		• ATtiny804/1604 Silicon Errata and Data Sheet Clarification
		• ATtiny806/1606 Silicon Errata and Data Sheet Clarification
		• ATtiny807/1607 Silicon Errata and Data Sheet Clarification
		
		to:
		• **ATtiny804/806/807/1604/1606/1607 Silicon Errata and Data Sheet Clarification (this document)**
		
		Refer to 4.2 Appendix - Obsolete Revision History for further details.
		The following items are referring to changes between the latest revisions of the obsolete documents and this document:
		
		• Added new errata:
		  – Device: 2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values
		  – CCL: 2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT
		  – TCA: 2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode
		  – TCB: 2.7.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode
		  – USART:
		      • 2.8.2 Open-Drain Mode Does Not Work When TXD is Configured as Output
		      • 2.8.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode
		
		• Removed old data sheet clarifications, as the corresponding data sheet has been updated with correct information

4.2   Appendix - Obsolete Revision History

Notes: Due to document structure change from pin organized documents, the following obsolete document revision history is provided as a reference.
•   ATtiny804/1604 Silicon Errata and Data Sheet Clarification (DS40002126B)
•   ATtiny806/1606 Silicon Errata and Data Sheet Clarification (DS40002127B)
•   ATtiny807/1607 Silicon Errata and Data Sheet Clarification (DS40002128B)

4.2.1   Obsolete Document DS40002126

Doc. Rev.	Date	Comments
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarification for ADC electrical characteristics
A	06/2019	Initial document release.

4.2.2 Obsolete Document DS40002127

Doc. Rev.	Date	Comments
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarification for ADC electrical characteristics
A	06/2019	Initial document release

4.2.3 Obsolete Document DS40002128

Doc. Rev.	Date	Comments
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarification for ADC electrical characteristics
A	06/2019	Initial document release

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