Product Bulletin

Document #:PB25352X
Issue Date:01 Apr 2023

Title of Change:	NCH-RSL15 Datasheet Update with Sleep Mode Errata
Effective date:	01 Apr 2023
Contact information:	Contact your local onsemi Sales Office or *Ben.Widsten@onsemi.com*
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Datasheet Update
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

onsemi Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

The NCH-RSL15 datasheet Rev. 4 includes the following updates:

- Addition of section 'RSL15 Errata for Chip Identification 2.02.00' describing the Sleep Mode errata
- Table 9. SLEEP MODE CURRENT CONSUMPTION has the following updates:
  - Rows with GPIO wakeup source and RAM retention removed due to errata
  - Entries with RTC timer wakeup source and RAM retention slightly increased current due to errata
  - Rows with RC32 active and RAM retention removed as superfluous
- Table 10. ULP DATA ACQUISITION SUBSYSTEM PERFORMANCE has the following updates:
  - Entries with RAM retention increased current slightly due to errata

For reference, the updated datasheet Rev. 4 tables are shown below.

Table 9. SLEEP MODE CURRENT CONSUMPTION:

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Operating Conditions	Symbol	Wakeup Source	VBAT	DC Conversion	Min	Typ	Max	Unit
Clocks stopped All peripherals disabled **No RAM retained** 32 kHz RC32 inactive 32 kHz XTAL32K inactive	Ids1	GPIO	3.0 V	BUCK Mode		36		nA
			1.8 V	BUCK Mode		37		
			1.25 V	LDO Mode		60		
System clocks stopped All peripherals disabled **No RAM retained** **32 kHz RC32 active** 32 kHz XTAL32K inactive	Ids2	RTC timer	3.0 V	BUCK Mode		83		nA
			1.8 V	BUCK Mode		98		
			1.25 V	LDO Mode		147		
System clocks stopped All peripherals disabled **No RAM retained** 32 kHz RC32 inactive **32 kHz XTAL32K active**	Ids3	RTC timer	3.0 V	BUCK Mode		57		nA
			1.8 V	BUCK Mode		66		
			1.25 V	LDO Mode		97		
System clocks stopped All peripherals disabled **8 KB RAM retained** 32 kHz RC32 inactive **32 kHz XTAL32K active**	Ids4	RTC timer	3.0 V	BUCK Mode		165		nA
			1.8 V	BUCK Mode		233		
			1.25 V	LDO Mode		253		
System clocks stopped All peripherals disabled **16 KB RAM retained** 32 kHz RC32 inactive **32 kHz XTAL32K active**	Ids5	RTC timer	3.0 V	BUCK Mode		208		nA
			1.8 V	BUCK Mode		303		
			1.25 V	LDO Mode		473		
System clocks stopped All peripherals disabled **32 KB RAM retained** 32 kHz RC32 inactive **32 kHz XTAL32K active**	Ids6	RTC timer	3.0 V	BUCK Mode		303		nA
			1.8 V	BUCK Mode		448		
			1.25 V	LDO Mode		701		

NOTES: • Buck mode measurements were captured with an additional 10 μF in parallel with VBAT and a 200 Ω resistor in series in order to obtain a more accurate measurement with the measurement device.
• Current values include increases due to workarounds imposed by errata in section 'RSL15 Errata for Chip Identification 2.02.00'.

Table 10. ULP DATA ACQUISITION SUBSYSTEM PERFORMANCE:

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Operating Condition	Min	Typ	Max	Unit
Continuous ADC operation in Smart Sense mode with wakeup on ADC threshold Configuration/conditions: VBAT = 3 V, BUCK Mode, Successive Approximation ADC enabled and selected, XTAL32K, VREF = VBAT reference selected, ADC Fs = 256 sps, accumulation 4 samples. Processor would wake to Run mode by ADC threshold but this is not included in this measurement		206		nA
Continuous ADC operation in Smart Sense mode, wakeup on FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 KB RAM retained, XTAL32K, Successive Approximation ADC enabled, VREF = VBAT, ADC Fs = 1 ksps, accumulation 16 samples, FIFO Size 16. Processor wakes to Run mode every 256 ms to transfer samples to RAM		2.1		μA
Continuous ADC operation in Smart Sense mode, wakeup on FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 KB RAM retained. XTAL32K, Successive Approximation ADC enabled, VREF = VDDA, ADC Fs = 1 ksps, Accumulation 16 samples, FIFO Size 16. Processor wakes to Run mode every 256 ms to transfer samples to RAM		4.1		μA
Continuous Pulse Counter accumulation in Smart Sense mode, wakeup when FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 KB RAM retained, XTAL32K, Pulse Counter enabled, Pulse Count Interval 1000 ms, accumulation of 5 samples, result stored in FIFO. Processor wakes to Run mode every 5 s to transfer sample to RAM		348		nA

NOTE: Current values include increases due to workarounds imposed by errata in section 'RSL15 Errata for Chip Identification 2.02.00'.

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

NCH-RSL15-284-101Q40-ACG	NCH-RSL15-512-101Q40-ACG	