Product Bulletin

Document #:PB25635Z
Issue Date:19 Jul 2023

Title of Change:	NCV7428 Datasheet Update (editorial changes)
Effective date:	19 Jul 2023
Contact information:	Contact your local onsemi Sales Office or Jelle.Genne@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Datasheet Update (editorial changes)
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

onsemi Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

Datasheet update from Rev. 7 to Rev. 8
The change will not impact form, fit, or function of the products.

Correction of data sheet, issuance of errata and editorial changes:

Front page: Case code removed from the package reference section.
Info on the case code is at the back of the document.
Front page: Marking diagram updated, added decoding of the last two xy digits of the marking 1st line.
Table 3: Ambient temperature removed from Absolute Maximum Ratings table.
Table 4: VOUT5 and VOUT33 removed from Operating Ranges table.
Table 6: LIN Transmitter duty cycle parameters – Added Normal and Low slope clarification to Condition fields.
Case outline information: Updated from 506DG to 507AB as per FPCN22120ZC (switchover DC = 2311).
Throughout document: Minor editorial changes.

No impact on product performance, no impact on electrical characteristics.

	From	To
Datasheet	NCV7428/D, Rev. 7	NCV7428/D, Rev. 8

Front page: Case code removed from the package reference section

Front page: Added decoding of the last two xy digits of the marking 1st line

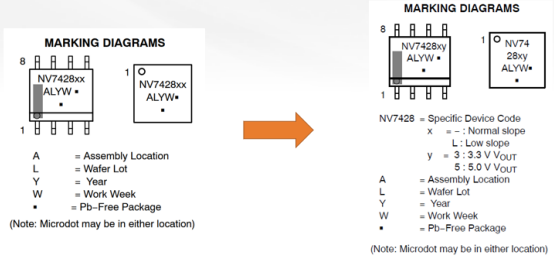


Table 3: Ambient temperature removed from Absolute Maximum Ratings table

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_S	Maximum DC voltage at V_S pin	−0.3	45	V
V_{OUT}	Maximum voltage at V_{OUT} pin	−0.3	6	V
V_{LIN}	Maximum voltage at LIN bus pin	−45	45	V
$V_{Dig\_IO\_inputs}$	Maximum voltage at digital input pins (TxD, EN)	−0.3	45	V
$V_{Dig\_IO\_outputs}$	Maximum voltage at digital output pins (RxD, RSTN)	−0.3	V_{OUT}+0.3	V
T_{AMB}	Ambient temperature range	−40	+125	°C
T_J	Junction temperature range	−40	+170	°C
T_{STG}	Storage temperature range	−55	+150	°C
V_{ESD}	System ESD at pins VS, LIN as per IEC 61000−4−2: 330 Ω / 150 pF (Verified by external test house)	≥ ±14		kV
	Human body model at pins VS, LIN stressed towards GND with 1500 Ω / 100 pF	≥ ±8		kV
	Human body model at all pins as per JESD22−A114 / AEC−Q100−002	≥ ±4		kV
	Charge device model at all pins as per JESD22−C101 / AEC−Q100−011	≥ ±500		V
	Machine model; (200 pF; 0.75 μH; 10 Ω) as per JESD22−A115 / AEC−Q100−003	±200		V
MSL	Moisture Sensitivity Level SOIC DFN	2 1		−
T_{SLD}	Lead temperature Soldering − Reflow (SMD styles only), Pb−Free (Note 1)	260		°C

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_S	Maximum DC voltage at V_S pin	−0.3	45	V
V_{OUT}	Maximum voltage at V_{OUT} pin	−0.3	6	V
V_{LIN}	Maximum voltage at LIN bus pin	−45	45	V
$V_{Dig\_IO\_inputs}$	Maximum voltage at digital input pins (TxD, EN)	−0.3	45	V
$V_{Dig\_IO\_outputs}$	Maximum voltage at digital output pins (RxD, RSTN)	−0.3	V_{OUT}+0.3	V
T_J	Junction temperature range	−40	+170	°C
T_{STG}	Storage temperature range	−55	+150	°C
V_{ESD}	System ESD at pins VS, LIN as per IEC 61000−4−2: 330 Ω / 150 pF (Verified by external test house)	≥ ±14		kV
	Human body model at pins VS, LIN stressed towards GND with 1500 Ω / 100 pF	≥ ±8		kV
	Human body model at all pins as per JESD22−A114 / AEC−Q100−002	≥ ±4		kV
	Charge device model at all pins as per JESD22−C101 / AEC−Q100−011	≥ ±500		V
	Machine model; (200 pF; 0.75 μH; 10 Ω) as per JESD22−A115 / AEC−Q100−003	±200		V
MSL	Moisture Sensitivity Level SOIC DFN	2 1		−
T_{SLD}	Lead temperature Soldering − Reflow (SMD styles only), Pb−Free (Note 1)	260		°C

Table 4: VOUT5 and VOUT33 removed from Operating Ranges table

Table 4. OPERATING RANGES

Symbol	Parameter	Min	Max	Units
V_S	VS operating voltage for parametric operation (Note 2)	5.5	28	V
	VS operating voltage for limited operation (Note 2)	4	28	V
V_{OUT5}	Regulated voltage at V_{OUT} supply output for 5 V versions	4.9	5.1	V
V_{OUT33}	Regulated voltage at V_{OUT} supply output for 3.3 V versions	3.234	3.366	V
I_{VOUT}	Current delivered by the V_{OUT} regulator	70		mA
V_{LIN}	Operating voltage at LIN bus pin	0	V_S	V
$V_{Dig\_IO\_inputs}$	Operating voltage at digital input pins (TxD, EN)	0	5.5	V
$V_{Dig\_IO\_outputs}$	Operating voltage at digital output pins (RxD, RSTN)	0	V_{OUT}	V

Table 4. OPERATING RANGES

Symbol	Parameter	Min	Max	Units
V_S	VS operating voltage for parametric operation (Note 2)	5.5	28	V
	VS operating voltage for limited operation (Note 2)	4	28	V
I_{VOUT}	Current delivered by the V_{OUT} regulator	70	−	mA
V_{LIN}	Operating voltage at LIN bus pin	0	V_S	V
$V_{Dig\_IO\_inputs}$	Operating voltage at digital input pins (TxD, EN)	0	5.5	V
$V_{Dig\_IO\_outputs}$	Operating voltage at digital output pins (RxD, RSTN)	0	V_{OUT}	V

Table 7: LIN Transmitter duty cycle parameters – Added Normal and Low slope clarification to Condition fields

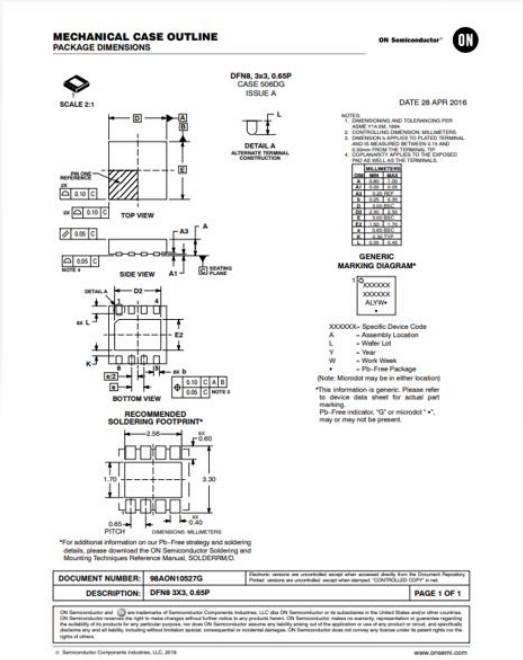
Table 7. AC CHARACTERISTICS (V_S = 5.5 V to 28 V; T_J = −40°C to +150°C; unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF)

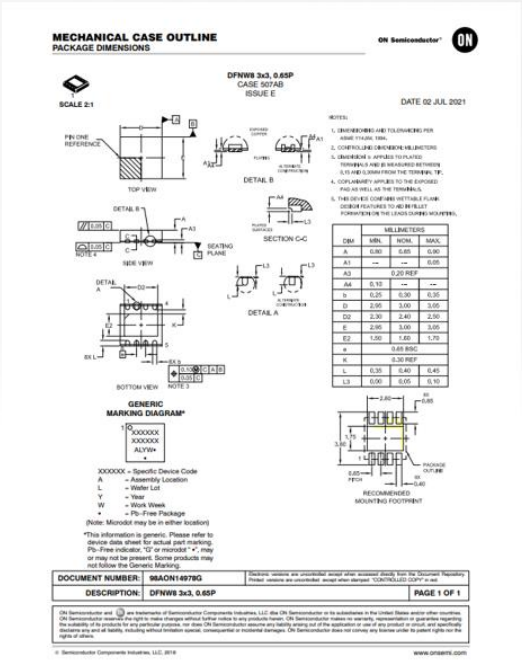
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
D1	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	$TH_{REC(max)}$ = 0.744 x V_S $TH_{DOM(max)}$ = 0.581 x V_S t_{BIT} = 50 μs V_S = 7 V to 18 V	0.396		0.5	
D2	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	$TH_{REC(min)}$ = 0.422 x V_S $TH_{DOM(min)}$ = 0.284 x V_S t_{BIT} = 50 μs V_S = 7.6 V to 18 V	0.5		0.581	
D3	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	$TH_{REC(max)}$ = 0.778 x V_S $TH_{DOM(max)}$ = 0.616 x V_S t_{BIT} = 96 μs V_S = 7 V to 18 V	0.417		0.5	
D4	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	$TH_{REC(min)}$ = 0.389 x V_S $TH_{DOM(min)}$ = 0.251 x V_S t_{BIT} = 96 μs V_S = 7.6 V to 18 V	0.5		0.590	
t_{fallNS}	LIN falling edge normal slope	Normal Mode; V_S = 12 V			22.5	μs

Table 7. AC CHARACTERISTICS (V_S = 5.5 V to 28 V; T_J = −40°C to +150°C; unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
D1	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	Normal slope $TH_{REC(max)}$ = 0.744 x V_S $TH_{DOM(max)}$ = 0.581 x V_S t_{BIT} = 50 μs V_S = 7 V to 18 V	0.396	−	0.5	−
D2	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	Normal slope $TH_{REC(min)}$ = 0.422 x V_S $TH_{DOM(min)}$ = 0.284 x V_S t_{BIT} = 50 μs V_S = 7.6 V to 18 V	0.5	−	0.581	−
D3	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	Normal and Low slope $TH_{REC(max)}$ = 0.778 x V_S $TH_{DOM(max)}$ = 0.616 x V_S t_{BIT} = 96 μs V_S = 7 V to 18 V	0.417	−	0.5	−
D4	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	Normal and Low slope $TH_{REC(min)}$ = 0.389 x V_S $TH_{DOM(min)}$ = 0.251 x V_S t_{BIT} = 96 μs V_S = 7.6 V to 18 V	0.5	−	0.590	−

Case outline information page updated as per FPCN22120ZC


MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS
ON Semiconductor
DFN8, 3x3, 0.65P
CASE 506DG
ISSUE A
DATE 28 APR 2016
SCALE 2:1
TOP VIEW
SIDE VIEW
BOTTOM VIEW
DETAIL A
ALTERNATE TERMINAL CONSTRUCTION
GENERIC MARKING DIAGRAM*
RECOMMENDED SOLDERING FOOTPRINT*
DOCUMENT NUMBER: 98AON10527G
DESCRIPTION: DFN8 3X3, 0.65P
PAGE 1 OF 1


MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS
ON Semiconductor
DFNW8 3x3, 0.65P
CASE 507AB
ISSUE E
DATE 02 JUL 2021
SCALE 2:1
TOP VIEW
SIDE VIEW
BOTTOM VIEW
DETAIL A
DETAIL B
SECTION C-C
GENERIC MARKING DIAGRAM*
RECOMMENDED MOUNTING FOOTPRINT
DOCUMENT NUMBER: 98AON14978G
DESCRIPTION: DFNW8 3x3, 0.65P
PAGE 1 OF 1

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

NCV7428D15R2G	NCV7428D13R2G	NCV7428D1L5R2G
NCV7428D1L3R2G	NCV7428MW5R2G	NCV7428MWL3R2G
NCV7428MWL5R2G	NCV7428MW3R2G	