Product Change Notification / SYST-04TNIL668

Date:

15-Jan-2024

Product Category:

Ethernet PHYs

PCN Type:

Document Change

Notification Subject:

LAN8670/1/2 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-04TNIL668_Affected_CPN_01152024.pdf
SYST-04TNIL668_Affected_CPN_01152024.csv

Notification Text:

SYST-04TNIL668

Microchip has released a new Document for the LAN8670/1/2 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at LAN8670/1/2 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: Updated for Rev C2 Silicon/Package Marking.

Impacts to Data Sheet: None

Reason for Change: To improve productivity

Change Implementation Status: Complete

Date Document Changes Effective: 15 Jan 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

LAN8670/1/2 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

LAN8670B1-E/LMX
LAN8670B1T-E/LMX
LAN8670C1-E/LMX
LAN8670C2-E/LMX
LAN8670C1-E/LMXVAO
LAN8670C2-E/LMXVAO
LAN8670C1T-E/LMX
LAN8670C2T-E/LMX
LAN8670C1T-E/LMXVAO
LAN8670C2T-E/LMXVAO
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LAN8671B1T-E/U3B
LAN8671C1-E/U3B
LAN8671C2-E/U3B
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LAN8671C2-E/U3BVAO
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LAN8671C2T-E/U3B
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LAN8672B1-E/LNX
LAN8672B1T-E/LNX
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LAN8672C1-E/LNXVAO
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LAN8672C2T-E/LNX
LAN8672C1T-E/LNXVAO
LAN8672C2T-E/LNXVAO

LAN8670/1/2

Silicon Errata and Data Sheet Clarifications

The LAN8670/1/2 devices that you have received conform functionally to the Device Data Sheet (DS60001573H), except for the anomalies described in this document.

The issues discussed in the following pages are for hardware revisions listed in Table 1. The silicon issues are summarized in Table 2. Items relating to data sheet changes are summarized in Table 3 of the Data Sheet Clarifications section.

TABLE 1: SILICON PART ID AND HARDWARE REVISION VALUES

Part Number	Part ID [1]	Hardware Revision [1]	Package Marking
LAN8670 LAN8671 LAN8672	010110	0101	C2
	010110	0100	C1
	010110	0010	B1

Note 1: The Part ID and Hardware Revision are located in the PHY_ID2 register Model Number and Revision Number fields, respectively. See Data Sheet (DS60001573H) for details.

FIGURE 1: TOP MARKING FOR LAN8670 DEVICE

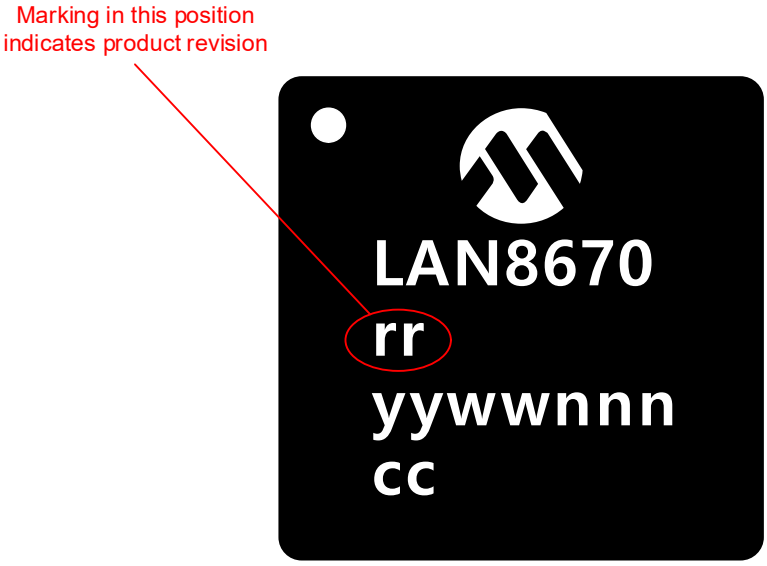

FIGURE 2: TOP MARKING FOR LAN8671 DEVICE

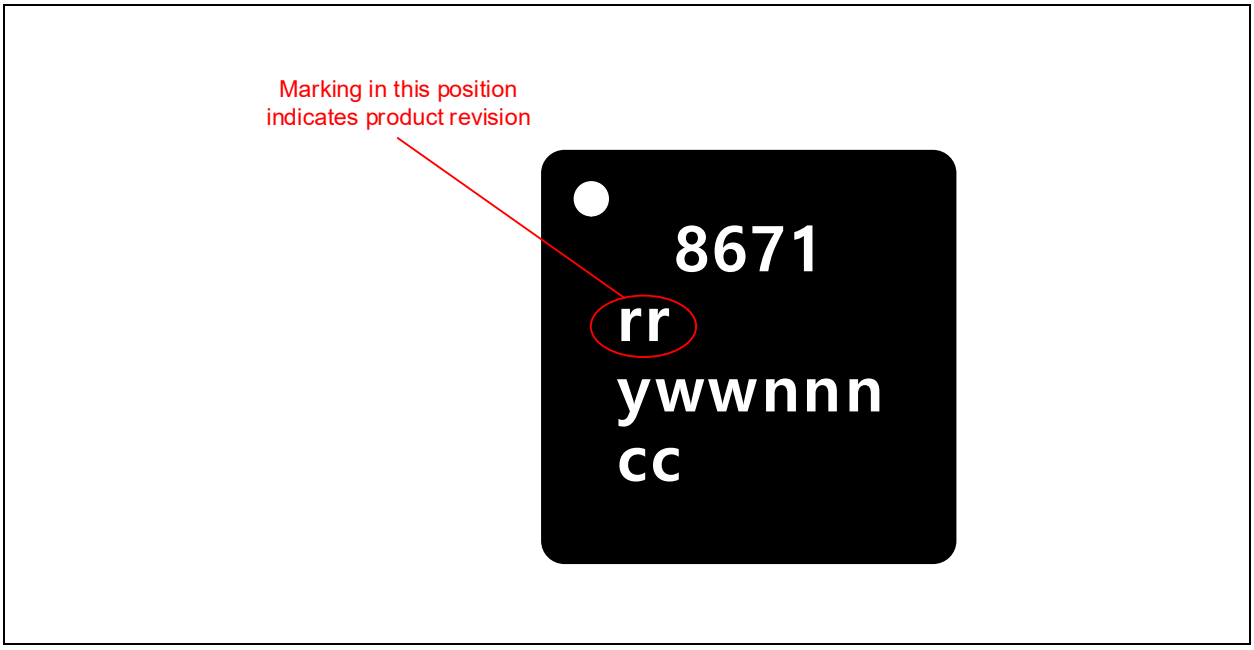

FIGURE 3: TOP MARKING FOR LAN8672 DEVICE

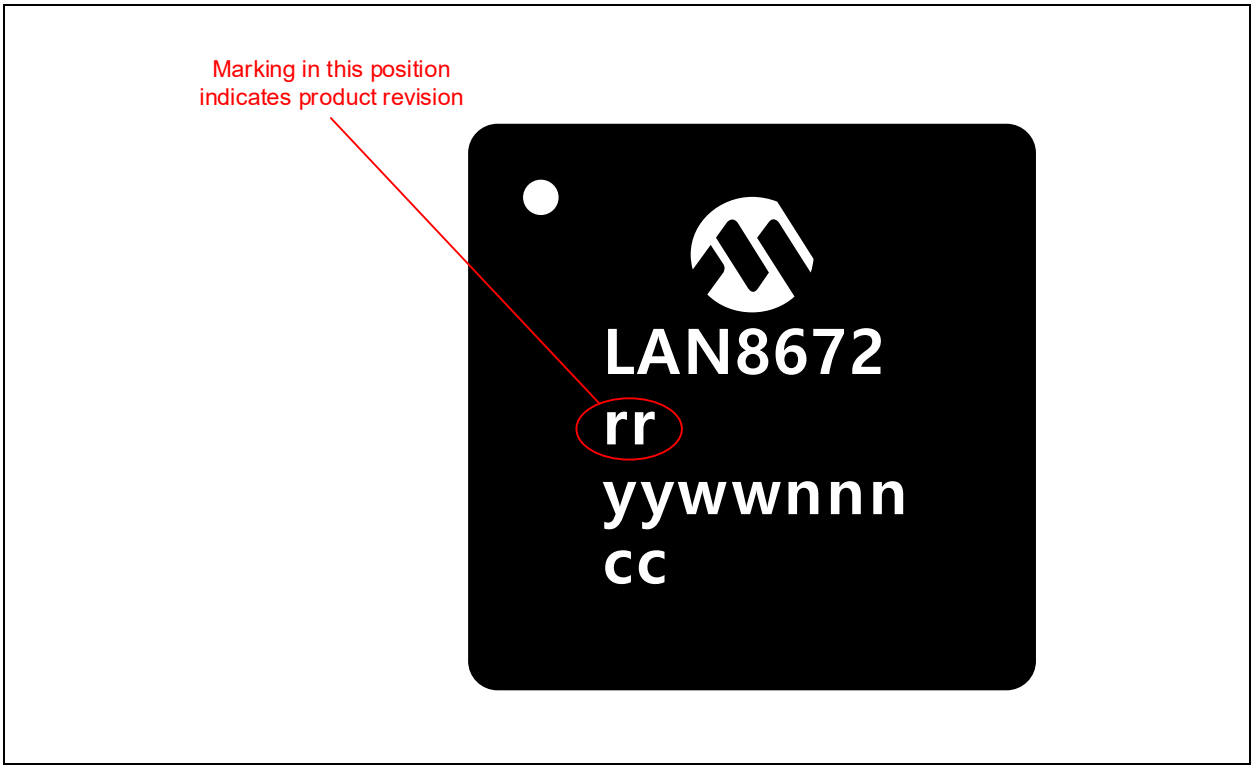

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Issue Summary	Affected Devices		
		Rev B1	Rev C1	Rev C2
s1.	Media interface mode (RMII) identification	LAN8671	-	-
s2.	Package Type identification	LAN8671	-	-
s3.	RMII CSMA/CD operation in mixed PLCA segments	LAN8670 LAN8671	LAN8670 LAN8671	LAN8670 LAN8671
s4.	Incorrect reset indication on IRQ_N	ALL	-	-
s5.	Multi-coordinator PLCA action	ALL	ALL	ALL
s6.	Transmission of collision fragments with PLCA and RMII	LAN8670 LAN8671	LAN8670 LAN8671	LAN8670 LAN8671
s7.	In RMII mode: incorrect assertion of Carrier Sense may occur following a logical collision	LAN8670 LAN8671	LAN8670 LAN8671	-
s8.	Revert to CSMA/CD when PLCA Beacons are missing	ALL	-	-
s9.	Packet pattern matcher incorrectly matches for all message types	ALL	-	-
s10.	SLPCAL field of SLPCTL0 register may deliver invalid result on read	-	ALL	ALL
s11.	When configured as a PLCA coordinator, the device does not stop transmitting beacons immediately upon entering sleep mode	-	ALL	ALL
s12.	A trade-off exists between noise immunity and carrier sense latency	-	ALL	ALL

Legend

- Erratum is not applicable.

Silicon Errata Issues:

s1. Module: Media interface mode (RMII) identification

Resolved with the release of Silicon Rev C1.

s2. Module: Package Type identification

Resolved with the release of Silicon Rev C1.

s3. Module: RMII CSMA/CD operation in mixed PLCA segments

DESCRIPTION

The LAN8670/1 RMII cannot be operated with PLCA disabled on a network with other PLCA-enabled nodes. When the device is configured for CSMA/CD operation (i.e., PLCA is disabled), then the reception of PLCA BEACON and COMMIT symbols from the network will be improperly transferred via the RMII to the MAC resulting in undefined behavior including dropped packets.

The LAN8672 does not support RMII operation.

END USER IMPLICATIONS

The RMII may only be used with PLCA disabled when all other nodes on the mixing segment are also configured for pure CSMA/CD operation.

Work Around

None.

s4. Module: Incorrect reset indication on IRQ_N

Resolved with the release of Silicon Rev C1.

s5. Module: Multi-coordinator PLCA action

DESCRIPTION

When operating as a PLCA Coordinator, if the PHY receives an unexpected BEACON from an additional coordinator on the segment, it will set the Unexpected BEACON Received (UNEXPB) bit in the Status 1 (STS1) register. The PHY will then enter a recovery state in which it can receive packets but will transmit neither packets nor BEACONs for the next two PLCA bus cycles. Should the duplicate Coordinator continue sending periodic BEACONs, then the PHY will remain in the recovery state unable to transmit to avoid collisions with the duplicate Coordinator in Transmit Opportunity 0.

Clause 148 of the IEEE 802.3cg-2019™ specification describes that when this condition occurs, the PHY should avoid transmitting in its transmit opportunity until the end of the current bus cycle when the PHY will again transmit its BEACON to the segment.

END USER IMPLICATIONS

The PHY will halt transmitting packets and BEACONs to the network when configured as a PLCA Coordinator and an unexpected BEACON is detected. This results in the node becoming an inactive Coordinator.

Work Around

The station management entity should monitor the Unexpected BEACON Received bit and configure the PHY as a PLCA Follower.

s6. Module: Transmission of collision fragments with PLCA and RMII

DESCRIPTION

Clause 4 of the IEEE Std 802.3-2018™ specifies the MAC shall implement an Inter-Packet Gap (IPG) delay of 96 bit times (BT) between packets. This IPG is split into two parts. The first part, IPG part 1, requires that no carrier be sensed. If carrier is sensed during IPG part 1, then the timer is restarted. Once IPG part 1 is complete, the MAC may transmit following IPG part 2. The IPG part 1 is nominally 64 BT, but may be less, including zero. The IPG part 2 timing is nominally 32 BT, but is always equal to the full IPG duration minus the IPG part 1.

Some MACs implement an IPG part 1 of very small duration. If the IPG part 1 time is too small, then the MAC may attempt to transmit after the PHY has asserted carrier indication with CRSDV. The result is that the MAC will quickly detect a collision and send a collision fragment to the PHY. When PLCA is enabled, the PHY, not expecting the MAC to transmit after carrier was indicated, will not detect the collision and end up transmitting the collision fragment to the network.

END USER IMPLICATIONS

Use of a MAC with an IPG part 1 time of less than 18 bits will result in the transmission of short 10.4 µs packets onto the network.

Work Around

While the transmission of the collision fragments to the network are benign, they may be eliminated by reducing the size of the PLCA delay line buffer with the register configuration provided below. This will cause the PHY to detect a normal logical collision preventing the transmission of the collision fragment. Additionally, the PHY will capture the next transmit opportunity guaranteeing the MAC the ability to transmit according to the PLCA algorithm.

Access	MMD	Address	Data	Mask
RMW	0x1F	0x008F	0x00D0	0x07F0

Legend:
R - Read
W - Write
RMW - Read-Modified Write

s7. Module: In RMII mode: incorrect assertion of Carrier Sense may occur following a logical collision

Resolved with the release of Silicon Rev C2.

s8. Module: Revert to CSMA/CD when PLCA Beacons are missing

Resolved with the release of Silicon Rev C1.

s9. Module: Packet pattern matcher incorrectly matches for all message types

Resolved with the release of Silicon Rev C1.

s10. Module: SLPCAL field of SLPCTL0 register may deliver invalid result on read

DESCRIPTION

When reading the SLPCTL0 register, the SLPCAL field returns 0x0001. This bitfield must always be written as 0x0000.

END USER IMPLICATIONS

Sleep mode may not function properly if this bitfield is set to anything other than 0.

Work Around

When writing to the SLPCTL0, including when performing read-modify-write sequences, ensure that the SLPCAL bitfield is always written as 0x0000.

s11. Module: When configured as a PLCA coordinator, the device does not stop transmitting beacons immediately upon entering sleep mode

DESCRIPTION

The device does not stop transmitting beacons immediately upon entering sleep mode when configured as a PLCA coordinator. The coordinator node, NODE_ID = 0, transmits a beacon at the start of each PLCA bus cycle. When sleep mode begins, the transmitter is not disabled until VDDA drops below its valid level. When configured to sleep on the inactivity timeout, the coordinator node will recognize the beacon as bus activity and wake itself back up.

END USER IMPLICATIONS

The coordinator mode will not reliably remain in sleep mode when configured to sleep on an inactivity timeout, as it will interpret its own beacon as network activity. Continued presence of beacons will cause other devices on the mixing segment to detect signal activity, so any other devices that are configured to sleep on inactivity will not sleep.

Work Around

The coordinator node (NODE_ID = 0) must never be configured to sleep on inactivity timers. It must be put into sleep mode by its station controller. In addition, immediately before entering sleep, the coordinator must have PLCA disabled to stop the beacon.

1. Clear the EN bit of the PLCA_CTRL0 to disable the beacon.
2. Enter sleep mode and configure a non-zero delay by writing to the following bitfields of SLPCTL0:
   - Set SLPEN to 1
   - Set WKINEN and MDIWKEN to configure desired wake source(s)
   - SLPCAL must be written as 0x0.
   - Set SLPINHDLY to 1 or greater.

s12. Module: A trade-off exists between noise immunity and carrier sense latency

DESCRIPTION

When configured to work in noisy environments, such as those required to pass standard EMI/EMC tests, it is necessary to use additional filtering, which increases carrier sense latency. The recommended default configuration, which is required to pass these tests, results in a longer carrier assertion time, which imposes a limitation on the usable range of the PLCA Transmit Opportunity Timer. As a reminder, this value must be configured equally among all nodes in the mixing segment. Values below the default can, theoretically, provide insignificant increases in throughput at the cost of system robustness.

END USER IMPLICATIONS

- The default value, in the specification and for this device, is 3.2us (TO_TMR=32). Using this value is strongly recommended except when collisions are detected on a PLCA enabled multidrop mixing segment containing third party devices.
- This device should never be configured with TO_TMR < 29, and values less than 32 require the user thoroughly test the final system for robustness.

Workaround:

The Transmit Opportunity timer (TO_TMR) should be configured with the default value of 32. In the event that a smaller value is used, it must always be 29 or greater.

If collisions are detected during operation with devices from third-party vendors on the mixing segment, the Transmit Opportunity Timer may need to be increased to greater than 32. As the necessary value will be dependent upon various latency characteristics of other devices on the mixing segment, as well as the propagation delay on the physical medium, contact Microchip support.

TABLE 3: DATA SHEET CLARIFICATION SUMMARY

Item Number	Port/Function	Issue Summary	Resolved with Data Sheet Revision
d1.	Table 3-7. Miscellaneous Pins	The table incorrectly states that clock oscillators may be used in MII mode.	DS60001573F
d2.	Section 4.1 Media Independent Interface (MII)	Text does not clearly state that a crystal must be used in MII mode.	DS60001573F
d3.	Section 4.8.1 Crystal Pins (XTI/XTO)	Text incorrectly states that clock oscillators may be used in MII mode.	DS60001573F
d4.	Figure 4-4. Crystal Oscillator Input	Figure incorrectly states that clock oscillators may be used in MII mode.	DS60001573F
d5.	Table 7-7. DC Electrical Characteristics (other than 10BASE-T1S PMA)	Note 3 incorrectly states that the MII crystal input XTI may be driven by a clock oscillator.	DS60001573F

Data Sheet Clarifications:

The following typographic corrections and clarifications are to be noted for the data sheet (DS60001573H):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

d1. Module: Table 3-7. Miscellaneous Pins

Resolved with the release of Data Sheet DS60001573F.

d2. Module: Section 4.1 Media Independent Interface (MII)

Resolved with the release of Data Sheet DS60001573F.

d3. Module: Section 4.8.1 Crystal Pins (XTI/XTO)

Resolved with the release of Data Sheet DS60001573F.

d4. Module: Figure 4-4. Crystal Oscillator Input

Resolved with the release of Data Sheet DS60001573F.

d5. Module: Table 7-7. DC Electrical Characteristics (other than 10BASE-T1S PMA)

Resolved with the release of Data Sheet DS60001573F.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000962E, 12/2023	s7	Updated for Rev C2 Silicon
DS80000962D, 7/2023	s7 s11	Updated details Clarified issue summary
DS80000962C, 6/2023		Updated for Rev C1 Silicon Data Sheet Clarifications resolved
DS80000962B, 1/2023		Added Data Sheet Clarification section
DS80000962A, 7/2021	All	Initial Release of Errata

NOTES:

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ISBN: 978-1-6683-3614-4

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