



Product Change Notification / DSNO-09TPSA420

Date:

17-Jul-2024

Product Category:

Antifuse Fpgas, General Purpose Fpgas, Radiation Tolerant Fpgas, System On Chip Fpgas

PCN Type:

Manufacturing Change

Notification Subject:

eSign# SPE0000007 Final Notice: Release of updated software version of Synplify Pro Microchip Edition v2023.09M-1 & Synplify Pro Standalone v2023.09-1 for various FPGA devices.

Affected CPNs:

[DSNO-09TPSA420_Affected_CPN_07172024.pdf](#)
[DSNO-09TPSA420_Affected_CPN_07172024.csv](#)

Notification Text:

PCN Status:Final Notification

PCN Type:Manufacturing Change

Microchip Parts Affected:Please open one of the files found in the Affected CPNs section.
Note: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change:Release of updated software version of Synplify Pro Microchip Edition v2023.09M-1 & Synplify Pro Standalone v2023.09-1 for various FPGA devices.

Note:

Synplify Pro Microchip Edition version 2023.09M-1 released on 14th May 2024 and is available for download on the webpage below:

<https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/synthesis-and-simulation/synplify-pro-me>

Pre and Post Change Summary:

	Pre Change	Post Change
Software	Synplify Pro standalone all-vendor versions 2023.03 and 2023.09, as well as Microchip Edition version 2023.09M could incorrectly extract the enable signal logic during RTL synthesis when the signal path contains a set of multiplexors connected in series around a register, and the MUXs are driven by bus ports.	The issue has been fixed in Synplify Pro Microchip Edition version 2023.09M-1 and later, as well as Synplify Pro standalone version 2023.09-1 and later.

Impacts to Data Sheet:None

Change Impact:None

Reason for Change:Synplify Pro standalone all-vendor versions 2023.03 and 2023.09, as well as Microchip Edition version 2023.09M could incorrectly extract the enable signal logic during RTL synthesis when the signal path contains a set of multiplexors connected in series around a register, and the MUXs are driven by bus ports. This is described in the attached **Customer Notice**.

Change Implementation Status:Completed

Estimated First Ship Date:May 14, 2024 (date code: 2420)

Note: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Time Table Summary:

	May 2024						July 2024				
Workweek	18	19	20	21	22	27	28	29	30	31	
Final PCN Issue Date							x				
Estimated Implementation Date			x								

Method to Identify Change:Not applicable. New software will be available as defined above.

Qualification Report:Not Applicable

Revision History:July 17, 2024: Issued final notification to reveal the updated version of the released Synplify software.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

[CN_SynPro_Enable_Extraction_Libero_SoC_v2024p1.pdf](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

A42MX09-PQG100IQ247
A42MX09-PQG100M
A42MX09-PQG144
A42MX09-PQG144I
A42MX09-PQG144M
A42MX09-PQG160
A42MX09-PQG160A
A42MX09-PQG160I
A42MX09-PQG160M
A42MX09-TQG176
A42MX09-TQG176A
A42MX09-TQG176I
A42MX09-TQG176IX218
A42MX09-TQG176M
A42MX09-VQG100
A42MX09-VQG100A
A42MX09-VQG100I
A42MX09-VQG100IQ156
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MPF300T-1FCG784NE
MPF300T-1FCG784NI
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MPF300T-1FCSG536I
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MPF300T-1FCVG484E
MPF300T-1FCVG484I
MPF300T-1FCVG484T2
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MPF300T-FCG484I
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RTSX72SU-LG624E
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RTSX72SU-LG624PROTO
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A42MX09-1VQG100M
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A42MX09-2TQG176I
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A42MX09-3PQG160
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A42MX09-3TQG176I
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M2S005S-VFG256X416
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M2S010-1FG484I
M2S010-1FGG484
M2S010-1FGG484I
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M2S010-1TQG144I
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M2S010-1VF256I
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M2S010-1VF400I
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M2S010-FGG484IX414
M2S010-FGG484IX416
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M2S010-FGG484IX418
M2S010-FGG484X416
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M2S010-TQG144Q159
M2S010-TQG144Q179
M2S010-TQG144Q184



Customer Notification (CN)

Subject: Synplify Pro FPGA Synthesis Enable Extraction Issue

June 2024

Description:

This customer notification applies to FPGA Synthesis software used with Microchip FPGAs and SoCs. Synplify Pro Microchip Edition v2023.09M-1 software has been released to address the issue of incorrect enable signal extraction in specific design scenarios. The issue affects Synplify Pro standalone all-vendor versions 2023.03 and 2023.09, as well as Microchip Edition version 2023.09M which was bundled with Libero SoC v2024.1. This issue affected all FPGA technologies supported by the respective Synplify Pro versions listed above. This issue has been fixed in Synplify Pro Microchip Edition version 2023.09M-1 and later, as well as Synplify Pro standalone version 2023.09-1 and later.

Reason for Change:

Synplify Pro standalone all-vendor versions 2023.03 and 2023.09, as well as Microchip Edition version 2023.09M could incorrectly extract the enable signal logic during RTL synthesis when the signal path contains a set of multiplexors connected in series around a register, and the MUXs are driven by bus ports.

The following scenario is incorrectly synthesized:

```
module top (d1, clk1, en1, en2, q1);
input [1:0] d1;
input clk1, en1, en2;
output [1:0] q1;

wire [1:0] w1, w2;
reg [1:0] r1;

foo i1 (w2);
assign w1 = en1 ? d1 : r1 & w2;
always @(posedge clk1)
    if (en2)
        r1 <= w1;

assign q1 = en2 ? w1 : r1;
```



```
endmodule  
  
module foo (q);  
output [1:0] q;  
assign q = 2'b11;  
endmodule
```

The RTL schematic below representing the code above shows a register, dff, driven by back-to-back feedback MUXs which are driven by bus port d1[1:0].

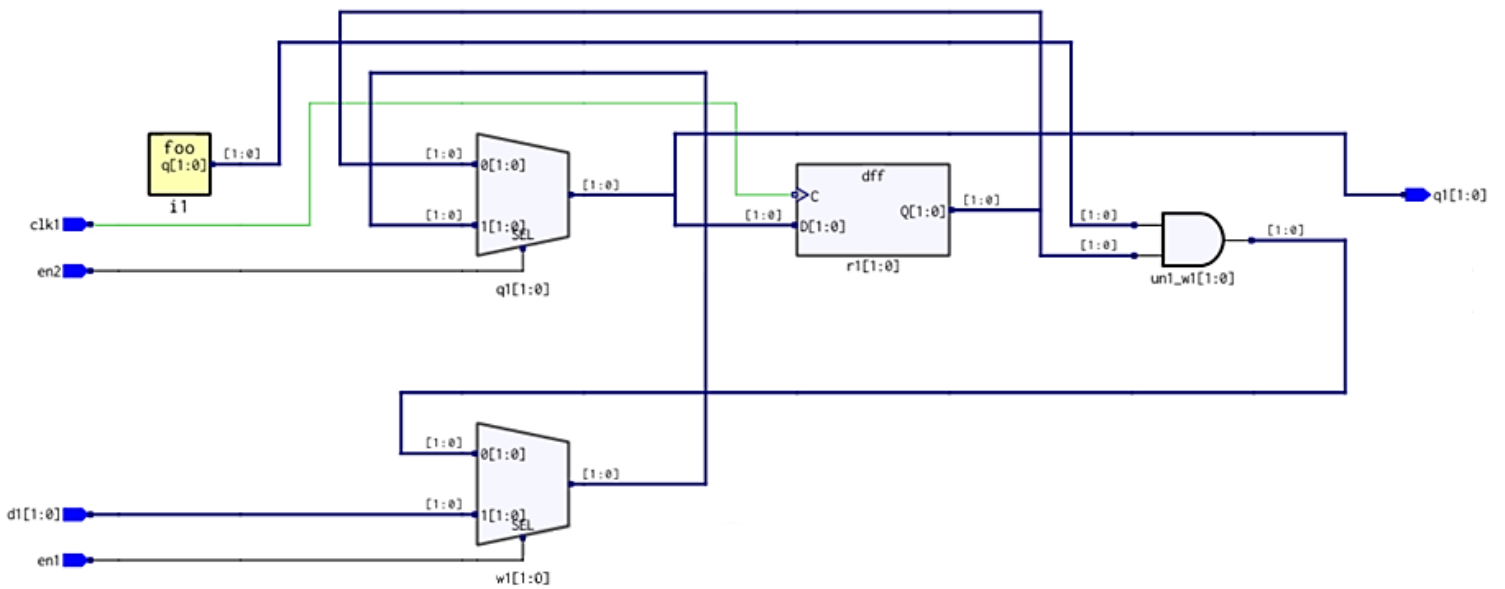


Figure 1: RTL Schematic View of Affected RTL Structure



Due to the issue present in Synplify Pro standalone all-vendor versions 2023.03 and 2023.09, as well as Microchip Edition version 2023.09M, the mapped netlist incorrectly left the d1[1] pin unconnected. After technology mapping, the Most Significant Bit (MSB) d1[1] of port d1[1:0] was lost and only d1[0] was preserved in the mapped schematic view below:

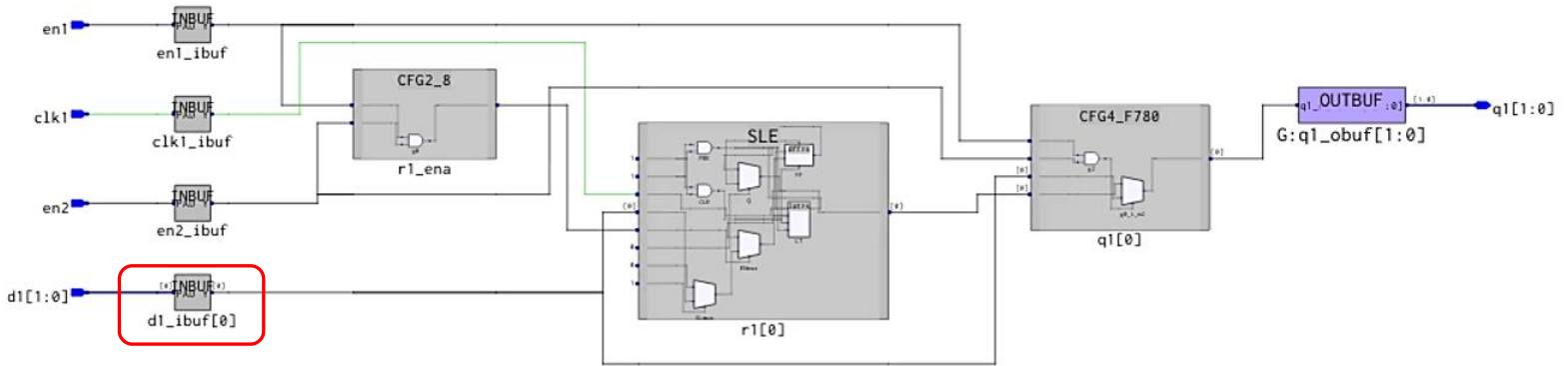


Figure 2: Incorrectly Mapped Netlist Schematic showing Missing d1[1] Connection

In contrast, when synthesized with Synplify Pro v2023.09M-1 software containing the fix for this issue, both bits d1[1] and d1[0] are driving the logic, and MSB d1[1] is no longer dropped, as shown in the figure below.

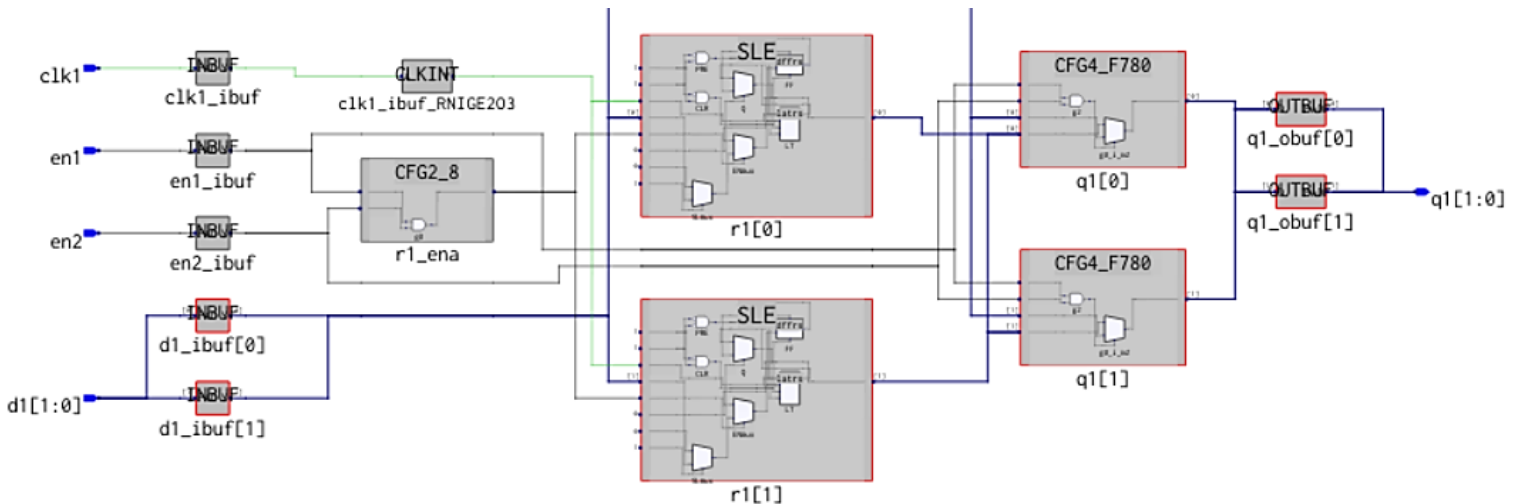


Figure 3: Correctly Mapped Netlist Schematic using Synplify Pro v2023.09M-1 Software



Application Impact:

During design verification, an affected design would experience a simulation mismatch between RTL and post-synthesis simulation results. The post-synthesis design functionality would not match the pre-synthesis RTL functionality.

Required Action:

New and ongoing designs:

Microchip recommends upgrading to Synplify Pro ME v2023.09M-1 or later, to prevent this enable signal extraction issue from affecting the design functionality.

Designs completed prior to the release of Synplify Pro ME v2023.09M-1:

No further actions are listed if the affected design conditions and tool versions described above don't apply to the completed design.

If the affected tool versions were used to synthesize the completed design, determine if the design contains the affected scenario described above by re-synthesizing the design using Synplify Pro ME v2023.09M-1 and checking the log message for the following message:

```
@N:BN159 : <source_file>(<line#>) | Found multibit flop  
<inst_name>[<width>:0] with cascaded feedback multiplexer in the data path.
```

Completed designs using affected tool versions and containing the affected logic:

Analyze the netlist to confirm if any enable bit was mapped incorrectly and determine the impact to the specific design. Review post-synthesis simulation results and full system functional hardware test results conducted on each production unit over the entire operating conditions range to assess whether this logic was exercised successfully.

As needed, the netlist can be corrected by upgrading to Synplify Pro ME v2023.09M-1 or later and re-synthesizing the design. Use the updated netlist to rerun the design flow, generate a new design bitstream and reprogram the device.

Download Updated Synplify Pro ME Software

Synplify Pro ME v2023.09M-1 or later software can be downloaded from the following webpage:



<https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/synthesis-and-simulation/synplify-pro-me#Download%20Software>

After installing Synplify Pro ME v2023.09M-1, it can be used within Libero SoC by adding a new Synthesis Tool Profile from the Project Menu->Tool Profiles window, using the following settings:

Name (example): Synplify Pro v2023.09M-1

Tool Integration: Synplify Pro ME

Location on Windows: <path_to_install_dir>\bin\synplify_pro.exe

Location on Linux: <path_to_install_dir>/bin/synplify_pro

Contact Information

For any questions about this subject, contact Microchip FPGA-BU Technical Support at the web portal below:

<http://www.microchip.com/support>

Regards,

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